THE DATASHEET OF

MAX4951BECTP+

19-5023; Rev 1; 11/10

EVALUATION KIT AVAILABLE

SATA I/II/III Bidirectional Redriver with Input Equalization and Preemphasis

General Description

The MAX4951BE dual-channel buffer is ideal to redrive serial ATA (SATA) I, SATA II, and SATA III signals and features high electrostatic discharge (ESD) ±8kV Human Body Model (HBM) protection. The MAX4951BE can be placed nearly anywhere on the motherboard to overcome board losses and produce an eSATA-compatible signal level. This device is SATA specification v.2.6 (gold standard)-compliant, while overcoming losses in the PCB and eSATA connector.

The MAX4951BE features very low standby current for power-sensitive applications. This device features hardware SATA-drive cable detection, keeping the power low in standby mode. The device also features an independent channel, dynamic power-down mode where power consumption is reduced when no input signal is present.

The MAX4951BE preserves signal integrity at the receiver by reestablishing full output levels and can reduce the total system jitter (TJ) by providing input equalization. This device features channel-independent digital preemphasis controls to drive SATA outputs over longer trace lengths or to meet eSATA specifications. SATA Out-Of-Band (OOB) signaling is supported using high-speed OOB signal detection on the inputs and squelch on the corresponding outputs. Inputs and outputs are all internally 50Ω terminated and must be AC-coupled to the SATA controller IC and SATA device.

The MAX4951BE operates from a single +3.3V (typ) supply, and is available in a small, 4mm x 4mm TQFN package with flow-through traces for ease of layout. This device is specified over the 0°C to +70°C operating temperature range.

Applications

Laptop Computers
Servers
Desktop Computers
Docking Stations
Data Storage/Workstations

Features

- **Single +3.3V Supply Operation**
- **Low-Power, 500µA (typ) eSATA Cable Detect**
- **Drive Detection**
- **Dynamic Power Reduction**
  Reduced Power Consumption in Active Mode
- **Fixed Input Equalization**
  Permits Longer Traces Leading to the Device
- **Selectable Output Preemphasis**
  Improved Output Eye
- **SATA I (1.5Gbps) and SATA II (3.0Gbps) Compliant**
- **SATA III (6.0Gbps) Compliant**
- **Supports eSATA Output Levels**
- **Supports SATA OOB Signaling**
- **OOB Detection: 8ns (max)**
- **Internal Input/Output 50Ω Termination Resistors**
- **Inline Signal Traces for Flow-Through Layout**
- **Space-Saving, 4mm x 4mm TQFN Package with Exposed Pad**
- **High ESD Protection on All Pins: ±8kV (HBM)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4951BECTP+	0°C to +70°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

SATA I/II/III Bidirectional Redriver with Input Equalization and Preemphasis

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND unless otherwise noted.)
V_{CC} ....-0.3V to +4.0V
AINP, AINM, BINP, BINM, EN, $\overline{CAD}$,
PA, PB (Note 1)......................................-0.3V to (V_{CC} +0.4V)
Short-Circuit Output Current
(BOUTP, BOUTM, AOUTP, AOUTM)........................... ±30mA
Continuous Current at Inputs
(AINP, AINM, BINP, BINM).. ±5mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 25.6mW/°C above +70°C).................2051mW
ESD Protection on All Pins (HBM).......................................±8kV
Operating Temperature Range............................ 0°C to +70°C
Storage Temperature Range........................... -55°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: All I/O pins are clamped by internal diodes.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})...........39°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).................6°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_L = 12nF, R_L = 50Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Power-Supply Range	V_{CC}			3.0		3.6	V
Operating Supply Current	I_{CC}	PA = PB = V_{CC}; D10.2 pattern, f = 1.5Gbps			77	92	mA
		PA = PB = GND; D10.2 pattern, f = 1.5Gbps			62	76	
Average Supply Current in Normal Operation		Duty cycle is 25% active, 75% idle; D10.2 pattern	Preemphasis on		30		mA
			Preemphasis off		26		
Standby Supply Current	I_{STBY}	EN = GND or $\overline{CAD}$ = V_{CC}			500	750	µA
Dynamic Power-Down Current	I_{DYNPD}				14	20	mA
Single-Ended Input Resistance	$Z_{RX-SE-DC}$	Single-ended to V_{CC} (Note 4)		40	50		Ω
Differential Input Resistance	$Z_{RX-DIFF-DC}$	(Note 4)		85	100	115	Ω
Single-Ended Output Resistance	$Z_{TX-SE-DC}$	Single-ended to V_{CC} (Note 4)		40	50		Ω
Differential Output Resistance	$Z_{TX-DIFF-DC}$	(Note 4)		85	100	115	Ω
AC PERFORMANCE							
Differential Input Return Loss (Notes 4, 5)	$RL_{RX-DIFF}$	f = 150MHz to 300MHz		18			dB
		f = 300MHz to 600MHz		14			
		f = 600MHz to 1200MHz		10			
		f = 1.2GHz to 2.4GHz		8			
		f = 2.4GHz to 3.0GHz		3			
		f = 3.0GHz to 5.0GHz		1			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_L = 12nF, R_L = 50Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Input Return Loss (Notes 4, 5)	RL_{RX-CM}	f = 150MHz to 300MHz		5			dB
		f = 300MHz to 600MHz		5			
		f = 600MHz to 1200MHz		2			
		f = 1.2GHz to 2.4GHz		1			
		f = 2.4GHz to 3.0GHz		1			
		f = 3.0GHz to 5.0GHz		1			
Differential Output Return Loss (Notes 4, 5)	$RL_{TX-DIFF}$	f = 150MHz to 300MHz		14			dB
		f = 300MHz to 600MHz		8			
		f = 600MHz to 1200MHz		6			
		f = 1.2GHz to 2.4GHz		6			
		f = 2.4GHz to 3.0GHz		3			
		f = 3.0GHz to 5.0GHz		1			
Common-Mode Output Return Loss (Notes 4, 5)	RL_{TX-CM}	f = 150MHz to 300MHz		8			dB
		f = 300MHz to 600MHz		5			
		f = 600MHz to 1200MHz		2			
		f = 1.2GHz to 2.4GHz		1			
		f = 2.4GHz to 3.0GHz		1			
		f = 3.0GHz to 5.0GHz		1			
Common-Mode to Differential Input Return Loss (Notes 4, 5)	$RL_{RX-CM-DM}$	f = 150MHz to 300MHz		30			dB
		f = 300MHz to 600MHz		20			
		f = 600MHz to 1200MHz		10			
		f = 1.2GHz to 2.4GHz		10			
		f = 2.4GHz to 3.0GHz		4			
		f = 3.0GHz to 5.0GHz		4			
Common-Mode to Differential Output Return Loss (Notes 4, 5)	$RL_{TX-CM-DM}$	f = 150MHz to 300MHz		30			dB
		f = 300MHz to 600MHz		30			
		f = 600MHz to 1200MHz		20			
		f = 1.2GHz to 2.4GHz		10			
		f = 2.4GHz to 3.0GHz		4			
		f = 3.0GHz to 5.0GHz		4			
Differential Input Signal Range	$V_{RX-DFF-PP}$	SATA I, SATA II (Note 4)		225		1600	mV_{P-P}
Differential Output Swing	$V_{TX-DFF-PP}$	f = 750MHz (Note 4)	PA = PB = GND	425	525	625	mV_{P-P}
Output Preemphasis	$TX-DFF-PP-PE_{DB}$	f = 750MHz	PA = PB = V_{CC}		2.8		dB
Input Equalization		$V_{RX-DFF-PP}$ = 300mV_{P-P}, $t_{IN,RISE/FALL}$ = 20ps			2.7		dB
Preemphasis Time Period	t_{PE}	f = 750MHz	PA = PB = V_{CC}		150		ps
Propagation Delay	t_{PD}				150		ps

SATA I/II/III Bidirectional Redriver with Input Equalization and Preemphasis

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_L = 12nF, R_L = 50Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 3)

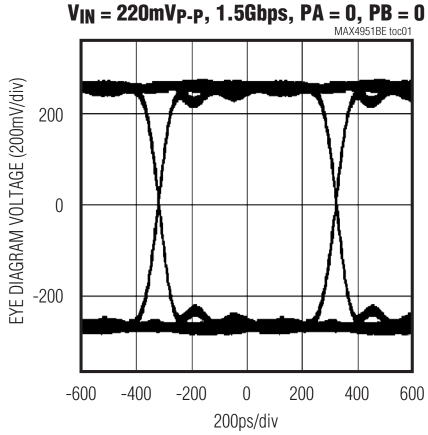
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise/Fall Time (Notes 5, 6)	t_R, t_F	PA = PB = GND SATA I/II (Note 7)	67		130	ps
		PA = PB = GND SATA III (Note 8)	40		68	
Deterministic Jitter (Notes 5, 9)	$t_{TX-DJ-DD}$	PA = PB = GND			20	ps_{P-P}
Random Jitter (Notes 5, 9)	$t_{TX-RJ-DD}$	PA = PB = GND			1.5	ps_{RMS}
OOB Detector Threshold		SATA OOB pattern, f = 750MHz	50		150	mV_{P-P}
OOB Output Startup/Shutdown Time		(Note 10)		4	8	ns
OOB Differential-Offset Delta	$\Delta V_{OOB,DFF}$	Difference between OOB and active-mode output offset	-120		120	mV
OOB Common-Mode Delta	$\Delta V_{OOB,CM}$	Difference between OOB and active common-mode voltage	-15		+15	mV
OOB Output Disable	$V_{OOB,OUT}$	V_{IN} < 50mV_{P-P}, output voltage in squelch			30	mV_{P-P}
LOGIC INPUT						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.6	V
Input Logic Hysteresis	V_{HYST}			0.1		V
Input Pullup Resistance	R_{PU}	Pin: $\overline{CAD}$	200	330		kΩ
Input Pulldown Resistance	R_{PD}	Pins: EN, PA, PB	200	330		kΩ
ESD PROTECTION						
All Pins		HBM		±8		kV

Note 3: All devices are 100% production tested at T_A = +70°C. All temperature limits are guaranteed by design.
Note 4: This specification meets SATA v.2.6, gold standard.
Note 5: Guaranteed by design.
Note 6: Rise and fall times are measured using 20% and 80% levels.
Note 7: For SATA 2.0, refer to *SATA 2.6-Gold Specification*, page 111, Figure 191.
Note 8: For SATA 3.0, refer to *SATA Revision 3.0 Release Candidate*, page 222, Figure 124.
Note 9: DJ measured using a K28.5 pattern; RJ measured using a D10.2 pattern.
Note 10: Total time for OOB detection circuit to enable/squelch the output.

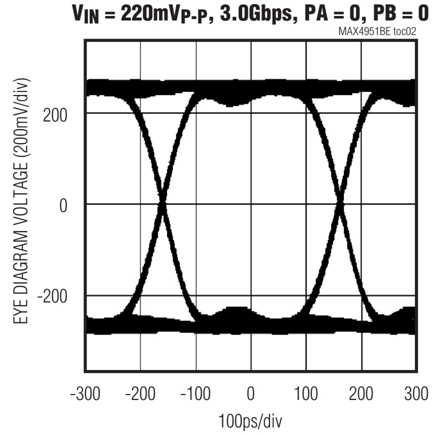
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

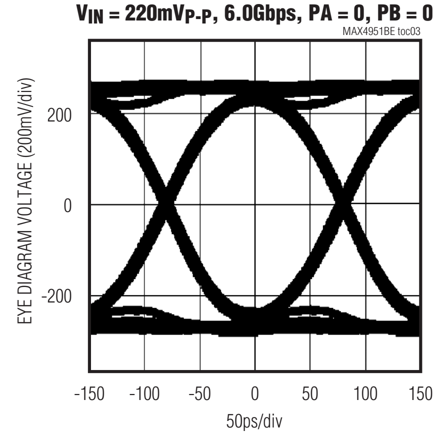
V_{IN} = 220mV$_{P-P}$, 1.5Gbps, PA = 0, PB = 0



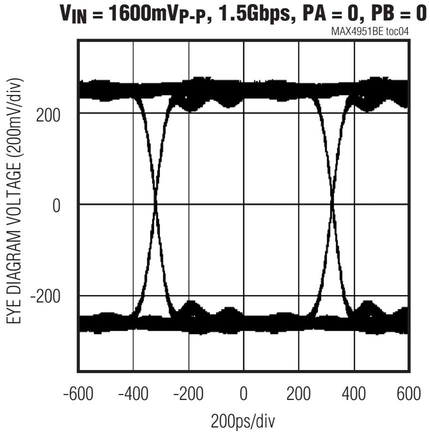
V_{IN} = 220mV$_{P-P}$, 3.0Gbps, PA = 0, PB = 0



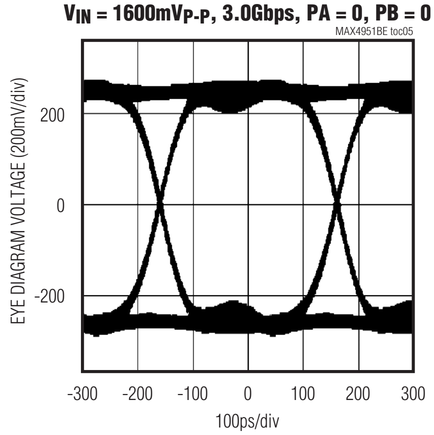
V_{IN} = 220mV$_{P-P}$, 6.0Gbps, PA = 0, PB = 0



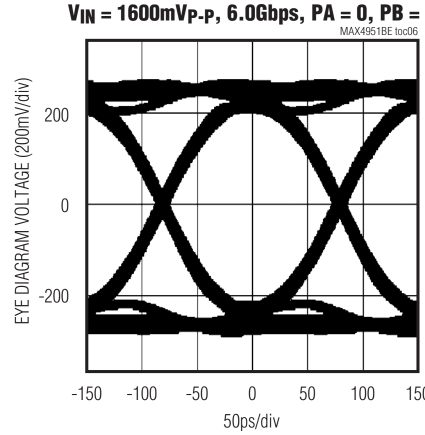
V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, PA = 0, PB = 0



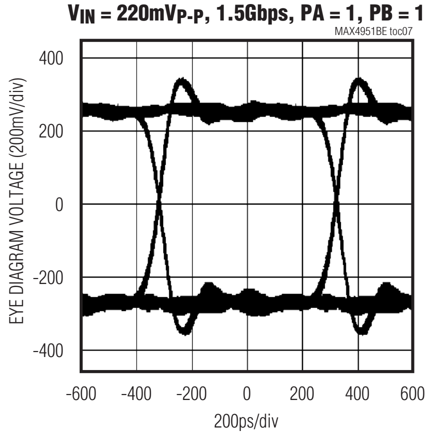
V_{IN} = 1600mV$_{P-P}$, 3.0Gbps, PA = 0, PB = 0



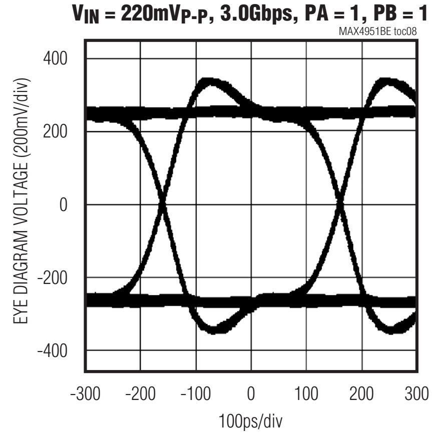
V_{IN} = 1600mV$_{P-P}$, 6.0Gbps, PA = 0, PB = 0



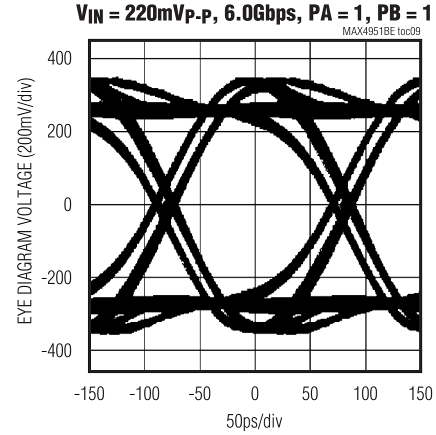
V_{IN} = 220mV$_{P-P}$, 1.5Gbps, PA = 1, PB = 1



V_{IN} = 220mV$_{P-P}$, 3.0Gbps, PA = 1, PB = 1



V_{IN} = 220mV$_{P-P}$, 6.0Gbps, PA = 1, PB = 1

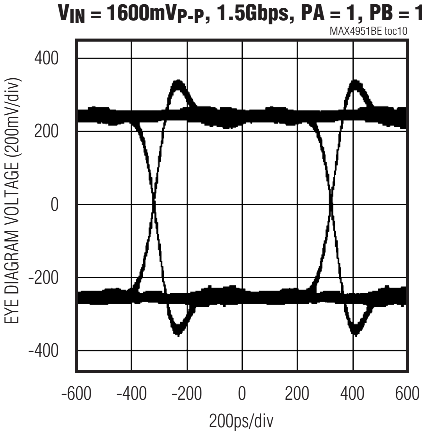


SATA I/II/III Bidirectional Redriver with Input Equalization and Preemphasis

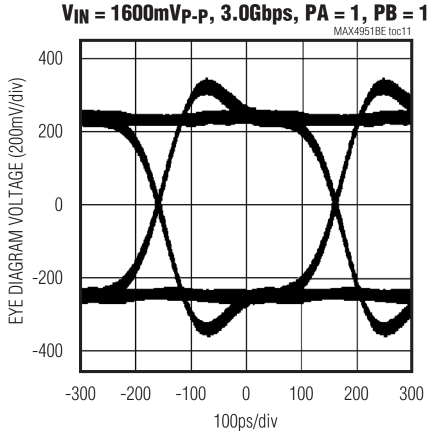
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

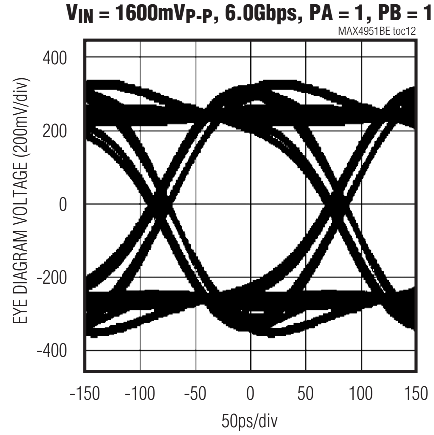
V_{IN} = 1600mV_{P-P}, 1.5Gbps, PA = 1, PB = 1



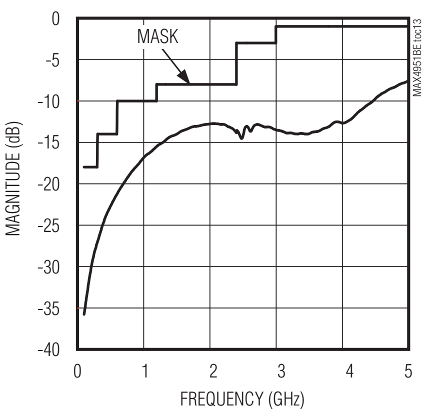
V_{IN} = 1600mV_{P-P}, 3.0Gbps, PA = 1, PB = 1



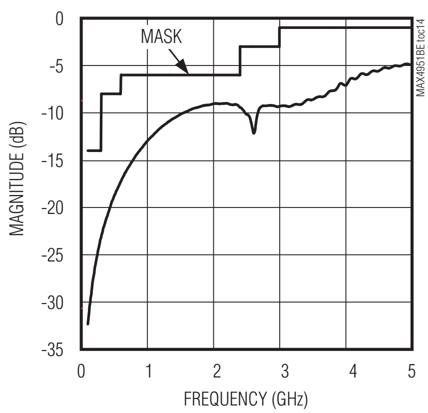
V_{IN} = 1600mV_{P-P}, 6.0Gbps, PA = 1, PB = 1



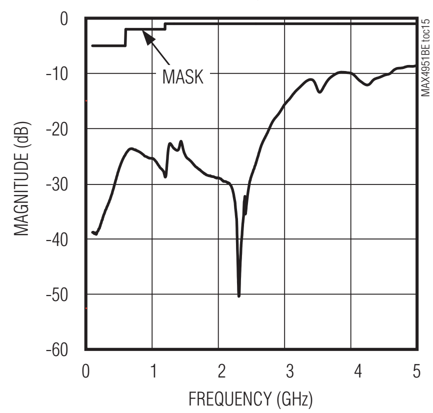
DIFFERENTIAL INPUT RETURN LOSS vs. FREQUENCY



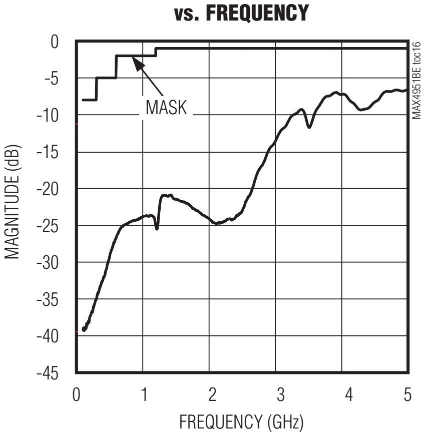
DIFFERENTIAL OUTPUT RETURN LOSS vs. FREQUENCY



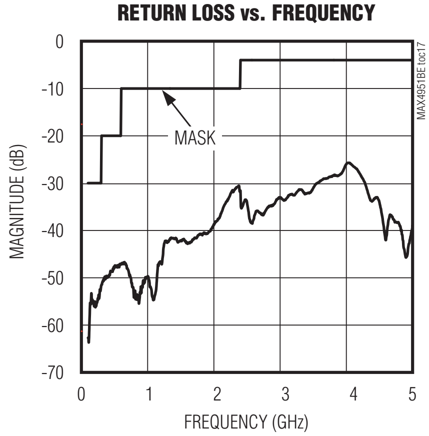
COMMON-MODE INPUT RETURN LOSS vs. FREQUENCY



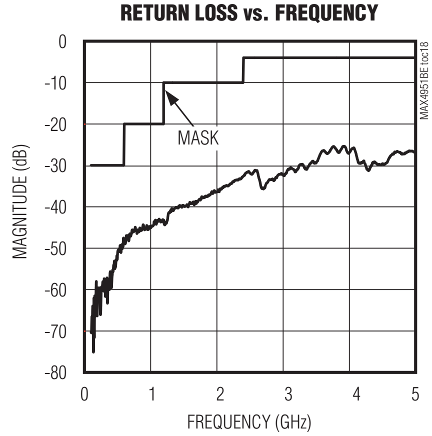
COMMON-MODE OUTPUT RETURN LOSS vs. FREQUENCY



COMMON-MODE TO DIFFERENTIAL INPUT RETURN LOSS vs. FREQUENCY



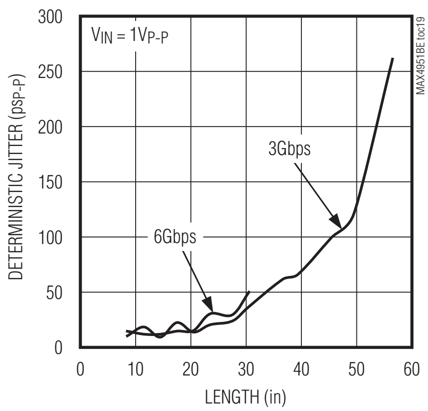
COMMON-MODE TO DIFFERENTIAL OUTPUT RETURN LOSS vs. FREQUENCY



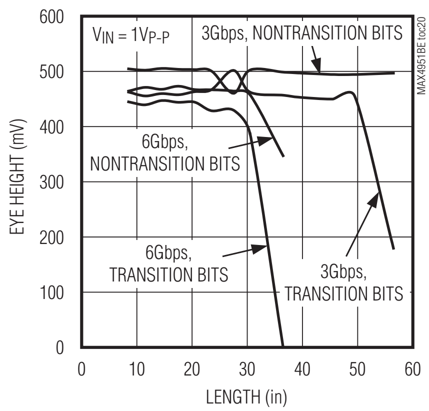
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

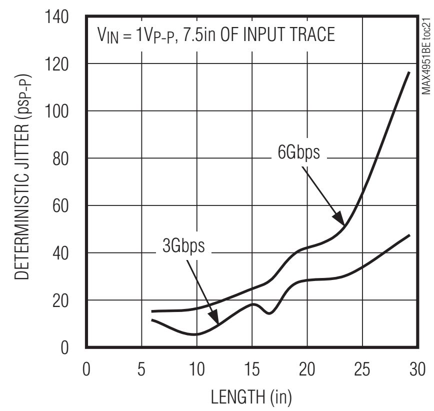
DETERMINISTIC JITTER vs. INPUT LENGTH, PA = 0, PB = 0



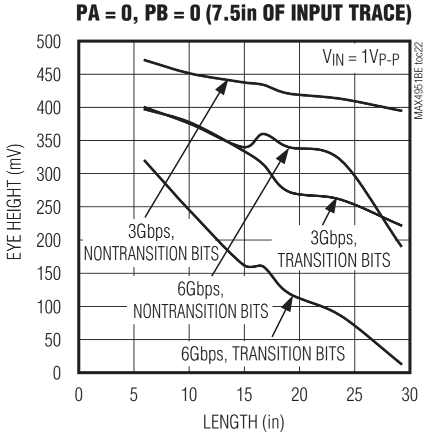
EYE HEIGHT vs. INPUT LENGTH, PA = 0, PB = 0



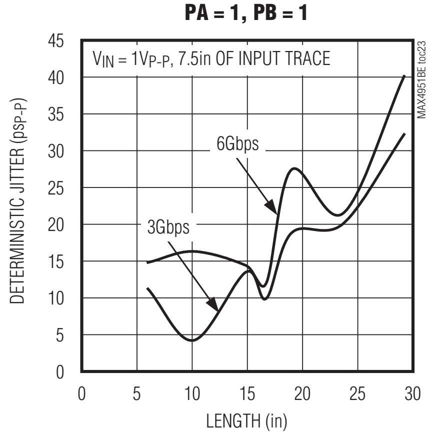
DETERMINISTIC JITTER vs. OUTPUT LENGTH, PA = 0, PB = 0



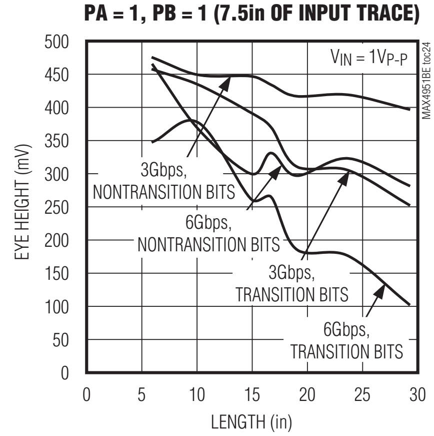
EYE HEIGHT vs. OUTPUT LENGTH, PA = 0, PB = 0 (7.5in OF INPUT TRACE)



DETERMINISTIC JITTER vs. OUTPUT LENGTH, PA = 1, PB = 1

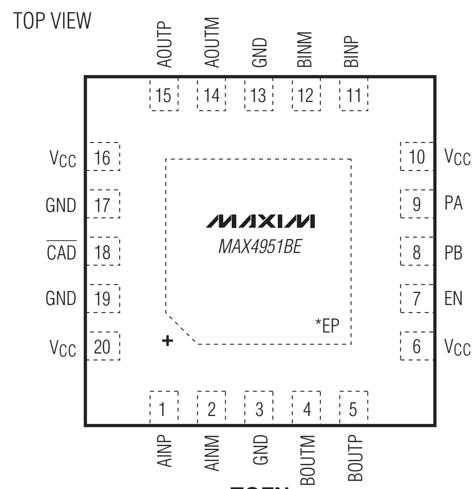


EYE HEIGHT vs. OUTPUT LENGTH, PA = 1, PB = 1 (7.5in OF INPUT TRACE)



SATA I/II/III Bidirectional Redriver with Input Equalization and Preemphasis

Pin Configuration



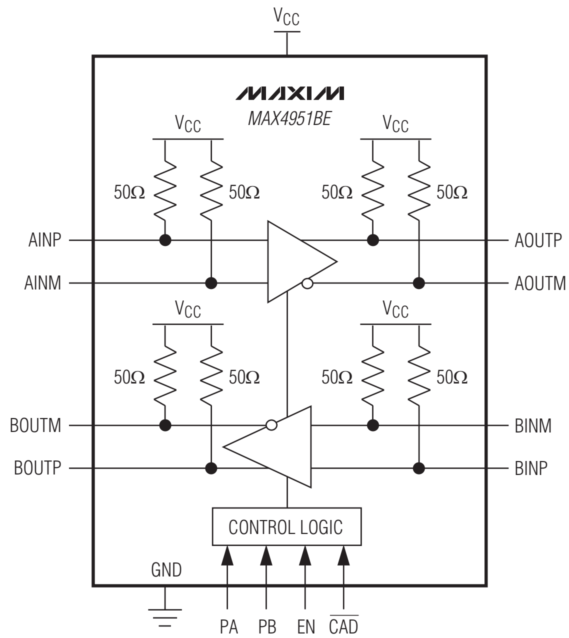
TQFN (4mm × 4mm)

*CONNECT EXPOSED PAD (EP) TO GND.

Pin Description

PIN	NAME	FUNCTION
1	AINP	Noninverting Input from Host Channel A
2	AINM	Inverting Input from Host Channel A
3, 13, 17, 19	GND	Ground
4	BOUTM	Inverting Output to Host Channel B
5	BOUTP	Noninverting Output to Host Channel B
6, 10, 16, 20	V_{CC}	Positive Supply Voltage Input. Bypass V_{CC} to GND with 1µF and 0.01µF capacitors in parallel as close to the device as possible.
7	EN	Active-High Enable Input. Drive EN low to put the device in standby mode. Drive EN high for normal operation. EN is internally pulled down with a 330kΩ (typ) resistor.
8	PB	Channel B Preemphasis Enable Input. Drive PB high to enable channel B output preemphasis. Drive PB low for standard SATA output level. PB is internally pulled down with a 330kΩ (typ) resistor.
9	PA	Channel A Preemphasis Enable Input. Drive PA high to enable channel A output preemphasis. Drive PA low for standard SATA output level. PA is internally pulled down with a 330kΩ (typ) resistor.
11	BINP	Noninverting Input from Device Channel B
12	BINM	Inverting Input from Device Channel B
14	AOUTM	Inverting Output to Device Channel A
15	AOUTP	Noninverting Output to Device Channel A
18	$\overline{CAD}$	Active-Low Cable-Detect Input. Drive $\overline{CAD}$ high to put the device in standby mode. Drive $\overline{CAD}$ low for normal operation. $\overline{CAD}$ is internally pulled up with a 330kΩ (typ) resistor.
—	EP	Exposed Pad. Internally connected to GND. EP must be electrically connected to a ground plane for proper thermal and electrical operation.

Functional Diagram/Truth Table



EN	$\overline{CAD}$	STATUS
0	0	Low-Power Standby
0	1	Low-Power Standby
1	0	Active
1	1	Low-Power Standby

EN	PA	PB	CHANNEL A	CHANNEL B
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Preemphasis	Standard SATA
1	0	1	Standard SATA	Preemphasis
1	1	1	Preemphasis	Preemphasis

Note: *PA, PB, EN are internally pulled down to GND by 330kΩ resistors. $\overline{CAD}$ is internally pulled up to V_{CC} by a 330kΩ resistor.*

X = Don't care.

Detailed Description

The MAX4951BE consists of two identical buffers that take SATA input signals and return them to full output levels while withstanding high ESD ±8kV (HBM) protection. This device meets SATA I/II specifications and can meet SATA III specifications.

Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to V_{CC} (see the *Functional Diagram/Truth Table*) and must be AC-coupled to the SATA controller IC and SATA device for proper operation.

SATA I/II/III Bidirectional Redriver with Input Equalization and Preemphasis

OOB Signal Detection

The MAX4951BE provides full OOB signal support through high-speed, OOB-detection circuitry. SATA OOB differential input signals of 50mV$_{P-P}$ or less are detected as OFF and are not passed to the output. This prevents the system from responding to unwanted noise. SATA OOB differential input signals of 150mV$_{P-P}$ or more are detected as on and passed to the output. This allows OOB signals to transmit through the MAX4951BE. The time for the OOB-detection circuit to detect an inactive SATA OOB input and squelch the associated output, or to detect an active SATA OOB input and enable the output, is less than 4ns (typ).

Enable Input

The MAX4951BE features an active-high enable input (EN). EN has an internal pulldown resistor of 330kΩ (typ). When EN is driven low or left unconnected, the MAX4951BE enters low-power standby mode and the buffers are disabled, reducing the supply current to 500µA (typ). Drive EN high for normal operation.

Cable-Detect Input

The MAX4951BE features an active-low, cable-detect input ($\overline{CAD}$). $\overline{CAD}$ has an internal pullup resistor of 330kΩ (typ). When $\overline{CAD}$ is driven high or left unconnected, the MAX4951BE enters low-power standby mode and the buffers are disabled, reducing supply current to 500µA (typ). This signal is normally driven low by inserting an eSATA cable into a properly wired socket (see Figure 3). If the cable-detect feature is not desired, simply ground this pin.

Dynamic Power-Down Mode

The MAX4951BE features a dynamic power-down mode where the device shuts down the major power consumption circuitry. The MAX4951BE detects whether the input signal does not exist for a 4µs (typ) duration. Normal power and normal operation resume when a signal above the OOB-threshold level is detected at the input. This function is implemented separately for both channels.

Output Preemphasis Selection Inputs

The MAX4951BE has two preemphasis-control logic inputs, PA and PB. PA and PB have internal pulldown resistors of 330kΩ (typ). PA and PB enable preemphasis to the outputs of their corresponding buffers (see the *Functional Diagram/Truth Table*). Drive PA or PB low or leave unconnected for standard SATA output levels. Drive PA or PB high to provide preemphasis to the output. The preemphasis output signal compensates for attenuation from longer trace lengths or to meet eSATA specifications.

ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX4951BE is protected against ESD ±8kV (HBM). The ESD structures withstand ±8kV in normal operation and powered down states. After an ESD event, the MAX4951BE continues to function without latchup.

HBM

The MAX4951BE is characterized for ±8kV ESD protection using the HBM (MIL-STD-883, Method 3015). Figure 1 shows the HBM and Figure 2 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

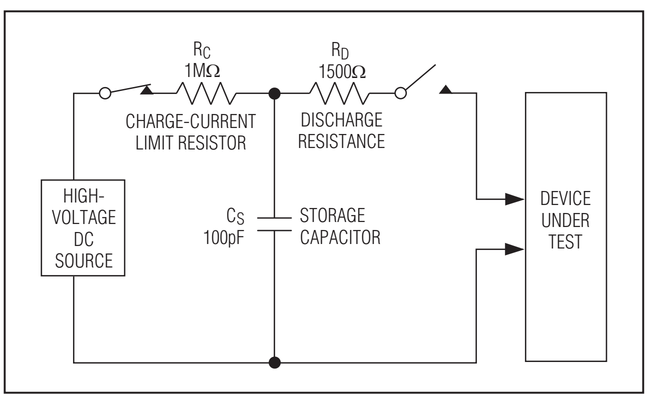


Figure 1. Human Body ESD Test Model

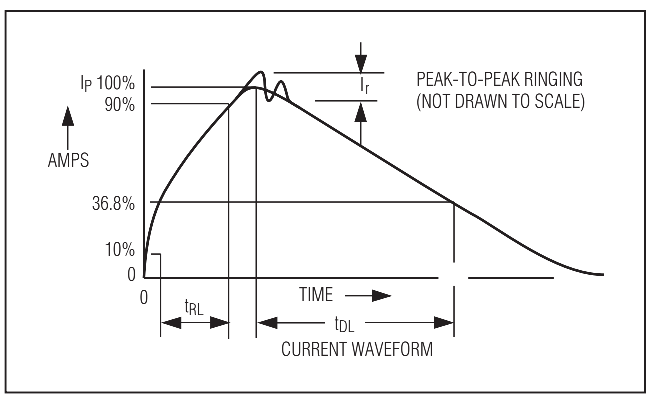


Figure 2. Human Body Current Waveform

Applications Information

Figure 3 shows a typical application with the MAX4951BE used to drive an eSATA output. The diagram assumes that the MAX4951BE is close to the SATA host controller. PB is set low to drive standard SATA levels to the host, and PA is set high to drive eSATA levels to the device. If the MAX4951BE is further from the controller, set PB high to compensate for attenuation. The MAX4951BE is backward-pin-compatible with MAX4951 (see Figure 4).

Exposed-Pad Package

The exposed-pad, 20-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX4951BE must be soldered to GND for proper thermal and electrical performance. For more information on exposed-pad packages, refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Layout

Use controlled-impedance transmission lines to interface with the MAX4951BE high-speed inputs and outputs. Place power-supply decoupling capacitors as close as possible to V_{CC} pin.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply V_{CC} before applying signals, especially if the signal is not current limited.

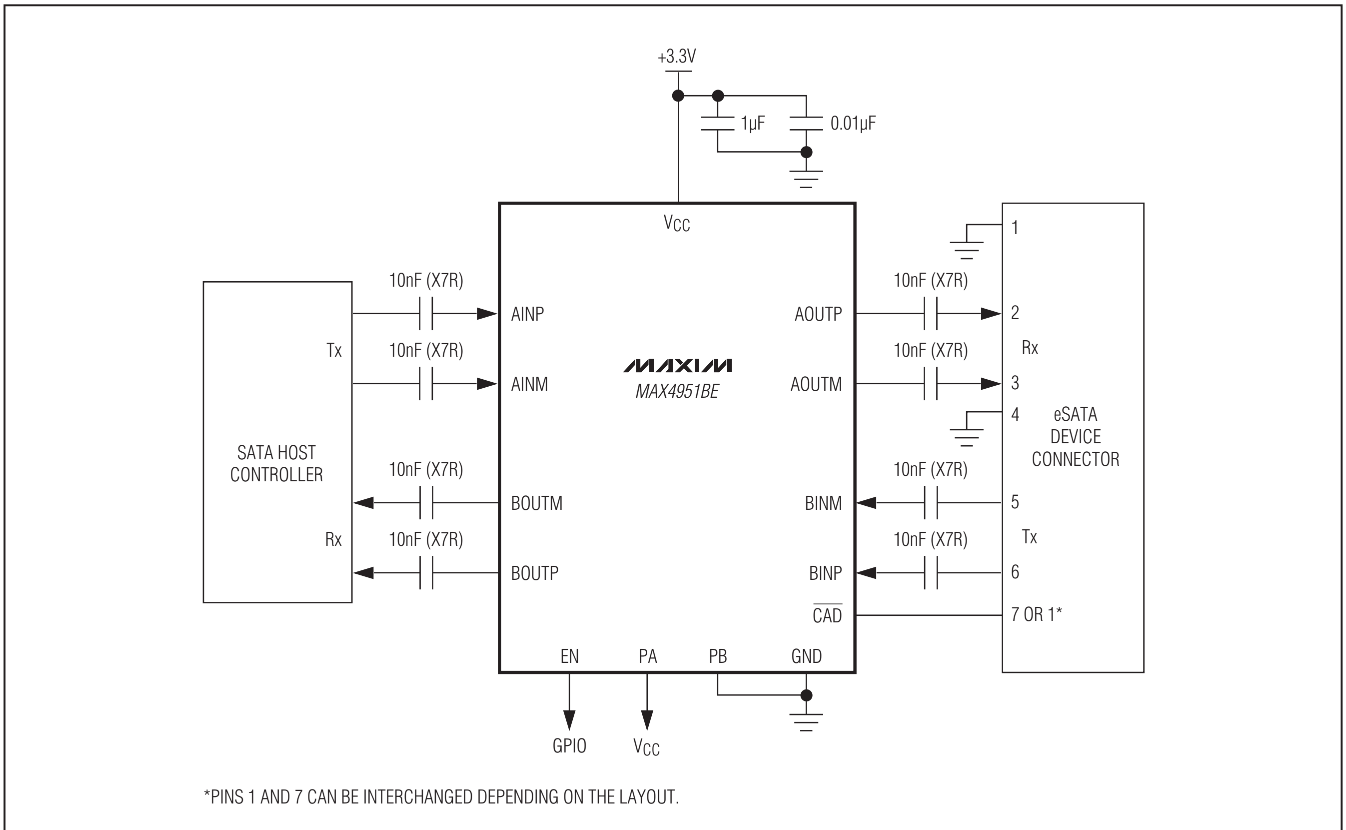


Figure 3. Typical Application Circuit for MAX4951BE Driving an eSATA Output

SATA I/II/III Bidirectional Redriver with Input Equalization and Preemphasis

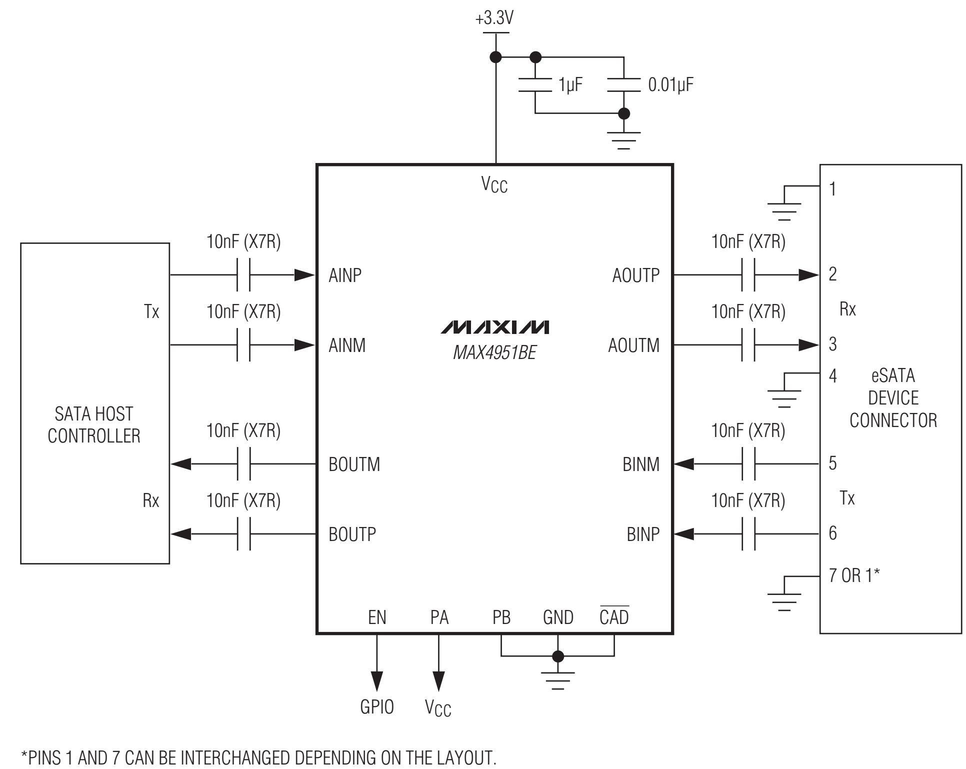


Figure 4. Typical Application Circuit for Backward Pin Compatibility with the MAX4951

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2044+2	**21-0139**	**90-0036**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	11/10	Deleted the "Meets SATA I, II Input/Output-Return Loss Mask" feature from the *Features* section, deleted the "Top Mark" column from the *Ordering Information*	1