THE DATASHEET OF

MAX527DCWG+

19-4500; Rev 3; 2/95

MAXIM

Calibrated Quad 12-Bit Voltage-Output D/A Converters

General Description

The MAX526/MAX527 contain four 12-bit, voltage-output digital-to-analog converters (DACs). Precision output buffer amplifiers are included on-chip to provide voltage outputs. The MAX527 operates with ±5V power supplies, while the MAX526 utilizes -5V and +12V to +15V supplies. Offset, gain, and linearity are factory calibrated to provide the MAX526's 1LSB total unadjusted error (TUE).

These devices feature double-buffered interface logic with a 12-bit input register and a 12-bit DAC register. Data in the DAC register sets the DAC output voltage. The MAX526/MAX527 have an 8-bit-wide data bus. Data is loaded into the input register using two write operations with an 8-bit LSB write load and a 4-bit MSB write load. An asynchronous load DAC ($\overline{LDAC}$) input transfers data from the input register to the DAC register. All logic inputs are TTL and CMOS compatible.

The MAX526/MAX527 are available in 24-pin, 300 mil plastic DIP, Ceramic SB, and wide SO packages.

Applications

Minimum Component Count Analog Systems

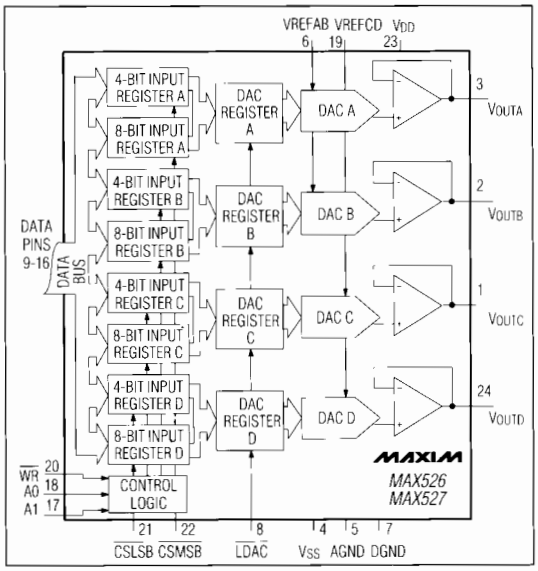
Digital Offset/Gain Adjustment

Arbitrary Function Generators

Industrial Process Controls

Automatic Test Equipment

Functional Diagram



Features

- ♦ **Reference Input Range Includes Ground (C, D grades)**
- ♦ **Full 12-Bit Performance Without Adjustments**
- ♦ **1 LSB Total Unadjusted Error (MAX526)**
- ♦ **Buffered Voltage Outputs**
- ♦ **Fast Output Settling**
  3µs for MAX526
  5µs for MAX527
- ♦ **Double-Buffered Digital Inputs**
- ♦ **Microprocessor and TTL/CMOS Compatible**
- ♦ **±5V Supply Operation (MAX527)**

Ordering Information

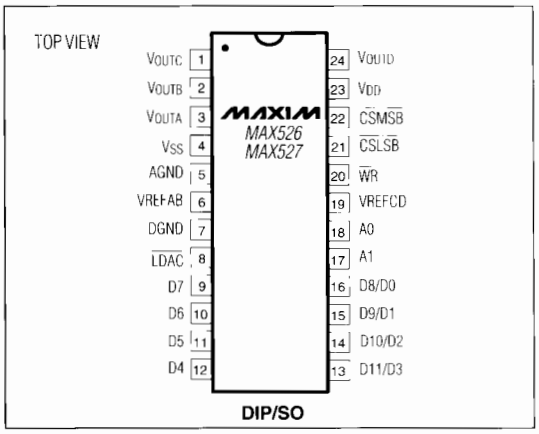
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX526CCNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX526DCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX526CCWG	0°C to +70°C	24 Wide SO	±1/2
MAX526DCWG	0°C to +70°C	24 Wide SO	±1
MAX526DC/D	0°C to +70°C	Dice*	±1
MAX526CENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX526DENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX526CEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX526DEWG	-40°C to +85°C	24 Wide SO	±1
MAX526CMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1/2
MAX526DMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



Calibrated Quad 12-Bit Voltage-Output D/A Converters

ABSOLUTE MAXIMUM RATINGS – MAX526

V_{DD} to AGND or DGND .....-0.3V, +17V
V_{SS} to AGND or DGND .....-7V, to 0.3V
Digital Input Voltage to AGND or DGND .....0.3V, V_{DD} + 0.3V
VREF to AGND or DGND .....-0.3V, V_{DD} + 0.3V
V_{OUT} to AGND or DGND .....V_{DD}, V_{SS}
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 13.33mW/°C above +70°C) 733mW
Wide SO (derate 11.76mW/°C above +70°C).....647mW
Ceramic SB (derate 14.29mW/°C above +70°C).....1143mW
Operating Temperature Ranges:
MAX526_C_G .....0°C to +70°C
MAX526_E_G.....-40°C to +85°C
MAX526_MYG .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10 sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX526

(V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE – ANALOG SECTION (R_L = 5kΩ, C_L = 100pF)							
Resolution	N			±12			Bits
Total Unadjusted Error (Note 1)	TUE	MAX526C	T_A = +25°C			±1.0	LSB
		MAX526D				±2.0	
		MAX526CC				±2.0	
		MAX526DC				±3.0	
		MAX526CE				±2.5	
		MAX526DE				±3.5	
		MAX526CM				±3.0	
		MAX526DM				±4.0	
Integral Nonlinearity	INL	MAX526C			±0.15	±0.50	LSB
		MAX526D				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		MAX526C	T_A = +25°C			±1.0	LSB
		MAX526D				±2.0	
		MAX526CC				±2.0	
		MAX526DC				±3.0	
		MAX526CE				±2.5	
		MAX526DE				±3.5	
		MAX526CM				±3.0	
		MAX526DM				±4.0	
Gain Error		MAX526_C/E/M, R_L = ∞				±1.0	LSB
		MAX526_C/E				±1.5	
		MAX526_M				±2.0	
Power-Supply Rejection	ΔGain/ΔV_{DD}	V_{DD} from +10.8V to +16.5V	T_A = +25°C		±0.001	±0.01	LSB/%
	ΔGain/ΔV_{SS}	V_{SS} from -4.5V to -5.5V			±0.001	±0.01	
	ΔOffset/ΔV_{DD}	V_{DD} from +10.8V to +16.5V			±0.007	±0.075	
	ΔOffset/ΔV_{SS}	V_{SS} from -4.5V to -5.5V			±0.003	±0.03	
MATCHING PERFORMANCE							
Total Unadjusted Error (Note 1)	TUE	MAX526C	T_A = +25°C			±1.0	LSB
		MAX526D				±2.0	
Gain Error			T_A = +25°C		0.1	±1.0	LSB
Offset Error		MAX526C	T_A = +25°C		0.5	±1.0	LSB
		MAX526D			0.5	±2.0	
Integral Nonlinearity	INL		T_A = +25°C		0.2	±1.0	LSB

ELECTRICAL CHARACTERISTICS – MAX526 (continued)

(V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT (Note 2)							
Reference Input Range	REF			0		V_{DD} - 4	V
Reference Input Resistance	RREF			5			kΩ
MULTIPLYING MODE PERFORMANCE							
Reference 3dB Bandwidth					700		kHz
Reference Feedthrough		Input code = all 0s	VREF = 10Vp-p at 400HZ		-100		dB
			VREF = 10Vp-p at 4000HZ		-82		
Total Harmonic Distortion plus Noise	THD+N	VREF = $2V_{p-p}$ at 50kHz			0.012		%
DIGITAL INPUTS							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance	C_{IN}	(Note 3)				10	pF
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)							
Voltage-Output Slew Rate					5		V/µs
Output Settling Time		To ±1/2LSB of full scale			3		µs
Digital Feedthrough					5		nV-s
Digital Crosstalk					5		nV-s
POWER SUPPLIES							
Positive Supply Range	V_{DD}			10.8		16.5	V
Negative Supply Range	V_{SS}			-4.5		-5.5	V
Positive Supply Current	I_{DD}	(Note 4)	T_A = +25°C		11	20	mA
						28	
Negative Supply Current	I_{SS}	(Note 4)	T_A = +25°C		8	18	mA
						26	

Note 1: TUE is specified with no resistive load.
Note 2: See *Reference Input* section.
Note 3: Guaranteed by design. Not production tested.
Note 4: Digital inputs at 2.4V; with digital inputs at 0V, I_{DD} decreases typically by 1.5mA at +25°C.

TIMING CHARACTERISTICS – MAX526

(V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}		100			ns
$\overline{WR}$ Pulse Width	t_{WR}		100			ns
$\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{CWH}		0			ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		75			ns
Data to $\overline{WR}$ Hold	t_{DH}		10			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}		120			ns
Address to $\overline{WR}$ Setup	t_{AS}		25			ns
Address to $\overline{WR}$ Hold	t_{AH}		0			ns

Calibrated Quad 12-Bit Voltage-Output D/A Converters

ABSOLUTE MAXIMUM RATINGS – MAX527

V_{DD} to AGND or DGND .....-0.3V, +12V
V_{SS} to AGND or DGND .....-7V, to 0.3V
Digital Input Voltage to AGND or DGND .....0.3V, V_{DD} + 0.3V
VREF to AGND to DGND .....-0.3V, V_{DD} + 0.3V
V_{OUT} to AGND to DGND .....V_{DD}, V_{SS}
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 13.33mW/°C above +70°C) 733mW
Wide SO (derate 11.76mW/°C above +70°C).....647mW
Ceramic SB (derate 14.29mW/°C above +70°C).....1143mW
Operating Temperature Ranges:
MAX527_C_G .....0°C to +70°C
MAX527_E_G.....-40°C to +85°C
MAX527_MYG .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10 sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX527

(V_{DD} = +5V, V_{SS} = -5V, VREF = 2.5V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE – ANALOG SECTION (R_L = 5kΩ, C_L = 100pF)							
Resolution	N			12			Bits
Integral Nonlinearity	INL	MAX527C			±0.15	±0.50	LSB
		MAX527D				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		MAX527C	T_A = +25°C			±3	mV
		MAX527D				±6	
		MAX527CC				±6	
		MAX527DC				±9	
		MAX527CE				±7	
		MAX527DE				±11	
		MAX527CM				±9	
		MAX527DM				±15	
Gain Error		MAX527_C/E, R_L = ∞				±1.0	LSB
		MAX527_M, R_L = ∞				±1.0	
		MAX527_C				±2.0	
		MAX527_E				±2.5	
		MAX527_M				±3.0	
Power-Supply Rejection	ΔGain/ΔV_{DD}	V_{DD} from +4.5V to +5.5V	T_A = +25°C		±0.002	±0.02	LSB/%
	ΔGain/ΔV_{SS}	V_{SS} from -4.5V to -5.5V			±0.002	±0.02	
	ΔOffset/ΔV_{DD}	V_{DD} from +4.5V to +5.5V			±0.005	±0.05	
	ΔOffset/ΔV_{SS}	V_{SS} from -4.5V to -5.5V			±0.005	±0.05	
MATCHING PERFORMANCE							
Gain Error			T_A = +25°C		0.1	±1.0	LSB
Offset Error (Note 1)		MAX527C	T_A = +25°C		0.5	±5	LSB
		MAX527D			0.5	±10	
Integral Nonlinearity	INL		T_A = +25°C		0.2	±1.0	LSB
REFERENCE INPUT (Note 2)							
Reference Input Range	REF	Note 2		0		V_{DD} - 2.20	V
Reference Input Resistance	RREF			5			kΩ

ELECTRICAL CHARACTERISTICS (continued) – MAX527

(V_{DD} = +5V, V_{SS} = -5V, VREF = +2.5V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MULTIPLYING MODE PERFORMANCE							
Reference 3dB Bandwidth					700		kHz
Reference Feedthrough		400Hz			-100		dB
		4000Hz			-82		
Total Harmonic Distortion plus Noise	THD+N	VREF = 850mV$_{p-p}$ at 100kHz			0.024		%
DIGITAL INPUTS							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance	C_{IN}	(Note 3)				10	pF
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)							
Voltage-Output Slew Rate					3		V/µs
Output Settling Time		To ±1/2LSB of full scale			5		µs
Digital Feedthrough					5		nV-s
Digital Crosstalk					5		nV-s
POWER SUPPLIES							
Positive Supply Range	V_{DD}			4.75		5.5	V
Negative Supply Range	V_{SS}			-4.5		-5.5	V
Positive Supply Current	I_{DD}	(Note 4)	T_A = +25°C		5.5	12	mA
						18	
Negative Supply Current	I_{SS}	(Note 4)	T_A = +25°C		3.6	10	mA
						16	

Note 1: TUE is specified with no resistive load.
Note 2: See *Reference Input* section.
Note 3: Guaranteed by design. Not production tested.
Note 4: Digital inputs at 2.4V.

TIMING CHARACTERISTICS – MAX527

(V_{DD} = +5V, V_{SS} = -5V, VREF = +2.5V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

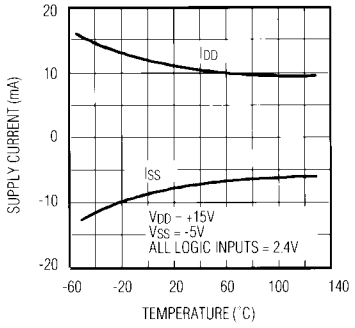
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}	MAX527_C/E	180			ns
		MAX527_M	200			
$\overline{WR}$ Pulse Width	t_{WR}	MAX527_C/E	180			ns
		MAX527_M	200			
$\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{CWH}		0			ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		75			ns
Data to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}	MAX527_C/E	120			ns
		MAX527_M	150			
Address to $\overline{WR}$ Setup	t_{AS}		25			ns
Address to $\overline{WR}$ Hold	t_{AH}		0			ns

Calibrated Quad 12-Bit Voltage-Output D/A Converters

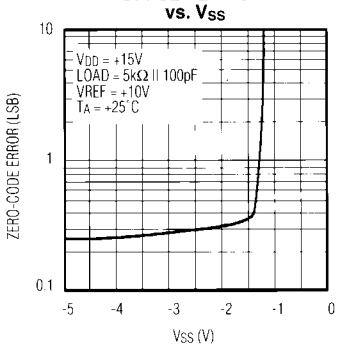
Typical Operating Characteristics

MAX526

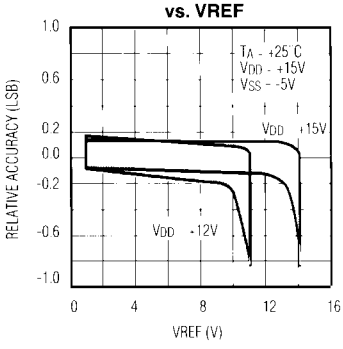
MAX526 SUPPLY CURRENT vs. TEMPERATURE



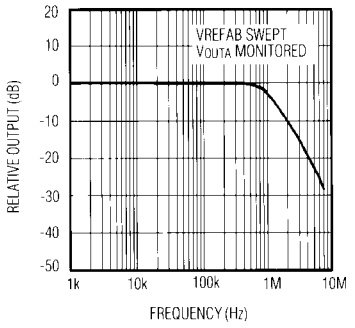
MAX526 OFFSET ERROR vs. VSS



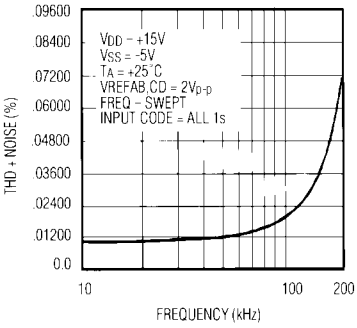
MAX526 RELATIVE ACCURACY vs. VREF



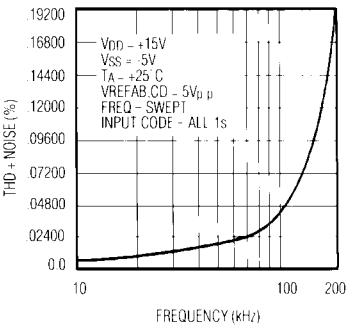
MAX526 REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



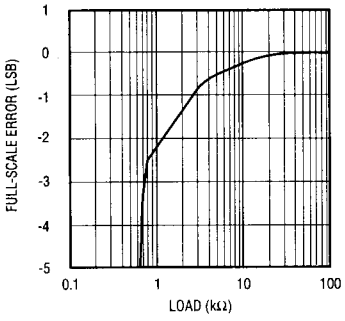
MAX526 THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



MAX526 THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY

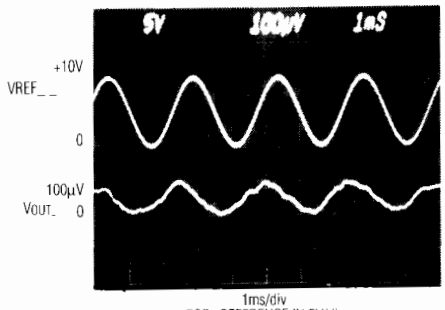


MAX526 FULL-SCALE ERROR vs. LOAD



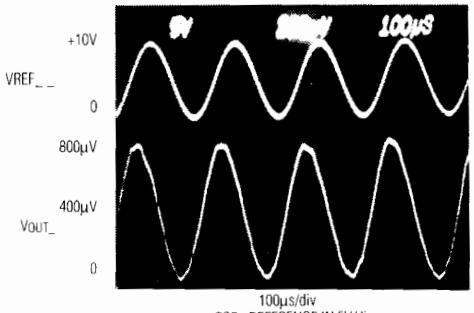
Typical Operating Characteristics (continued)

MAX526
REFERENCE
FEEDTHROUGH AT 400Hz



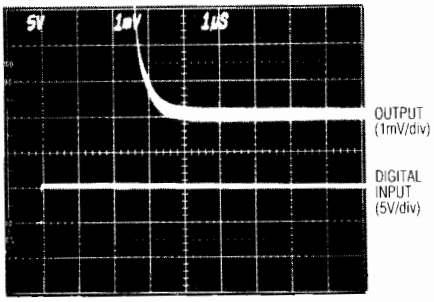
1ms/div
TOP: REFERENCE IN 5V/div
BOTTOM: V_{OUTA} 100µV/div
INPUT CODE – ALL 0s

MAX526
REFERENCE
FEEDTHROUGH AT 4000Hz



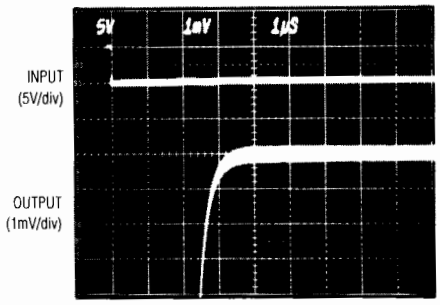
100µs/div
TOP: REFERENCE IN 5V/div
BOTTOM: V_{OUTA} 200µV/div
INPUT CODE – ALL 0s

MAX526
POSITIVE SETTLING TIME TO FULL-SCALE STEP – ALL BITS OFF TO ALL BITS ON



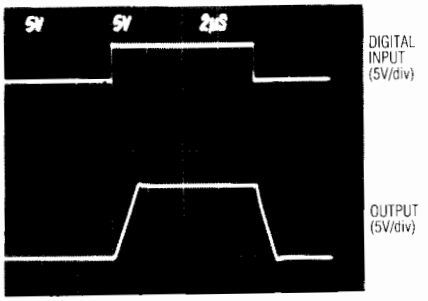
VREF = 10V, C_L = 100pF, R_L = 5kΩ

MAX526
NEGATIVE SETTLING TIME TO FULL-SCALE STEP – ALL BITS ON TO ALL BITS OFF



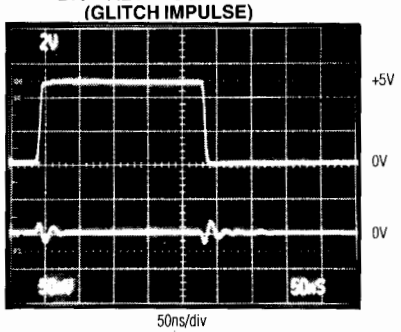
VREF – 10V, C_L – 100pF, R_L – 5kΩ

MAX526
DYNAMIC RESPONSE
ALL BITS OFF, ON, OFF



V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, C_L = 100pF, R_L = 5kΩ

MAX526
DIGITAL FEEDTHROUGH
(GLITCH IMPULSE)



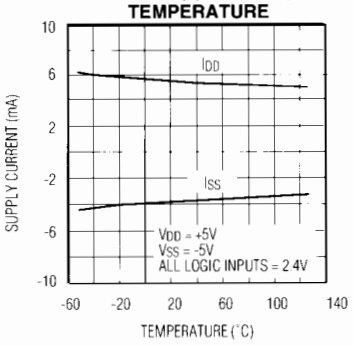
50ns/div
TOP: DIGITAL TRANSITION ON ALL DATA BITS 5V/div
BOTTOM: DAC OUPUT WITH WR HIGH 50mV/div

Calibrated Quad 12-Bit Voltage-Output D/A Converters

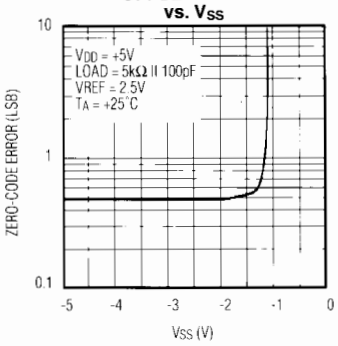
Typical Operating Characteristics

MAX527

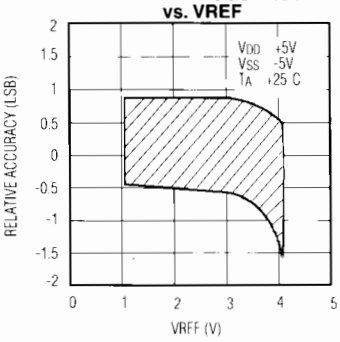
MAX527 SUPPLY CURRENT vs. TEMPERATURE



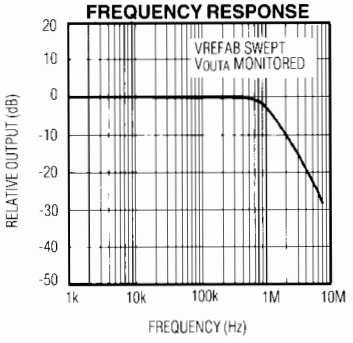
MAX527 OFFSET ERROR vs. VSS



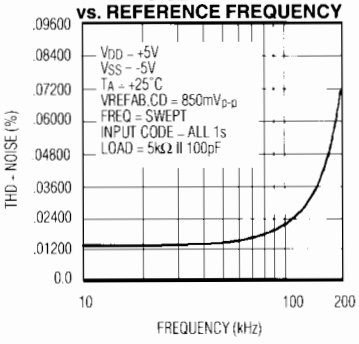
MAX527 RELATIVE ACCURACY vs. VREF



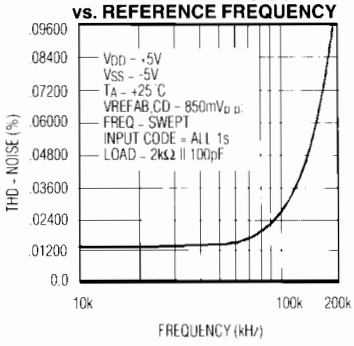
MAX527 REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



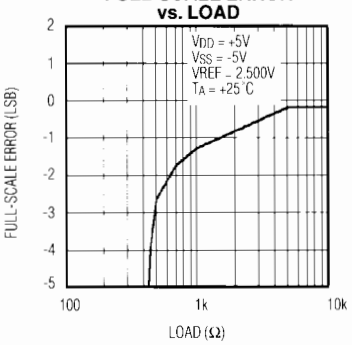
MAX527 THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



MAX527 THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY

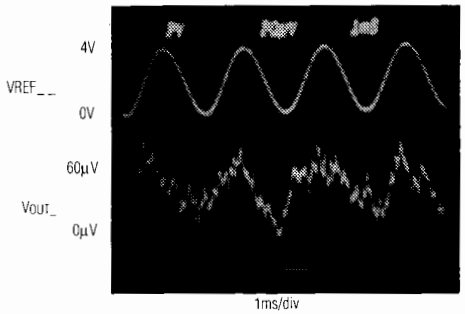


MAX527 FULL-SCALE ERROR vs. LOAD



Typical Operating Characteristics (continued)

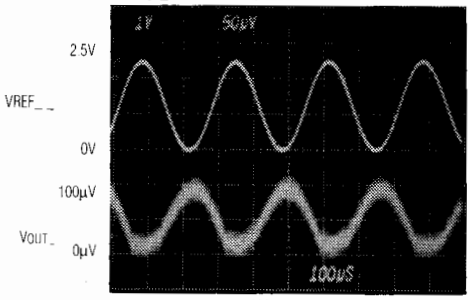
MAX527
REFERENCE
FEEDTHROUGH AT 400Hz



1ms/div

TOP: REFERENCE IN 2V/div
BOTTOM: VOUTA 20µV/div
INPUT CODE = ALL 0s

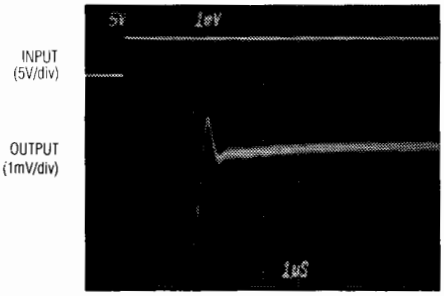
MAX527
REFERENCE
FEEDTHROUGH AT 4000Hz



100µs/div

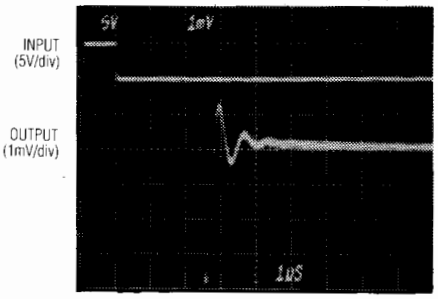
TOP: REFERENCE IN 5V/div
BOTTOM: VOUTA 50µV/div
INPUT CODES = ALL 0s

MAX527
POSITIVE SETTLING TIME TO FULL-SCALE STEP–ALL BITS OFF TO ALL BITS ON



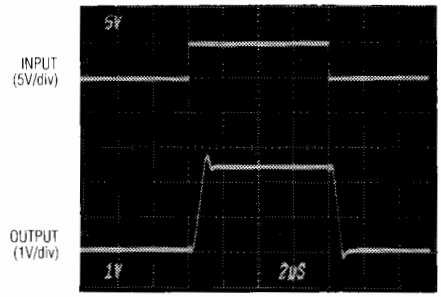
C_L = 100pF, R_L = 5kΩ, VREF = 2.5V

MAX527
NEGATIVE SETTLING TIME TO FULL-SCALE STEP–ALL BITS ON TO ALL BITS OFF



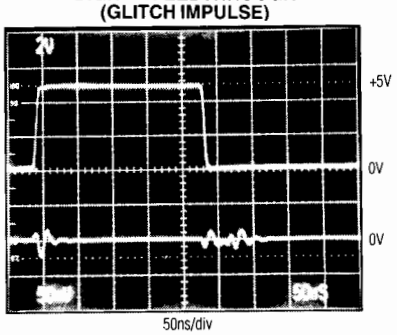
C_L = 100pF, R_L = 5kΩ, VREF = 2.5V

MAX527
DYNAMIC RESPONSE
ALL BITS OFF, ON, OFF



V_{DD} = +5V, V_{SS} = -5V, VREF = 2.5V, C_L = 100pF, R_L = 5kΩ

MAX527
DIGITAL FEEDTHROUGH
(GLITCH IMPULSE)



50ns/div

TOP: DIGITAL TRANSITION ON ALL DATA BITS 5V/div
BOTTOM: DAC OUPUT WITH WR HIGH 50mV/div

Calibrated Quad 12-Bit Voltage-Output D/A Converters

Pin Description

PIN	NAME	FUNCTION
1	V_{OUTC}	DAC C Output Voltage
2	V_{OUTB}	DAC B Output Voltage
3	V_{OUTA}	DAC A Output Voltage
4	V_{SS}	Negative Power Supply
5	AGND	Analog Ground
6	VREFAB	Reference Voltage Input for DAC A and DAC B
7	DGND	Digital Ground
8	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of each input register to its respective DAC register.
9	D7	Data Bit 7
10	D6	Data Bit 6
11	D5	Data Bit 5
12	D4	Data Bit 4
13	D11/D3	Data Bit 11 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 3 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
14	D10/D2	Data Bit 10 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 2 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
15	D9//D1	Data Bit 9 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 1 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
16	D8/D0	Data Bit 8 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 0 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
17	A1	DAC Address Select Bit (MSB)
18	A0	DAC Address Select Bit (LSB)
19	VREFCD	Reference Voltage Input for DAC C and DAC D
20	$\overline{WR}$	Write Input (active low). $\overline{WR}$ along with $\overline{CSMSB}$ and $\overline{CSLSB}$ load data into the DAC input register selected by A1 and A0.
21	$\overline{CSLSB}$	Chip Select for LS Byte (active low). Selects the lower 8 bits of the addressed input register.
22	$\overline{CSMSB}$	Chip Select for MS Nibble (active low). Selects the upper 4 bits of the addressed input register.
23	V_{DD}	Positive Supply Voltage
24	V_{OUTD}	DAC D Output Voltage

Detailed Description

Analog Section

The MAX526/MAX527 contain four voltage output DACs. The DACs are "inverted" R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltages. The MAX526/MAX527 have two reference inputs: one shared by DAC A and DAC B (VREFAB), and the other shared by DAC C and DAC D (VREFCD). These inputs allow different full-scale output voltage ranges for each pair of DACs (Figure 1).

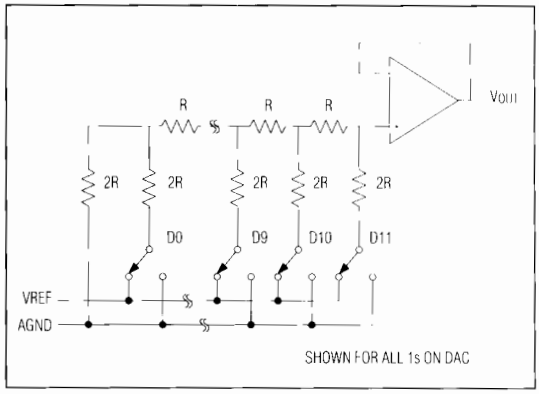


Figure 1. Simplified DAC Circuit Diagram

Reference Input

The MAX526/MAX527 can be used for multiplying applications. The reference accepts both DC and AC signals. The voltage at each VREF input sets the full-scale output voltages for its respective DACs. The input impedance of the VREF inputs are code dependent, with the lowest value (typically 6kΩ for VREFAB or VREFCD) occuring when the input code is 0101 0101 0101. The maximum value, typically 60kΩ, occurs when the input code is 0000 0000 0000. Since the input impedance at VREF is code dependent, load regulation of the reference used is important.

The guaranteed minimum input impedance of each reference input of the MAX526/MAX527 is 5kΩ. When the reference inputs are driven from the same source, the minimum impedance that must be driven by the reference source is 2.5kΩ. A voltage reference such as the MAX674 would typically deviate by 0.165LSB (0.33LSB worst case) when simultaneously driving both MAX526 reference inputs at 10V. Improve accuracy by driving VREFAB and VREFCD separately or by using a reference with excellent accuracy and superior load regulation, such as the MAX676/MAX677/MAX678.

Using an op amp to buffer the reference is another way to obtain high accuracy. The closed-loop output impedance of the op amp should be kept below 0.05Ω. This ensures errors of less than 0.08LSB when driving both reference inputs simultaneously. The MAX400 or OP07 are suitable for this application. The input capacitance at VREF is also code dependent and typically varies from 125pF to 300pF.

V_{OUTA-D} are represented by a digitally programmable voltage source as:

$$V_{OUT} = (N_B \times VREF) / 4096$$

where N_B is the numeric value of the DAC's binary input code (0 to 4095).

Output Buffer Amplifiers

All MAX526/MAX527 voltage outputs are internally buffered by precision unity-gain followers with a typical slew rate of 5V/µs for the MAX526 and 3V/µs for the MAX527.

With a full-scale transition at the MAX526 output (0V to +10V or +10V to 0V), the typical settling time to ±1/2LSB is 3µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance). Typical output dynamic response and settling performance of the MAX526 output amplifier are shown in the *Typical Operating Characteristics* section.

With a full-scale transition at the MAX527 output (0V to +2.5V or +2.5V to 0V), the typical settling time to ±1/2LSB is 5µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance). Typical output dynamic response and settling performance of the MAX527 output amplifiers are shown in the *Typical Operating Characteristics* section.

Digital Inputs and Interface Logic

Digital inputs are compatible with both TTL and 5V CMOS logic. The MAX526/MAX527 interface with microprocessors using an 8-bit-wide data bus. The double-buffered input structure consists of a 12-bit (8 + 4) input register and a 12-bit DAC register for each of the four DACs.

Each DAC's analog output reflects the data held in its DAC register. Address lines A0 and A1 select which DAC receives data from the data bus, as shown in Table 1. All MAX526/MAX527 control inputs are level-triggered. Figure 2 shows the MAX526/MAX527 input control logic.

Table 1. DAC Addressing

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

$\overline{CSMSB}$, $\overline{CSLSB}$, and $\overline{WR}$ load from the data bus to the input register selected by A0 and A1. Pulling $\overline{CSLSB}$ and $\overline{WR}$ low loads the lower 8 bits of the input register, while $\overline{CSMSB}$ and $\overline{WR}$ load the upper 4 bits. The order in which the data is loaded into the input register (i.e. upper 4 bits first or lower 8 bits first) is not important. It is possible to concurrently load the full 12 bits of the input register by pulling $\overline{CSLSB}$, $\overline{CSMSB}$, and $\overline{WR}$ low. Note that the same data will be written to the 4MSBs (D11-D8) and the 4LSBs (D3-D0), respectively. If the DACs are configured in the unipolar output mode (see Figure 5 and Table 3), this method can be used to quickly zero the DAC outputs.

Data is latched into the selected input register on the rising edge of $\overline{WR}$. Alternatively, data will be latched into

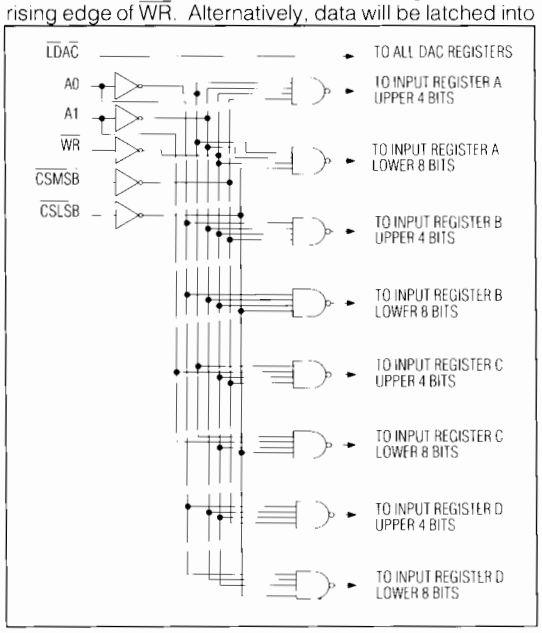


Figure 2. Input Control Logic

Calibrated Quad 12-Bit Voltage-Output D/A Converters

Table 2. Write-Cycle Truth Table

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	FUNCTION
L	H	L	H	Loads LS byte into selected input register
L	H	↓	H	Latches LS byte into selected input register
↓	H	L	H	Latches LS byte into selected input register
H	L	L	H	Loads MS nibble into selected input register
H	L	↓	H	Latches MS nibble into selected input register
H	↓	L	H	Latches MS nibble into selected input register
X	X	H	L	Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers
X	X	H	↓	Latches the four DAC registers. Input registers cannot be written to.
H	L	L	L	Loads MS nibble into selected input register and loads input registers into DAC registers.
↓	X	H	H	No operation. Device is not selected.
L	L	L	L	Loads all 12 bits of selected input register. Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers.
L	L	L	H	Loads all 12 bits into selected input register.
L	H	L	L	Loads LS byte into selected input register. Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers.
H	H	L	L	Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers.
H	H	L	H	No operation

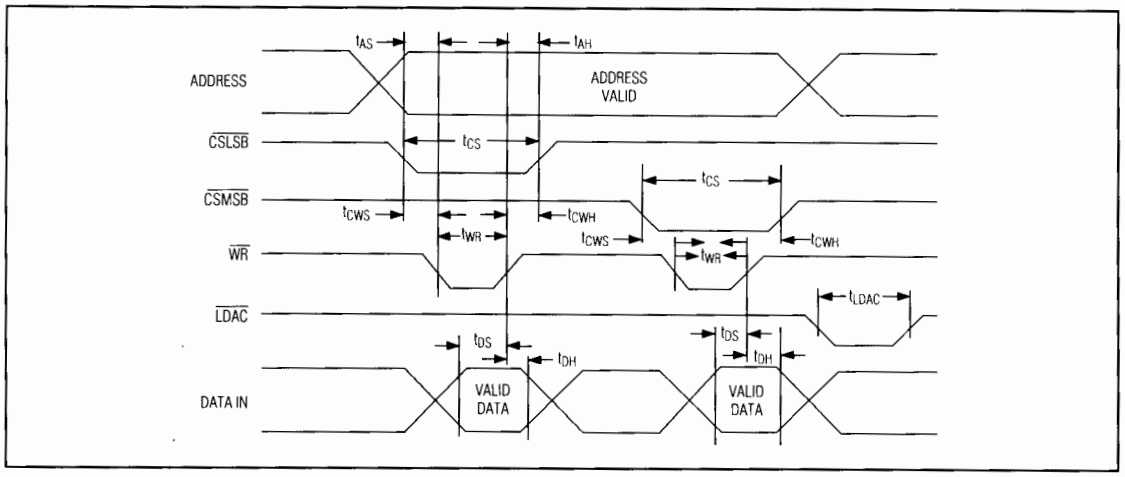


Figure 3. Write-Cycle Timing

the lower 8 bits of the input register on the rising edge of CSLSB, and the upper 4 bits will be latched on the rising edge of CSMSB.

Data is transferred from all input registers to the DAC registers by pulling LDAC low. This simultaneously updates all four DACs. Since LDAC is asynchronous with respect to WR, be sure that incorrect data is not latched to the output. Table 2 shows the truth table for operation of WR, LDAC, CSLSB, and CSMSB. Figure 3 shows the MAX526 /MAX527write-cycle timing.

Application Information

Ground Management

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground available. If separate ground buses are used, two clamp diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND. This will ensure that the two ground pins always remain within one diode drop of each other.

Careful PCB ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Figure 4 shows a suggested circuit-board layout for minimizing crosstalk.

Unipolar Output

In unipolar operation, the output voltages and the reference inputs are the same polarity. Figure 5 shows the MAX526/MAX527 unipolar output circuit. The unipolar output codes are listed in Table 3.

Table 3. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+VREF\left(\frac{4095}{4096}\right)$
1000	0000	0001	$+VREF\left(\frac{2049}{4096}\right)$
1000	0000	0000	$+VREF\left(\frac{2048}{4096}\right)=\frac{+VREF}{2}$
0111	1111	1111	$+VREF\left(\frac{2047}{4096}\right)$
0000	0000	0001	$+VREF\left(\frac{1}{4096}\right)$
0000	0000	0000	0V

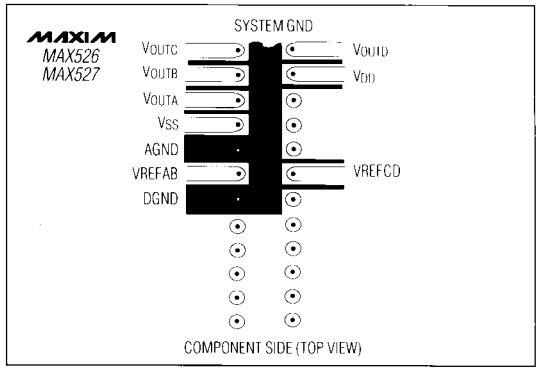


Figure 4. Suggested PCB Layout for Minimizing Crosstalk

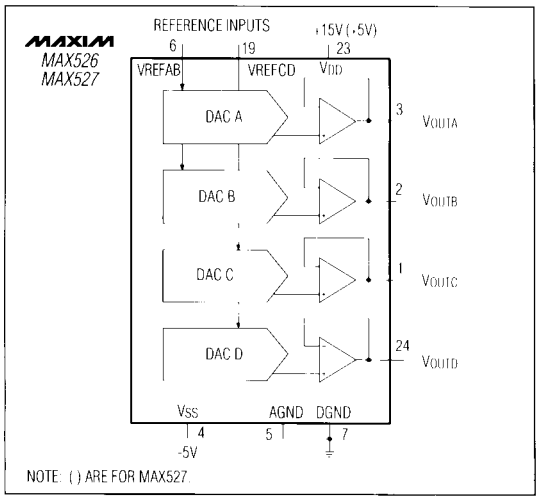


Figure 5. Unipolar Output Circuit

Bipolar Output

The MAX526/MAX527 outputs may be configured for bipolar output operation using Figure 6's circuit. One op amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = VREF\ ((2N_B / 4096) - 1)$$

where N_B is the numeric value of the DAC's binary input code.

Table 4 shows the digital code vs. output voltage for the circuit in Figure 6.

Calibrated Quad 12-Bit Voltage-Output D/A Converters

Using an AC Reference

In applications where VREF has AC signal components, the MAX526/MAX527 have multiplying capability within the VREF input range specifications. Figure 7 shows a technique for applying a sine wave signal to the reference input where the AC signal is offset before being applied to VREF. Note that VREF must never be more negative than DGND.

Total harmonic distortion plus noise (THD + N) of the MAX526 is typically less than 0.012% with input frequencies up to 35kHz for $5V_{p-p}$ swing; up to 50kHz for 2V swing. The typical -3dB frequency is 700kHz, as shown in the *Typical Operating Characteristics* graphs.

For the MAX527, THD + N is typically less than 0.024% with input frequencies up to 100kHz, a signal amplitude of 850mV, and a load of 5kΩ in parallel with 100pF. With a 2kΩ load in parallel with 100pF, the MAX527's THD is below 0.024% for input frequencies up to 95kHz.

Table 4. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+VREF\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+VREF\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-VREF\left(\frac{1}{2048}\right)$
0000	0000	0001	$-VREF\left(\frac{2047}{2048}\right)$
0000	0000	0000	$-VREF\left(\frac{2048}{2048}\right) = -VREF$

NOTE: $1LSB = (VREF)\left(\frac{1}{4096}\right)$

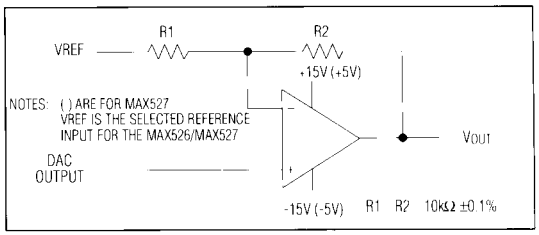


Figure 6. Bipolar Output Circuit

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "0" input code. This application is shown in Figure 8. The output voltage at V_{OUTA} is:

$$V_{OUTA} = V_{BIAS} + N_B \times V_{IN}$$

where N_B is the numeric value of the DAC's binary input code. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Note that AGND should not be biased more negative than DGND

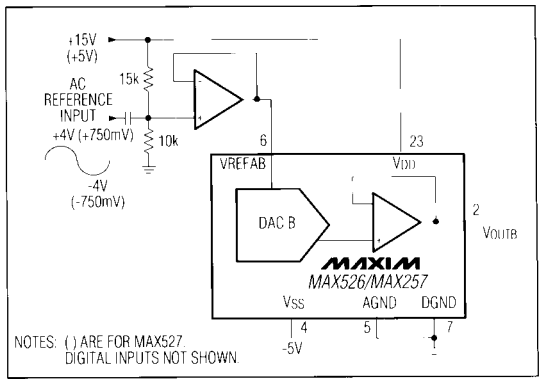


Figure 7. AC Reference Input Circuit

Supply Voltage and Decoupling

For full MAX526 performance, V_{DD} should be 4V higher than VREF in the 10.8V to 16.5V range. When using the MAX527, V_{DD} should be at least 2.2V higher than VREF in the 4.75V to 5.5V range. Both V_{DD} and V_{SS} supplies should be bypassed with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND, with short lead lengths as close to the supply pins as possible.

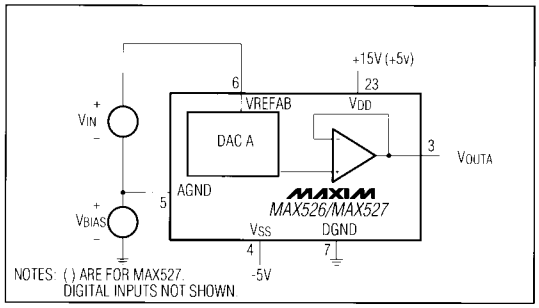


Figure 8. AGND Bias Circuit

Power-Supply Sequencing

On power-up, V_{SS} should come up first, V_{DD} next, followed by VREFAB or VREFCD. If supply sequencing is not possible, tie an external Schottky diode between V_{SS} and AGND as shown in Figure 9.

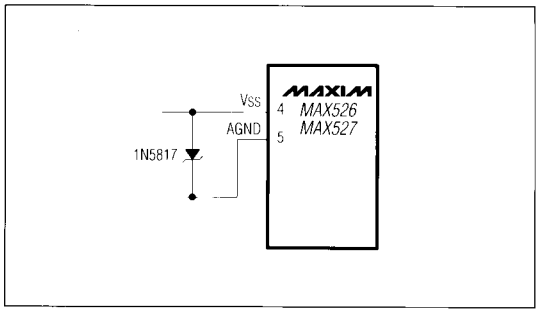


Figure 9. When V_{SS} and V_{DD} cannot be sequenced, tie a Schottky diode between V_{SS} and AGND.

Calibrated Quad 12-Bit Voltage-Output D/A Converters

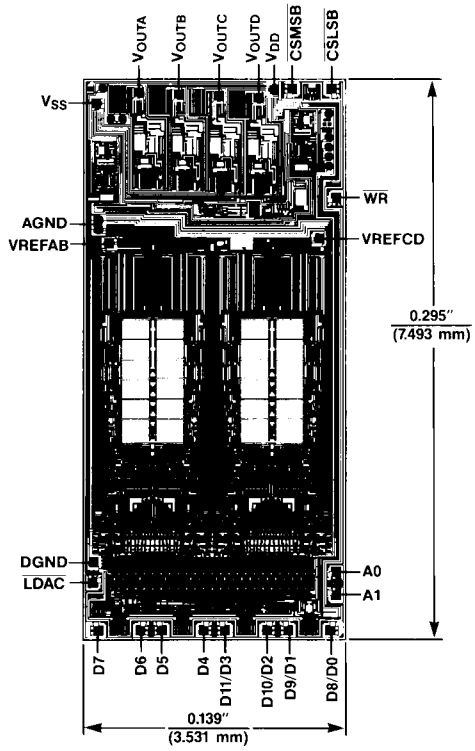
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX527CCNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX527DCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX527CCWG	0°C to +70°C	24 Wide SO	±1/2
MAX527DCWG	0°C to +70°C	24 Wide SO	±1
MAX527DC/D	0°C to +70°C	Dice*	±1
MAX527CENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX527DENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX527CEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX527DEWG	-40°C to +85°C	24 Wide SO	±1
MAX527CMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1/2
MAX527DMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography

MAX526/MAX527



SUBSTRATE CONNECTS TO V_{DD}.
TRANSISTOR COUNT: 2720.

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