



**THE DATASHEET OF
MAX768EEE+**





Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

MAX768

General Description

The MAX768 low-noise, dual-output, regulated charge pump provides a negative output for biasing GaAsFET power amplifiers, and a positive output for powering voltage-controlled oscillators (VCOs) in wireless handsets. The outputs can also be used to power LCDs. Output ripple is less than 2mVp-p. The MAX768 is intended for use in low-voltage systems where a simple charge-pump inverter is inadequate, or where the VCO needs more range to improve its signal-to-noise ratio. The input range is 2.5V to 5.5V, enabling direct power from 1Li+ and 3-cell NiMH/NiCd batteries.

The MAX768 includes a voltage-doubler charge pump, followed by an inverting charge pump. This combination produces unregulated outputs that are $\pm 2x$ the input. Two internal low-dropout linear regulators provide the low-noise, regulated positive and negative outputs. Output current is guaranteed to be at least 5mA per output. The linear regulators use CMOS devices, so the quiescent current remains independent of output loading (even in dropout), and the dropout voltage approaches zero with no load current.

The MAX768 has two preset switching frequencies (25kHz or 100kHz), or can be synchronized by an external clock from 20kHz to 240kHz. This flexibility permits users to optimize their designs based on noise, capacitor size, and quiescent-supply-current criteria.

The device features Dual Mode™ operation: the output voltage is preset to +5V and -5V, or can be adjusted by adding external resistor dividers. Other features include independent shutdowns and a logic output that signals when the negative voltage has risen to within 10% of its regulation setpoint (to protect the power amplifier GaAsFET). The MAX768 is available in a space-saving, 16-pin QSOP, which is the same size as a standard 8-pin SO.

Applications

- GaAsFET Power Amp Bias
- Voltage-Controlled Oscillator (VCO) Supply
- Tuner Diode Power Supply
- Positive and Negative LCD Supply
- Cellular Phone
- PCS and Cordless Phone
- Wireless Handsets
- Wireless Handheld Computers
- Wireless PCMCIA Cards
- Modems

Features

- ♦ **Dual Positive/Negative Regulated Outputs: $\pm 5V_{OUT}$ from $3V_{IN}$**
- ♦ **Output-Ready Indicator to Protect GaAsFET PAs**
- ♦ **2.5V to 5.5V Input Voltage Range**
- ♦ **Low-Noise Output Ripple: $< 2mV_{p-p}$**
- ♦ **Synchronizable Switching Frequency**
- ♦ **Uses Only Small, Low-Cost Capacitors**
- ♦ **0.1 μ A Independent Shutdown Controls**
- ♦ **Adjustable Output Voltages**
- ♦ **Small 16-Pin QSOP Package**

Ordering Information

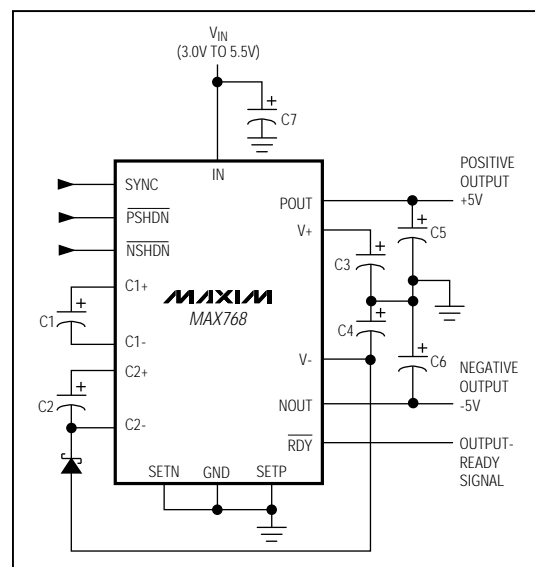
PART	TEMP. RANGE	PIN-PACKAGE
MAX768C/D	0°C to +70°C	Dice*
MAX768EEE	-40°C to +85°C	16 QSOP

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Pin Configuration appears at end of data sheet.

Dual Mode is a trademark of Maxim Integrated Products.

Typical Operating Circuit



Maxim Integrated Products 1

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ABSOLUTE MAXIMUM RATINGS

V _{IN} , C1-, SYNC, PSHDN, NSHDN to GND	-0.3V to +6V	Continuous Power Dissipation (T _A = +70°C)	
V+, C1+, C2+, RDY to GND	-0.3V to +12V	QSOPT (derate 8.70mW/°C above +70°C)	696mW
SETP to GND	-0.3V to +3V	Operating Temperature Range	
SETN to GND	-3V to +0.3V	MAX768EEE	-40°C to +85°C
V-, C2- to GND	-12V to +0.3V	Maximum Junction Temperature	+150°C
OUTP, OUTN Short Circuited to GND	Continuous	Storage Temperature Range	-65°C to +165°C
NOUT to V-	-0.3V to +12V	Lead Temperature (soldering, 10sec)	+300°C
POUT to V+	-12V to +0.3V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, SYNC = IN, SETN = SETP = GND, NSHDN = PSHDN = IN, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 2.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		3.0		5.5	V
Minimum Input Start-Up Voltage	I _{LOAD} = 0		2.5		V
Positive Output Voltage	0mA < I _{LOAD} < 5mA, V _{IN} = 3.0V to 5.5V	4.81	5.00	5.14	V
Negative Output Voltage	0mA < I _{LOAD} < 5mA, V _{IN} = 3.0V to 5.5V	-5.10	-5.00	-4.82	V
Positive Output Voltage Adjustable Range	(Note 2)	1.25		11	V
Negative Output Voltage Adjustable Range	(Note 3)	-11		-1.25	V
Maximum POUT, NOUT Output Currents	V _{IN} = 3V, V _{POUT} ≥ 4.81V, V _{NOUT} ≤ -4.82V	5			mA
No-Load Supply Current at 100kHz (both regulators active)	V _{IN} = 3.0V		0.8	1.4	mA
	V _{IN} = 5.5V		1.5		
No-Load Supply Current at 100kHz (negative regulator off)	NSHDN = GND		0.3		mA
No-Load Supply Current at 25kHz (both regulators active)	V _{SYNC} = GND		0.45	0.80	mA
Dropout Voltage (2 × V _{IN} - V _{OUT})	2 × V _{IN} - V _{OUT}	I _{POUT} = I _{NOUT} = 0.1mA		20	mV
		I _{POUT} = I _{NOUT} = 5mA		420 900	
Line Regulation	V _{IN} = 3V to 5.5V	-0.12	0.0	0.12	%/V
Load Regulation	I _{POUT} = 0mA to 5mA, I _{NOUT} = 0mA to -5mA		0.06	0.12	%/mA
Output Voltage Noise	C _{POUT} = C _{NOUT} = 10μF, 10kHz < f < 1MHz	POUT		1.2	mVp-p
		NOUT		1.7	
Shutdown/SYNC Logic-Low Input Threshold				0.4	V
Shutdown/SYNC Logic-High Input Threshold		2.0			V
SHUTDOWN					
SHDN Input Bias Current	V _{SHDN} = 3V		0.1	2	μA
Shutdown Supply Current	NSHDN = PSHDN = SYNC = GND		0.1	10	μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = +3V$, $SYNC = IN$, $SETN = SETP = GND$, $\overline{NSHDN} = \overline{PSHDN} = IN$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. See Figure 2.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
SYNC						
SYNC Frequency Range (external)		20		240	kHz	
SYNC Duty Cycle (external)		40		60	%	
Oscillator Frequency (internal)	SYNC = GND (divide by 4)	21.5	25	28.5	kHz	
	$V_{SYNC} = 3V$	85	100	115		
SYNC Input Leakage Current			0.1	2	μA	
SET INPUT						
Positive Set-Reference Voltage	$I_{POUT} = 0.1mA$	$T_A = +25^\circ C$	1.217	1.25	1.283	V
		$T_A = -40^\circ C$ to $+85^\circ C$	1.215	1.25	1.285	
Negative Set-Reference Voltage	$I_{NOUT} = 0.1mA$	$T_A = +25^\circ C$	-1.270	-1.25	-1.230	V
		$T_A = -40^\circ C$ to $+85^\circ C$	-1.275	-1.25	-1.225	
SETP, SETN Input Leakage Current	$V_{SETP} = V_{SETN} = 1.3V$		0.01	0.1	μA	
RDY OUTPUT						
\overline{RDY} Output Threshold	Percent of V_{NOUT} , $I_{NOUT} = 5mA$	85	94	98	%	
Output Low Voltage	$I_{SINK} = 2mA$			0.25	V	
Output Off Current	$V_{RDY} = 10V$		0.01	2	μA	
Maximum Sink Current			10		mA	

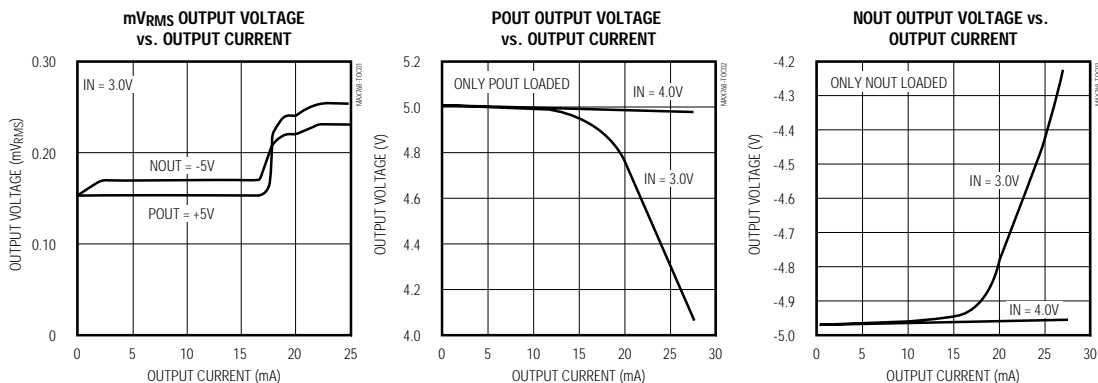
Note 1: Parameters to $-40^\circ C$ are guaranteed by design, not production tested.

Note 2: Maximum output voltage range is from the positive reference voltage to $2 \times V_{IN}$ - dropout voltage.

Note 3: Maximum output voltage range is from the negative reference voltage to $-2 \times V_{IN}$ + dropout voltage.

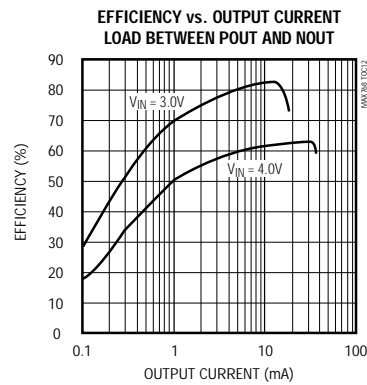
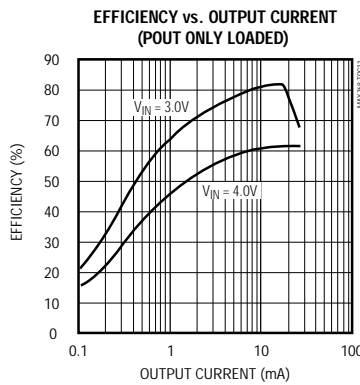
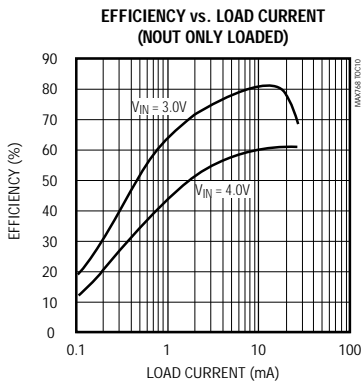
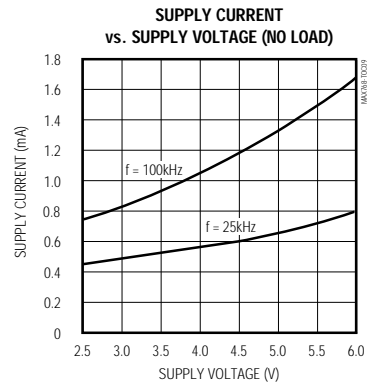
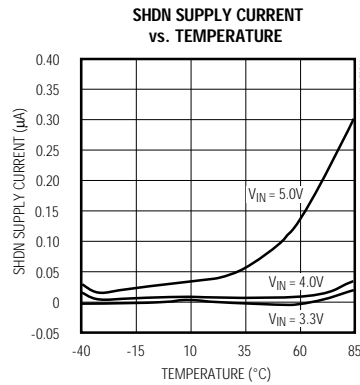
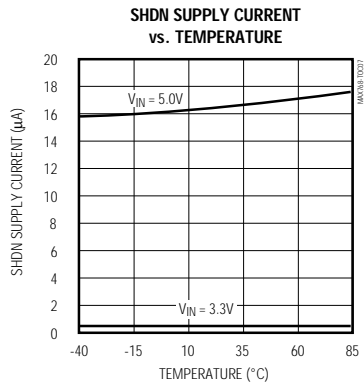
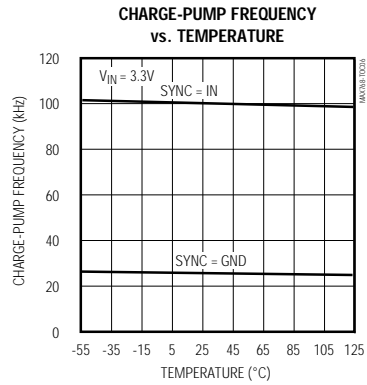
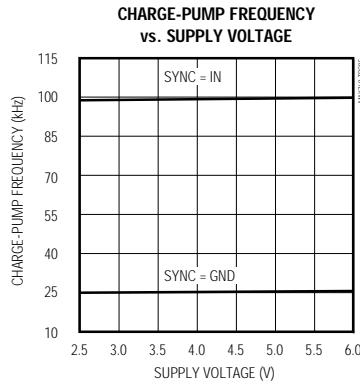
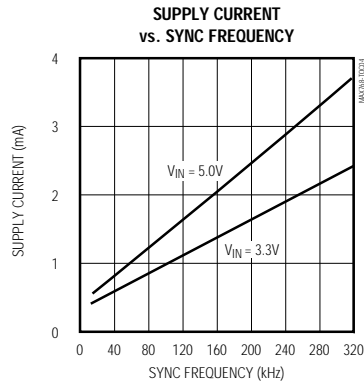
Typical Operating Characteristics

($SYNC = IN$, $T_A = +25^\circ C$, unless otherwise noted.)



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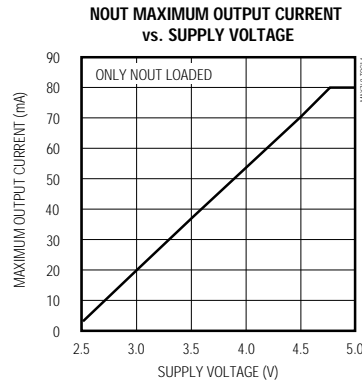
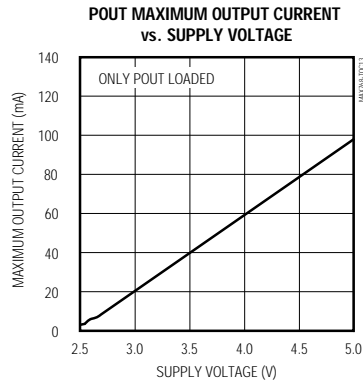
Typical Operating Characteristics (continued)
 (SYNC = IN, T_A = +25°C, unless otherwise noted.)



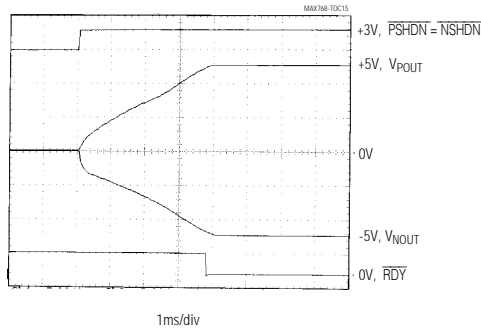
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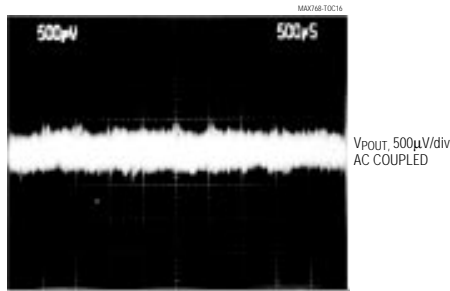
Typical Operating Characteristics (continued)
 (SYNC = IN, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



TIME TO EXIT SHUTDOWN

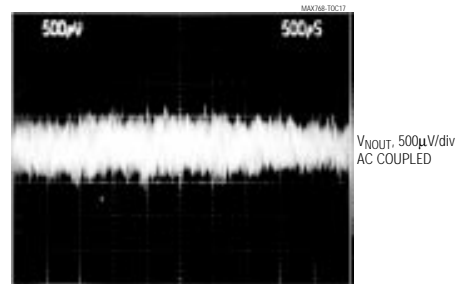


POUT OUTPUT NOISE AND RIPPLE



POUT = +5V AT 5mA
 IN = 3.0V

NOUT OUTPUT NOISE AND RIPPLE



NOUT = -5V AT 5mA
 IN = 3.0V

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Pin Description

PIN	NAME	FUNCTION
1	C1-	Negative Terminal of the Doubler Charge-Pump Capacitor. See Table 2 for capacitor selection.
2	GND	Ground
3	C2-	Negative Terminal of the Inverter Charge-Pump Capacitor
4	V-	Inverter Charge-Pump Output. See Table 2 for capacitor selection.
5	NOUT	Negative Regulator Output. See Table 2 for capacitor selection.
6	SETN	Set Negative Output Voltage Input. Connect SETN to GND for factory-preset -5V. Connect a resistor divider between NOUT, SETN, and GND for custom output voltage setting.
7	$\overline{\text{NSHDN}}$	Negative-Supply Shutdown Input. Pull $\overline{\text{NSHDN}}$ low to turn off the inverting charge pump, the negative regulator, and the bias-ready indicator. If $\overline{\text{PSHDN}}$ is also low, the part completely shuts down.
8	$\overline{\text{PSHDN}}$	Positive-Supply Shutdown Input. Pull $\overline{\text{PSHDN}}$ low to turn off the positive regulator. If $\overline{\text{NSHDN}}$ is also low, the part completely shuts down.
9	SYNC	Clock Synchronizing Input. Connect an external $20\text{kHz} \leq f_{\text{CLK}} \leq 240\text{kHz}$ to SYNC to synchronize the MAX768 to that frequency. Connect SYNC to GND to select the internal 25kHz clock, or to IN for the internal 100kHz clock.
10	$\overline{\text{RDY}}$	Output-Ready Indicator. This open-drain output pulls to GND when the negative output voltage (NOUT) is within 10% of the regulation voltage.
11	SETP	Set Positive Output Voltage Input. Connect SETP to GND for factory-preset +5V output. Connect a resistor divider between POUT, SETP, and GND for custom output voltage setting.
12	POUT	Positive Regulator Output. See Table 2 for capacitor selection.
13	V+	Doubler Charge-Pump Output. See Table 2 for capacitor selection.
14	C1+	Positive Terminal of the Doubler Charge-Pump Capacitor. See Table 2 for capacitor selection.
15	IN	Supply (3V to 5.5V). Bypass IN with 4.7 μF to GND.
16	C2+	Positive Terminal of the Inverter Charge-Pump Capacitor. See Table 2 for capacitor selection.

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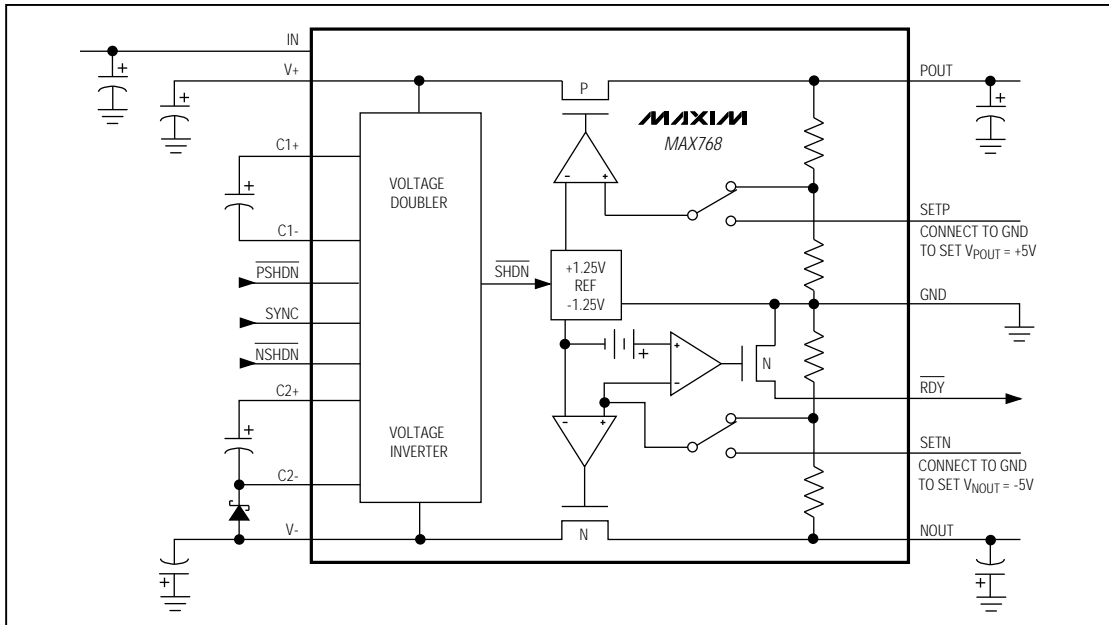


Figure 1. Functional Diagram

Detailed Description

The MAX768 requires only seven external capacitors to implement a regulated voltage doubler/inverter. These can be ceramic or polarized electrolytic capacitors ranging from 2.2μF to 47μF. Figure 1 is a functional diagram of the MAX768. The applied input voltage (V_{IN}) is first doubled to a value of $2V_{IN}$ by a capacitor charge pump and then stored in the V_+ reservoir capacitor. Next, the voltage at V_+ is inverted to $-2V_{IN}$ and stored at the V_- reservoir capacitor. The voltages at V_+ and V_- are then linearly regulated and appear at $POUT$ and $NOUT$, respectively. The ripple noise induced by the doubling and inverting charge pump is reduced by the linear regulators to 1.2mVp-p for $POUT$ and 1.7mVp-p for $NOUT$. In addition, the linear regulator's excellent AC rejection attenuates noise from the incoming supply. A minimum of 5mA is available at each output. When $NOUT$ is more negative than 90% of the regulated output voltage, the open-drain RDY output pulls to GND.

The charge pump operates in three modes: when $\overline{SYNC} = GND$, the charge pump operates at 25kHz; when $\overline{SYNC} = IN$, it operates at 100kHz, or \overline{SYNC} can be overdriven with an external clock in the 20kHz to 240kHz range. The clock must have a 40% to 60% duty cycle.

Applications Information

Setting the Output Voltage

Connect $SETP$ or $SETN$ directly to GND to select a fixed +5V or -5V output voltage, respectively (Figure 2). Select an alternative voltage for either output by connecting $SETP$ or $SETN$ to the midpoint of a resistor voltage divider from $POUT$ or $NOUT$, respectively, to GND (Figure 3). ($2 \times V_{IN}$) must be 1.0V above the absolute value of the output voltage to ensure proper regulation. Calculate the output voltage from the formulas below. Choose $R1$ and $R3$ at between 100kΩ to 400kΩ.

$$R2 = (R1) \left(\frac{V_{POUT}}{V_{PSET REF}} - 1 \right)$$

$$R4 = (R3) \left(\frac{V_{NOUT}}{V_{NSET REF}} - 1 \right)$$

where $V_{PSET REF} = 1.25V$ (typical) and $V_{NSET REF} = -1.25V$ (typical).

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Table 1. Shutdown-Control Logic

PSHDN	NSHDN	POUT STATUS	NOUT STATUS	SUPPLY CURRENT (mA)
1	1	Positive output active	Negative output active	0.8
1	0	Positive output active	Negative output inactive	0.7
0	1	Positive output inactive	Negative output active	0.3
0	0	Shutdown (low-power mode)	Shutdown (low-power mode)	0.0001

Table 2. Charge-Pump Capacitor Selection (Figure 2)

SYNC INPUT	FREQUENCY (kHz)	CAPACITORS		
		C1, C2, C3, C4	C5, C6	C7
GND	25	10µF	10µF	4.7µF
IN	100	2.2µF		
External Clock	20 to 240	C = 220µF/f (kHz)		

Shutdown

The MAX768 has two active-low, TTL logic-level shutdown inputs: PSHDN and NSHDN. When both inputs are pulled low, the MAX768 shuts down and the supply current is reduced to 10µA max over temperature. Pulling PSHDN low turns off the positive linear regulator; the doubler charge pump remains active. Pulling the NSHDN input low while PSHDN remains high turns off the inverter charge pump, the negative linear regulator, and the output-ready indicator (Table 1).

Capacitors

The overall dropout voltage is a function of the charge pump's output resistance and the voltage drop across the linear regulator. The charge-pump output resistance is a function of the switching frequency and the capacitor's ESR value. Therefore, minimizing the charge-pump capacitors' ESR minimizes dropout voltage.

$$R_{POUT} = 84 + 8(C1_{ESR}) + (C3_{ESR}) + \frac{2}{f_{OSC}C1}$$

$$R_{NOUT} = 84 + 8(C1_{ESR}) + 4(C2_{ESR}) + (C4_{ESR}) + \frac{2}{f_{OSC}C1} + \frac{1}{f_{OSC}C2}$$

See Table 2 for capacitor selection. All capacitors should be either surface-mount ceramic chip or tantalum. External capacitor values may be adjusted to optimize size, performance, and cost.

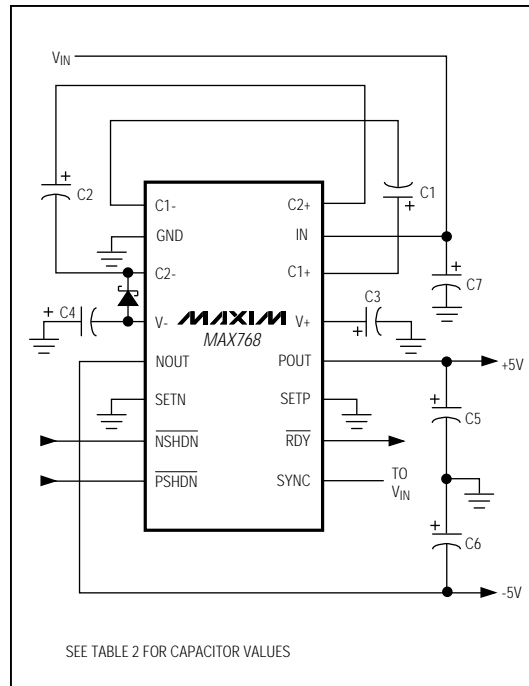


Figure 2. MAX768 Standard Application Circuit

Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

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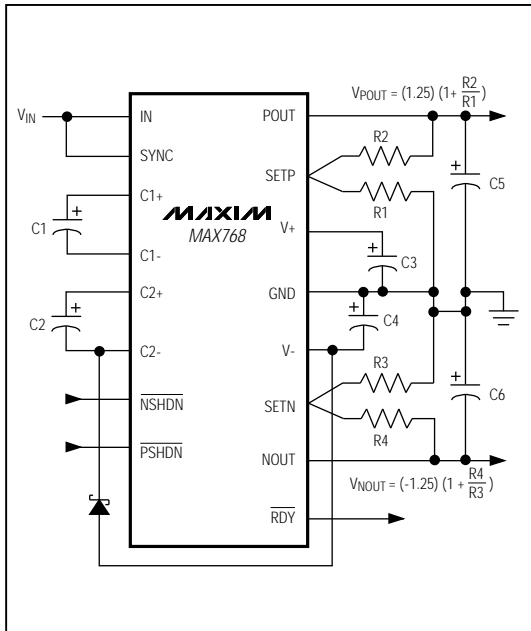


Figure 3. MAX768 Adjustable Configuration

Switching-Frequency Control

For applications sensitive to the MAX768's internal switching frequency, connect an external TTL/CMOS (within IN and GND) clock to SYNC. The clock must be a 20kHz to 240kHz square wave between 40% and 60% duty cycle.

Schottky Diodes

When under heavy loads, where POUT is sourcing into NOUT (i.e., load current flows from POUT to NOUT, rather than from supply to ground), do not allow NOUT to pull above ground. In applications where large currents from POUT to NOUT are likely, use a Schottky diode (1N5817) between GND and NOUT, with the anode connected to GND (Figure 4).

Connect a 1N5817-type Schottky diode from C2- to V- to assure proper start-up.

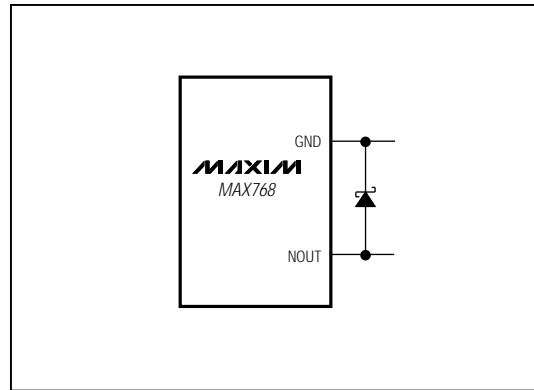


Figure 4. A Schottky diode protects the MAX768 when a large current flows from POUT to NOUT.

Layout and Grounding

Good layout is important, primarily for good noise performance:

- 1) Mount all components as close together as possible.
- 2) Keep traces short to minimize parasitic inductance and capacitance. This includes connections to SETP and SETN.
- 3) Use a ground plane.

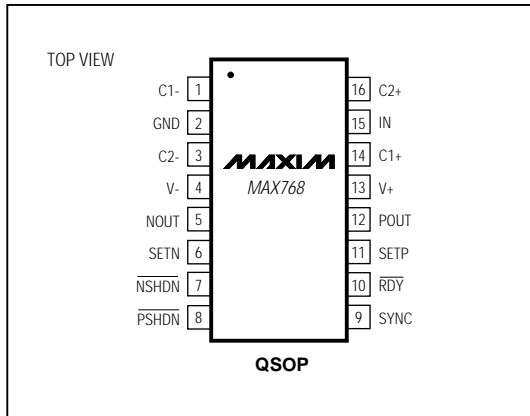
Noise and Ripple Measurement

Accurately measuring output noise and ripple can be difficult. Brief differences in ground potential between the circuit and the oscilloscope (which result from the charge pump's switching action) cause ground currents in the probe's wires, inducing sharp voltage spikes. For best results, measure directly across output capacitor C3, C4, C5, or C6. Do not use the oscilloscope probe's ground lead; instead, remove the cover's ground lead and touch the ground ring on the probe directly to the ground terminal of C3, C4, C5, or C6. Or, use a Tektronix chassis-mount test jack (part no. 131-0258) to connect your scope probe directly. This direct connection provides the most accurate noise and ripple measurement.

Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

Pin Configuration

Chip Information

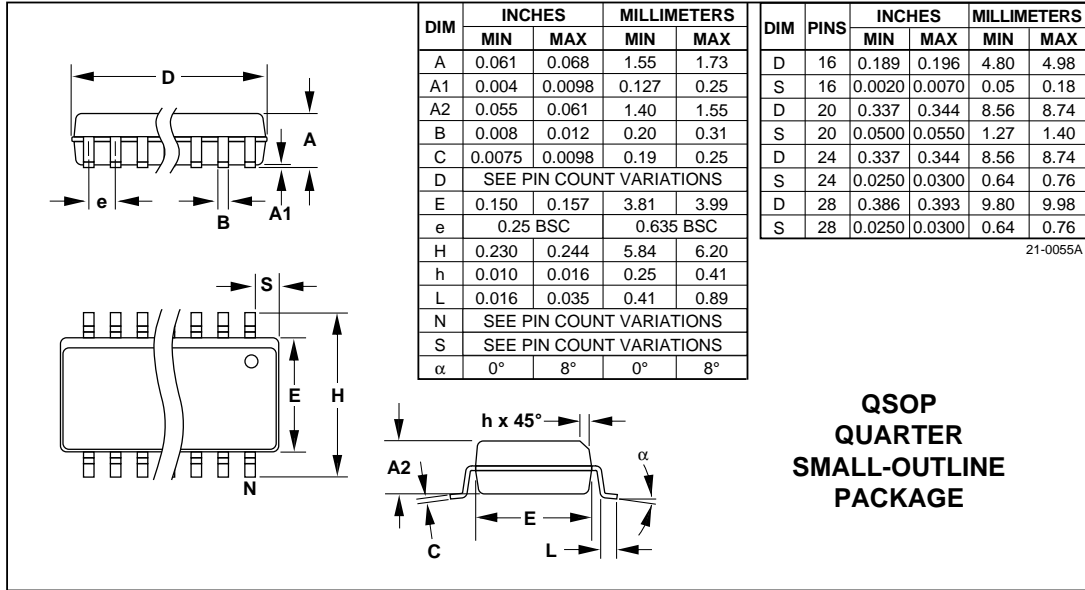


TRANSISTOR COUNT: 657
 SUBSTRATE CONNECTED TO GND

Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

Package Information

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NOTES

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