



**THE DATASHEET OF  
MB3773PF-G-BND-JNE1**





**MB3773**

## Power Supply Monitor with Watch-Dog Timer

### Description

MB3773 generates the reset signal to protect an arbitrary system when the power-supply voltage momentarily is intercepted or decreased. It is IC for the power-supply voltage watch and "Power on reset" is generated at the normal return of the power supply. MB3773 sends the microprocessor the reset signal when decreasing more than the voltage, which the power supply of the system specified, and the computer data is protected from an accidental deletion.

In addition, the watch-dog timer for the operation diagnosis of the system is built into, and various microprocessor systems can provide the fail-safe function. If MB3773 does not receive the clock pulse from the processor for a specified period, MB3773 generates the reset signal.

### Features

- Precision voltage detection ( $V_S = 4.2\text{ V} \pm 2.5\%$ )
- Detection threshold voltage has hysteresis function
- Low voltage output for reset signal ( $V_{CC} = 0.8\text{ V Typ}$ )
- Precision reference voltage output ( $V_R = 1.245\text{ V} \pm 1.5\%$ )
- With built-in watch-dog timer of edge trigger input.
- External parts are few.(1 piece in capacity)
- The reset signal outputs the positive and negative both theories reason.
- One type of package (SOP-8pin : 1 type)

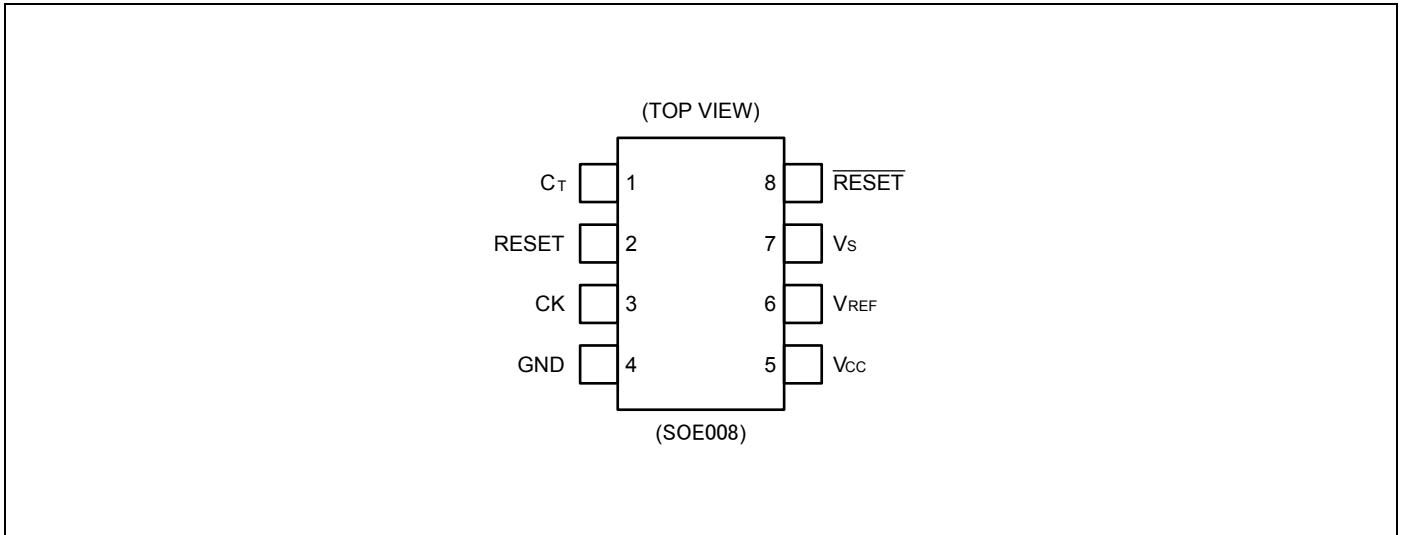
### Application

- Industrial Equipment
- Arcade Amusement etc.

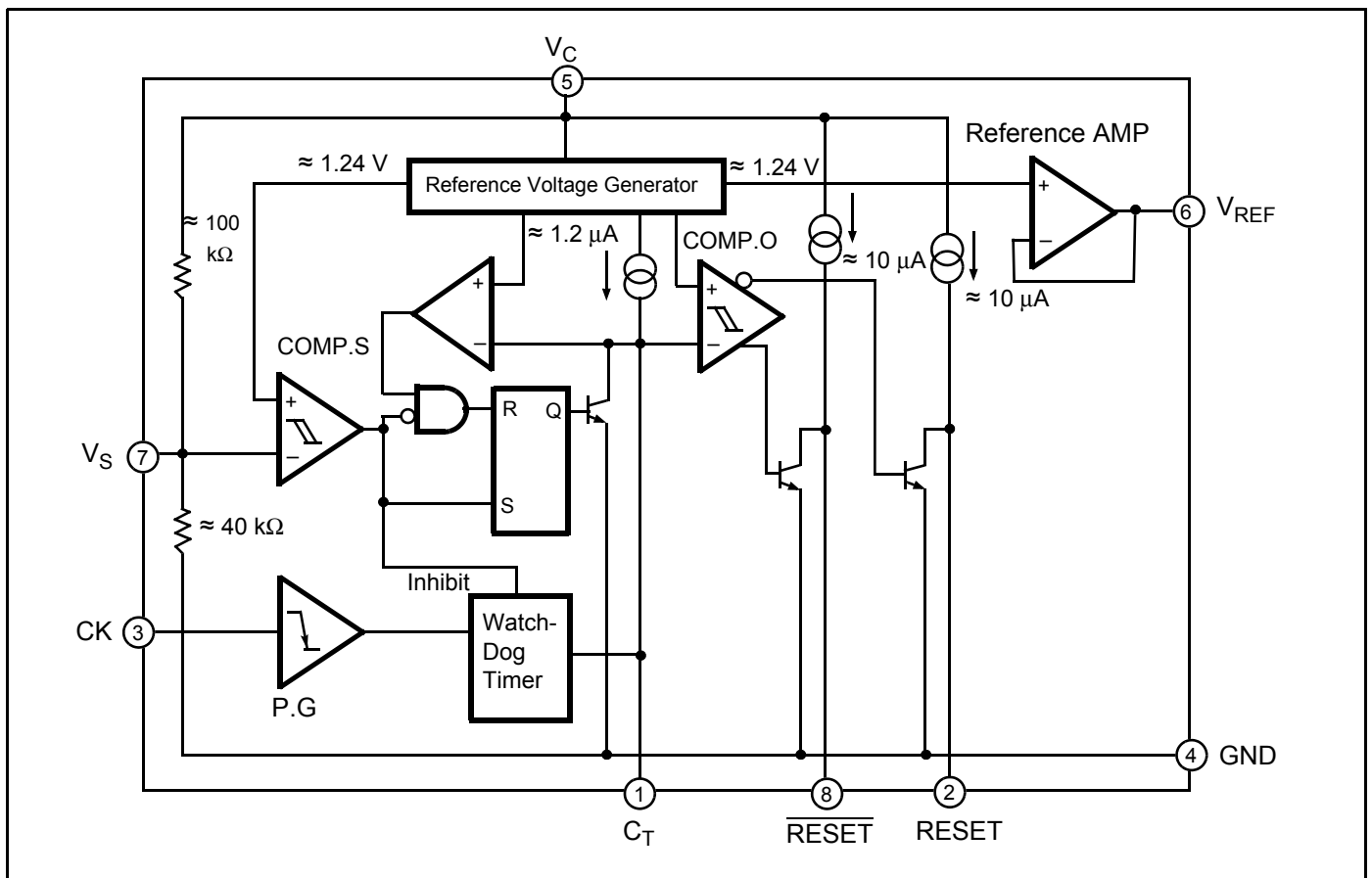
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### 1. Pin Assignment



### 2. Block Diagram



### 3. Functional Descriptions

Comp.S is comparator including hysteresis. It compares the reference voltage and the voltage of  $V_s$ , so that when the voltage of  $V_s$  terminal falls below approximately 1.23 V, reset signal outputs.

Instantaneous breaks or drops in the power can be detected as abnormal conditions by the MB3773 within a 2  $\mu$ s interval.

However, because momentary breaks or drops of this duration do not cause problems in actual systems in some cases, a delayed trigger function can be created by connecting capacitors to the  $V_s$  terminal.

Comp.O is comparator for turning on/off the RESET/RESET outputs and compares the voltage of the  $C_T$  terminal and the threshold voltage. Because the RESET/RESET outputs have built-in pull-up circuit, there is no need to connect to external pull-up resistor when connected to a high impedance load such as CMOS logic IC.

(It corresponds to 500 k $\Omega$  at  $V_{CC} = 5$  V.) when the voltage of the CK terminal changes from the "high" level into the "Low" level, pulse generator is sent to the watch-dog timer by generating the pulse momentarily at the time of drop from the threshold level.

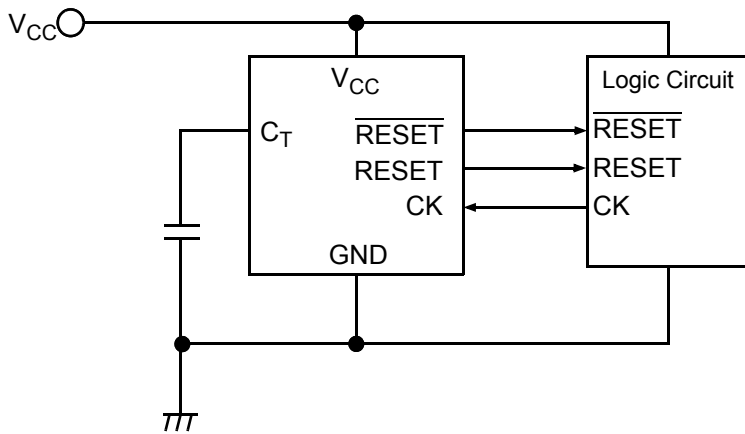
When power-supply voltages fall more than detecting voltages, the watch-dog timer becomes an interdiction.

The Reference amplifier is an op-amp to output the reference voltage.

If the comparator is put up outside, two or more power-supply voltage monitor and overvoltage monitor can be done.

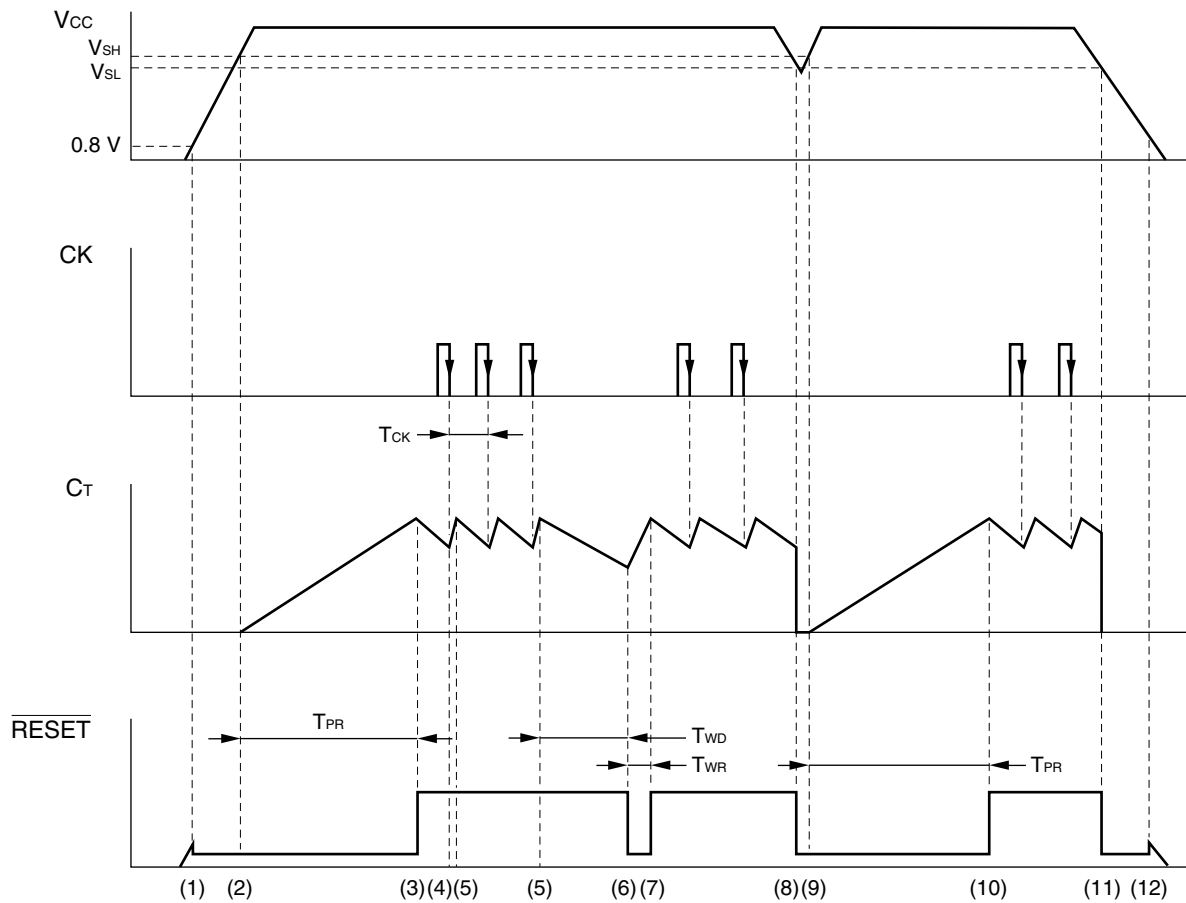
If it uses a comparator of the open-collector output, and the output of the comparator is connected with the  $V_s$  terminal of MB3773 without the pull-up resistor, it is possible to voltage monitor with reset-hold time.

MB3773 Basic Operation



$T_{PR} \text{ (ms)} \approx 1000 \cdot C_T \text{ (\mu F)}$   
 $T_{WD} \text{ (ms)} \approx 100 \cdot C_T \text{ (\mu F)}$   
 $T_{WR} \text{ (ms)} \approx 20 \cdot C_T \text{ (\mu F)}$

Example :  $C_T = 0.1 \mu\text{F}$   
 $T_{RR} \text{ (ms)} \approx 100 \text{ (ms)}$   
 $T_{WD} \text{ (ms)} \approx 10 \text{ (ms)}$   
 $T_{WR} \text{ (ms)} \approx 2 \text{ (ms)}$



## 4. Operation Sequence

1. When  $V_{CC}$  rises to about 0.8 V,  $\overline{\text{RESET}}$  goes “Low” and RESET goes “High”.  
The pull-up current of approximately 1  $\mu\text{A}$  ( $V_{CC} = 0.8 \text{ V}$ ) is output from RESET.
2. When  $V_{CC}$  rises to  $V_{SH}$  ( $\approx 4.3\text{V}$ ), the charge with  $C_T$  starts.  
At this time, the output is being reset.
3. When  $C_T$  begins charging,  $\overline{\text{RESET}}$  goes “High” and RESET goes “Low”.  
After  $T_{PR}$  reset of the output is released.  
Reset hold time:  $T_{PR} (\text{ms}) \approx 1000 \times C_T (\mu\text{F})$   
After releasing reset, the discharge of  $C_T$  starts, and watch-dog timer operation starts.  
 $T_{PR}$  is not influenced by the CK input.
4. C changes from the discharge into the charge if the clock (Negative edge) is input to the CK terminal while discharging  $C_T$ .
5. C changes from the charge into the discharge when the voltage of  $C_T$  reaches a constant threshold ( $\approx 1.4 \text{ V}$ ).  
4 and 5 are repeated while a normal clock is input by the logic system.
6. When the clock is cut off, gets, and the voltage of  $C_T$  falls on threshold ( $\approx 0.4 \text{ V}$ ) of reset on,  $\overline{\text{RESET}}$  goes “Low” and RESET goes “High”.  
Discharge time of  $C_T$  until reset is output:  $T_{WD}$  is watch-dog timer monitoring time.  
 $T_{WD} (\text{ms}) \approx 100 \times C_T (\mu\text{F})$   
Because the charging time of  $C_T$  is added at accurate time from stop of the clock and getting to the output of reset of the clock,  $T_{WD}$  becomes maximum  $T_{WD} + T_{WR}$  by minimum  $T_{WD}$ .
7. Reset time in operating watch-dog timer:  $T_{WR}$  is charging time where the voltage of  $C_T$  goes up to off threshold ( $\approx 1.4 \text{ V}$ ) for reset.  
 $T_{WR} (\text{ms}) \approx 20 \times C_T (\mu\text{F})$   
Reset of the output is released after  $C_T$  reaches an off threshold for reset, and  $C_T$  starts the discharge, after that if the clock is normally input, operation repeats 4 and 5, when the clock is cut off, operation repeats 6 and 7.
8. When  $V_{CC}$  falls on  $V_{SL}$  ( $\approx 4.2 \text{ V}$ ), reset is output.  $C_T$  is rapidly discharged of at the same time.
9. When  $V_{CC}$  goes up to  $V_{SH}$ , the charge with  $C_T$  is started.  
When  $V_{CC}$  is momentarily low,  
After falling  $V_{SL}$  or less  $V_{CC}$ , the time to going up is the standard value of the  $V_{CC}$  input pulse width in  $V_{SH}$  or more.  
After the charge of  $C_T$  is discharged, the charge is started if it is  $T_{PI}$  or more.
10. Reset of the output is released after  $T_{PR}$ , after  $V_{CC}$  becomes  $V_{SH}$  or more, and the watch-dog timer starts. After that, when  $V_{CC}$  becomes  $V_{SL}$  or less, 8 to 10 is repeated.
11. While power supply is off, when  $V_{CC}$  becomes  $V_{SL}$  or less, reset is output.
12. The reset output is maintained until  $V_{CC}$  becomes 0.8 V when  $V_{CC}$  falls on 0 V.

## 5. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply voltage	$V_{CC}$	- 0.3	+ 18	V
Input voltage	$V_S$	- 0.3	$V_{CC} + 0.3 (\leq +18)$	V
	$V_{CK}$	- 0.3	+ 18	V
$\overline{RESET}$ , RESET Supply voltage	$V_{OH}$	- 0.3	$V_{CC} + 0.3 (\leq +18)$	V
Power dissipation ( $T_a \leq +85^\circ\text{C}$ )	$P_D$	—	200	mW
Storage temperature	$T_{STG}$	- 55	+ 125	$^\circ\text{C}$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 6. Recommended Operating Conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Supply voltage	$V_{CC}$	+ 3.5	+ 16	V
RESET, $\overline{RESET}$ sink current	$I_{OL}$	0	20	mA
VREF output current	$I_{OUT}$	- 200	+ 5	$\mu\text{A}$
Watch clock setting time	$t_{WD}$	0.1	1000	ms
CK Rising/falling time	$t_{FC}, t_{RC}$	—	100	$\mu\text{s}$
Terminal capacitance	$C_T$	0.001	10	$\mu\text{F}$
Operating ambient temperature	$T_a$	- 40	+ 85	$^\circ\text{C}$

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.



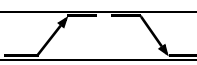
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

## 7. Electrical Characteristics

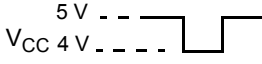
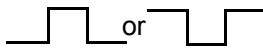

### 7.1 DC Characteristics

 $(V_{CC} = 5\text{ V}, T_a = +25^\circ\text{C})$ 

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply current	$I_{CC}$	Watch-dog timer operating	—	600	900	$\mu\text{A}$
Detection voltage	$V_{SL}$	$V_{CC}$ 	4.10	4.20	4.30	V
		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.05	4.20	4.35	
	$V_{SH}$	$V_{CC}$ 	4.20	4.30	4.40	
		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.15	4.30	4.45	
Hysteresis width	$V_{HYS}$	$V_{CC}$ 	50	100	150	mV
Reference voltage	$V_{REF}$	—	1.227	1.245	1.263	V
		$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.215	1.245	1.275	
Reference voltage change rate	$\Delta V_{REF1}$	$V_{CC} = 3.5\text{ V}$ to $16\text{ V}$	—	3	10	mV
Reference voltage output loading change rate	$\Delta V_{REF2}$	$I_{OUT} = -200\ \mu\text{A}$ to $+5\ \mu\text{A}$	-5	—	+5	mV
CK threshold voltage	$V_{TH}$	$T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	0.8	1.25	2.0	V
CK input current	$I_{IH}$	$V_{CK} = 5.0\text{ V}$	—	0	1.0	$\mu\text{A}$
	$I_{IL}$	$V_{CK} = 0.0\text{ V}$	-1.0	-0.1	—	
$C_T$ discharge current	$I_{CTD}$	Watch-dog timer operating $V_{CT} = 1.0\text{ V}$	7	10	14	$\mu\text{A}$
High level output voltage	$V_{OH1}$	$V_S$ open, $I_{\overline{\text{RESET}}} = -5\ \mu\text{A}$	4.5	4.9	—	V
	$V_{OH2}$	$V_S = 0\text{ V}$ , $I_{\overline{\text{RESET}}} = -5\ \mu\text{A}$	4.5	4.9	—	
Output saturation voltage	$V_{OL1}$	$V_S = 0\text{ V}$ , $I_{\overline{\text{RESET}}} = 3\text{ mA}$	—	0.2	0.4	V
	$V_{OL2}$	$V_S = 0\text{ V}$ , $I_{\overline{\text{RESET}}} = 10\text{ mA}$	—	0.3	0.5	
	$V_{OL3}$	$V_S$ open, $I_{\overline{\text{RESET}}} = 3\text{ mA}$	—	0.2	0.4	
	$V_{OL4}$	$V_S$ open, $I_{\overline{\text{RESET}}} = 10\text{ mA}$	—	0.3	0.5	
Output sink current	$I_{OL1}$	$V_S = 0\text{ V}$ , $V_{\overline{\text{RESET}}} = 1.0\text{ V}$	20	60	—	mA
	$I_{OL2}$	$V_S$ open, $V_{\overline{\text{RESET}}} = 1.0\text{ V}$	20	60	—	
$C_T$ charge current	$I_{CTU}$	Power on reset operating $V_{CT} = 1.0\text{ V}$	0.5	1.2	2.5	$\mu\text{A}$
Min supply voltage for $\overline{\text{RESET}}$	$V_{CCL1}$	$V_{\overline{\text{RESET}}} = 0.4\text{ V}$ , $I_{\overline{\text{RESET}}} = 0.2\text{ mA}$	—	0.8	1.2	V
Min supply voltage for RESET	$V_{CCL2}$	$V_{\overline{\text{RESET}}} = V_{CC} - 0.1\text{ V}$ , $R_L$ (between pin 2 and GND) = $1\text{ M}\Omega$	—	0.8	1.2	V

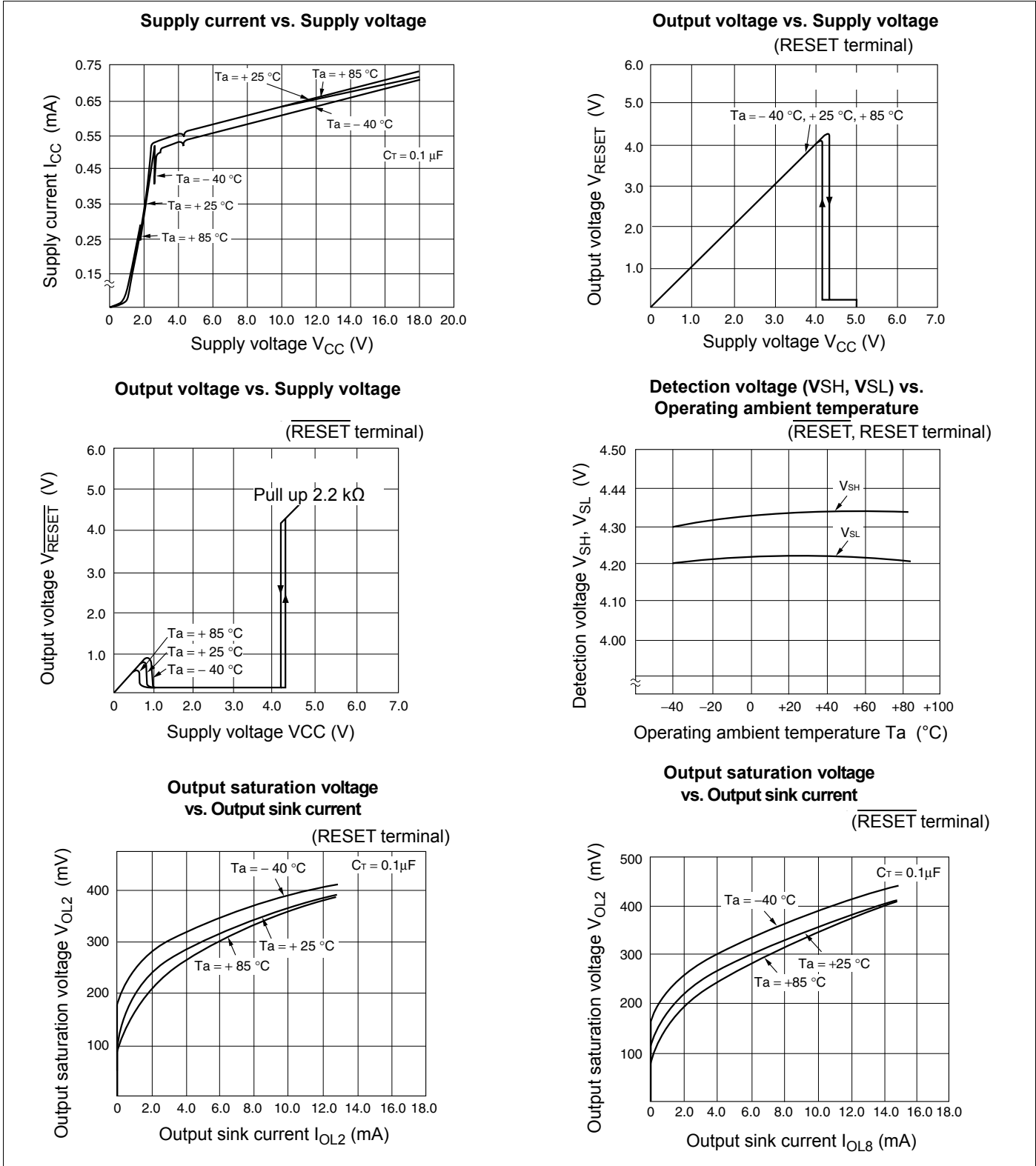
**7.2 AC Characteristics**

 (V<sub>CC</sub> = 5 V, Ta = + 25°C)

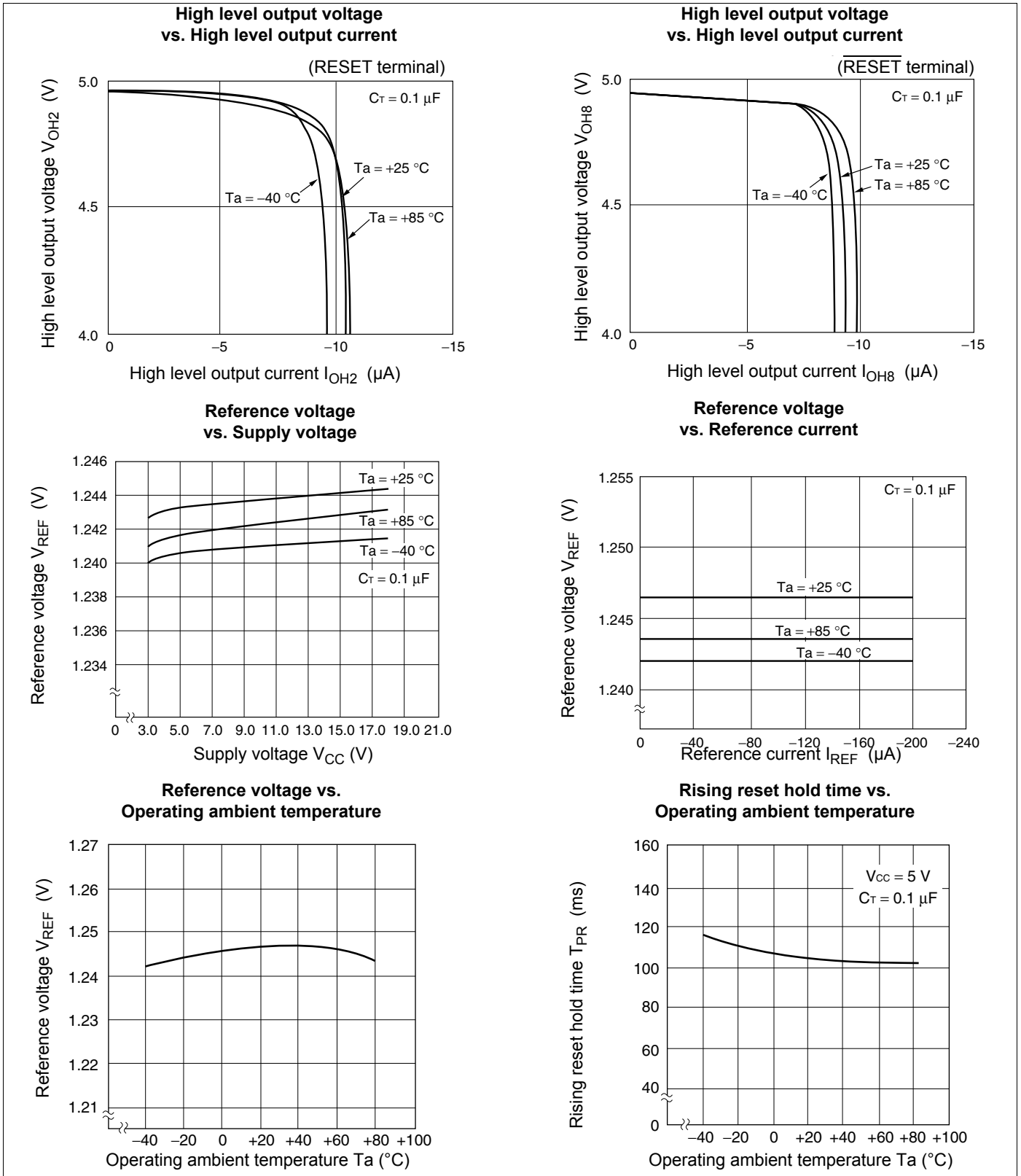
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
V <sub>CC</sub> input pulse width	T <sub>PI</sub>		8.0	—	—	μs
CK input pulse width	T <sub>CKW</sub>		3.0	—	—	μs
CK input frequency	T <sub>CK</sub>	—	20	—	—	μs
Watch-dog timer watching time	T <sub>WD</sub>	C <sub>T</sub> = 0.1 μF	5	10	15	ms
Watch-dog timer reset time	T <sub>WR</sub>	C <sub>T</sub> = 0.1 μF	1	2	3	ms
Rising reset hold time	T <sub>PR</sub>	C <sub>T</sub> = 0.1 μF, V <sub>CC</sub> 	50	100	150	ms
Output propagation delay time from VCC	T <sub>PD1</sub>	RESET, R <sub>L</sub> = 2.2 kΩ, C <sub>L</sub> = 100 pF	—	2	10	μs
	T <sub>PD2</sub>	RESET, R <sub>L</sub> = 2.2 kΩ, C <sub>L</sub> = 100 pF	—	3	10	
Output rising time*	t <sub>R</sub>	R <sub>L</sub> = 2.2 kΩ, C <sub>L</sub> = 100 pF	—	1.0	1.5	μs
Output falling time*	t <sub>F</sub>	R <sub>L</sub> = 2.2 kΩ, C <sub>L</sub> = 100 pF	—	0.1	0.5	

\* : Output rising/falling time are measured at 10 % to 90 % of voltage.

### 8. Typical Characteristic Curves



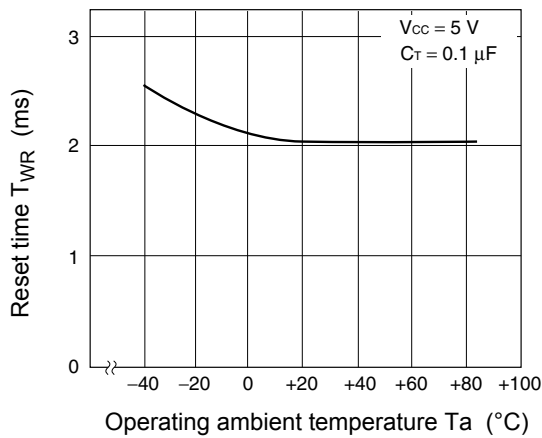
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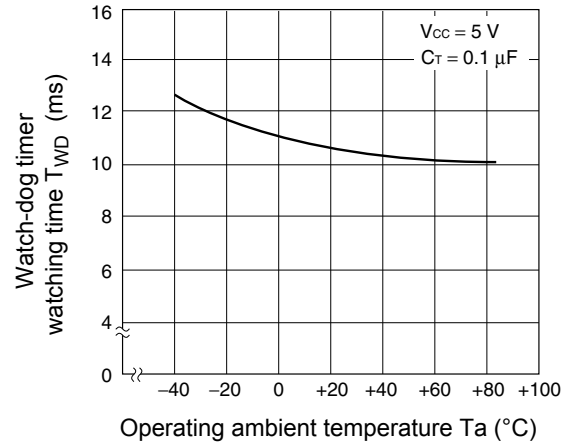
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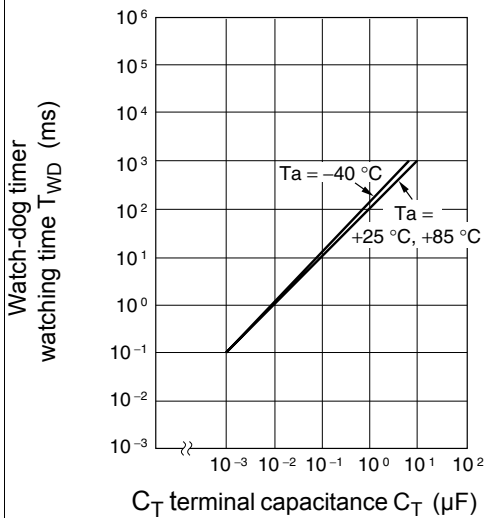
**Reset time vs.  
Operating ambient temperature**  
(At watch-dog timer)



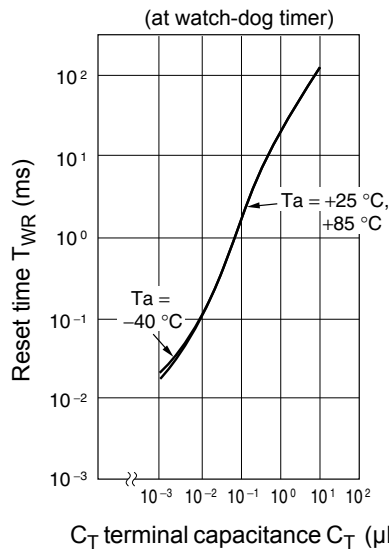
**Watch-dog timer watching time vs.  
Operating ambient temperature**



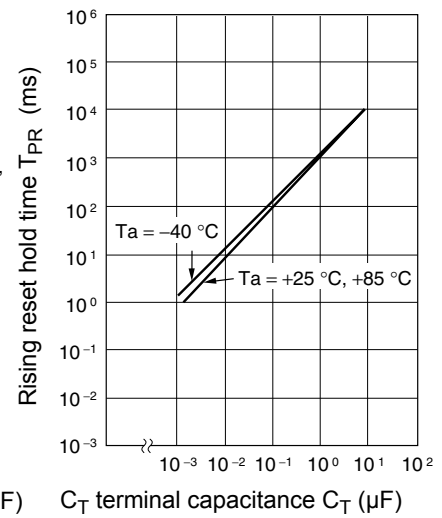
**Watch-dog timer watching time  
vs.  
 $C_T$  terminal capacitance**



**Reset time vs.  
 $C_T$  terminal capacitance**

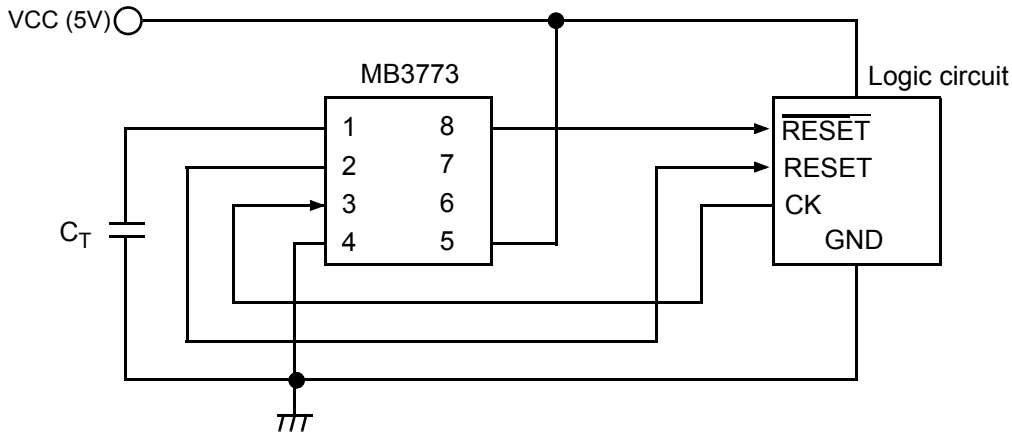


**Rising reset hold time vs.  
 $C_T$  terminal capacitance**



### 9. Application Circuit

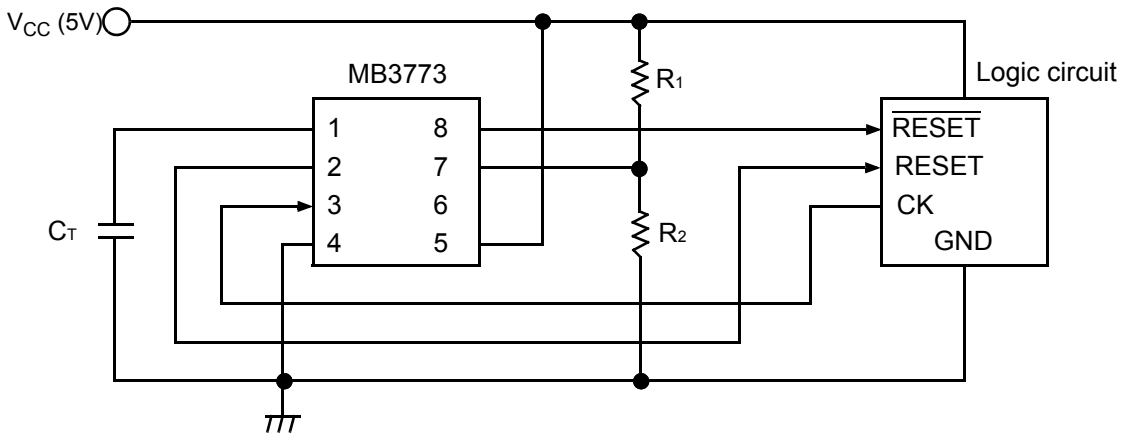
**EXAMPLE 1: Monitoring 5V Supply Voltage and Watch-dog Timer**



Notes :

- Supply voltage is monitored using  $V_S$ .
- Detection voltage are  $V_{SH}$  and  $V_{SL}$ .

**EXAMPLE 2: 5V Supply Voltage Monitoring (external fine-tuning type)**



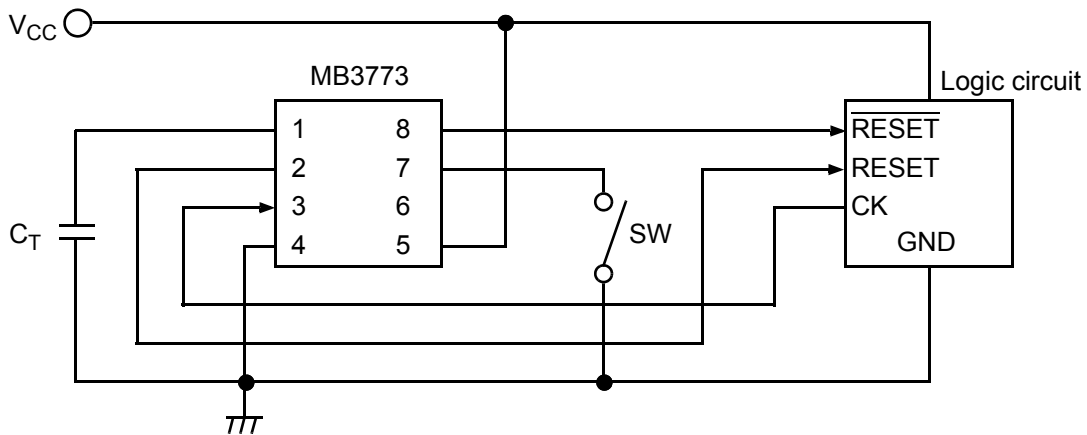
Notes :

- $V_S$  detection voltage can be adjusted externally.
- Based on selecting  $R_1$  and  $R_2$  values that are sufficiently lower than the resistance of the IC's internal voltage divider, the detection voltage can be set according to the resistance ratio of  $R_1$  and  $R_2$  (Refer to the table below.)

$R_1$ (k $\Omega$ )	$R_2$ (k $\Omega$ )	Detection voltage: $V_{SL}$ (V)	Detection voltage: $V_{SH}$ (V)
10	3.9	4.4	4.5
9.1	3.9	4.1	4.2

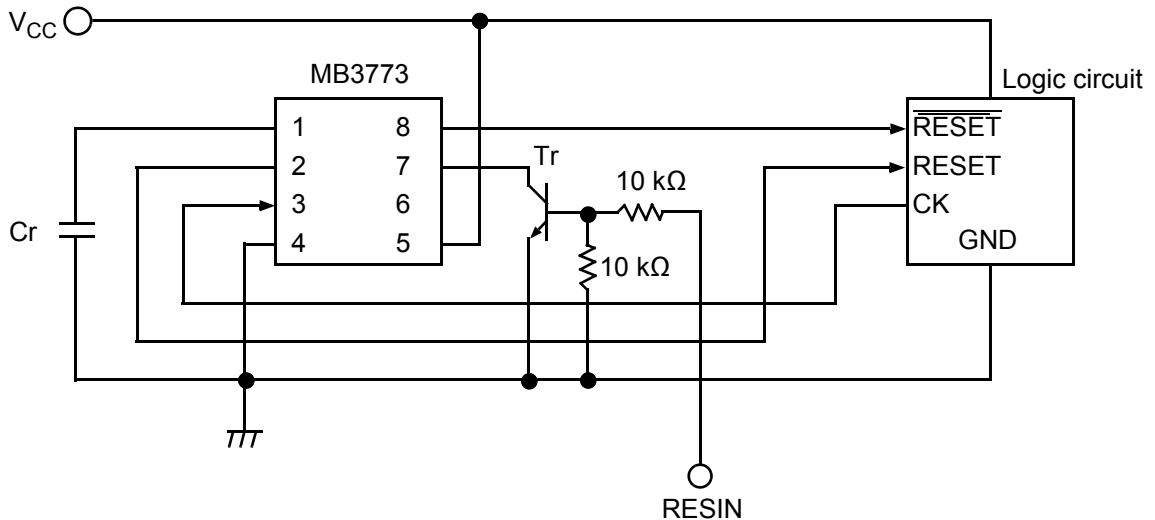
**EXAMPLE 3: With Forced Reset (with reset hold)**

(a)

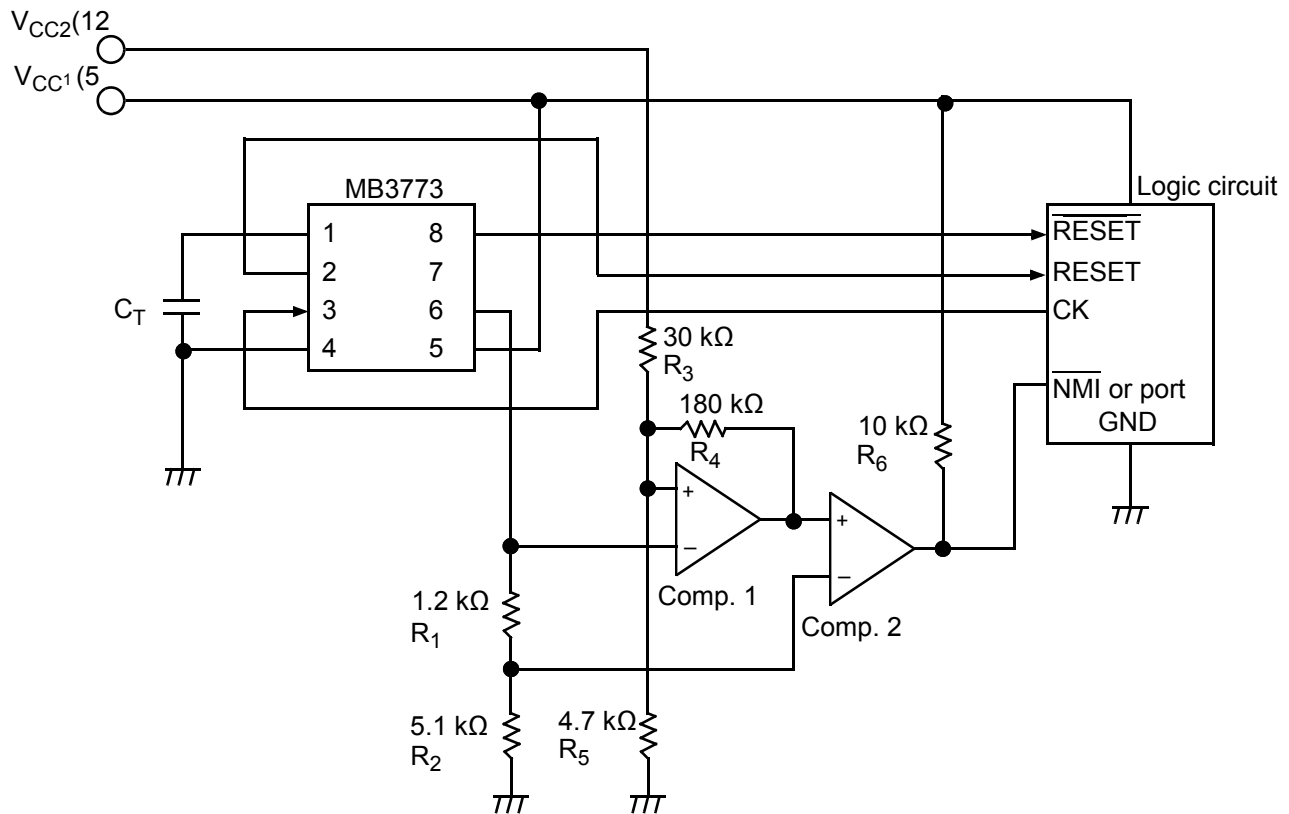


Note : Grounding pin 7 at the time of SW ON sets  $\overline{\text{RESET}}$  (pin 8) to Low and RESET (pin 2) to High.

(b)



Note : Feeding the signal to terminal RESIN and turning on  $Tr$  sets the  $\overline{\text{RESET}}$  terminal to Low and the RESET terminal to High.

**EXAMPLE 4: Monitoring Two Supply Voltages (with hysteresis, reset output and  $\overline{\text{NMI}}$ )**


Example : Comp. 1, Comp. 2  
: MB4204, MB47393

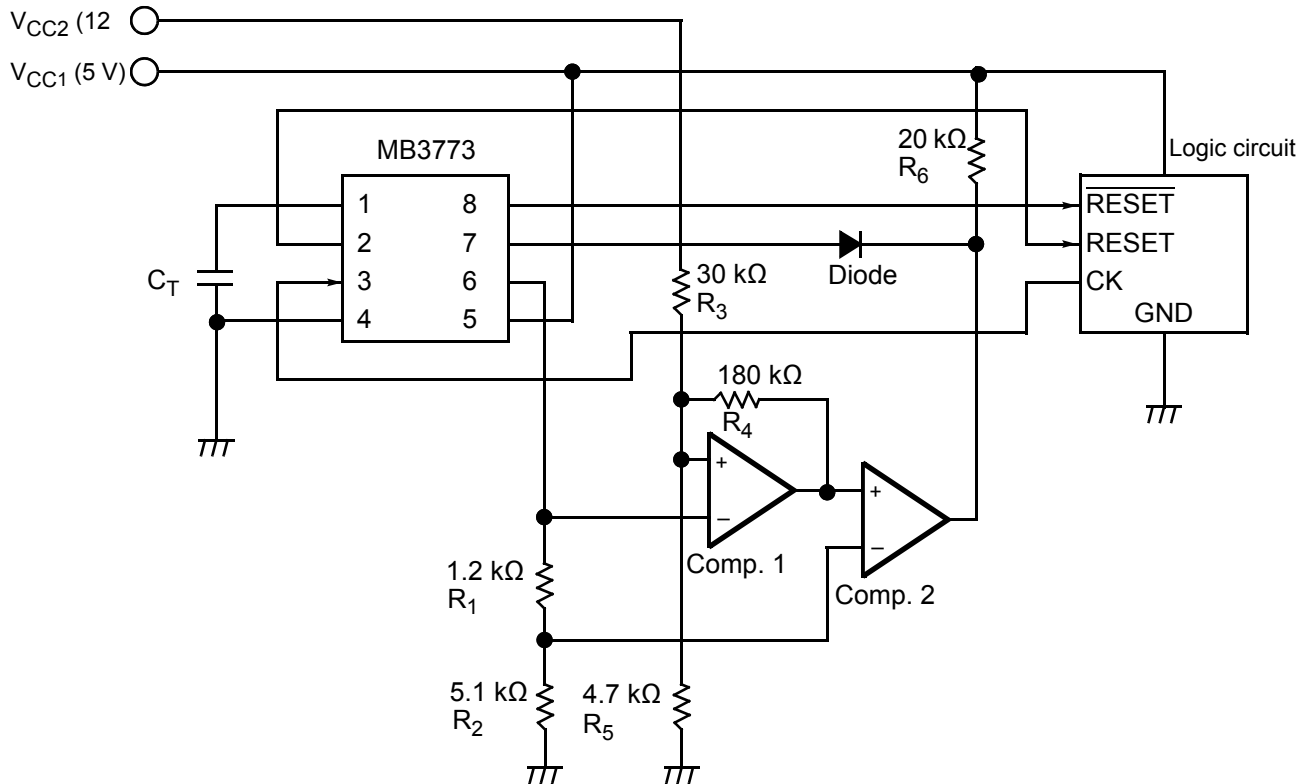
**Notes :**

- The 5 V supply voltage is monitored by the MB3773.
- The 12 V supply voltage is monitored by the external circuit. Its output is connected to the  $\overline{\text{NMI}}$  terminal and, when voltage drops, Comp. 2 interrupts the logic circuit.
- Use  $V_{CC1}$  (= 5 V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.
- The detection voltage of the  $V_{CC2}$  (= 12 V) supply voltage is approximately 9.2 V/9.4 V and has a hysteresis width of approximately 0.2 V.  
 $V_{CC2}$  detection voltage and hysteresis width can be found using the following formulas:

$$\rightarrow \text{Detection voltage } V_{2H} = \frac{R_3 + (R_4 // R_5)}{R_4 // R_5} \times V_{REF} \quad (\text{Approximately } 9.4 \text{ V in the above illustration})$$

$$V_{2L} = \frac{R_3 + R_5}{R_5} \times V_{REF} \quad (\text{Approximately } 9.2 \text{ V in the above illustration})$$

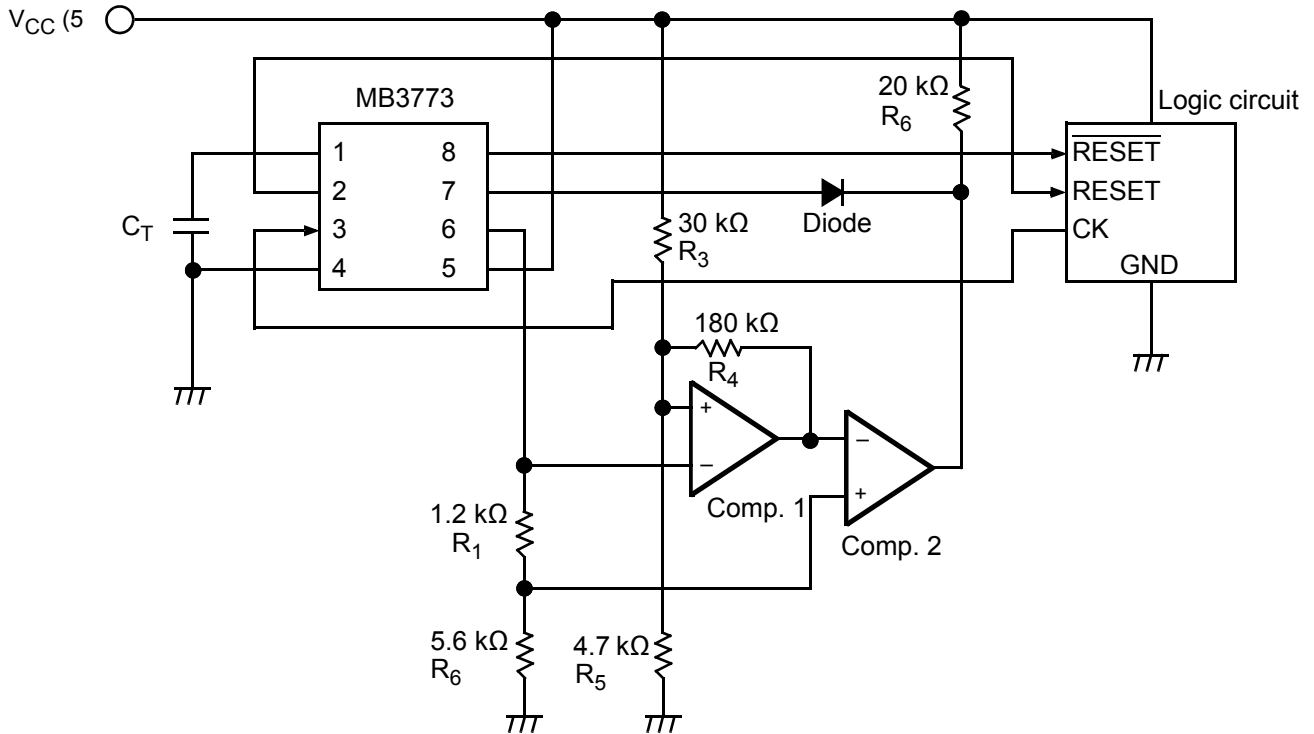
$$\rightarrow \text{Hysteresis width } V_{HYS} = V_{2H} - V_{2L}$$

**EXAMPLE 5: Monitoring Two Supply Voltages (with hysteresis and reset output)**


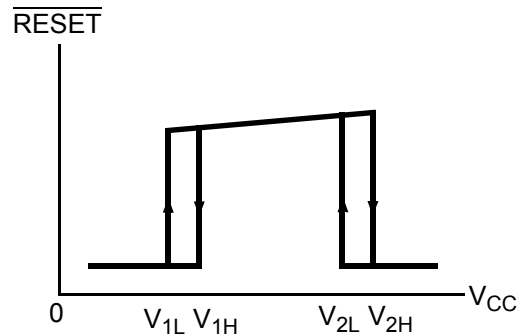
Example : Comp. 1, Comp. 2  
 : MB4204, MB47393

**Notes :**

- When either 5 V or 12 V supply voltage decreases below its detection voltage ( $V_{SL}$ ), the MB3773 RESET terminal is set to High and the MB3773 RESET terminal is set to Low.
- Use  $V_{CC1}$  (= 5 V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.
- The detection voltage of the  $V_{CC2}$  (= 12 V) supply voltage is approximately 9.2 V/9.4 V and has a hysteresis width of approximately 0.2 V. For the formulas for finding hysteresis width and detection voltage, refer to section 4.

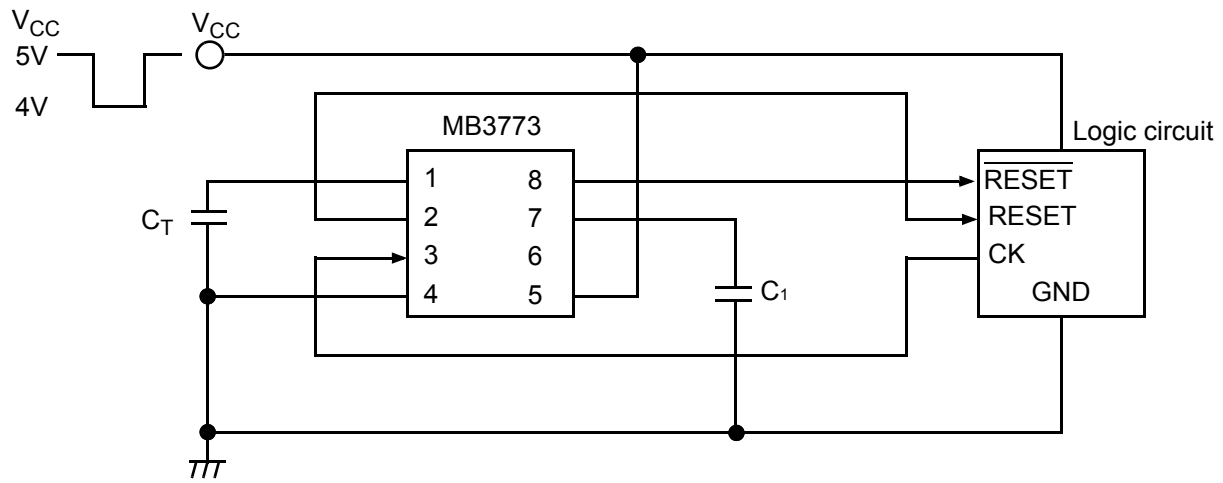
**EXAMPLE 6: Monitoring Low voltage and Overvoltage Monitoring (with hysteresis)**


Example : Comp. 1, Comp. 2  
: MB4204, MB47393


**Notes :**

- Comp. 1 and Comp. 2 are used to monitor for overvoltage while the MB3773 is used to monitor for low voltage. Detection voltages  $V_{1L}/V_{1H}$  at the time of low voltage are approximately 4.2 V/4.3 V. Detection voltages  $V_{2L}/V_{2H}$  at the time of overvoltage are approximately 6.0 V/6.1 V. For the formulas for finding hysteresis width and detection voltage, see EXAMPLE 4.
- Use  $V_{CC}$  (= 5 V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.

**EXAMPLE 7: Monitoring Supply Voltage Using Delayed Trigger**



Note : Adding voltage such as shown in the figure to  $V_{CC}$  increases the minimum input pulse width by  $50 \mu\text{s}$  ( $C_1 = 1000 \text{ pF}$ ).

**EXAMPLE 8: Stopping Watch-dog Timer (Monitoring only supply voltage)**

These are example application circuits in which the MB3773 monitors supply voltage alone without resetting the microprocessor even if the latter, used in standby mode, stops sending the clock pulse to the MB3773.

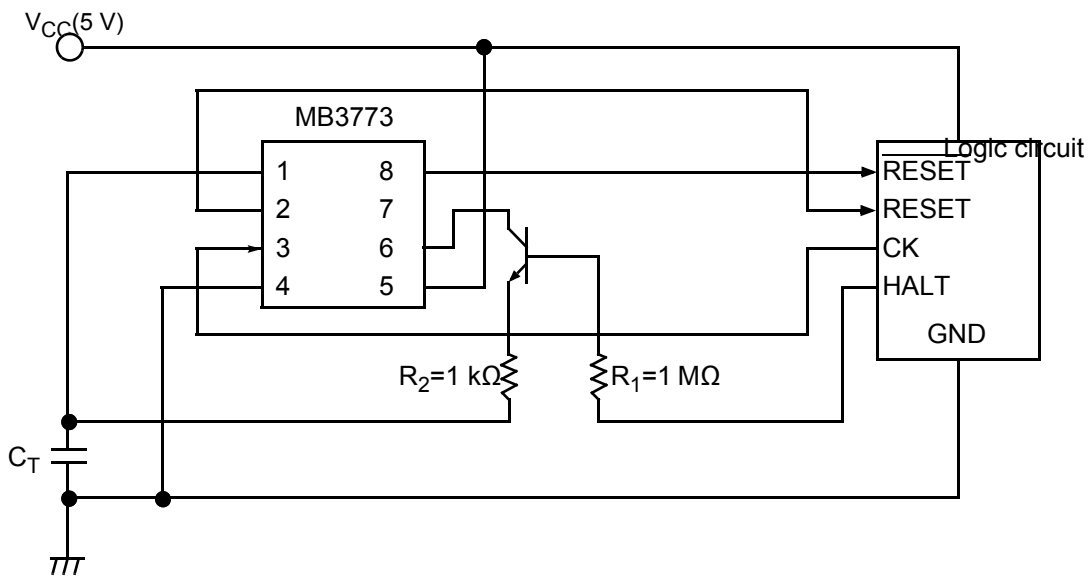
- The watch-dog timer is inhibited by clamping the  $C_T$  terminal voltage to  $V_{REF}$ .

The supply voltage is constantly monitored even while the watch-dog timer is inhibited.

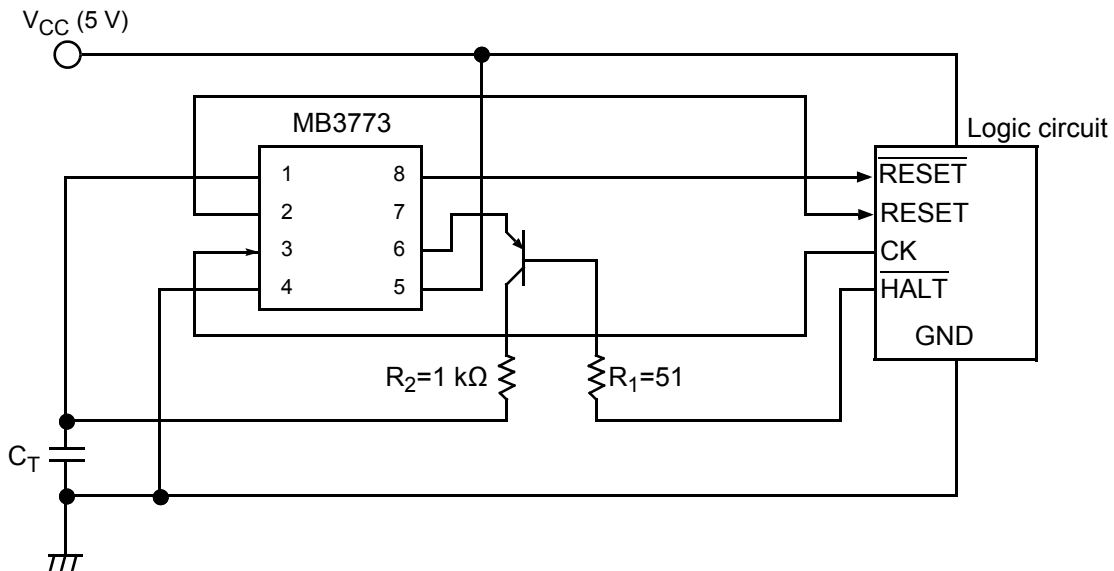
For this reason, a reset signal is output at the occurrence of either instantaneous disruption or a sudden drop to low voltage. Note that in application examples (a) and (b), the hold signal is inactive when the watch-dog timer is inhibited at the time of resetting.

If the hold signal is active when the microprocessor is reset, the solution is to add a gate, as in examples (c) and (d).

(a) Using NPN transistor

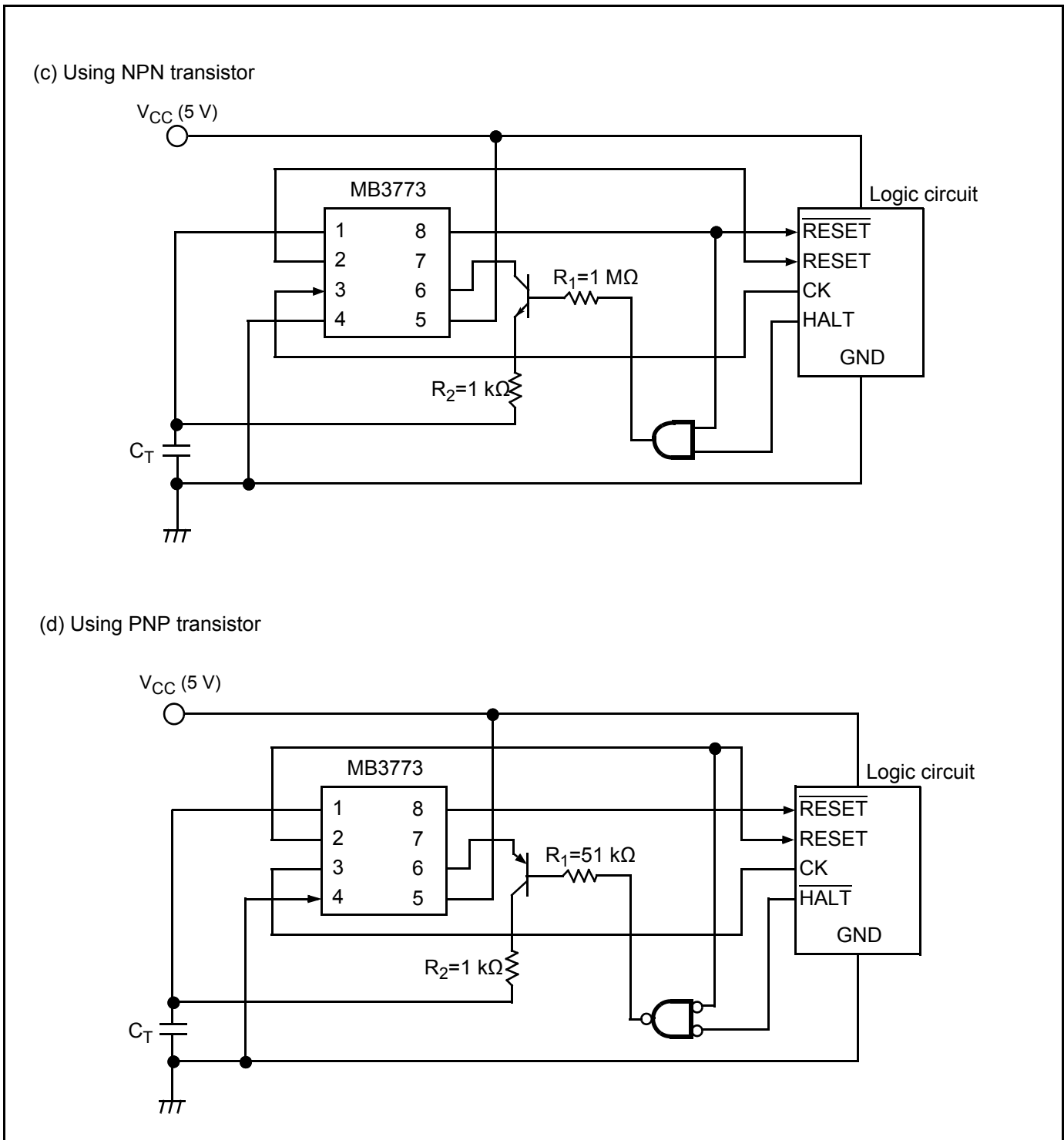


(b) Using PNP transistor

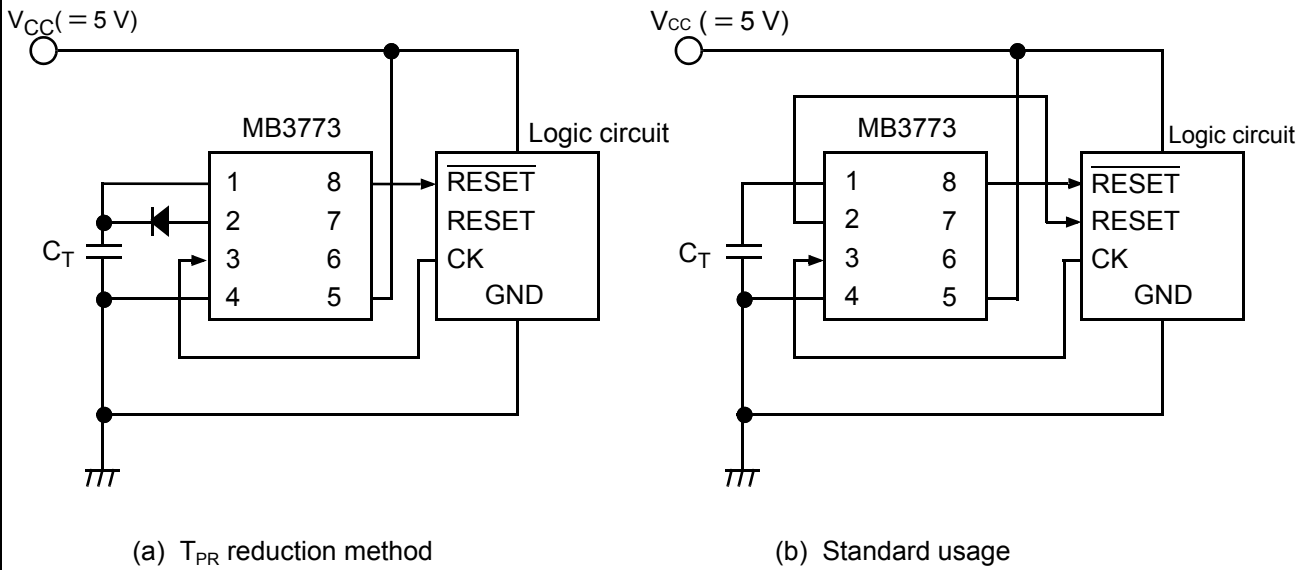


(Continued)

(Continued)



**EXAMPLE 9: Reducing Reset Hold Time**



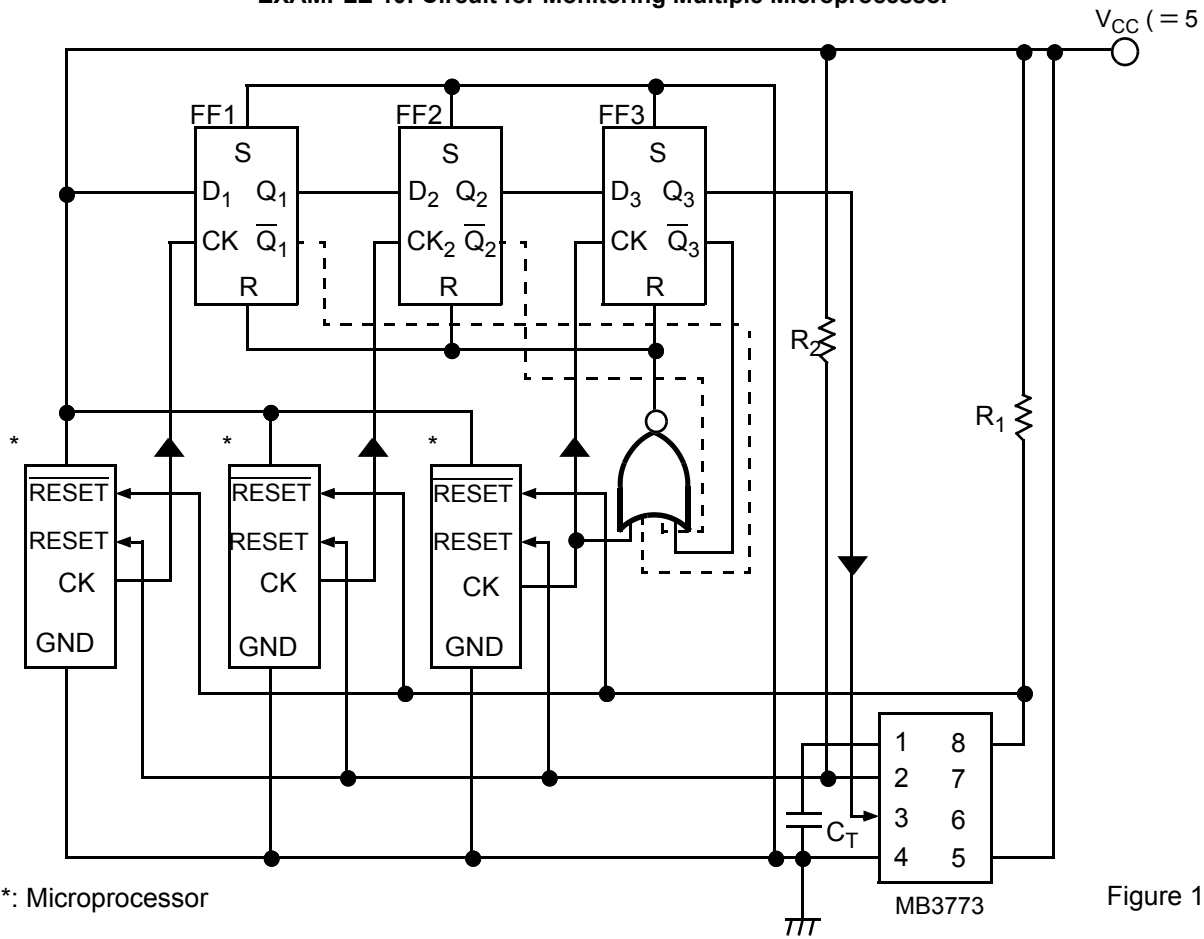
Notes :

- $\overline{\text{RESET}}$  is the only output that can be used.
- Standard  $T_{PR}$ ,  $T_{WD}$  and  $T_{WR}$  value can be found using the following formulas.  
 Formulas:  $T_{PR} \text{ (ms)} \approx 100 \times C_T \text{ (}\mu\text{F)}$   
 $T_{WD} \text{ (ms)} \approx 100 \times C_T \text{ (}\mu\text{F)}$   
 $T_{WR} \text{ (ms)} \approx 16 \times C_T \text{ (}\mu\text{F)}$
- The above formulas become standard values in determining  $T_{PR}$ ,  $T_{WD}$  and  $T_{WR}$ .  
 Reset hold time is compared below between the reduction circuit and the standard circuit.

$C_T = 0.1 \mu\text{F}$

	<b><math>T_{PR}</math> reduction circuit</b>	<b>Standard circuit</b>
$T_{PR} \approx$	10 ms	100 ms
$T_{WD} \approx$	10 ms	10 ms
$T_{WR} \approx$	1.6 ms	2.0 ms

**EXAMPLE 10: Circuit for Monitoring Multiple Microprocessor**



\*: Microprocessor

Notes :

- - - - - connects from FF1 and FF2 outputs  $\bar{Q}_1$  and  $\bar{Q}_2$  to the NOR input.
- Depending on timing, these connections may not be necessary.
- Example :  $R_1 = R_2 = 2.2 \text{ k}\Omega$   
 $C_T = 0.1 \text{ }\mu\text{F}$

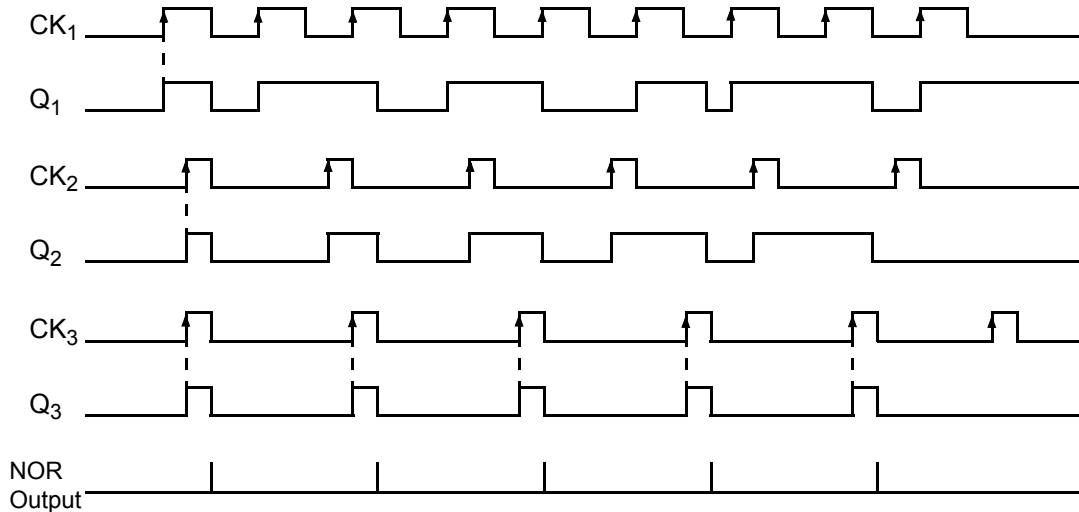


Figure 1

Figure 2

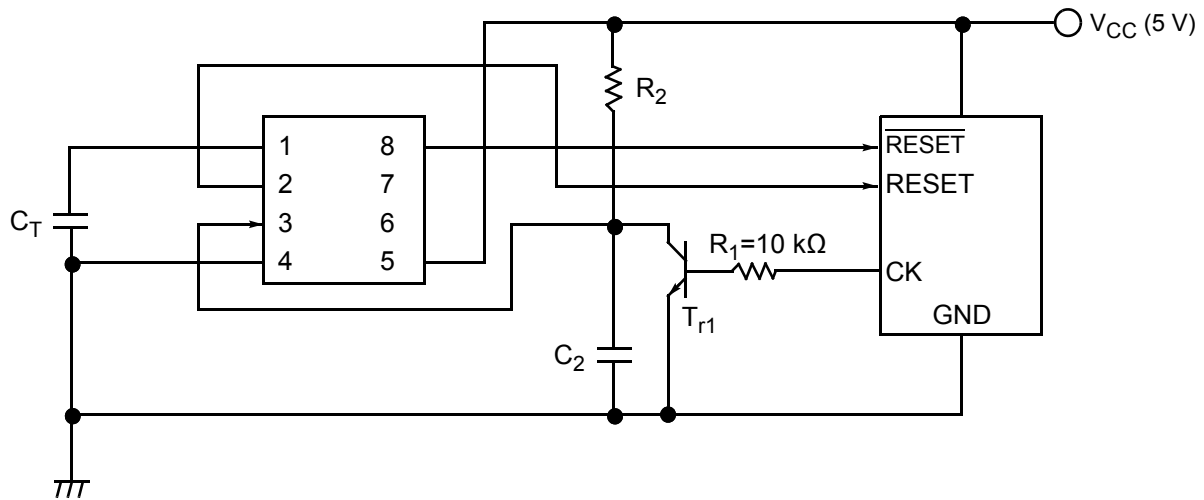
### Description of Application Circuits

Using one MB3773, this application circuit monitors multiple microprocessor in one system. Signals from each microprocessor are sent to FF1, FF2 and FF3 clock inputs. Figure 2 shows these timings. Each flip-flop operates using signals sent from microprocessor as its clock pulse. When even one signal stops, the relevant receiving flip-flop stops operating. As a result, cyclical pulses are not generated at output Q<sub>3</sub>. Since the clock pulse stops arriving at the CK terminal of the MB3773, the MB3773 generates a reset signal. Note that output Q<sub>3</sub> frequency f will be in the following range, where the clock frequencies of CK<sub>1</sub>, CK<sub>2</sub> and CK<sub>3</sub> are f<sub>1</sub>, f<sub>2</sub> and f<sub>3</sub> respectively.

$$\Rightarrow \frac{1}{f_0} \leq \frac{1}{f} \leq \frac{1}{f_1} + \frac{1}{f_2} + \frac{1}{f_3}$$

where f<sub>0</sub> is the lowest frequency among f<sub>1</sub>, f<sub>2</sub> and f<sub>3</sub>.

**EXAMPLE 11: Circuit for Limiting Upper Clock Input Frequency**

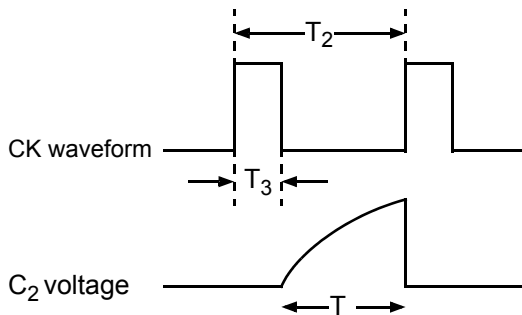


**Notes :**

- This is an example application to limit upper frequency  $f_H$  of clock pulses sent from the microprocessor. If the CK cycle sent from the microprocessor exceeds  $f_H$ , the circuit generates a reset signal. (The lower frequency has already been set using  $C_T$ .)
- When a clock pulse such as shown below is sent to terminal CK, a short  $T_2$  prevents  $C_2$  voltage from reaching the CK input threshold level ( $\approx 1.25$  V), and will cause a reset signal to be output. The  $T_1$  value can be found using the following formula :

$$T_1 \approx 0.3 C_2 R_2$$

where  $V_{CC} = 5$  V,  $T_3 \geq 3.0 \mu s$ ,  $T_2 \geq 20 \mu s$



Example : Setting C and R allow the upper  $T_1$  value to be set (Refer to the table below).

C	R	$T_1$
0.01 $\mu F$	10 k $\Omega$	30 $\mu s$
0.1 $\mu F$	10 k $\Omega$	300 $\mu s$

**10. Notes on Use**

- Take account of common impedance when designing the earth line on a printed wiring board.
- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.
- Do not apply a negative voltage
  - Applying a negative voltage of -0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

**11. Ordering Information**

Part number	Package	Remarks
MB3773PF-□□□E1	8-pin plastic SOP (SOE008)	-

**12. RoHS Compliance Information of Lead (Pb) Free version**

The LSI products of Cypress with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

### 13. Package Dimension

Package Code: SOE008

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**DETAIL A**

**SECTION A-A'**

SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	2.25
A1	0.05	—	0.20
D	6.35 BSC		
E	7.80 BSC		
E1	5.30 BSC		
θ	0°	—	8°
c	0.13	—	0.20
b	0.39	0.47	0.55
L	0.45	0.60	0.75
L 1	1.25 REF		
L 2	0.25 BSC		
e	1.27 BSC		

**NOTES**

- ALL DIMENSIONS ARE IN MILLIMETER.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DATUMS A & B TO BE DETERMINED AT DATUM H.
- "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
- THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
- DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
- "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
- JEDEC SPECIFICATION NO. REF : N/A

002-15857 Rev. \*\*

## Document History

Spanion Publication Number: DS04-27401-8Ea

Document Title: MB3773 Power Supply Monitor with Watch-Dog Timer Document Number: 002-08513				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	TAOA	05/11/2006	Migrated to Cypress and assigned document number 002-08513. No change to document contents or format.
*A	5199075	TAOA	04/04/2016	Updated to Cypress format.
*B	5592858	HIXT	01/23/2017	Updated <a href="#">Pin Assignment</a> : Change the package name from FPT-8P-M01 to SOE008 Updated <a href="#">Ordering Information</a> : Change the package name from FPT-8P-M01 to SOE008 Updated <a href="#">Package Dimension</a> : Updated to Cypress format Deleted "Marking Format (Lead Free version)" Deleted "Labeling Sample (Lead free version)" Deleted "MB3773PF-□□□E1 Recommended Conditions of Moisture Sensitivity Level" Deleted the part number, "MB3773PF-□□□", from <a href="#">Ordering Information</a> Deleted the words in the Remarks, "Lead Free version", from <a href="#">Ordering Information</a>
*C	5788613	MASG	06/28/2017	Adapted Cypress new logo.

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