THE DATASHEET OF

MC33063AQDRQ1

MC33063A-Q1 1.5-A Peak Boost, Buck, Inverting Switching Regulator

1 Features

- AEC-Q100 Qualified With the Following Results:
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Wide Input Voltage Range: 3 V to 40 V
- High Output Switch Current: Up to 1.5 A
- Adjustable Output Voltage
- Oscillator Frequency: Up to 100 kHz
- Precision Internal Reference: 2%
- Short-Circuit Current Limiting
- Low Standby Current

2 Applications

Automotive: Buck, Boost, and Inverting Topologies

3 Description

The MC33063A-Q1 device is an easy-to-use IC containing all the primary circuitry needed for building simple DC-DC converters. The device primarily consists of an internal temperature-compensated reference, a comparator, an oscillator, a PWM controller with active current limiting, a driver, and a high-current output switch. Thus, the device requires minimal external components to build converters in the boost, buck, and inverting topologies.

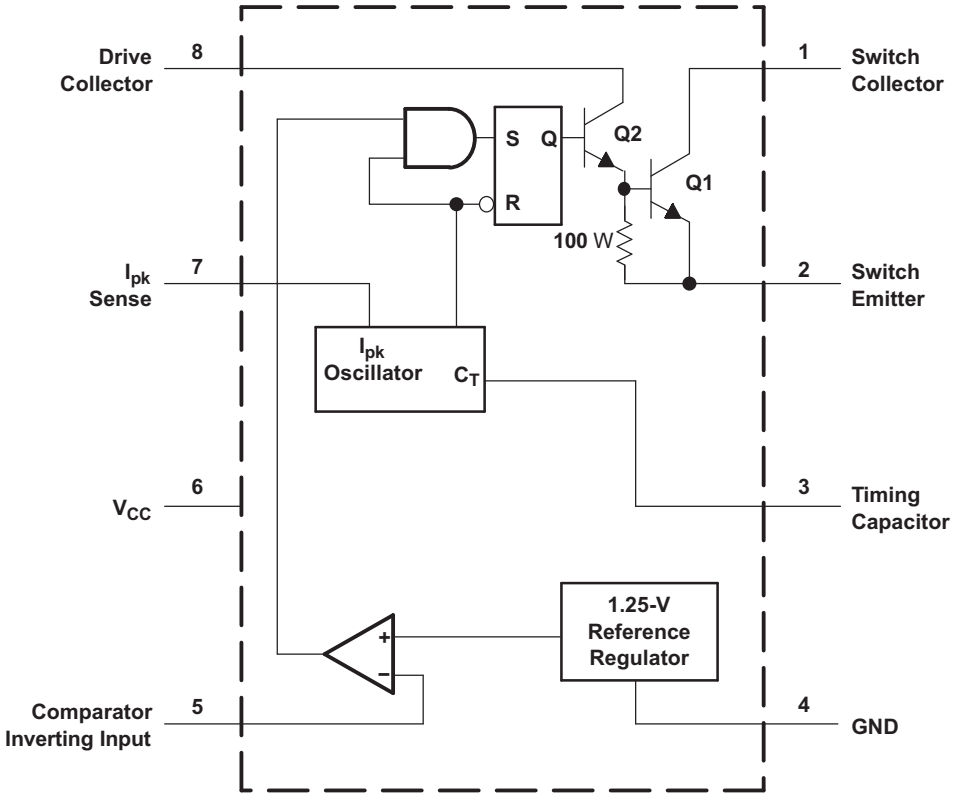
The MC33063A-Q1 device is characterized for operation from –40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MC33063A-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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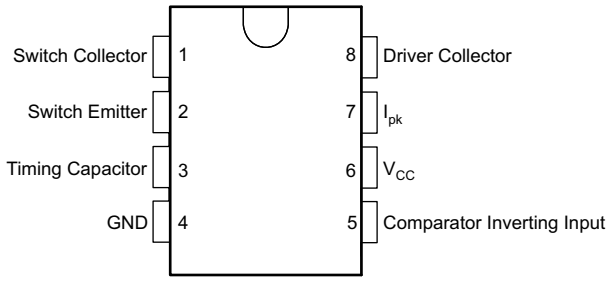
4 Revision History

Changes from Revision B (September 2008) to Revision C **Page**

- Added the *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Switch Collector	—	Switch Collector
2	Switch Emitter	—	Switch Emitter
3	Timing Capacitor	—	Timing Capacitor
4	GND	—	Ground
5	Comparator Inverting Input	I	Comparator Inverting Input
6	V_{CC}	I	Supply
7	I_{PK}	I	Peak Current
8	Driver Collector	—	Driver Collector

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CC}			40	V
Comparator Inverting Input voltage range, V_{IR}		–0.3	40	V
Switch Collector voltage, $V_{C(switch)}$			40	V
Switch Emitter voltage, $V_{E(switch)}$	V_{PIN1} = 40 V		40	V
Switch Collector to Switch Emitter voltage, $V_{CE(switch)}$			40	V
Driver Collector voltage, $V_{C(driver)}$			40	V
Driver Collector current, $I_{C(driver)}$			100	mA
Switch current, I_{SW}			1.5	A
Operating virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
	Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±750	
		Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		40	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		MC33063A-Q1 D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)(3)	121.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	62.3	
ψ_{JT}	Junction-to-top characterization parameter	19.9	
ψ_{JB}	Junction-to-board characterization parameter	61.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Oscillator Characteristics

V_{CC} = 5 V, T_A = full operating range (unless otherwise noted) (see block diagram)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
f_{osc}	Oscillator frequency	V_{PIN5} = 0 V, C_T = 1 nF	25°C	24	33	42	kHz
I_{chg}	Charge current	V_{CC} = 5 V to 40 V	25°C	24	35	42	µA
I_{dischg}	Discharge current	V_{CC} = 5 V to 40 V	25°C	140	220	260	µA
I_{dischg}/I_{chg}	Discharge-to-charge current ratio	V_{PIN7} = V_{CC}	25°C	5.2	6.5	7.5	
V_{Ipk}	Current-limit sense voltage	I_{dischg} = I_{chg}	25°C	250	300	350	mV

6.6 Output Switch Characteristics(1)

V_{CC} = 5 V, T_A = full operating range (unless otherwise noted). See the *Functional Block Diagram*.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$V_{CE(sat)}$	Saturation voltage – Darlington connection	I_{SW} = 1 A, pins 1 and 8 connected	Full range		1	1.3	V
$V_{CE(sat)}$	Saturation voltage – non-Darlington connection(2)	I_{SW} = 1 A, R_{PIN8} = 82 Ω to V_{CC}, Forced β ~ 20	Full range		0.45	0.7	V
h_{FE}	DC current gain	I_{SW} = 1 A, V_{CE} = 5 V	25°C	50	75		
$I_{C(off)}$	Collector off-state current	V_{CE} = 40 V	Full range		0.01	100	µA

(1) Low duty-cycle pulse testing is used to maintain junction temperature as close to ambient temperature as possible.
(2) In the non-Darlington configuration, if the output switch is driven into hard saturation at low switch currents (≤300 mA) and high driver currents (≥30 mA), it may take up to 2 µs for the switch to come out of saturation. This condition effectively shortens the off time at frequencies ≥30 kHz, becoming magnified as temperature increases. The following output drive condition is recommended in the non-Darlington configuration:
Forced β of output switch = $I_{C,SW}$ / ($I_{C,driver}$ – 7 mA) ≥ 10, where ~7 mA is required by the 100-Ω resistor in the emitter of the driver to forward bias the V_{be} of the switch.

6.7 Comparator Characteristics

V_{CC} = 5 V, T_A = full operating range (unless otherwise noted). See the *Functional Block Diagram*.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{th}	Threshold voltage		25°C	1.225	1.25	1.275	V
			Full range	1.21		1.29	
ΔV_{th}	Threshold-voltage line regulation	V_{CC} = 5 V to 40 V	Full range		1.4	5	mV
I_{IB}	Input bias current	V_{IN} = 0 V	Full range		–20	–400	nA

6.8 Total Device Characteristics

V_{CC} = 5 V, T_A = full operating range (unless otherwise noted). See the *Functional Block Diagram*.

PARAMETER		TEST CONDITIONS	T_A	MIN	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5 V to 40 V, C_T = 1 nF, V_{PIN7} = V_{CC}, V_{PIN5} > V_{th}, V_{PIN2} = GND, All other pins open	Full range		4	mA

6.9 Typical Characteristics

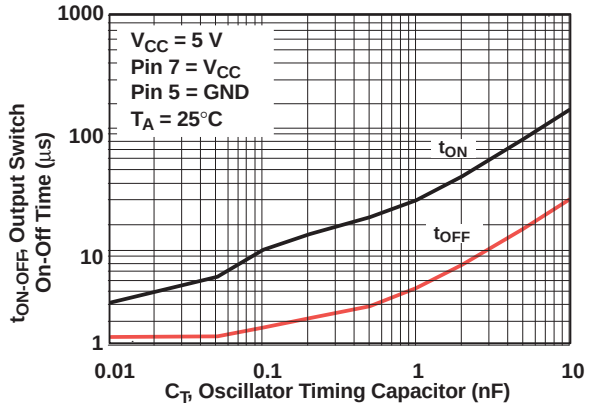


Figure 1. Output Switch On-Off Time vs Oscillator Timing Capacitor

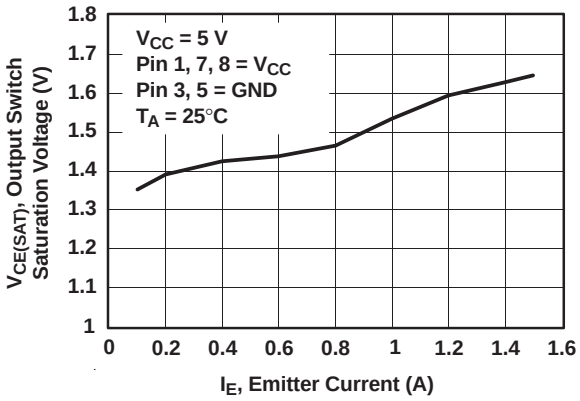


Figure 2. Output Switch Saturation Voltage vs Emitter Current (Emitter-Follower Configuration)

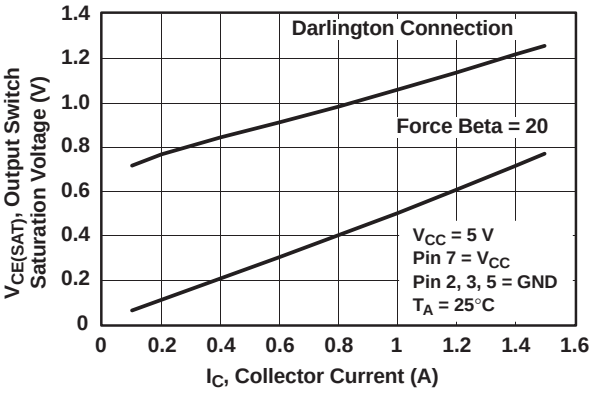


Figure 3. Output Switch Saturation Voltage vs Collector Current (Common-Emitter Configuration)

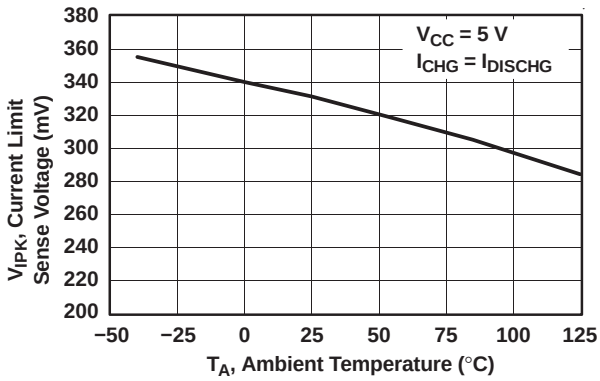


Figure 4. Current-Limit Sense Voltage vs Temperature

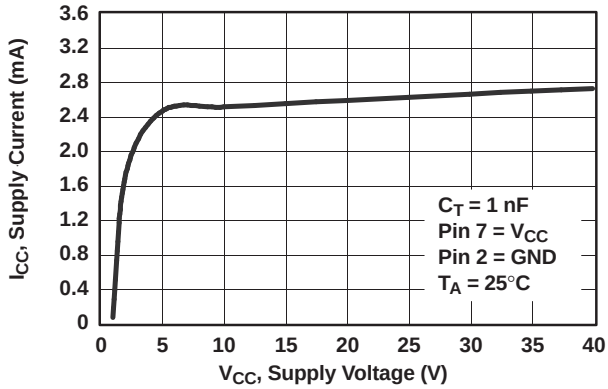


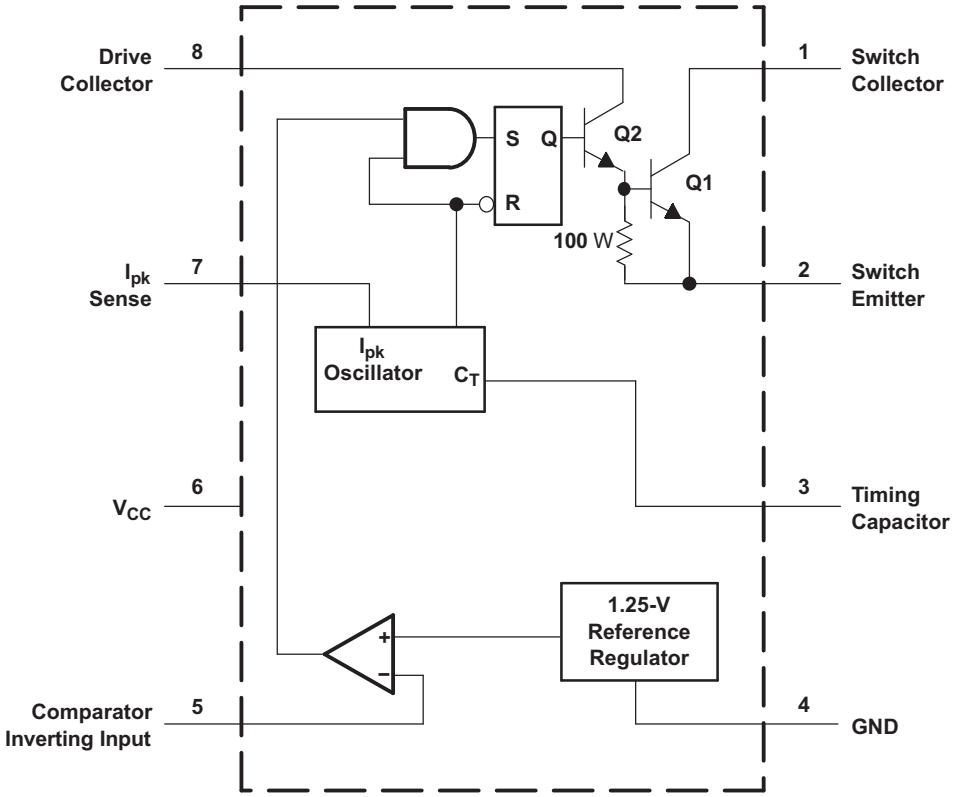
Figure 5. Standby Supply Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The MC33063A-Q1 device primarily consists of an internal temperature-compensated reference, a comparator, an oscillator, a PWM controller with active current limiting, a driver, and a high-current output switch. The MC33063A-Q1 device requires minimal external components to build converters in the boost, buck, and inverting topologies.

7.2 Functional Block Diagram



7.3 Feature Description

The device includes the following components:

- Temperature-compensated reference voltage
- Oscillator
- Active peak-current limit
- Output switch
- Output voltage-sense comparator

7.3.1 Reference Voltage

The reference voltage is set at 1.25 V and is used to set the output voltage of the converter.

Feature Description (continued)

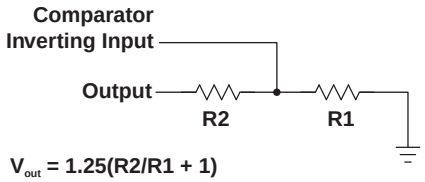


Figure 6. Reference Voltage Circuit

7.3.2 Current Limit

Current limit is accomplished by monitoring the voltage drop across an external sense resistor located in series with VCC and the output switch. The voltage drop developed across the sense resistor is monitored by the current-sense pin, Ipk. When the voltage drop across the sense resistor becomes greater than the preset value of 330 mV, the current-limit circuitry provides an additional current path to charge the timing capacitor (CT) rapidly, to reach the upper oscillator threshold and, thus, limiting the amount of energy stored in the inductor. The minimum sense resistor is 0.2 W. Figure 7 shows the timing capacitor charge current versus current-limit sense voltage. To set the peak current, Ipk = 330 mV/Rsense.

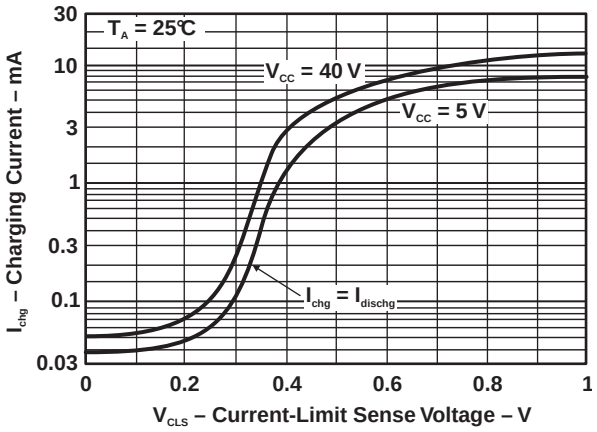


Figure 7. Timing Capacitor Charge Current vs Current-Limit Sense Voltage

7.3.3 Current Limit of Typical Operation Waveforms

The output switch is an NPN Darlington transistor. The collector of the output transistor is tied to pin 1, and the emitter is tied to pin 2. This allows the designer to use the MC33063 device in buck, boost, or inverter configurations. The maximum collector-emitter saturation voltage at 1.5 A (peak) is 1.3 V, and the maximum peak current of the output switch is 1.5 A. For higher peak output current, an external transistor can be used. Figure 8 shows the typical operation waveforms.

Feature Description (continued)

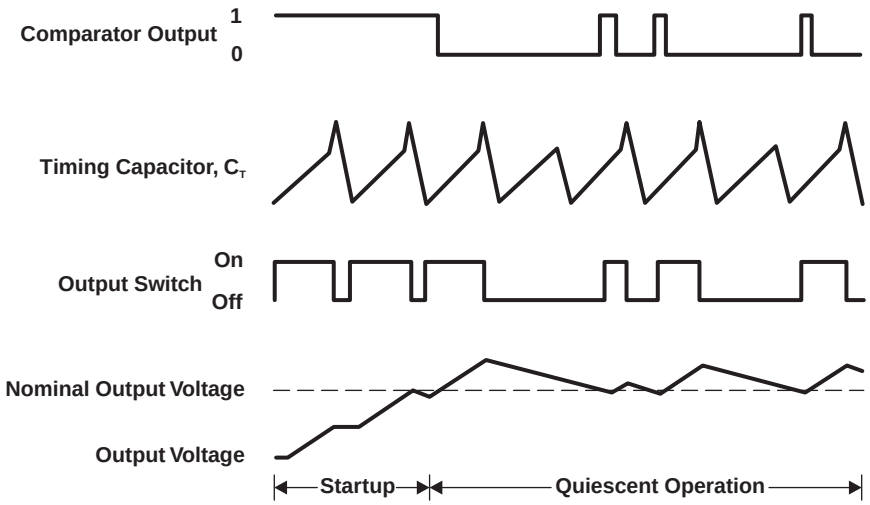


Figure 8. Typical Operation Waveforms

7.4 Device Functional Modes

The oscillator is composed of a current source and a current sink that charge and discharge the external timing capacitor (CT) between an upper and lower preset threshold. The typical charge current is 35 mA, and the typical discharge current is 200 mA, yielding approximately a 6:1 ratio. Thus, the ramp-up period is six times longer than that of the ramp-down period (see Figure 9). The upper threshold is 1.25 V, which is same as the internal reference voltage, and the lower threshold is 0.75 V. The oscillator runs constantly, at a pace controlled by the value of CT.

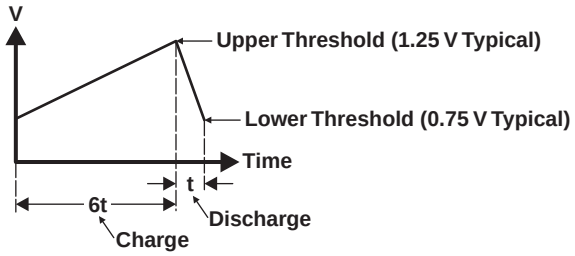


Figure 9. Oscillator Voltage Thresholds

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The MC33063A-Q1 device requires minimal external components to build converters in the boost, buck, and inverting topologies.

8.2 Typical Applications

8.2.1 Step-Up Converter

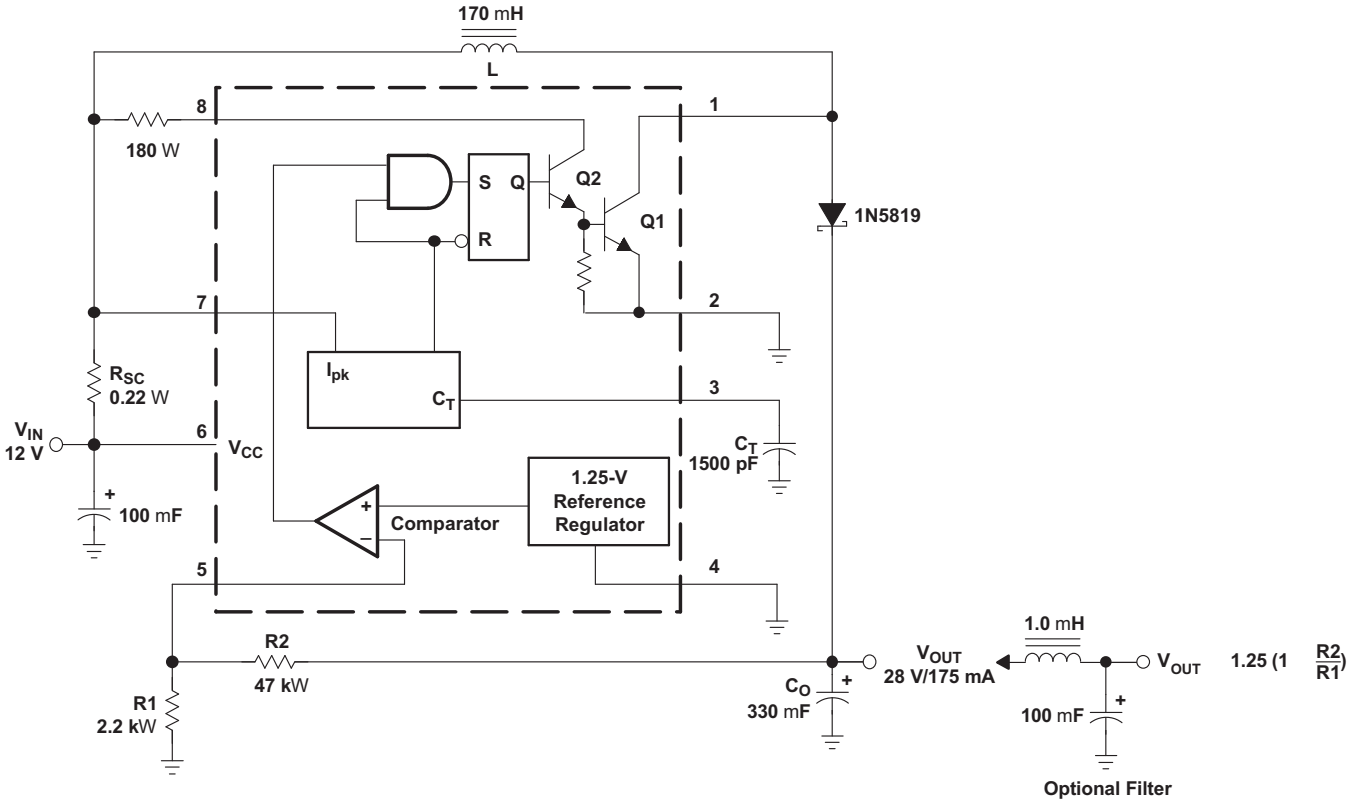
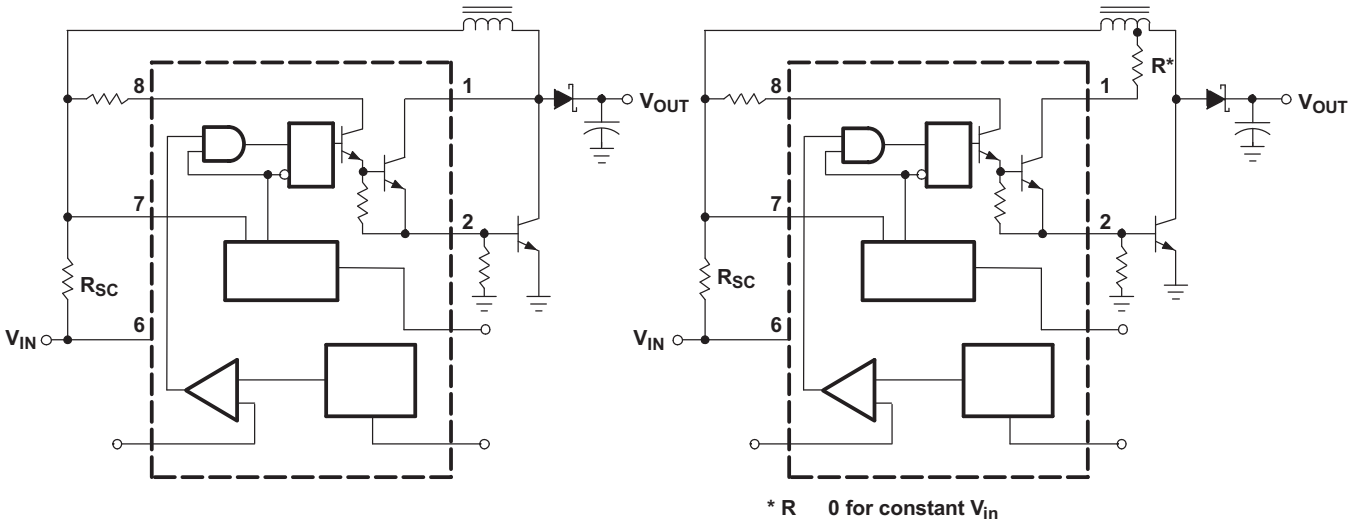


Figure 10. Step-Up Converter

Typical Applications (continued)



a) EXTERNAL npn SWITCH

b) EXTERNAL pnp SATURATED SWITCH (see Note A)

Figure 11. External Switches

8.2.1.1 Design Requirements

Table 1. Step-Up Converter

TEST	CONDITIONS	RESULTS
Line regulation	V_{IN} = 8 V to 16 V, I_O = 175 mA	30 mV ± 0.05%
Load regulation	V_{IN} = 12 V, I_O = 75 mA to 175 mA	10 mV ± 0.017%
Output ripple	V_{IN} = 12 V, I_O = 175 mA	400 mV_{PP}
Efficiency	V_{IN} = 12 V, I_O = 175 mA	87.7%
Output ripple with optional filter	V_{IN} = 12 V, I_O = 175 mA	40 mV_{PP}

8.2.1.2 Detailed Design Procedure

CALCULATION	STEP UP	STEP DOWN	VOLTAGE INVERTING
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{SC}	$\frac{0.3}{I_{pk(switch)}}$	$\frac{0.3}{I_{pk(switch)}}$	$\frac{0.3}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$

CALCULATION	STEP UP	STEP DOWN	VOLTAGE INVERTING
C_O	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$

8.2.1.3 Application Curve

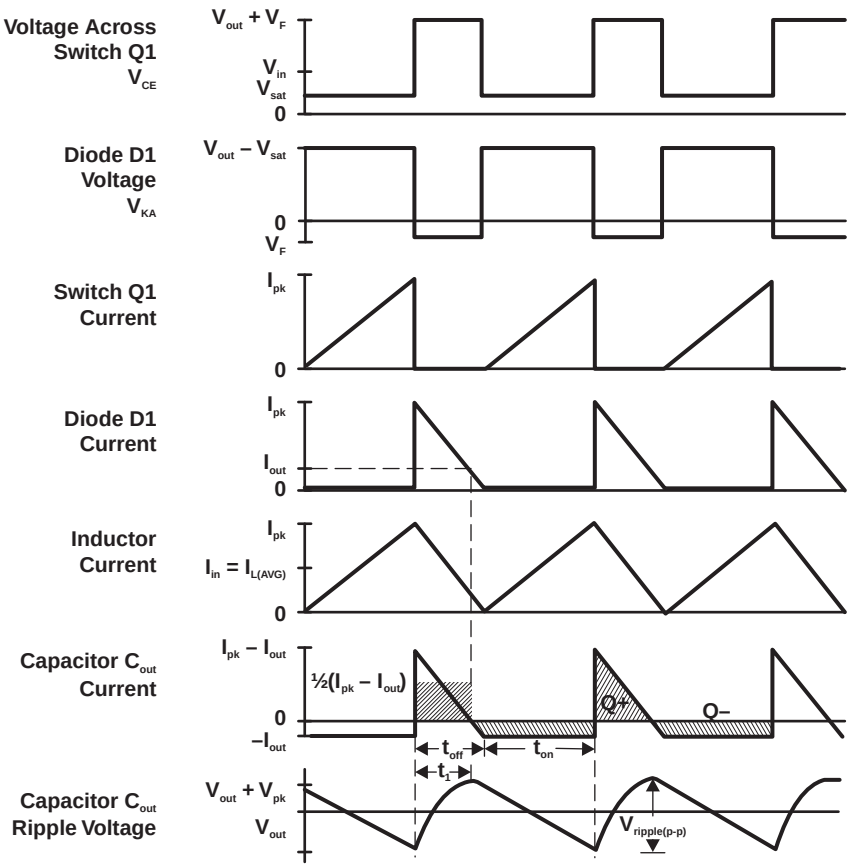


Figure 12. Boost Switching Regulator Waveforms

8.2.2 Step-Down Converter

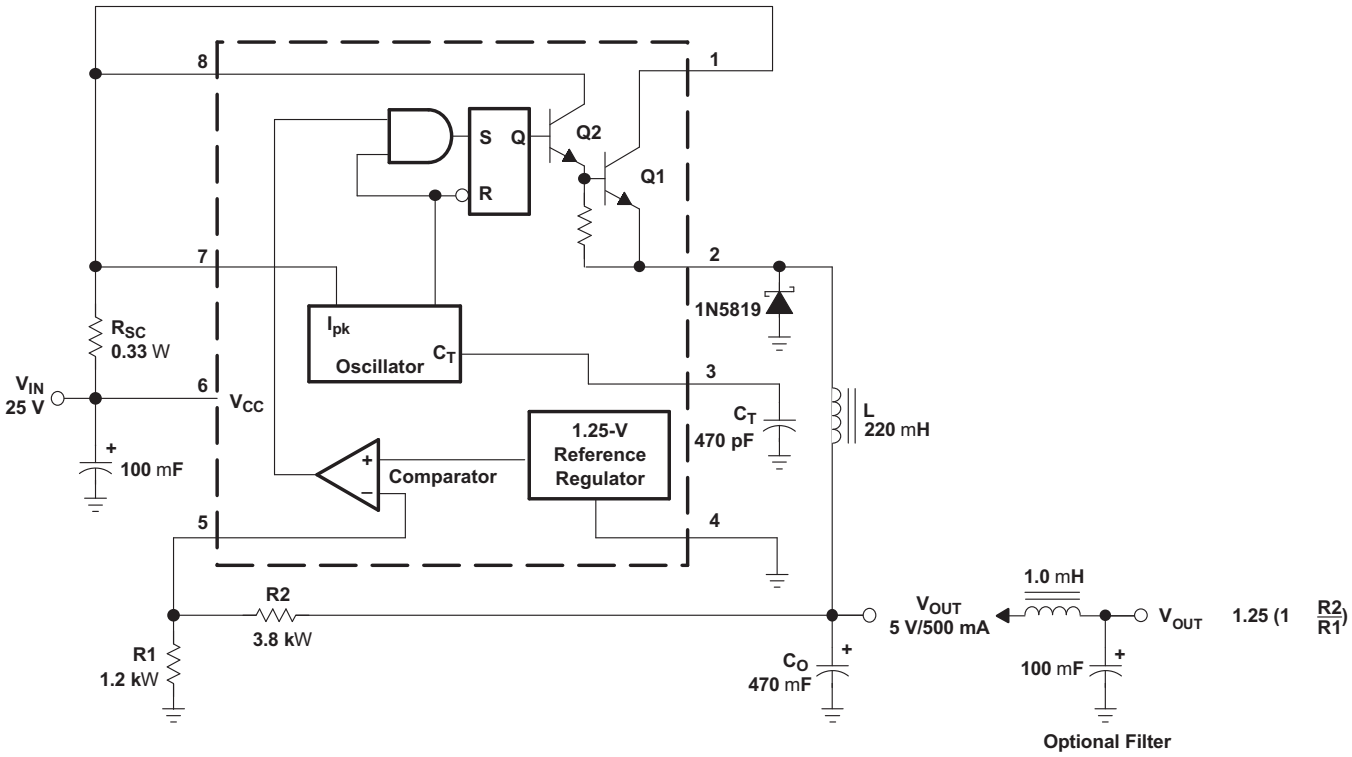


Figure 13. Step-Down Converter

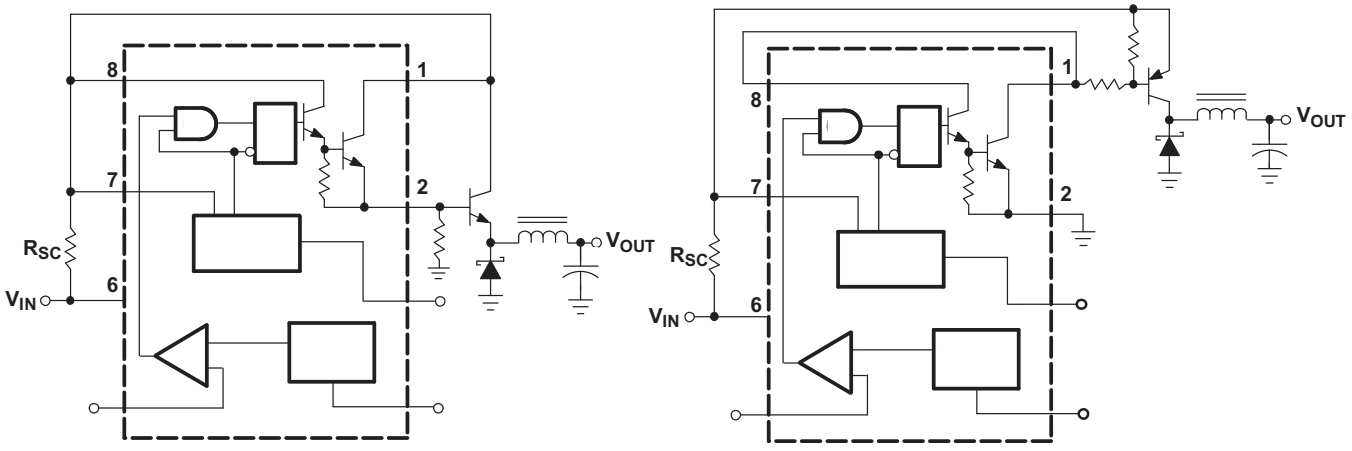


Figure 14. External Current-Boost Connections for I_C Peak Greater Than 1.5 A

8.2.2.1 Design Requirements

Table 2. Step-Down Converter

TEST	CONDITIONS	RESULTS
Line regulation	V_{IN} = 15 V to 25 V, I_O = 500 mA	12 mV ± 0.12%
Load regulation	V_{IN} = 25 V, I_O = 50 mA to 500 mA	3 mV ± 0.03%
Output ripple	V_{IN} = 25 V, I_O = 500 mA	120 mV_{PP}
Short-circuit current	V_{IN} = 25 V, RL = 0.1 Ω	1.1 A
Efficiency	V_{IN} = 25 V, I_O = 500 mA	83.7%
Output ripple with optional filter	V_{IN} = 25 V, I_O = 500 mA	40 mV_{PP}

8.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure*.

8.2.2.3 Application Curves

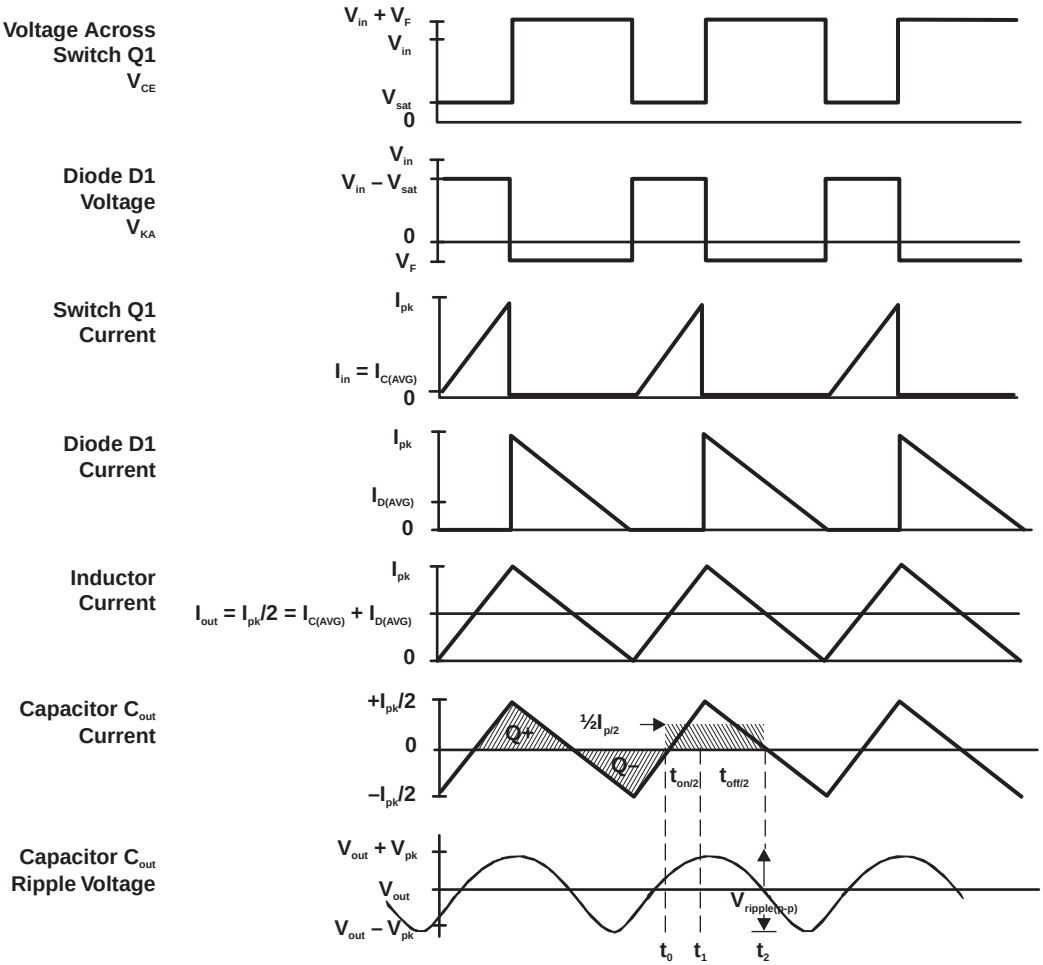


Figure 15. Buck Switching Regulator Waveforms

8.2.3 Voltage Inverter Converter

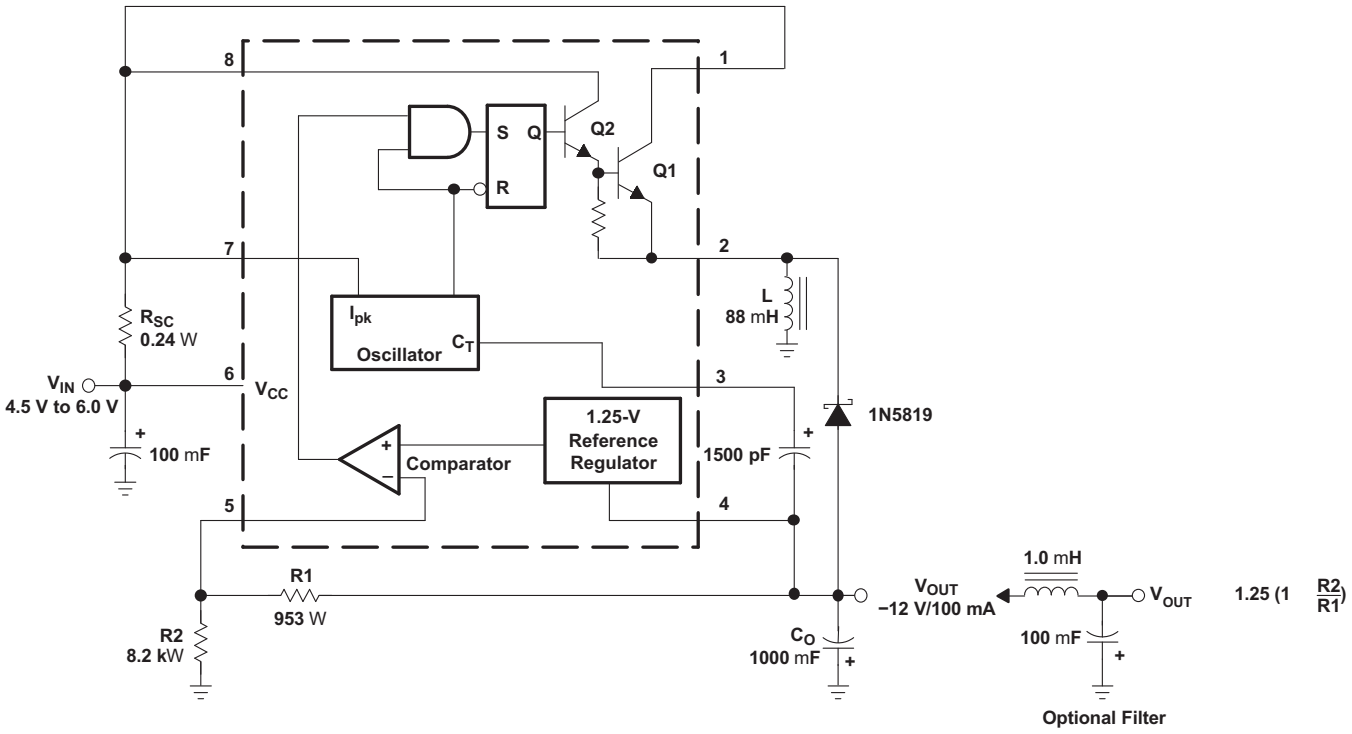


Figure 16. Voltage-Inverting Converter

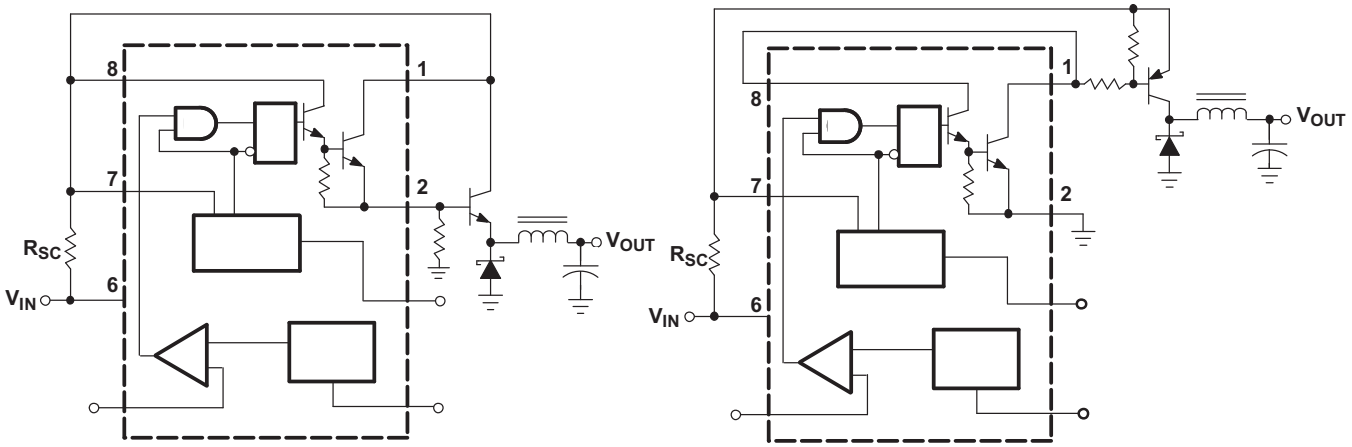


Figure 17. External Current-Boost Connections for Voltage Inverter Converter

8.2.3.1 Design Requirements

TEST	CONDITIONS	RESULTS
Line regulation	V_{IN} = 4.5 V to 6 V, I_O = 100 mA	3 mV ± 0.12%
Load regulation	V_{IN} = 5 V, I_O = 10 mA to 100 mA	0.022 V ± 0.09%
Output ripple	V_{IN} = 5 V, I_O = 100 mA	500 mVPP
Short-circuit current	V_{IN} = 5 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{IN} = 5 V, I_O = 100 mA	62.2%
Output ripple with optional filter	V_{IN} = 5 V, I_O = 100 mA	70 mVPP

8.2.3.2 Detailed Design Procedure

See *Detailed Design Procedure*.

8.2.3.3 Application Curves

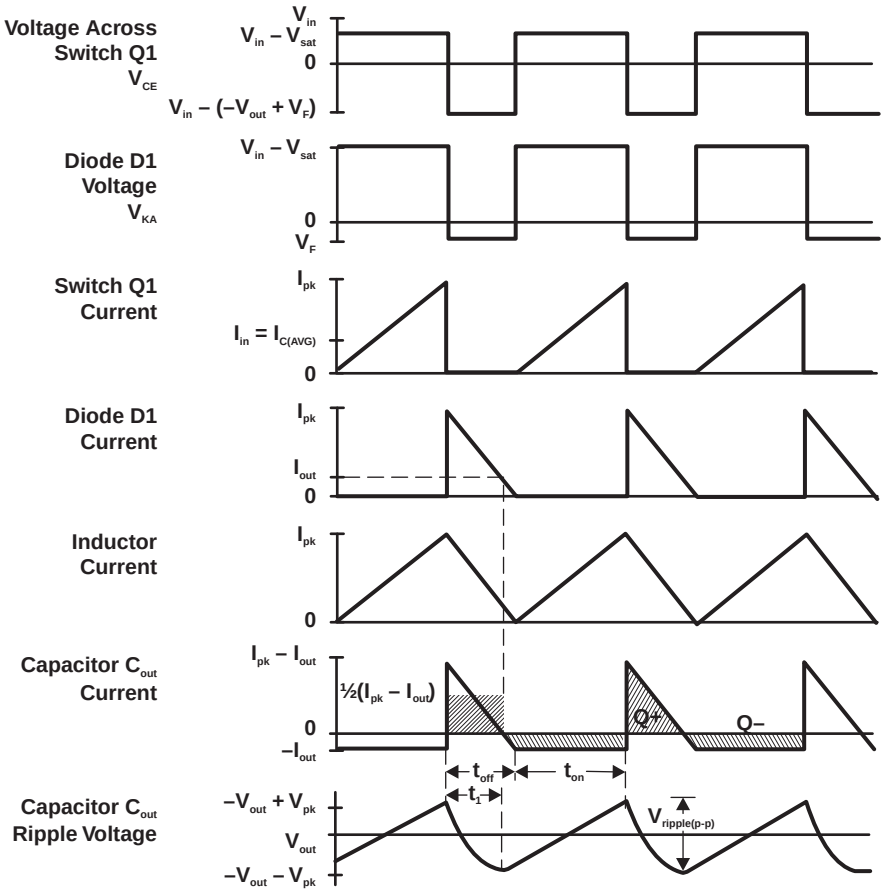


Figure 18. Inverter Switching Regulator Waveforms

8.2.4 12 V Battery Based Automotive Supply

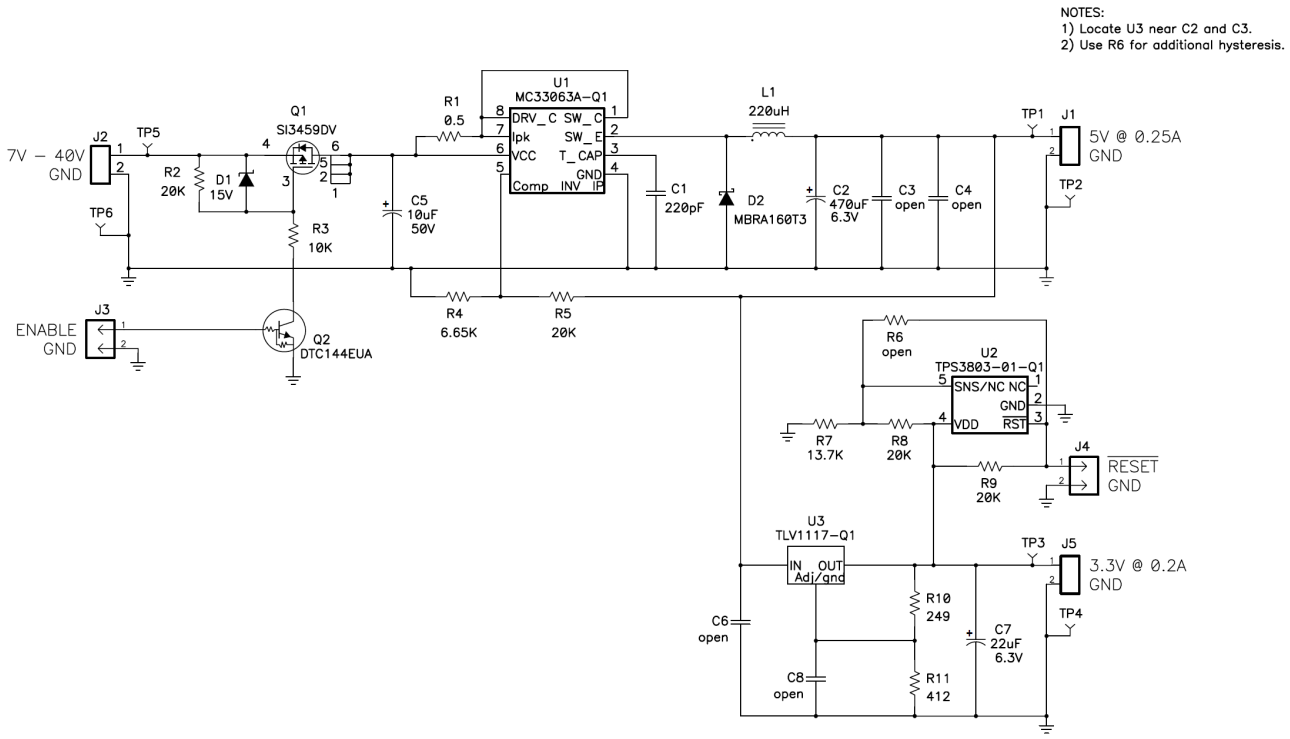


Figure 19. 12 V Battery Based Automotive Supply Schematic

8.2.4.1 Design Requirements

Input Supply Voltage: 7 to 40 V

Output Supply Voltage: 5 V at 0.25 A

An additional supply rail of 3.3 at 0.2 A along with a power supply supervisor is required for this application.

8.2.4.2 Detailed Design Procedure

See *Detailed Design Procedure*.

8.2.4.3 Application Curve

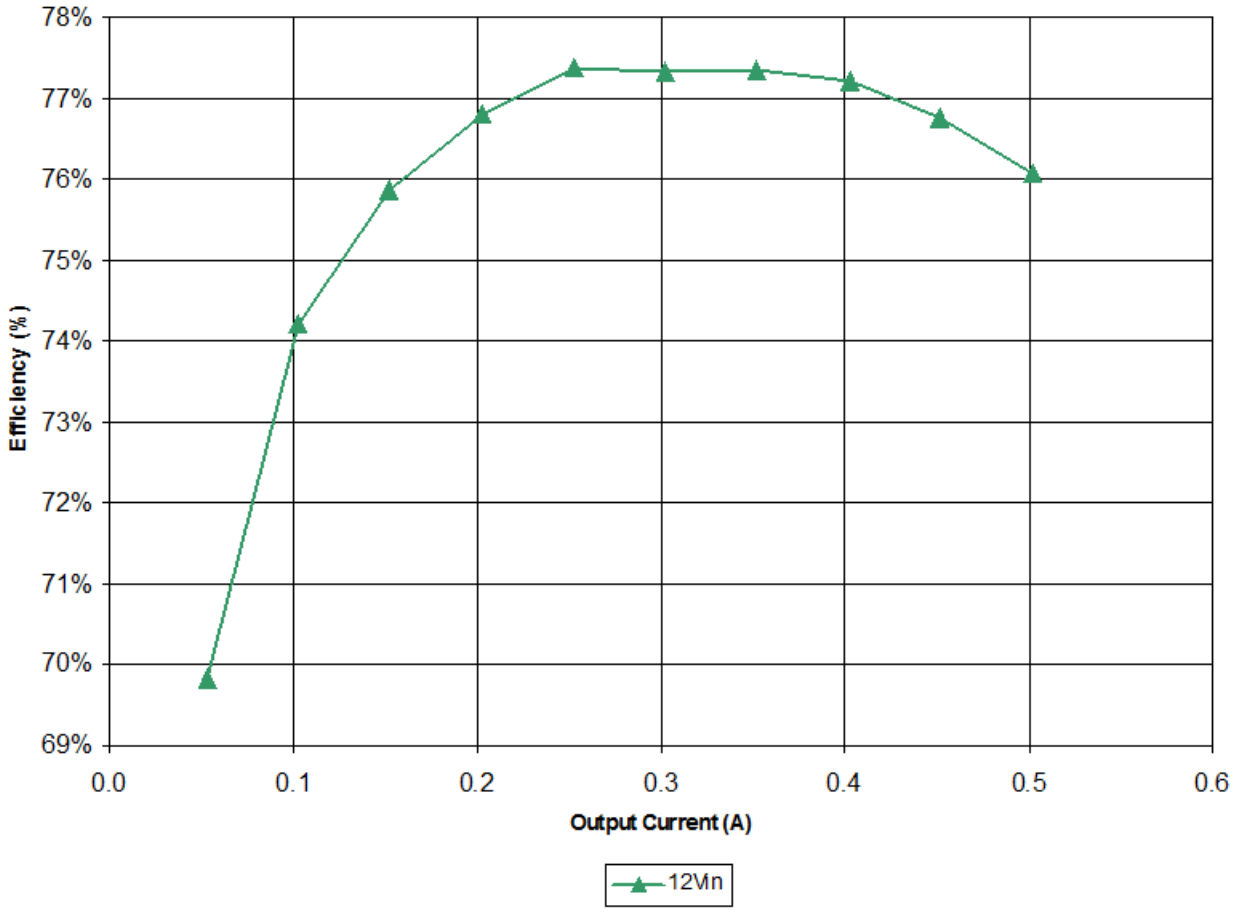


Figure 20. Application Example 4 Efficiency

9 Power Supply Recommendations

The input decoupling capacitors must be located as close as possible to the MC33063-Q1. In addition, the voltage set-point resistor divider components must also be kept close to the IC to eliminate any noise pick-up into the feedback loop.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the input voltage pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the input pin, and the anode of the catch diode.

10.2 Layout Example

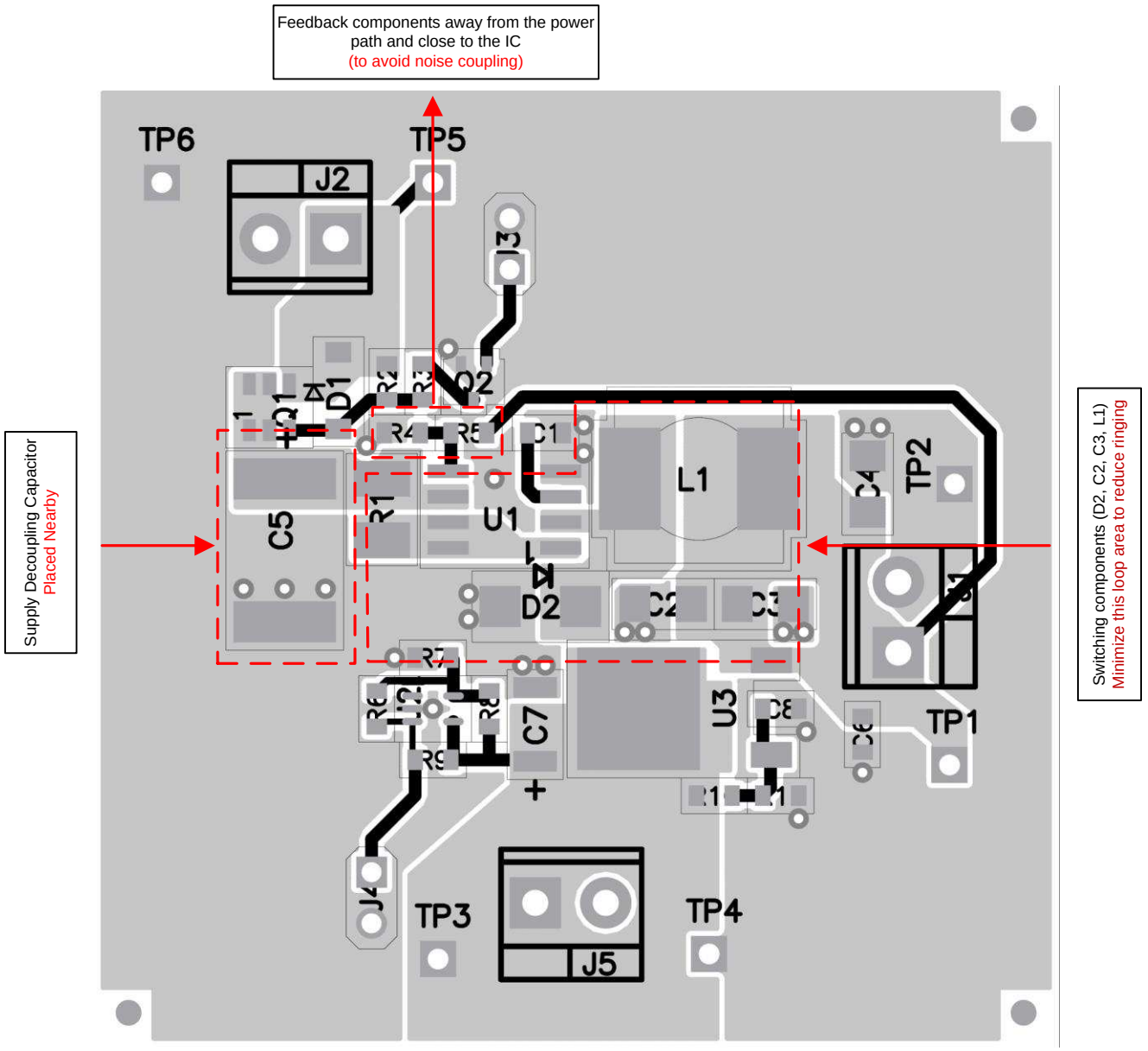


Figure 21. MC33063A-Q1 Layout Top Layer Example

Layout Example (continued)

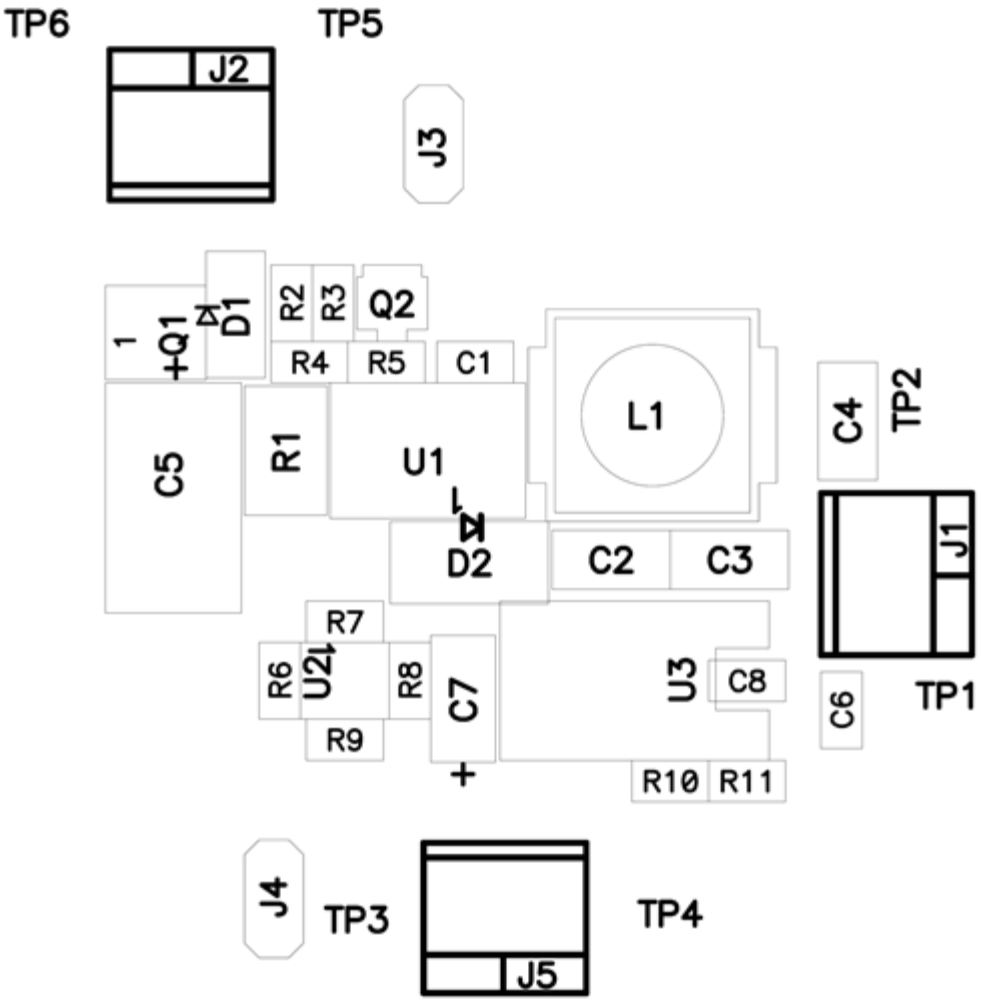


Figure 22. MC33063A-Q1 Layout Middle Layer Example

Layout Example (continued)

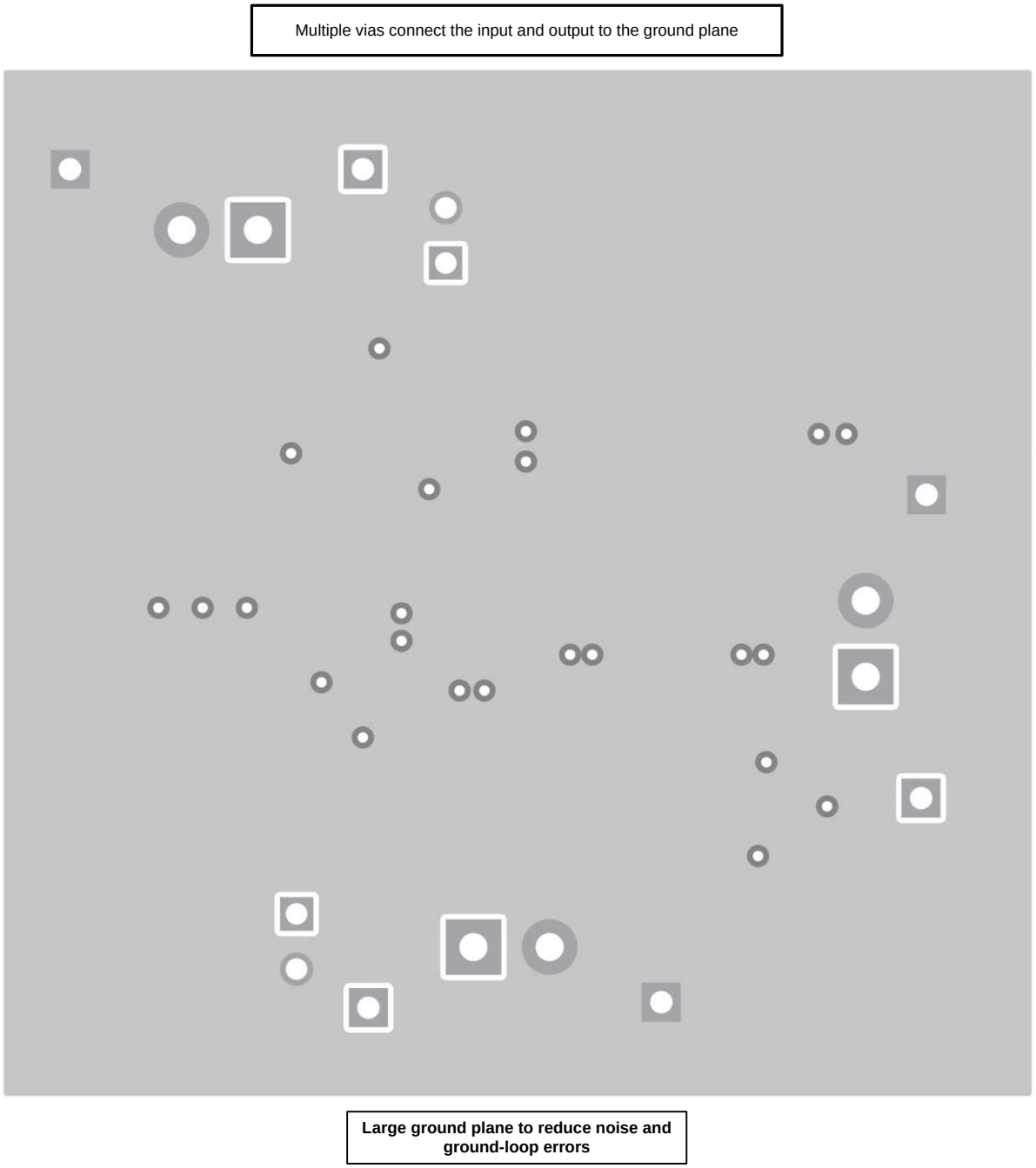


Figure 23. MC33063A-Q1 Layout Bottom Layer Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC33063AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	33063AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

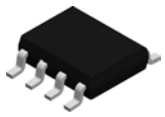
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF MC33063A-Q1 :

- Catalog: MC33063A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

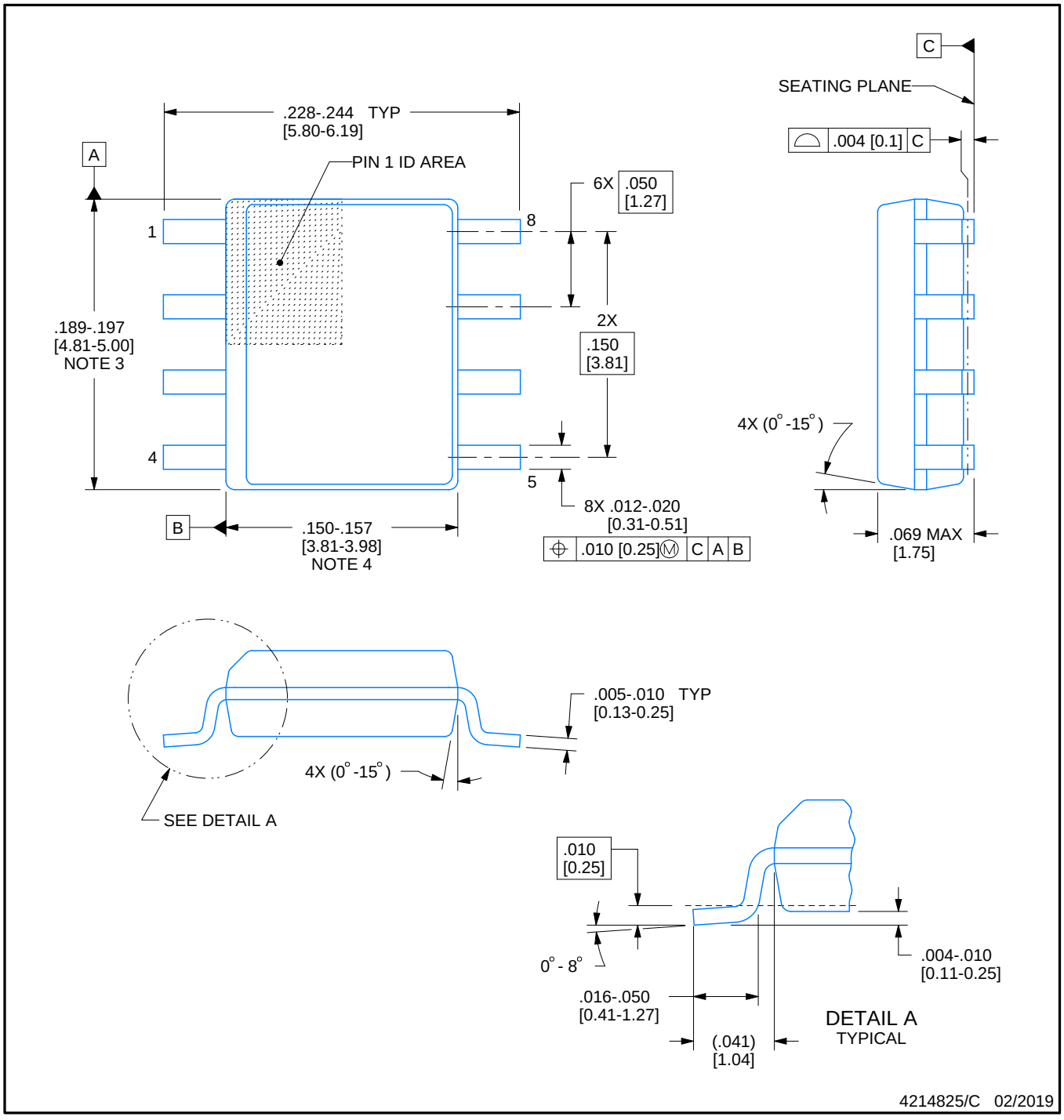


PACKAGE OUTLINE

D0008A

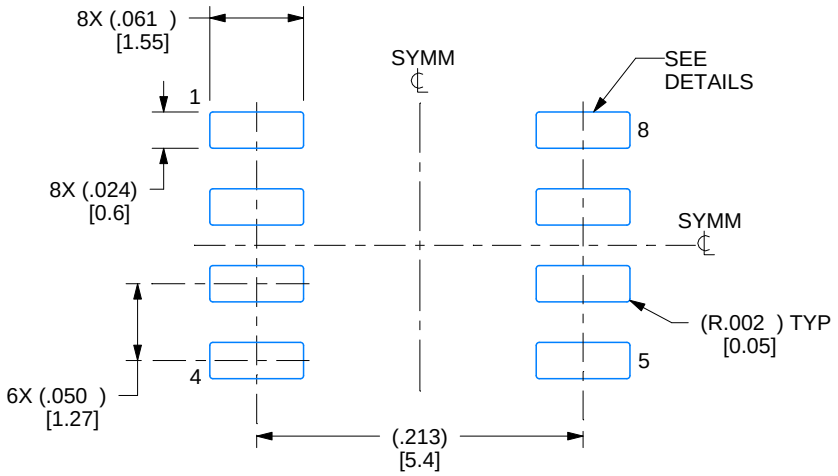
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

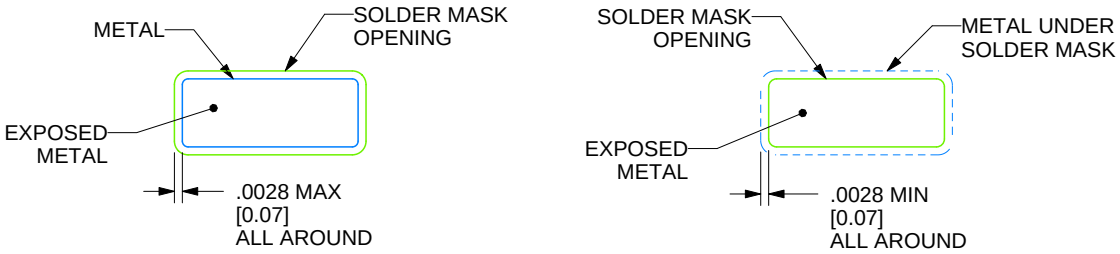


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

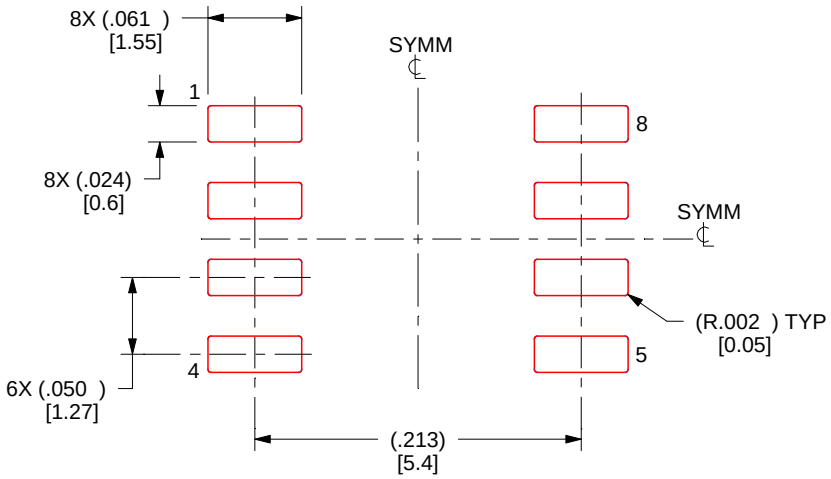
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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