



THE DATASHEET OF MC74HC4040AFELG



MC74HC4040A

12-Stage Binary Ripple Counter

High-Performance Silicon-Gate CMOS

The MC74C4040A is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half of that of the preceding one. The state counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040A for some designs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

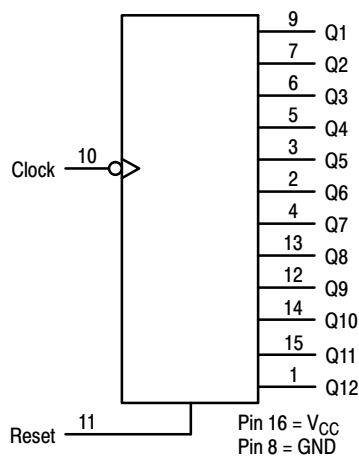
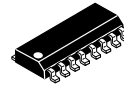


Figure 1. Logic Diagram

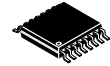


ON Semiconductor®

<http://onsemi.com>

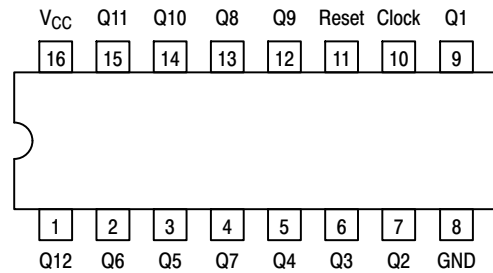


SOIC-16
D SUFFIX
CASE 751B



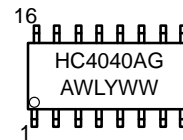
TSSOP-16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT

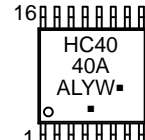


16-Lead Package (Top View)

MARKING DIAGRAMS



SOIC-16



TSSOP-16

- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or \blacksquare = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to Next State
X	H	All Outputs Are Low

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74HC4040A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C
TSSOP Package: -6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V	
T_A	Operating Temperature Range, All Package Types	-55	+125	°C	
t_r, t_f	Input Rise and Fall Time (Figure 2)	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 0 0 0	1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$ $ I_{out} \leq 20\mu\text{A}$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$ $ I_{out} \leq 20\mu\text{A}$	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20\mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 2.4\text{ mA}$ $ I_{out} \leq 4.0\text{ mA}$ $ I_{out} \leq 5.2\text{ mA}$	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20\mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 2.4\text{ mA}$ $ I_{out} \leq 4.0\text{ mA}$ $ I_{out} \leq 5.2\text{ mA}$	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu\text{A}$	6.0	4	40	160	μA

MC74HC4040A

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 5)	2.0	10	9.0	8.0	MHz
		3.0	15	14	12	
		4.5	30	28	25	
		6.0	50	45	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q1* (Figures 2 and 5)	2.0	96	106	115	ns
		3.0	63	71	88	
		4.5	31	36	40	
		6.0	25	30	35	
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 3 and 5)	2.0	65	72	90	ns
		3.0	30	36	40	
		4.5	30	35	40	
		6.0	26	32	35	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Q _n to Q _{n+1} (Figures 4 and 5)	2.0	69	80	90	ns
		3.0	40	45	50	
		4.5	17	21	28	
		6.0	14	15	22	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 5)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	15	19	
C _{in}	Maximum Input Capacitance		10	10	10	pF

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_p = [93.7 + 59.3 (n-1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_p = [30.25 + 14.6 (n-1)] \text{ ns}$$

$$V_{CC} = 3.0 \text{ V: } t_p = [61.5 + 34.4 (n-1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_p = [24.4 + 12 (n-1)] \text{ ns}$$

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V		pF
		31		

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 3)	2.0	30	40	50	ns
		3.0	20	25	30	
		4.5	5	8	12	
		6.0	4	6	9	
t _w	Minimum Pulse Width, Clock (Figure 2)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t _w	Minimum Pulse Width, Reset (Figure 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	15	19	24	
		6.0	13	16	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 2)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

MC74HC4040A

PIN DESCRIPTIONS

INPUTS

Clock (Pin 10)

Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

Reset (Pin 11)

Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

OUTPUTS

Q1 thru Q12 (Pins 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1)

Active-high outputs. Each Qn output divides the Clock input frequency by 2^N .

SWITCHING WAVEFORMS

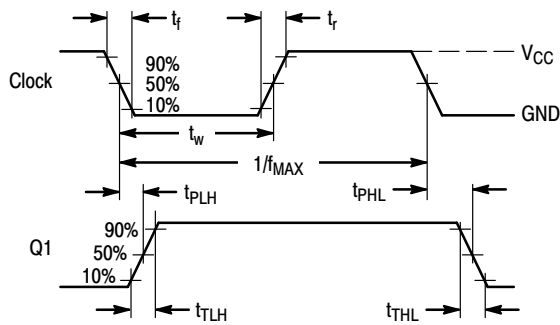


Figure 2.

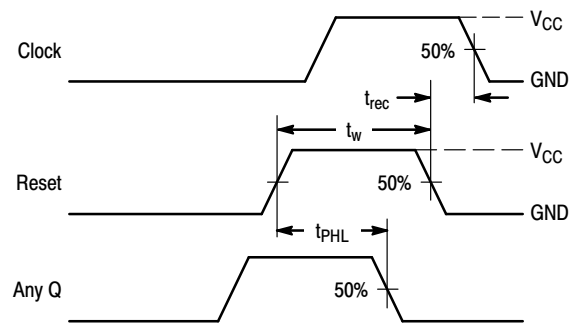


Figure 3.

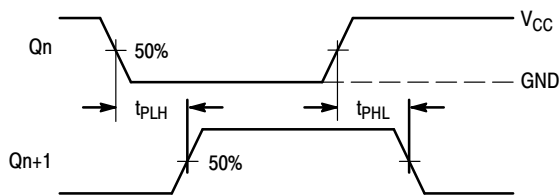
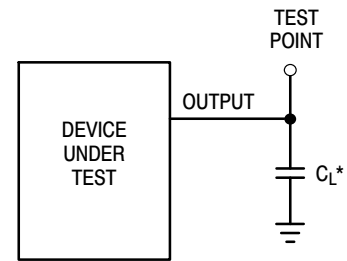


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit

MC74HC4040A

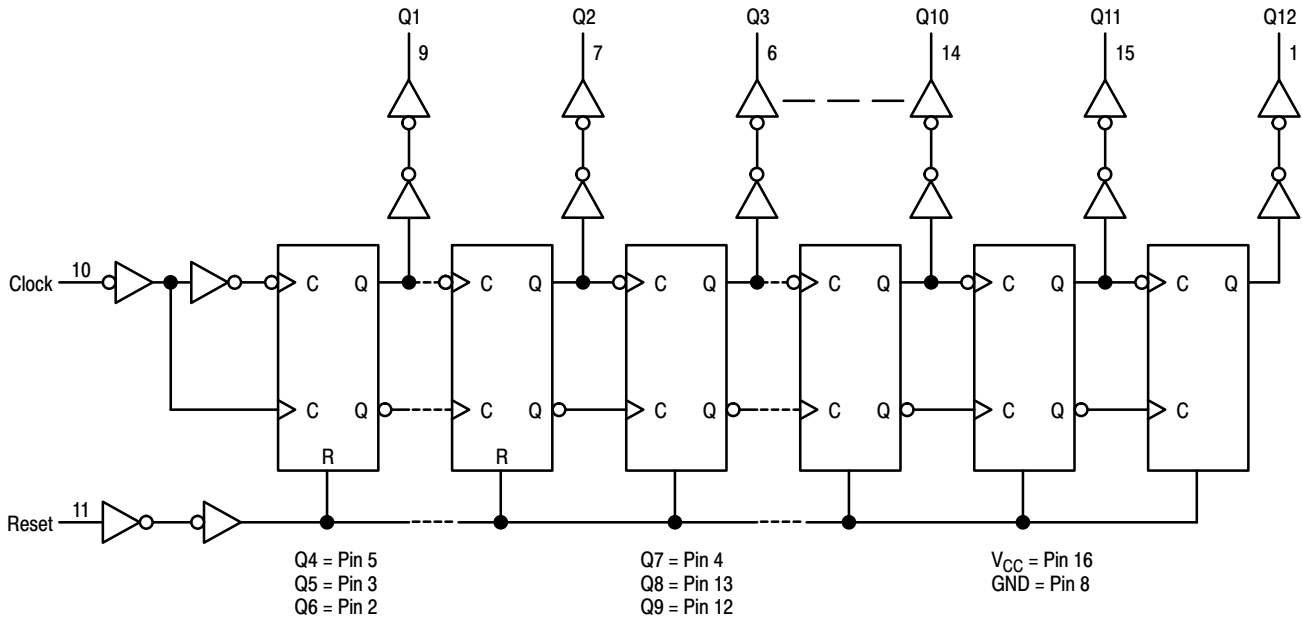


Figure 6. Expanded Logic Diagram

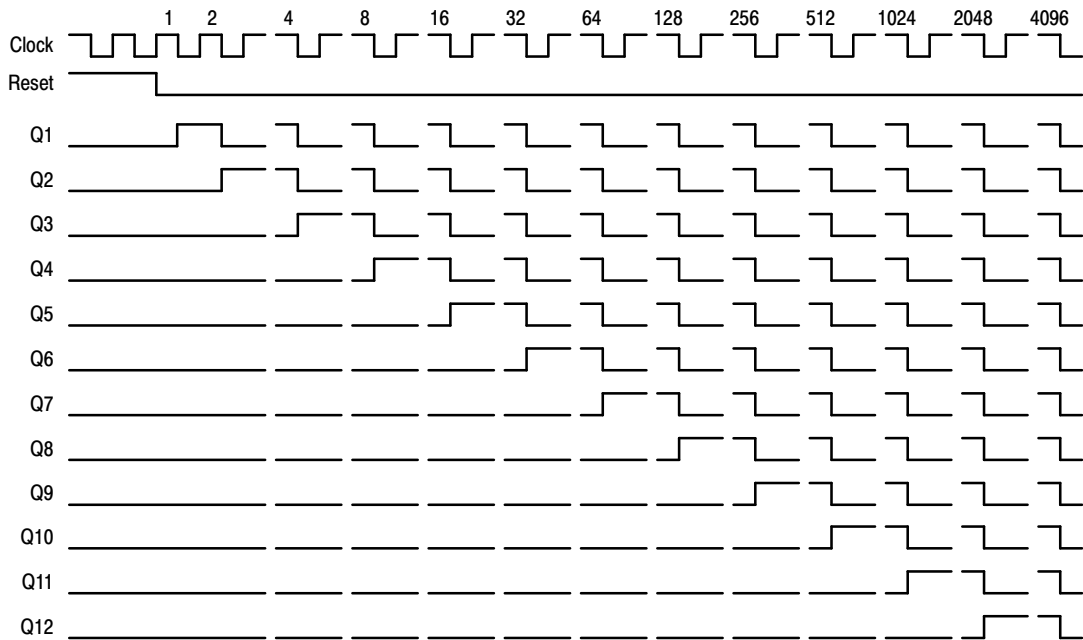


Figure 7. Timing Diagram

MC74HC4040A

APPLICATIONS INFORMATION

Time-Base Generator

A 60Hz sinewave obtained through a 100 K resistor connected to a 120 Vac power line through a step down transformer is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares-up the input

waveform and feeds the HC4040A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

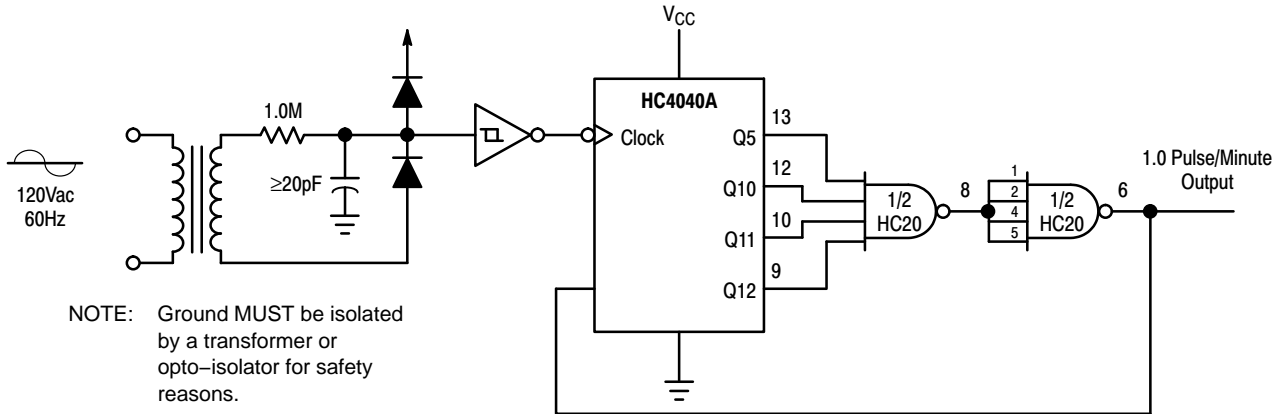


Figure 8. Time-Base Generator

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC4040ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4040ADR2G	SOIC-16 (Pb-Free)	2500 Units / Reel
NLV74HC4040ADR2G*	SOIC-16 (Pb-Free)	2500 Units / Reel
MC74HC4040ADTR2G	TSSOP-16 (Pb-Free)	2500 Units / Reel

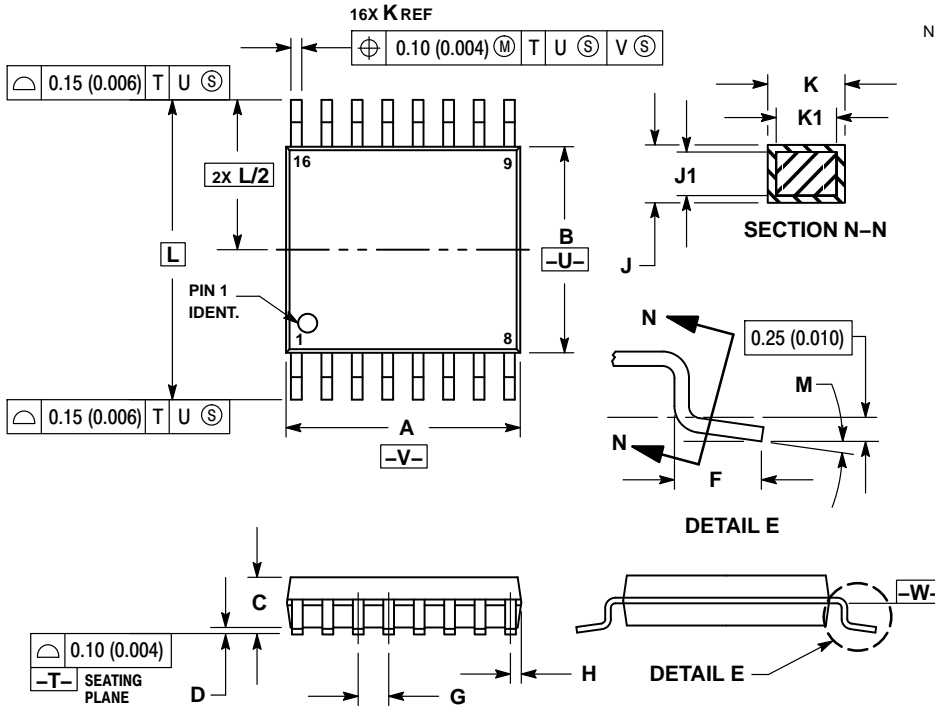
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC74HC4040A

PACKAGE DIMENSIONS

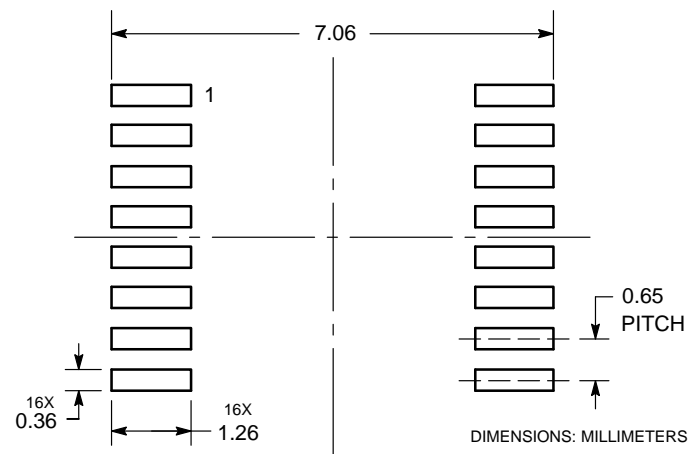
TSSOP-16
CASE 948F
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

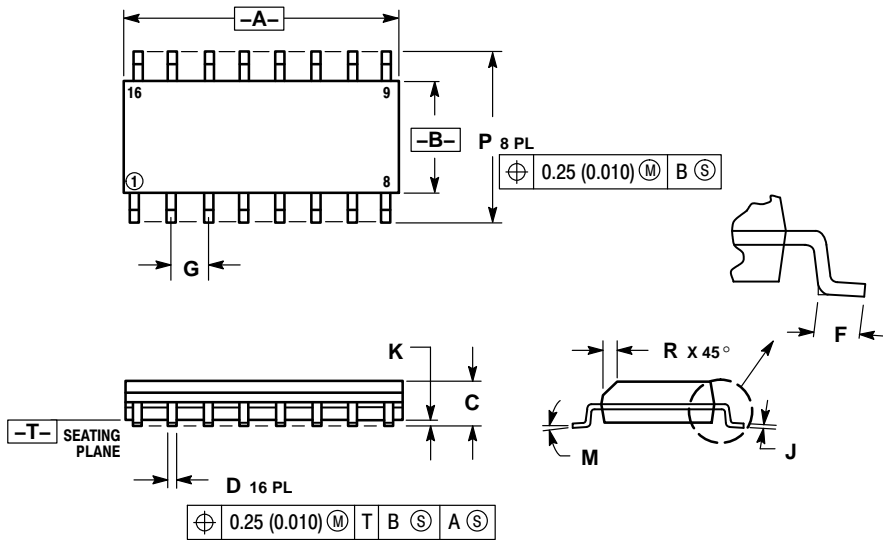


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC4040A

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

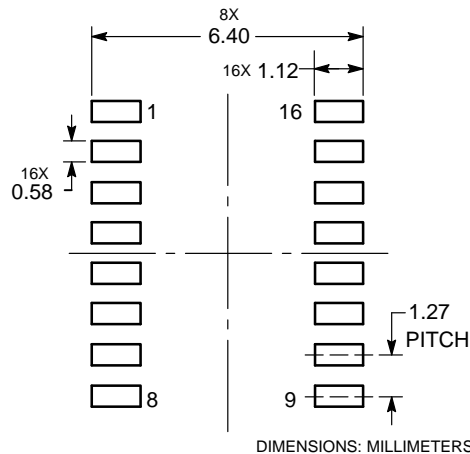


NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View MC74HC4040AFELG on WIN SOURCE](#)

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management