THE DATASHEET OF

MC74LCX257DR2G

www.win-source.net 0086-755-83957316

MC74LCX257

Low-Voltage CMOS Quad 2-Input Multiplexer

With 5.0 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The MC74LCX257 is a high performance, quad 2−input multiplexer with 3−state outputs operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX257 inputs to be safely driven from 5.0 V devices.

Four bits of data from two sources can be selected using the Select input. The four outputs present the selected data in the true (non−inverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the Output Enable ($\overline{OE}$) input. Current drive capability is 24 mA at the outputs.

Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5.0 V Tolerant − Interface Capability with 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >200 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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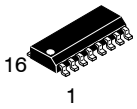
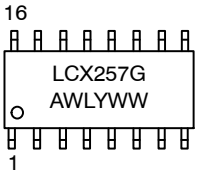
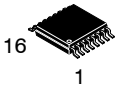
MARKING DIAGRAMS

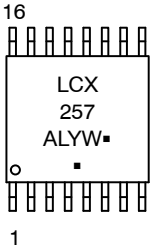


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A	=	Assembly Location
WL, L	=	Wafer Lot
Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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Publication Order Number:
MC74LCX257/D

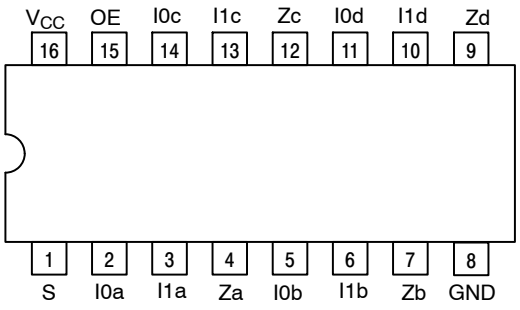


Figure 1. Pinout: 16−Lead Plastic Package
(Top View)

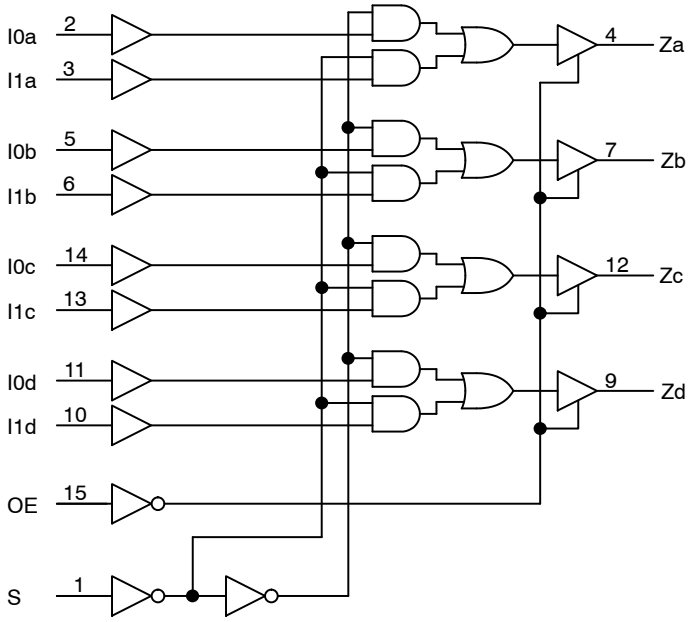


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
I0n	Source 0 Data Inputs
I1n	Source 1 Data Inputs
$\overline{OE}$	Output Enable Input
S	Select Input
Zn	Outputs

TRUTH TABLE

Inputs				Outputs
$\overline{OE}$	S	I0n	I1n	Zn
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High Voltage Level
L = Low Voltage Level
X = High or Low Voltage Level and Transitions are Acceptable
Z = High Impedance State

For ICC reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_I \le +7.0$	Output in 3−State	V
		$-0.5 \le V_O \le V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Type	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	 2.0 1.5	 2.5, 3.3 2.5, 3.3	 3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3−State)	 0 0		 V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			 −24 −12 −8	mA
I_{OL}	LOW Level Output Current V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			 +24 +12 +8	mA
T_A	Operating Free−Air Temperature	−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0		10	ns/V

ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX257DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74LCX257DTG	TSSOP−16 (Pb−Free)	96 Units / Rail
MC74LCX257DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = −40°C to +85°C Min	Max	Units
V_{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V_{CC} ≤ 3.6 V	2.0		
V_{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V_{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V_{CC} ≤ 3.6 V		0.8	
V_{OH}	HIGH Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = −100 μA	V_{CC} − 0.2		V
		V_{CC} = 2.3 V; I_{OH} = −8 mA	1.8		
		V_{CC} = 2.7 V; I_{OH} = −12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = −18 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = −24 mA	2.2		
V_{OL}	LOW Level Output Voltage	2.3 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 2.3 V; I_{OL} = 8 mA		0.6	
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 16 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
I_{OZ}	3−State Output Current	V_{CC} = 3.6 V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0 to 5.5 V		±5	μA
I_{OFF}	Power Off Leakage Current	V_{CC} = 0, V_{IN} = 5.5 V or V_{OUT} = 5.5 V		10	μA
I_{IN}	Input Leakage Current	V_{CC} = 3.6 V, V_{IN} = 5.5 V or GND		±5	μA
I_{CC}	Quiescent Supply Current	V_{CC} = 3.6 V, V_{IN} = 5.5 V or GND		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.3 ≤ V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} − 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS t_R = t_F = 2.5 ns; R_L = 500 Ω

Symbol	Parameter	Waveform	Limits: T_A = −40°C to +85°C, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF Min	Max	V_{CC} = 2.7 V, C_L = 50 pF Min	Max	V_{CC} = 2.5 V ± 0.2 V, C_L = 30 pF Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay In to Zn	1	1.5 1.5	6.0 6.0	1.5 1.5	6.5 6.5	1.5 1.5	7.2 7.2	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zn	1, 2	1.5 1.5	7.0 7.0	1.5 1.5	8.5 8.5	1.5 1.5	9.1 9.1	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	3	1.5 1.5	7.0 7.0	1.5 1.5	8.5 8.5	1.5 1.5	9.1 9.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time from High and Low Level	3	1.5 1.5	5.5 5.5	1.5 1.5	6.0 6.0	1.5 1.5	6.6 6.6	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

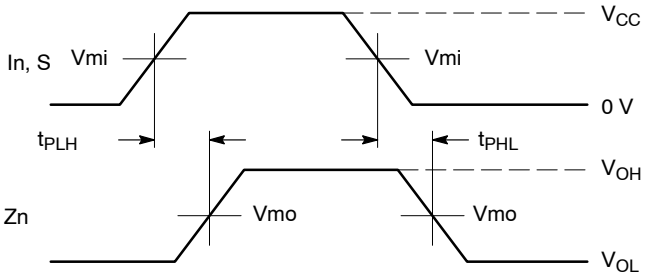
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Units
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		0.8 0.6		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		−0.8 −0.6		V

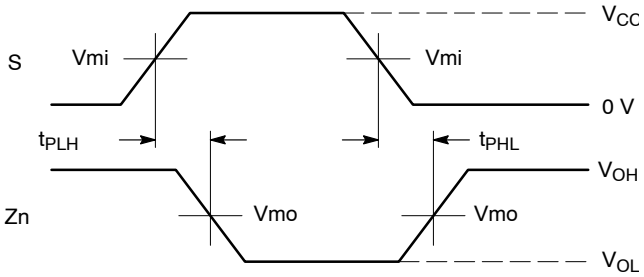
4. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

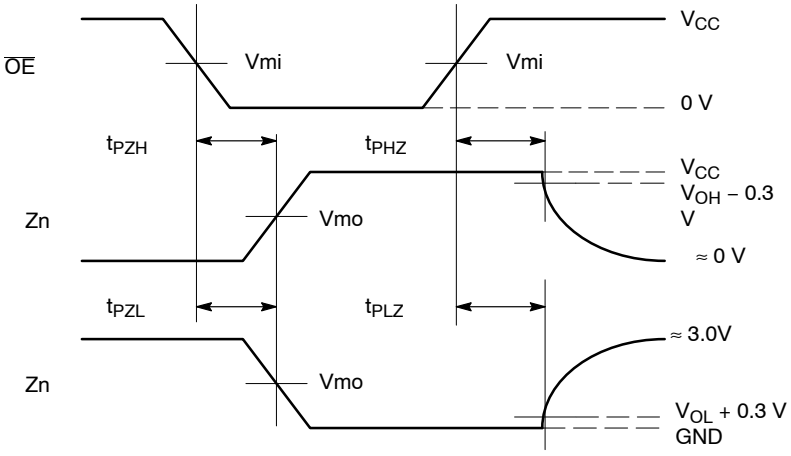
Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF



WAVEFORM 1 – NON−INVERTING PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1.0 MHz; t_W = 500 ns



WAVEFORM 2 – INVERTING PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1.0 MHz; t_W = 500 ns



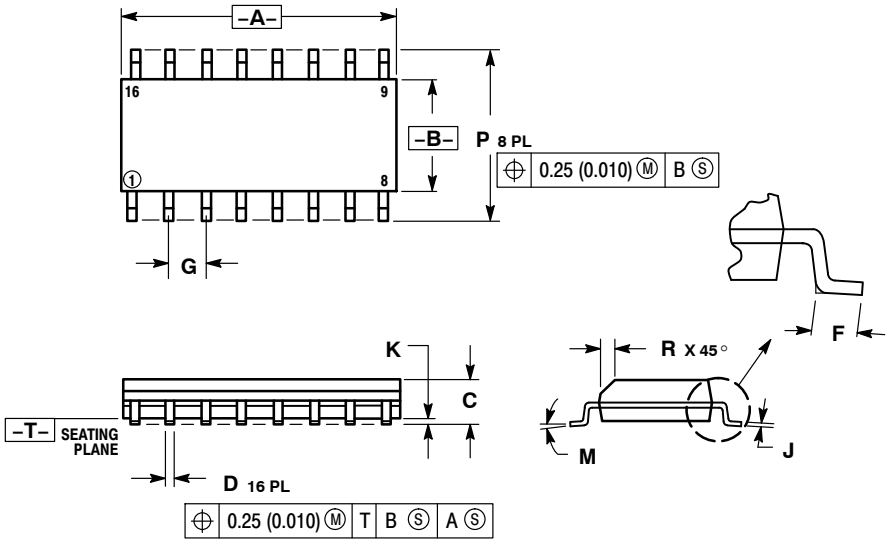
WAVEFORM 3 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1.0 MHz; t_W = 500 ns

Symbol	Vcc		
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
Vmi	1.5 V	1.5 V	Vcc/2
Vmo	1.5 V	1.5 V	Vcc/2
V_{HZ}	V_{OL} + 0.3 V	V_{OL} + 0.3 V	V_{OL} + 0.15 V
V_{LZ}	V_{OH} − 0.3 V	V_{OH} − 0.3 V	V_{OH} − 0.15 V

Figure 3. AC Waveforms

PACKAGE DIMENSIONS

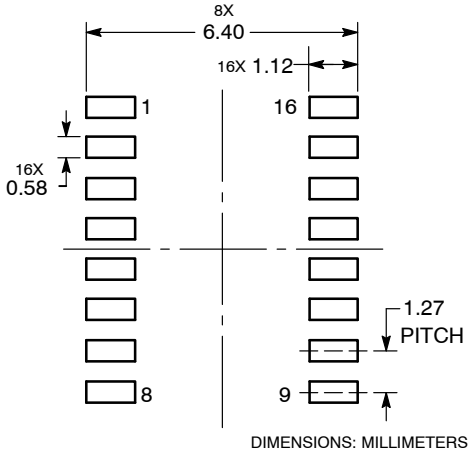
SOIC−16
D SUFFIX
CASE 751B−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

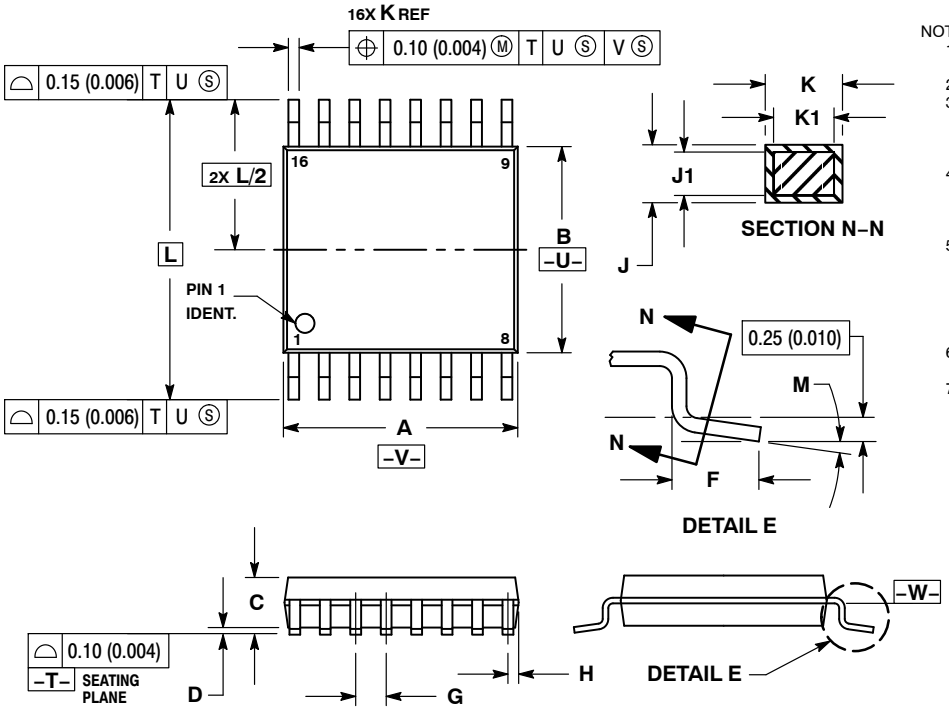
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

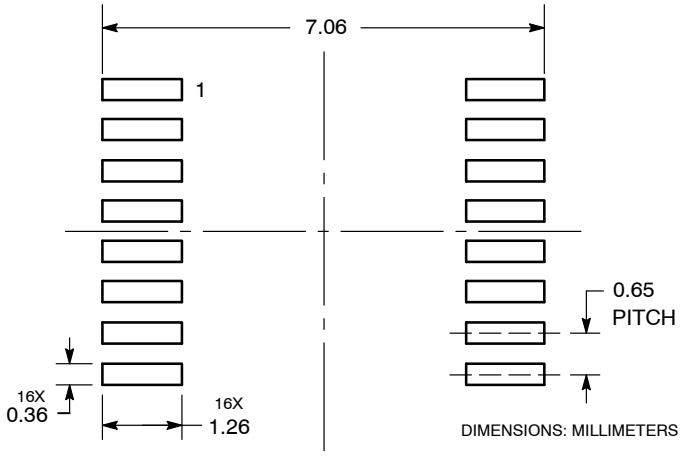
TSSOP−16
DT SUFFIX
CASE 948F−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



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