



**THE DATASHEET OF
MC74VHCT00ADR2G**



MC74VHCT00A

Quad 2-Input NAND Gate

The MC74VHCT00A is an advanced high speed CMOS 2-input NAND gate fabricated with silicon gate CMOS technology. It achieves high speed operation while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHCT00A input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHCT00A to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

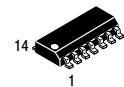
- High Speed: $t_{PD} = 5.0$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 3.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: 48 FETs or 12 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant



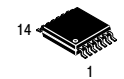
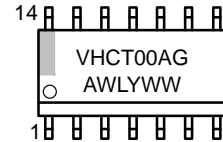
ON Semiconductor®

<http://onsemi.com>

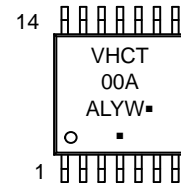
MARKING DIAGRAMS



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 6 of this data sheet.

MC74VHCT00A

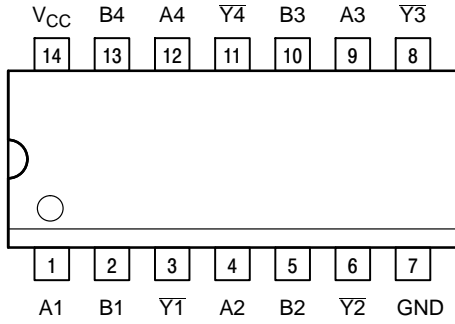


Figure 1. Pin Assignment
(Top View)

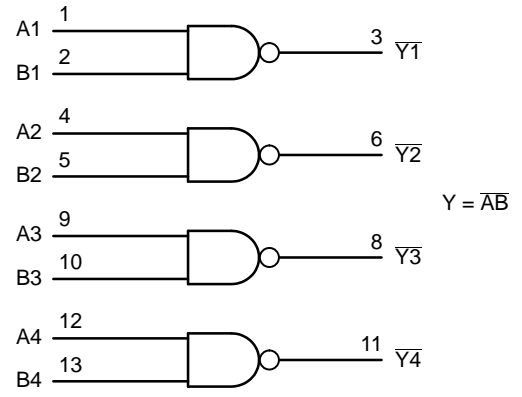


Figure 2. Logic Diagram

PIN ASSIGNMENT	
1	IN A1
2	IN B1
3	OUT Y1
4	IN A2
5	IN B2
6	OUT Y2
7	GND
8	OUT Y3
9	IN A3
10	IN B3
11	OUT Y4
12	IN A4
13	IN B4
14	V _{CC}

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

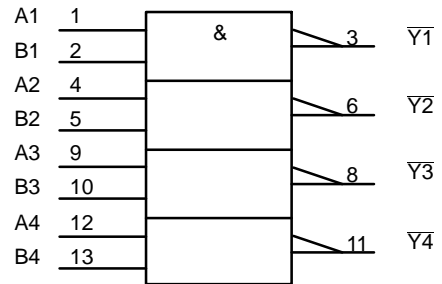


Figure 3. IEC LOGIC DIAGRAM

MC74VHCT00A

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage V _{CC} = 0 High or Low State	-0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current V _{OUT} < GND; V _{OUT} > V _{CC}	+20	mA
I _{OUT}	DC Output Current, per Pin	+25	mA
I _{CC}	DC Supply Current, V _{CC} and GND	+50	mA
P _D	Power Dissipation in Still Air, SOIC Package (Note 1) TSSOP Package (Note 1)	500 450	mW
T _L	Lead temperature, 1 mm from case for 10 s	260	°C
T _{stg}	Storage temperature	-65 to +150	°C
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 > 3000	V
I _{Latch-Up}	Latch-Up Performance (Note 5) Above V _{CC} and Below GND at 125°C	±300	mA

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Derating – SOIC Package: -7 mW/°C from 65° to 125°C
– TSSOP Package: -6.1 mW/°C from 65° to 125°C
- Tested to EIA/JESD22-A114-A
- Tested to EIA/JESD22-A115-A
- Tested to JESD22-C101-A
- Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	3.0	5.5	V
V _{IN}	DC Input Voltage	0.0	5.5	V
V _{OUT}	DC Output Voltage V _{CC} = 0 High or Low State	0.0 0.0	5.5 V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74VHCT00A

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

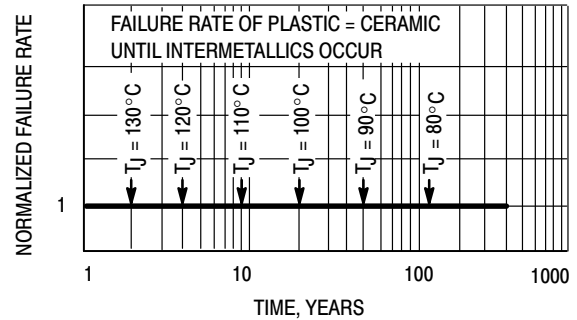


Figure 4. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0	V	
V _{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4	V	
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66	V	
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		20		40	μA
I _{CCT}	Quiescent Supply Current	Input: V _{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74VHCT00A

AC ELECTRICAL CHARACTERISTICS $C_{load} = 50 \text{ pF}$, Input $t_r = t_f = 3.0 \text{ ns}$

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or B to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		4.1 5.5	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		3.1 3.6	6.9 7.9		8.0 9.0		9.5 10.5	
C_{IN}	Maximum Input Capacitance			5.5 10			10		10	pF

Symbol	Parameter	Typical @ 25°C , $V_{CC} = 5.0 \text{ V}$		Unit
		Min	Max	
C_{PD}	Power Dissipation Capacitance (Note 6)		17	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$, $C_L = 50 \text{ pF}$, $V_{CC} = 5.0 \text{ V}$, Measured in SO Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.4	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.4	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

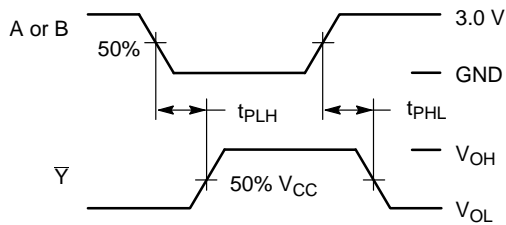
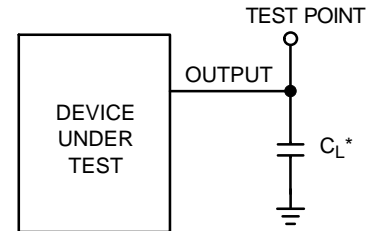


Figure 5. Switching Waveforms



*Includes all probe and jig capacitance

Figure 6. Test Circuit

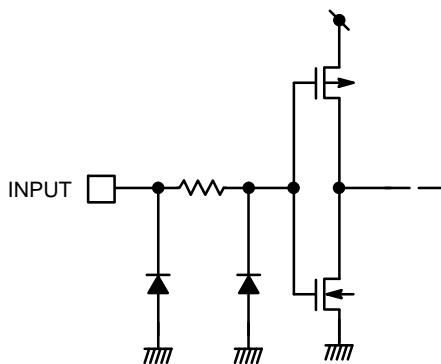
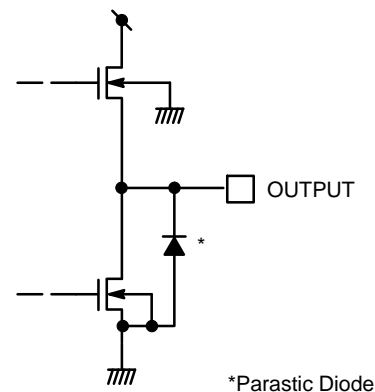


Figure 7. Input Equivalent Circuit



*Parastic Diode

Figure 8. Output Equivalent Circuit

MC74VHCT00A

ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT00ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHCT00ADTR2G	TSSOP-14 (Pb-Free)	2000 / Tape & Reel
NLV74VHCT00ADTR2G*		

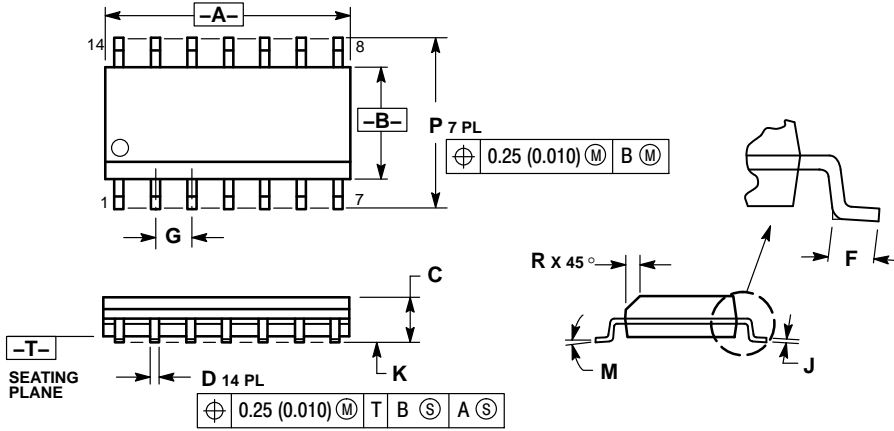
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC74VHCT00A

PACKAGE DIMENSIONS

SOIC-14
D SUFFIX
CASE 751A-03
ISSUE J

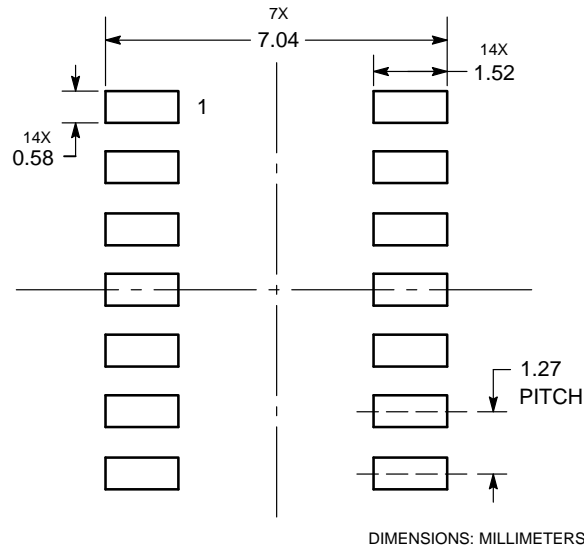


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

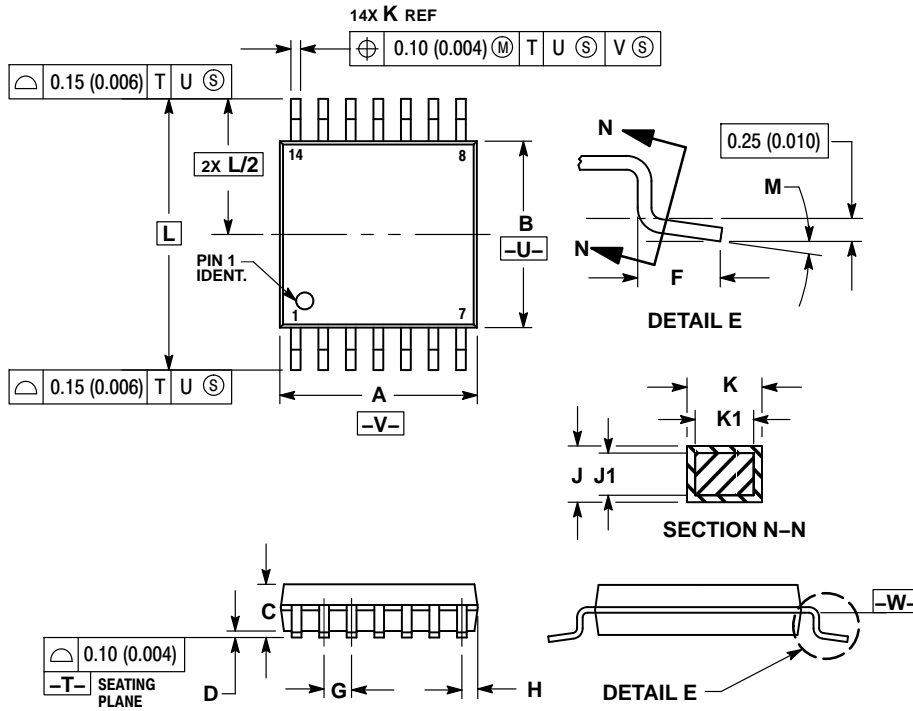
SOLDERING FOOTPRINT



MC74VHCT00A

PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G
ISSUE B

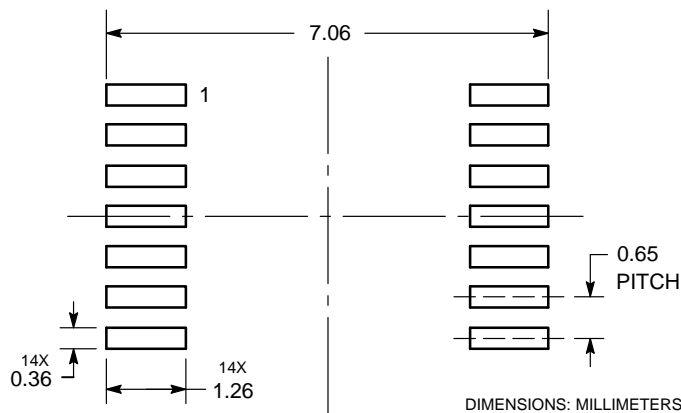


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ [View MC74VHCT00ADR2G on WIN SOURCE](#)

⊖ [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management