

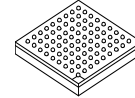


**THE DATASHEET OF
MCIMX27LMOP4A**





i.MX27 and i.MX27L



Package Information

Plastic Package
Case 1816-01
(MAPBGA-404)
Case 1931-04
(MAPBGA-473)

i.MX27 and i.MX27L Data Sheet

Multimedia Applications Processor

Ordering Information

See [Table 1](#) on [page 4](#) for ordering information.

1 Introduction

The i.MX27 and i.MX27L (MCIMX27/MX27L) multimedia applications processors represents the next step in low-power, high-performance application processors. Unless otherwise specified, the material in this data sheet is applicable to both the i.MX27 and i.MX27L processors and referred to singularly throughout this document as i.MX27.

The i.MX27L does not include the following features: ATA-6 HDD Interface, Memory Stick Pro, VPU: MPEG-4/ H.263/H.264 HW encoder/decoder, and eMMA (PrP processing, CSC, deblock, dering).

Based on an ARM926EJ-S™ microprocessor core, the i.MX27/27L processor provides the performance with low power consumption required by modern digital devices such as the following:

- Feature-rich cellular phones
- Portable media players and mobile gaming machines
- Personal digital assistants (PDAs) and wireless PDAs

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Introduction

- Portable DVD players
- Digital cameras

The i.MX27/MX27L processor features the advanced and power-efficient ARM926EJ-S core operating at speeds up to 400 MHz, and is optimized for minimal power consumption using the most advanced techniques for power saving (for example, DPTC, power gating, and clock gating). With 90 nm technology and dual V_t , the i.MX27/MX27L device provides the optimal performance vs. leakage current balance.

The performance of the i.MX27/MX27L processors are both boosted by an on-chip cache system, and features peripheral devices, such as an MPEG-4, H.263, an H.264 video codec (up to D1—720 x 486—@ 30 FPS), LCD, eMMA_lt, and CMOS Sensor Interface controllers.

The i.MX27/MX27L processors supports connections to various types of external memories, such as 266-MHz DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The i.MX27/MX27L devices can be connected to a variety of external devices using technology, such as high-speed USBOTG 2.0, the Advanced Technology Attachment (ATA), Multimedia/Secure Data (MMC/SDIO), and CompactFlash.

NOTE

The i.MX27L does not support the ATA-6 HDD interface.

1.1 Features

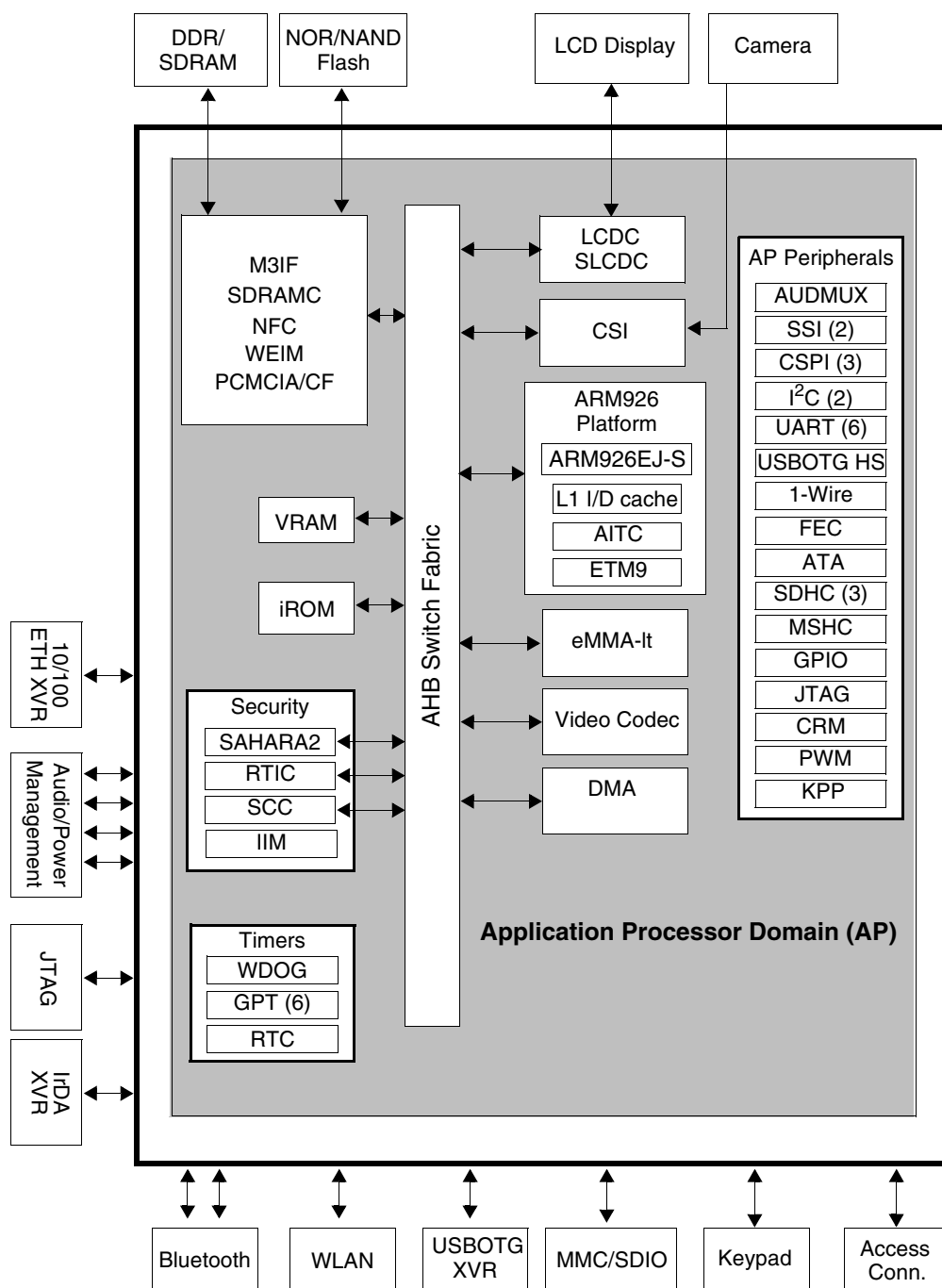
The i.MX27/MX27L processors are targeted for video and voice over-IP (V2IP) and smart remote controllers. It also provides low-power solutions for any high-performance and demanding multimedia and graphics applications.

The systems include the following features:

- Multi-standard video codec (i.MX27 only)
 - MPEG-4 part-II simple profile encoding/decoding
 - H.264/AVC baseline profile encoding/decoding
 - H.263 P3 encoding/decoding
 - Multi-party call: one stream encoding and two streams decoding simultaneously
 - Multi-format: encodes MPEG-4 bitstream, and decodes H.264 bitstream simultaneously
 - On-the-fly video processing that reduces system memory load (for example, the power-efficient viewfinder application with no involvement of either the memory system or the Arm CPU)
- Advanced power management (i.MX27/27L)
 - Dynamic process and temperature compensation
 - Multiple clock and power domains
 - Independent gating of power domains
- Multiple communication and expansion ports

1.2 Block Diagram

Figure 1 shows the i.MX27 simplified interface block diagram.



Note: The i.MX27L does not support the following:

- ATA-6 HDD Interface
- Memory Stick Pro
- VPU: MPEG-4/.263/H.264 HW encoder/decoder
- eMMA (PrP processing, CSC, deblock, dering)

Figure 1. i.MX27/MX27L Simplified Interface Block Diagram

1.3 Ordering Information

Table 1 provides ordering information for the MAPBGA, lead-free packages.

Table 1. Ordering Information

| Device | Temperature | Package |
|---------------|------------------|---------|
| MCIMX27VOP4A | -20° C to +85° C | 1816-01 |
| MCIMX27LVOP4A | -20° C to +85° C | 1816-01 |
| MCIMX27MOP4A | -40° C to +85° C | 1931-04 |
| MCIMX27LMOP4A | -40° C to +85° C | 1931-04 |
| MCIMX27VJP4A | -20° C to +85° C | 1816-01 |
| MCIMX27LVJP4A | -20° C to +85° C | 1816-01 |
| MCIMX27MJP4A | -40° C to +85° C | 1931-04 |
| MCIMX27LMJP4A | -40° C to +85° C | 1931-04 |

2 Functional Description and Application Information

2.1 ARM926 Microprocessor Core Platform

The ARM926 Platform consists of the ARM926EJ-S processor, ETM9, ETB9, a 6 × 3 Multi-Layer AHB crossbar switch (MAX), and a “primary AHB” complex.

- The instruction bus (I-AHB) of the ARM926EJ-S processor is connected directly to MAX Master Port 0.
- The data bus (D-AHB) of the ARM926EJ-S processor is connected directly to MAX Master Port 1.

Four alternate bus master interfaces are connected to MAX Master Ports 2–5. Three slave ports of the MAX are AHB-Lite compliant buses. Slave Port 0 is designated as the “primary” AHB. The primary AHB is internal to the platform and has five slaves connected to it: the AITC interrupt module, the MCTL memory controller, and two AIPI peripheral interface gaskets. Slave Ports 1 and 2 of the MAX are referred to as “secondary” AHBs. Each of the secondary AHB interfaces is only accessible off platform.

The ARM926EJ-S processor supports the 32-bit and 16-bit Arm Thumb instruction sets, enabling the user to trade off between high performance and high-code density. The ARM926EJ-S processor includes features for efficient execution of Java byte codes, providing Java performance similar to the just-in-time (JIT) compiler—which is a type of Java compiler—but without the associated code overhead.

The ARM926EJ-S processor supports the Arm debug architecture and includes logic to assist in both hardware and software debugging. The ARM926EJ-S processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including the following:

- An ARM9EJ-S integer core
- A Memory Management Unit (MMU)
- Separate instruction and data AMBA AHB bus interfaces
- ETM and JTAG-based debug support

The ARM926EJ-S processor provides support for external coprocessors enabling floating-point or other application-specific hardware acceleration to be added. The ARM926EJ-S processor implements Arm architecture version 5TEJ.

The four alternate bus master ports on the ARM926 Platform, which are connected directly to master ports of the MAX, are designed to support connections to multiple AHB masters external to the platform. An external arbitration AHB control module is needed if multiple external masters are desired to share an ARM926 Platform alternate bus master port. However, the alternate bus master ports on the platform support seamless connection to a single master with no external interface logic required.

A primary AHB MUX (PAHBMUX) module performs address decoding, read data muxing, bus watchdog, and other miscellaneous functions for the primary AHB within the platform. A clock control module (CLKCTL) is provided to support a power-conscious design methodology, as well as implementation of several clock synchronization circuits.

2.1.1 Memory System

The ARM926EJ-S complex includes 16-Kbyte Instruction and 16-Kbyte Data caches. The embedded 45-Kbyte SRAM (VRAM) can be used to avoid external memory accesses or it can be used for applications. There is also a 24-Kbyte ROM for bootstrap code.

2.2 Module Inventory

Table 2 shows an alphabetical listing of the modules in the i.MX27/MX27L multimedia applications processors. A cross-reference to each module's section and page number goes directly to a more detailed module description for additional information.

Table 2. Digital and Analog Modules

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|----------------|------------------------------------|-------------------------|---|------------------|
| 1-Wire® | 1-Wire Interface | Connectivity Peripheral | The 1-Wire module provides bi-directional communication between the ARM926EJ-S and the Add-Only-Memory EPROM (DS2502). The 1-Kbit EPROM is used to hold information about battery and communicates with the ARM926 Platform using the IP interface. | 2.3.1/9 |
| AIPI | AHB-Lite IP Interface Module | Bus Control | The AIPI acts as an interface between the Arm Advanced High-performance Bus Lite. (AHB-Lite) and lower bandwidth peripherals that conforms to the IP Bus specification, Rev 2.0. | 2.3.2/9 |
| AITC | ARM9EJ-S Interrupt Controller | Bus Control | AITC is connected to the primary AHB as a slave device. It generates the normal and fast interrupts to the ARM926EJ-S processor. | 2.3.3/10 |
| ARM926EJS | ARM926EJ-S | CPU | The ARM926EJ-S (ARM926) is a member of the Arm9 family of general-purpose microprocessors targeted at multi-tasking applications. | 2.3.4/10 |
| ATA | Advanced Technology(AT) Attachment | Connectivity Peripheral | The ATA block is an AT attachment host interface. It interfaces with IDE hard disc drives and ATAPI optical disc drives. | 2.3.5/10 |

Table 2. Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|------------------|---|---------------------------|---|---------------------------|
| AUDMUX | Digital Audio Multiplexer | Multimedia Peripheral | The AUDMUX interconnections allow multiple, simultaneous audio/voice/data flows between the ports in point-to-point or point-to-multipoint configurations. | 2.3.6/11 |
| CRM | Clock and Reset Module | Clock and Reset Control | The CRM generates clock and reset signals used throughout the i.MX27/MX27L processors and also for external peripherals. | 2.3.7/12 |
| CSI | CMOS Sensor Interface | Multimedia Interface | The CSI is a logic interface which enables the i.MX27/MX27L processors to connect directly to external CMOS sensors and a CCIR656 video source. | 2.3.8/12 |
| CSPI | Configurable Serial Peripheral Interface (x3) | Connectivity Peripheral | The i.MX27/MX27L processors have three CSPI modules. CSPI is equipped with two data FIFOs and is a master/slave configurable serial peripheral interface module, allowing the i.MX27/MX27L processors to interface with both external SPI master and slave devices. | 2.3.9/12 |
| DMAC | Direct Memory Access Controller | Standard System Resource | The DMAC of the i.MX27/MX27L processors provides 16 channels supporting linear memory, 2D memory, FIFO and end-of-burst enable FIFO transfers to support a wide variety of DMA operations. | 2.3.10/13 |
| eMMA_It | eMMA_It | H/W Accelerator Functions | eMMA_It consists of a PreProcessor and PostProcessor, and provides video acceleration. The PrP and PP can be used for generic video pre and post processing such as scaling, resizing, and color space conversions. | 2.3.11/13 |
| EMI | External Memory Interface | Memory Interface (EMI) | The EMI includes <ul style="list-style-type: none"> • Multi-Master Memory Interface (M3IF) • Enhanced SDRAM/MDDR memory controller (ESDRAMC) • PCMCIA memory controller (PCMCIA) • NAND Flash Controller (NFC) • Wireless External Interface Module (WEIM) | — |
| ESDRAMC | Enhanced SDRAM Controller | External Memory Interface | The ESDRAMC provides interface and control for synchronous DRAM memories for the system. | 2.3.12/15 |
| FEC | Fast Ethernet Controller | Connectivity Peripheral | The FEC performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC supports connection and functionality for the 10/100 Mbps 802.3 media independent interface (MII). It requires an external transceiver (PHY) to complete the interface to the media. | 2.3.13/15 |
| GPIO | General Purpose I/O Module | Pins | The GPIO provides 32 bits of bidirectional, general purpose I/O. This peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. | 2.3.14/16 |
| GPT | General Purpose Timer | Timer Peripheral | The GPT is a multipurpose module used to measure intervals or generate periodic output. | 2.3.15/16 |
| I ² C | Inter IC Communication | Connectivity Peripheral | The I ² C provides serial interface to control the sensor interface and other external devices. Data rates of up to 100 Kbits/s are supported. | 2.3.16/17 |

Table 2. Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|----------------|---|---------------------------|---|---------------------------|
| IIM | IC Identification Module | Security | The IIM provides an interface for reading—and in some cases, programming, and overriding identification and control information stored in on-chip fuse elements. Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, SAHARA2 | 2.3.17/17 |
| JTAGC | JTAG Controller | Debug | The JTAGC provides debug access to the ARM926 core, built-in self-test (BIST), and boundary scan test control. | 2.3.18/17 |
| KPP | Keypad Port | Connectivity Peripheral | The KPP is used for key pad matrix scanning or as a general purpose I/O. This peripheral simplifies the software task of scanning a keypad matrix. | 2.3.19/17 |
| LCDC | Liquid Crystal Display Controller | Multimedia Interface | The LCDC provides display data for external gray-scale or color LCD panels. | 2.3.20/17 |
| M3IF | Multi-Master Memory Interface | External Memory Interface | The M3IF controls memory accesses from one or more masters through different port interfaces to different external memory controllers ESDCTL/MDDRC, PCMCIA, NFC, and WEIM. | 2.3.21/18 |
| MAX | Multi-layer AHB Crossbar Switch | Bus Control | The ARM926EJ-S processor's instruction and data buses and all alternate bus master interfaces arbitrate for resources via a 6 × 3 MAX. There are six fully functional master ports (M0–M5) and three fully functional slave ports (S0–S2). The MAX is uni-directional. All master and slave ports are AHB-Lite compliant. | 2.3.22/18 |
| MSHC | Memory Stick Host Controller | Connectivity Peripheral | The MSHC is placed in between the AIPI and the customer memory stick to support data transfer from the i.MX27 device to the customer memory stick. Note: The i.MX27L does not support the MSHC feature. | 2.3.23/19 |
| NFC | NAND Flash Controller | External Memory Interface | The NFC is a submodule of EMI. The NFC implements the interface to standard NAND Flash memory devices. | 2.3.24/19 |
| PCMCIA | Personal Computer Memory Card International Association | External Memory Interface | The PCMCIA host adapter module provides the control logic for PCMCIA socket interfaces, and requires some additional external analog power switching logic and buffering. | 2.3.25/20 |
| PLL | Phase Lock Loop | Clock and Reset Control | The two DPLLs provide clock generation in digital and mixed analog/digital chips designed for wireless communication and other applications. | 2.3.26/20 |
| PWM | Pulse-Width Modulator | Timer Peripheral | The PWM has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. | 2.3.27/20 |
| RTC | Real Time Clock | Timer Peripheral | The RTC module provides a current stamp of seconds, minutes, hours, and days. Alarm and timer functions are also available for programming. The RTC supports dates from the year 1980 to 2050. | 2.3.28/20 |

Table 2. Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|----------------|---|--------------------------|---|---------------------------|
| RTIC | Run-Time Integrity Checkers | Security | The RTIC ensures the integrity of the contents of the peripheral memory and assists with boot authentication. Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, SAHARA2 | 2.3.29/21 |
| SAHARA2 | Symmetric/Asymmetric Hashing and Random Accelerator | Security | SAHARA2 is a security co-processor which forms part of the Platform Independent Security Architecture (PISA), and can be used on cell phone baseband processors or wireless PDAs. Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, SAHARA2 | 2.3.30/21 |
| SCC | Security Controller Module | Security | The SCC is a hardware component composed of two blocks—the Secure RAM module, and the Security Monitor. The Secure RAM provides a way of securely storing sensitive information. The Security Monitor implements the security policy, checking algorithm sequencing, and controlling the Secure State. Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, SAHARA2 | 2.3.31/21 |
| SDHC | Secured Digital Host Controller | Connectivity Peripheral | The SDHC controls the MMC (MultiMediaCard), SD (Secure Digital) memory, and I/O cards by sending commands to cards and performing data accesses to and from the cards. | 2.3.32/21 |
| SLCDC | Smart Liquid Crystal Display Controller | Multimedia Interface | The SLCDC module transfers data from the display memory buffer to the external display device. | 2.3.33/22 |
| SSI | Synchronous Serial Interface | Multimedia Peripheral | The SSI is a full-duplex, serial port that allows the chip to communicate with a variety of serial devices, such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I ² S) and Intel AC97 standard. | 2.3.34/22 |
| UART | Universal Asynchronous Receiver/Transmitter | Connectivity Peripheral | The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility. | 2.3.35/23 |
| USB | Universal Serial Bus–2 Host Controllers and 1 OTG (On-The-Go) | Connectivity Peripherals | The i.MX27/MX27L processors provide two USB Host controllers and one USBOTG of which: <ul style="list-style-type: none"> • USB Host 1 is designed to support transceiverless connection to the on-board peripherals in Low Speed and Full Speed mode, and connection to the ULPI (UTMI+Low-Pin Count) and Legacy Full Speed transceivers • USB Host 2 is designed to support transceiverless connection to the Cellular Modem Baseband Processor • The USBOTG controller offers HS/FS/LS capabilities in Host mode and HS/FS in device mode. In Host mode, the controller supports direct connection of a FS/LS device (without external hub). In device (bypass) mode, the OTG port functions as gateway between the Host 1 Port and the OTG transceiver. | 2.3.36/23 |

Table 2. Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|----------------|------------------------------------|---------------------------|--|---------------------------|
| Video Codec | Video Codec | Hardware Acceleration | Video Codec module supports full duplex video codec with 25 fps VGA image resolution, integrates H.264 BP, MPEG-4 SP and H.263 P3 video processing standard together. | 2.3.39/25 |
| WDOG | Watchdog Timer Module | Timer Peripheral | The WDOG module protects against system failures by providing a method for the system to recover from unexpected events or programming errors. | 2.3.37/24 |
| WEIM | Wireless External Interface Module | External Memory Interface | The Wireless External Module (WEIM) handles the interface to devices external to chip, including generation of chip selects, clock and control for external peripherals and memory. It provides asynchronous and synchronous access to devices with SRAM-like interface. | 2.3.38/25 |

2.3 Module Descriptions

This section provides a brief text description of all the modules included in the i.MX27/MX27L devices, arranged in alphabetical order.

2.3.1 1-Wire Module

The 1-Wire module provides bi-directional communication between the ARM926 core and the Add-Only Memory EPROM, DS2502. The 1-Kbit EPROM holds information about the battery and communicates with the ARM926 Platform using the IP interface. Through the 1-Wire interface, the ARM926 acts as the bus master while the DS2502 device is the slave. The 1-Wire peripheral does not trigger interrupts; hence it is necessary for the ARM926 to poll the 1-Wire to manage the module. The 1-Wire uses an external pin to connect to the DS2502. Timing requirements are met in hardware with the help of a 1 MHz clock. The clock divider generates a 1 MHz clock that is used as a time reference by the state machine. Timing requirements are crucial for proper operation, and the 1-Wire state machine and the internal clock provide the necessary signal. The clock must be configured to approximately 1 MHz. You can then set the 1-Wire register to send and receive bits over the 1-Wire bus.

2.3.2 AHB-Lite IP Interface Module (APII)

The APII acts as an interface between the Arm Advanced High-performance Bus Lite. (AHB-Lite) and lower bandwidth peripherals conforming to the IP bus specification Rev 2.0. There are two APII modules in i.MX27/MX27L processors.

The following list summarizes the key features of the APII:

- All peripheral read transactions require a minimum of two system clocks (R-AHB side) and all write transactions require a minimum of three system clocks (R-AHB side).
- The APII supports 8-bit, 16-bit, and 32-bit IP bus peripherals. Byte, half word, and full word reads and writes are supported.
- The APII supports multi-cycle accesses by providing 16-bit to 8-bit peripherals operations and 32-bit to both 16-bit and 8-bit peripherals operations.

- The APCI supports 31 external IP bus peripherals each with a 4-Kbyte memory map (a slot).

2.3.3 ARM926EJ-S Interrupt Controller (AIPC)

The ARM926EJ-S Interrupt Controller (AIPC) is a 32-bit peripheral that collects interrupt requests from up to 64 sources and provides an interface to the ARM926EJ-S core. The AIPC includes software controlled priority levels for normal interrupts.

The AIPC performs the following functions:

- Supports up to 64 interrupt sources
- Supports fast and normal interrupts
- Selects normal or fast interrupt request for any interrupt source
- Indicates pending interrupt sources via a register for normal and fast interrupts
- Indicates highest priority interrupt number via register. (Can be used as a table index.)
- Independently can enable or disable any interrupt source
- Provides a mechanism for software to schedule an interrupt
- Supports up to 16 software controlled priority levels for normal interrupts and priority masking
- Can single-bit disable all normal interrupts and all fast interrupts. (Used in enabling of secure operations.)

2.3.4 ARM926EJ-S Platform

The ARM926EJ-S (ARM926) is a member of the Arm9 family of general-purpose microprocessors targeted at multi-tasking applications. The ARM926 supports the 32-bit Arm and 16-bit Thumb instructions sets. The ARM926 includes features for efficient execution of Java byte codes. A JTAG port is provided to support the Arm Debug Architecture, along with associated signals to support the ETM9 real-time trace module. The ARM926EJ-S is a Harvard cached architecture including an ARM9EJ-S integer core, a Memory Management Unit (MMU), separate instruction and data AMBA AHB interfaces, separate instruction and data caches, and separate instruction and data tightly coupled memory (TCM) interfaces. The ARM926 co-processor, instruction TCM, and data TCM interfaces will be tied off within the ARM926 Platform and will not be available for external connection.

The ARM926EJ-S processor is a fully synthesizable macrocell, with a configurable memory system. Both instruction and data caches will be 16 kbytes on the platform. The cache is virtually accessed and virtually tagged. The data cache has physical tags as well. The MMU provides virtual memory facilities which are required to support various platform operating systems such as Symbian OS, Windows CE, and Linux. The MMU contains eight fully associative TLB entries for lockdown and 64 set associative entries. Refer to the *ARM926EJ-S Technical Reference Manual* for more information.

2.3.5 Advanced Technology Attachment (ATA)

The Advanced Technology Attachment (ATA) host controller complies with the ATA/ATAPI-6 specification. The primary use of the ATA host controller is to interface with IDE hard disc drives and Advanced Technology Attachment Packet Interface (ATAPI) optical disc drives. It interfaces with the ATA device over a number of ATA signals.

This host controller supports interface protocols as specified in ATA/ATAPI-6 standard, as follows:

- PIO mode 0, 1, 2, 3, and 4
- Multiword DMA mode 0, 1, and 2
- Ultra DMA modes 0, 1, 2, 3, and 4 with bus clock of 50 MHz or higher
- Ultra DMA mode 5 with bus clock of 80 MHz or higher

Before accessing the ATA bus, the host must program the timing parameters to be used on the ATA bus. The timing parameters control the timing on the ATA bus. Most timing parameters are programmable as a number of clock cycles (1 to 255). Some are implied. All of the ATA device-internal registers are visible to users, and they are defined as mirror registers in ATA host controller. As specified in ATA/ATAPI-6 standard, all the features/functions are implemented by reading/writing to the device's internal registers.

There are basically two protocols that can be active at the same time on the ATA bus, as follows:

- The first and simplest protocol (PIO mode access) can be started at any time by the ARM926 to the ATA bus. The PIO mode is a slow protocol, mainly intended to be used to program an ATA disc drive, but also can be used to transfer data to/from the disc drive.
- The second protocol is the DMA mode access. DMA mode is started by the ATA interface after receiving a DMA request from the drive, and only if the ATA interface has been programmed to accept the DMA request. In DMA mode, either multiword-DMA or ultra-DMA protocol is used on the ATA bus. All transfers between FIFO and the host IP or DMA IP bus are zero wait states transfer, so a high-speed transfer between FIFO and DMA/host bus is possible.

2.3.6 Digital Audio MUX (AUDMUX)

The Digital Audio MUX (AUDMUX) provides programmable interconnecting for voice, audio, and synchronous data routing between host serial interfaces—for example, SSI, SAP, and peripheral serial interfaces—such as, audio and voice codecs. The AUDMUX allows audio system connectivity to be modified through programming, as opposed to altering the design of the system into which the chip is designed. The design of the AUDMUX allows multiple simultaneous audio/voice/data flows between the ports in point-to-point or point-to-multipoint configurations.

Included in the AUDMUX are two types of interfaces. The internal ports connect to the processor serial interfaces, and the external ports connect to off-chip audio devices and serial interfaces of other processors. A desired connectivity is achieved by configuring the appropriate internal and external ports.

The module includes full 6-wire SSI interfaces for asynchronous receive and transmit, as well as a configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interface. The AUDMUX allows each host interface to be connected to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode).

2.3.7 Clock and Reset Module (CRM)

The Clock and Reset Module (CRM) generates clock and reset signals used throughout the i.MX27/MX27L processor and for external peripherals. It also enables system software to control, customize, or read the status of the following functions:

- Chip ID
- Multiplexing of I/O signals
- I/O Driving Strength
- I/O Pull Enable Control
- Well-Bias Control
- System boot mode selection
- DPTC Control

2.3.8 CMOS Sensor Interface (CSI)

The CMOS Sensor Interface (CSI) is a logic interface that enables the i.MX27/MX27L processors to connect directly to external CMOS sensors and CCIR656 video source.

The capabilities of the CSI include the following:

- Configurable interface logic to support popular CMOS sensors in the market
- Support traditional sensor timing interface
- Support CCIR656 video interface, progressive mode for smart sensor, interlace mode for PAL and NTSC input
- 8-bit input port for YCC, YUV, Bayer, or RGB data
- 32×32 FIFO storing image data supporting Core data read and DMA data burst transfer to system memory
- Full control of 8-bit and 16-bit data to 32-bit FIFO packing
- Direct interface to eMMA-It Pre-Processing block (PrP) - Not available on the i.MX27L
- Single interrupt source to interrupt controller from maskable sensor interrupt sources: Start of Frame, End of Frame, Change of Field, FIFO full
- Configurable master clock frequency output to sensor
- Asynchronous input logic design. Sensor master clock can be driven by either the i.MX27/MX27L processor or by external clock source.
- Statistic data generation for Auto Exposure (AE) and Auto White Balance (AWB) control of the camera (for Bayer data only)

2.3.9 Configurable Serial Peripheral Interface (CSPI)

The Configurable Serial Peripheral Interface (CSPI) is used for fast data communication with fewer software interrupts. There are three CSPI modules in the i.MX27/MX27L processors, which provide a full-duplex synchronous serial interface, capable of interfacing to the SPI master and slave devices. CSPI1 and CSPI2 are master/slave configurable and include three chip selects to support multiple peripherals. CSPI3 is only a master and has one chip-select signal. The transfer continuation function of the CSPI

enables unlimited length data transfers using 32-bit wide by 8-entry FIFO for both TX and RX data DMA support.

The CSPI Ready (SPI_RDY) and Chip Select (SS) control signals enable fast data communication with fewer software interrupts. When the CSPI module is configured as a master, it uses a serial link to transfer data between the CSPI and an external device. A chip-enable signal and a clock signal are used to transfer data between these two devices. When the CSPI module is configured as a slave, the user can configure the CSPI Control register to match the external SPI master's timing.

2.3.10 Direct Memory Access Controller (DMAC)

The Direct Memory Access Controller (DMAC) provides 16 channels to support linear memory, 2D memory, FIFO, and end-of-burst enable FIFO transfers to support a wide variety of DMA operations. Features include the following:

- Support of 16 channels linear memory, 2D memory, and FIFO for both source and destination
- Support of 8-bit, 16-bit, or 32-bit FIFO port size and memory port size data transfer
- Configurability of DMA burst length of up to a maximum of 16 words, 32 half-words, or 64 bytes for each channel
- Bus utilization control for a channel that is not triggered by DMA request
- Interrupts that are provided to interrupt handler on bulk data transfer complete or transfer error
- DMA burst time-out error to terminate DMA cycle when the burst cannot be completed in a programmed timing period
- Dedicated external DMA request and grant signal
- Support of increment, decrement, and no increment for source and destination addressing
- Support of DMA chaining

2.3.11 *enhanced* MultiMedia Accelerator Light (eMMA_Lt)

The *enhanced* MultiMedia Accelerator Light (eMMA_Lt) consists of the video pre-processor (PrP) and post-processor (PP). In contrast with i.MX21 processor's components, this eMMA does not include the video codec. A more powerful video codec is included as a separate module.

NOTE

The i.MX27L does not have a eMMA_Lt module.

Each module has individual control and configuration registers that are accessed via the IP interface, and are capable of bus mastering the AMBA bus to independently access system memory without any CPU intervention. This enables each module to be used independently of each other, and enables the pre-processor and post-processor modules to provide acceleration features for other software codec implementations and image processing software. These blocks work together to provide video acceleration, and to off-load the CPU from computation intensive tasks. The PrP and PP can be used for generic video pre- and post-processing, such as scaling, resizing, and color space conversions. A 32-bit-to-64-bit AHB gasket is used to convert a PrP AHB bus from a 32-bit to 64-bit protocol. A bypass function is implemented to bypass this 64-bit gasket if it is not needed.

eMMA_It supports the following image/video processing features:

- Pre-processor:
 - Data input:
 - System memory
 - Private DMA between CMOS Sensor Interface module and pre-processor
 - Data input formats:
 - Arbitrarily formatted RGB pixels (16 or 32 bits)
 - YUV 4:2:2 (Pixel interleaved)
 - YUV 4:2:0 (IYUV, YV12)
 - Input image size: 32×32 to 2044×2044
 - Image scaling:
 - Programmable independent CH-1 and CH-2 resizer. Can program to be in cascade or parallel.
 - Each resizer supports downscaling ratios from 1:1 to 8:1 in fractional steps.
 - Channel-1 output data format
 - Channel 1
 - RGB 16 and 32 bpp
 - YUV 4:2:2 (YUYV, YVYU, UYVY, VYUY)
 - Channel-2 output data format
 - YUV 4:2:2 (YUYV)
 - YUV 4:4:4
 - YUV 4:2:0 (IYUV, YV12)
 - RGB data and YUV data format can be generated concurrently
 - 32/64-bit AHB bus
- Post-processor
 - Input data:
 - From system memory
 - Input format:
 - YUV 4:2:0 (IYUV, YV12)
 - Image Size: 32×32 to 2044×2044
 - Output format:
 - YUV 4:2:2 (YUYV)
 - RGB16 and RGB32 bpp
 - Image Resize
 - Upscaling ratios ranging from 1:1 to 1:4 in fractional steps
 - Downscaling ratios ranging from 1:1 to 2:1 in fractional steps and a fixed 4:1
 - Ratios provide scaling between QCIF, CIF, QVGA (320×240 , 240×320)

2.3.12 Enhanced Synchronous Dynamic RAM Controller (ESDRAMC)

The Enhanced Synchronous Dynamic RAM Controller (ESDRAMC) provides an interface and control for synchronous DRAM memories for the system. SDRAM memories use a synchronous interface with all signals registered on a clock edge. A command protocol is used for initialization, read, write, and refresh operations to the SDRAM, and is generated on the signals by the controller (when required due to external or internal requests). It has support for both single data rate RAMs and double data rate SDRAMs. It supports 64 Mbits, 128 Mbits, 256 Mbits, and 512 Mbits, 1 Gbit, 2 Gbits, four bank synchronous DRAM by two independent chip selects and with up to 256 Mbytes addressable memory per chip select.

2.3.13 Fast Ethernet Controller (FEC)

The Fast Ethernet Controller (FEC) is designed to support both 10 and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII and the 10 Mbps-only 7-wire interface, which uses a subset of the MII pins for connection to an external Ethernet transceiver.

The FEC incorporates the following features:

- Support for three different Ethernet physical interfaces:
 - 100-Mbps IEEE 802.3 MII
 - 10-Mbps IEEE 802.3 MII
 - 10-Mbps 7-wire interface (industry standard)
- IEEE 802.3 full duplex flow control
- Programmable max frame length supports IEEE Std 802.1™ VLAN tags and priority
- Support for full-duplex operation (200 Mbps throughput) with a minimum system clock rate of 50 MHz
- Support for half-duplex operation (100 Mbps throughput) with a minimum system clock rate of 25 MHz
- Retransmission from transmit FIFO following a collision (no processor bus utilization)
- Automatic internal flushing of the receive FIFO for runts (collision fragments) and address recognition rejects (no processor bus utilization)
- Address recognition
 - Frames with broadcast address may be always accepted or always rejected
 - Exact match for single 48-bit individual (unicast) address
 - Hash (64-bit hash) check of individual (unicast) addresses
 - Hash (64-bit hash) check of group (multicast) addresses
 - Promiscuous mode
- Independent DMA engine with multiple channels allowing transmit data, transmit descriptor, receive data, and receive descriptor accesses to provide high performance
- Independent RISC-based controller that provides the following functions in the FEC:
 - Initialization (those internal registers not initialized by the user or hardware)

- High level control of the DMA channels (initiating DMA transfers)
- Interpreting buffer descriptors
- Address recognition for receive frames
- Random number generation for transmit collision backoff timer
- The Message Information Block (MIB) in FEC maintains counters for a variety of network events and statistics. The counters supported are the RMON (RFC 1757) Ethernet Statistics group and some of the IEEE 802.3 counters.

2.3.14 General Purpose I/O Module (GPIO)

The general-purpose input/output (GPIO) module provides dedicated general-purpose pins that can be configured as either inputs or outputs. When it is configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register. The GPIO includes all of the general purpose input/output logic necessary to drive a specific data to the pad and control the direction of the pad using registers in the GPIO module. The ARM926 is able to sample the status of the corresponding pads by reading the appropriate status register. The GPIO supports up to 32 interrupts and has the ability to identify interrupt edges as well as generate three active high interrupts.

2.3.15 General Purpose Timer (GPT)

The i.MX27/MX27L processors contains six identical 32-bit General Purpose Timers (GPT) with programmable prescalers and compare and capture registers. Each timer's counter value can be captured using an external event, and can be configured to trigger a capture event on the rising or/and falling edges of an input pulse. Each GPT can also generate an event on the TOUT pin, and an interrupt when the timer reaches a programmed value. Each GPT has an 11-bit prescaler that provides a programmable clock frequency derived from multiple clock sources, including ipg_clk_32k, ipg_clk_perclk, ipg_clk_perclk/4, and external clock from the TIN pin. The counter has two operation modes: free-run and restart mode. The GPT can work in low-power mode.

2.3.16 Inter IC Communication (I²C)

Inter IC Communication (I²C) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I²C enables additional devices to be connected to the bus for expansion and system development.

The I²C operates up to 400 kbps dependent on pad loading and timing. (For pad requirement details, refer to Phillips I²C Bus Specification, Version 2.1.) The I²C system is a true multiple-master bus, including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.

2.3.17 IC Identification Module (IIM)

The IC Identification Module (IIM) provides an interface for reading and in some cases programming and/or overriding identification and control information stored in on-chip fuse elements. The module supports laser fuses (L-Fuses) or electrically-programmable poly fuses (e-Fuses) or both.

Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, SAHARA2.

2.3.18 JTAG Controller (JTAGC)

The JTAG Controller (JTAGC) module supports debug access to the ARM926 Platform and tristate enable of the I/O pads. The overall strategy is to achieve good test and debug features without increasing the pin count and reducing the complexity of I/O muxing. The JTAG Controller is compatible with IEEE Std 1149.1™ Standard Test Access Port and Boundary Scan Architecture.

2.3.19 Keypad Port (KPP)

The Keypad Port (KPP) is designed to interface with a keypad matrix with 2-contact or 3-point contact keys. KPP is designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the KPP is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously in the keypad. The KPP supports up to 8 × 8 external key pad matrix. Its port pins can be used as general purpose I/O. Using an open drain design, the KPP includes glitch suppression circuit design, multiple keys, long key, and standby key detection.

2.3.20 Liquid Crystal Display Controller (LCDC)

The Liquid Crystal Display Controller (LCDC) provides display data for external gray-scale or color LCD panels. The LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.

The LCDC provides the following features:

- Configurable AHB bus width (32-bit/64-bit)

- Support for single (non-split) screen monochrome or color LCD panels and self-refresh type LCD panels
- 16 simultaneous gray-scale levels from a palette of 16 for monochrome display
- Support for:
 - Maximum resolution of 800×600
 - Passive color panel:
 - 4 (mapped to RGB444)/8 (mapped to RGB444)/12 (RGB444) bits per pixel (bpp)
 - TFT panel:
 - 4 (mapped to RGB666)/8 (mapped to RGB666)/12 (RGB444)/16 (RGB565)/18 (RGB666) bpp
 - 16 and 256 colors out of a palette of 4096 colors for 4 bpp and 8 bpp CSTN display, respectively
 - 16 and 256 colors out of a palette of 256 colors for 4 bpp and 8 bpp TFT display, respectively
 - True 4096 colors for a 12 bpp display
 - True 64-Kbyte colors for 16 bpp
 - True 256-Kbyte colors for 18 bpp
 - 16-bit AUO TFT LCD Panel
 - 24-bit AUO TFT LCD Panel

2.3.21 Multi-Master Memory Interface (M3IF)/M3IF-ESDCTL/MDDRC Interface

The M3IF-ESDCTL/MDDRC interface is optimized and designed to reduce access latency by generating multiple accesses through the dedicated ESDCTL/MDDRC arbitration (MAB) module, which controls the access to and from the Enhanced SDRAM/MDDR memory controller. For the other port interfaces, the M3IF only arbitrates and forwards the master requests received through the Master Port Gasket (MPG) interface and M3IF Arbitration (M3A) module toward the respective memory controller. The masters that interface with the M3IF include the Arm Platform, FEC, LCDC, H.264, and the USB. The controllers are the ESDCTL/MDDRC, PCMCIA, NFC, and WEIM.

2.3.22 Multi-Layer AHB Crossbar Switch (MAX)

The ARM926EJ-S processor's instruction and data buses—and all alternate bus master interfaces—arbitrate for resources via a 6×34 Multi-Layer AHB Crossbar Switch (MAX). There are six (M0–M5) fully functional master ports and three (S0–S2) fully functional slave ports. The MAX is uni-directional. All master and slave ports are AHB-Lite compliant.

The design of the crossbar switch enables concurrent transactions to proceed from any master port to any slave port. That is, it is possible for all three slave ports to be active at the same time as a result of three independent master requests. If a particular slave port is simultaneously requested by more than one master port, arbitration logic exists inside the crossbar to allow the higher priority master port to be granted the bus, while stalling the other requestor(s) until that transaction has completed. The slave port arbitration

schemes supported are fixed, programmable fixed, programmable default input port parking, and a round robin arbitration scheme.

The Crossbar Switch also monitors the `ccm_br` input (clock control module bus request), which requests a bus grant from all four slave ports. The priority of `ccm_br` is programmable and defaults to the highest priority. Upon receiving bus grants for all four output ports, the `ccm_bg` output will assert. At this point, the clock control and reset module (CRM) can turn off `hclk` and be assured there are no outstanding AHB transactions in progress. Once the CRM is granted a port, no other master will receive a grant on that port until the CRM bus request (`ccm_br`) negates.

2.3.23 Memory Stick Host Controller (MSHC)

The Memory Stick Host Controller (MSHC) is located between the AIPI and the Sony Memory Stick and provides support for data transfers between the i.MX27 processor and the Memory Stick (MS). The MSHC consists of two sub-modules; the MSHC gasket and the Sony Memory Stick Host Controller (SMSC). The SMSC module, which is the actual memory stick host controller, is compatible with Sony Memory Stick Ver 1.x and Memory Stick PRO. The gasket connects the AIPI IP bus to the SMSC interface to allow communication and data transfers via the IP Bus.

NOTE

The i.MX27L does not include the MSHC feature.

The MSHC gasket uses a reduced IP Bus interface that supports the IP bus read/write transfers that include a back-to-back read or write. DMA transfers also take place via the IP Bus interface.

A transfer can be initiated by the DMA or the host (through the AIPI) response to an MSHC DMA request or interrupt. The SMSC has two DMA address modes—a single address mode and a dual address mode.

The MSHC is set to dual-address mode for transfers with the DMA. In dual-address mode, when the MSHC requests a transfer with the DMA request (XDRQ), the DMA will initiate a transfer to the MSHC.

NOTE

Details regarding the operation of the MSHC module can be found separately in *Memory Stick/Memory Stick PRO Host Controller IP Specification 1.3*.

2.3.24 NAND Flash Controller (NFC)

NAND Flash Controller (NFC) interfaces standard NAND Flash devices to the i.MX27/MX27L processors and hides the complexities of accessing the NAND Flash. It provides a glueless interface to both 8-bit and 16-bit NAND Flash parts with page sizes of 512 Bytes or 2 Kbytes. Its addressing scheme enables it to access flash devices of almost limitless capacity. The 2-Kbyte RAM buffer of the NAND Flash is used as the boot RAM during a cold reset (if the i.MX27/MX27L device is configured for a boot to be carried out from the NAND Flash device). After the boot procedure completes, the RAM is available as buffer RAM. In addition, the NAND Flash controller provides an X16-bit and X32-bit interface to the AHB bus on the chip side, and an X8/X16 interface to the NAND Flash device on the external side.

2.3.25 Personal Computer Memory Card International Association (PCMCIA)

The Personal Computer Memory Card International Association (PCMCIA) provides the PCMCIA 2.1 standard, which defines the usage of memory and I/O devices as insertable and exchangeable peripherals for personal computers or PDAs. Examples of these types of devices include CompactFlash and WLAN adapters.

The `pcmcia_if` host adapter module provides the control logic for PCMCIA socket interfaces, and requires some additional external analog power switching logic and buffering. The additional external buffers allow the `pcmcia_if` host adapter module to support one PCMCIA socket. The `pcmcia_if` shares its chip level I/O with the external interface to memory (EIM) pins. Additional logic is required to multiplex the EIM and the `pcmcia_if` on the same pins.

2.3.26 Digital Phase Lock Loop (DPLL)

Two on-chip Digital Phase Lock Loop (DPLLs) provide clock generation in digital and mixed analog/digital chips designed for wireless communication and other applications. The DPLLs produce a high-frequency chip clock signals with a low frequency and phase jitter.

2.3.27 Pulse-Width Modulator (PWM)

The Pulse-Width Modulator (PWM) has a 16-bit counter and is optimized to generate sounds from stored sample audio images; it can also generate tones. The PWM uses 16-bit resolution and a 4×16 data FIFO to generate sound. The 16-bit up-counter has a source selectable clock with 4×16 FIFO to minimize interrupt overhead. Clock-in frequency is controlled by a 12-bit prescaler for the division of a clock. Capable of sound and melody generation, the PWM has an active-high or active-low configurable output, and can be programmed to be active in low-power and debug modes. The PWM can be programmed to generate interrupts at compare and rollover events.

2.3.28 Real Time Clock (RTC)

The Real Time Clock (RTC) module maintains the system clock, provides stopwatch, alarm, and interrupt functions, and supports the following features:

- Full clock—days, hours, minutes, seconds
- Minute countdown timer with interrupt
- Programmable daily alarm with interrupt
- Sampling timer with interrupt
- Once-per-day, once-per-hour, once-per-minute, and once-per-second interrupts
- Operation at 32.768 kHz or 32 kHz, or 38.4 kHz (determined by reference clock crystal)

The prescaler converts the incoming crystal reference clock to a 1 Hz signal, which is used to increment the seconds, minutes, hours, and days TOD counters. The alarm functions, when enabled, generate RTC interrupts when the TOD settings reach programmed values. The sampling timer generates fixed-frequency interrupts, and the minute stopwatch allows for efficient interrupts on very small boundaries.

2.3.29 Run-Time Integrity Checker (RTIC)

The Run-Time Integrity Checker (RTIC) is one of the security components in the i.MX27/MX27L processors. Its purpose is to ensure the integrity of the peripheral memory contents and assist with boot authentication. The RTIC has the ability to verify the memory contents during system boot and during run-time execution. If the memory contents at runtime fail to match the hash signature, an error in the security monitor is triggered.

Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, SAHARA2.

2.3.30 Symmetric/Asymmetric Hashing and Random Accelerator (SAHARA2)

SAHARA2 is a security co-processor, it implements encryption algorithms (AES, DES, and 3DES), hashing algorithms (MD5, SHA-1, SHA_224, and SHA-256), stream cipher algorithm (ARC4), and a hardware random number generator.

Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, SAHARA2.

2.3.31 Security Controller Module (SCC)

The Security Controller Module (SCC) is a hardware security component. Overall, its primary functionality is associated with establishing a centralized security state controller and hardware security state with a hardware configured, unalterable security policy.

Contact your NXP Semiconductor sales office or distributor for additional information on SCC, RTIC, IIM, and SAHARA2.

2.3.32 Secure Digital Host Controller (SDHC)

The Secure Digital Host Controller (SDHC) controls the MultiMedia Card (MMC), Secure Digital (SD) memory, and I/O cards by sending commands to cards and performing data accesses to/from the cards. The Multimedia Card/Secure Digital Host (MMC/SD) module integrates both MMC support along with SD memory and I/O functions. The SDHC is fully compatible with the MMC System Specification Version 3.0, as well as with the SD Memory Card Specification 1.0, and SD I/O Specification 1.0 with 1/4 channel(s). The maximum data rate in 4-bit mode is 100 Mbps. The SDHC uses a built-in programmable frequency counter for the SDHC bus, and provides a maskable hardware interrupt for an SDIO interrupt, internal status, and FIFO status. It has a pair of 32×16 -bit data FIFO buffers built in.

The MultiMedia Card (MMC) is a universal, low-cost data storage and communication media that is designed to cover a wide area of applications, including, for example, electronic toys, organizers, PDAs, and smart phones. The MMC communication is based on an advanced 7-pin serial bus designed to operate in a low-voltage range.

The Secure Digital Card (SD) is an evolution of MMC technology, with two additional pins in the form factor. It is specifically designed to meet the security, capacity, performance, and environment requirements inherent in newly emerging audio and video consumer electronic devices. The physical form

factor, pin assignment, and data transfer protocol are forward-compatible with the MultiMedia Card with some additions. Under SD, it can be categorized into Memory and I/O. The memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard, which is faster and provides the capability for a higher memory capacity. The I/O card provides high-speed data I/O with low-power consumption for mobile electronic devices.

2.3.33 Smart Liquid Crystal Display Controller Module (SLCDC)

The Smart Liquid Crystal Display Controller (SLCDC) module transfers data from the display memory buffer to the external display device. Direct Memory Access (DMA) transfers the data transparently with minimal software intervention. Bus utilization of the DMA is controllable and deterministic.

As cellular phone displays become larger and more colorful, demands on the processor increase. More CPU power is needed to render and manage the image. The role of the display controller is to reduce the CPU's involvement in the transfer of data from memory to the display device so the CPU can concentrate on image rendering. DMA is used to optimize the transfer. Embedded control information needed by the display device is automatically read from a second buffer in system memory and inserted into the data stream at the proper time to completely eliminate the CPU's role in the transfer.

A typical scenario for a cellular phone display is to have the display image rendered in main system memory. After the image is complete, the CPU triggers the SLCDC module to transfer the image to the display device. Image transfer is accomplished by burst DMA, which steals bus cycles from the CPU. Cycle-stealing behavior is programmable so bus use is kept within predefined bounds. After the transfer is complete, a maskable interrupt is generated indicating the status. For animated displays, it is suggested that a two-buffer ping-pong scheme be implemented so that the DMA is fetching data from one buffer while the next image is rendered into the other.

Several display sizes and types are used in the various products that use the SLCDC. The SLCDC module has the capability of directly interfacing to the selected display devices. Both serial and parallel interfaces are supported. The SLCDC module only supports writes to the display controller. SLCDC read operations from the display controller are not supported.

2.3.34 Synchronous Serial Interface (SSI)

The Synchronous Serial Interface (SSI) is a full-duplex serial port that allows the chip to communicate with a variety of serial devices. These serial devices can be standard codecs, Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.

The SSI is typically used to transfer samples in a periodic manner. The SSI consists of independent transmitter and receiver sections with independent clock generation and frame synchronization.

The SSI contains independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode. The SSI can work in Normal mode operation using frame sync, and in Network mode operation allowing multiple devices to share the port with as many as thirty-two time slots.

The SSI provides two sets of Transmit and Receive FIFOs. Each of the four FIFOs is 8×24 bits. The two sets of Tx/RX FIFOs can be used in Network mode to provide two independent channels for transmission

and reception. It also has programmable data interface modes such as I2S, LSB, and MSB aligned and programmable word lengths. Other program options include frame sync, clock generation, and programmable I2S modes (Master, Slave, or Normal). Oversampling clock, `ccm_ssi_clk` is available as output from SRCK in I2S Master mode.

In addition to AC97 support, the SSI has completely separate clock and frame sync selections for the receive and transmit sections. In the AC97 standard, the clock is taken from an external source and frame sync is generated internally. The SSI also has a programmable internal clock divider and Time Slot Mask registers for reduced CPU overhead (for Tx and RX both).

2.3.35 Universal Asynchronous Receiver/Transmitter (UART)

The i.MX27/MX27L processors contain six UART modules. Each UART module is capable of standard RS-232 non-return-to-zero (NRZ) encoding format and IrDA-compatible infrared modes. The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception); or it transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low-speed IrDA compatibility.

The UART transmits and receives characters that are either 7 or 8 bits in length (program selectable). To transmit, data is written from the peripheral data bus to a 32-byte transmitter FIFO (TxFIFO). This data is passed to the shift register and shifted serially out on the transmitter pin (TXD). To receive, data is received serially from the receiver pin (RXD) and stored in a 32-half-word-deep receiver FIFO (RxFIFO). The received data is retrieved from the RxFIFO on the peripheral data bus. The RxFIFO and TxFIFO generate maskable interrupts as well as DMA requests when the data level in each of the FIFO reaches a programmed threshold level.

The UART generates baud rates based on a programmable divisor and input clock. The UART also contains programmable auto baud detection circuitry to receive 1 or 2 stop bits as well as odd, even, or no parity. The receiver detects framing errors, idle conditions, BREAK characters, parity errors, and overrun errors.

2.3.36 Universal Serial Bus (USB)

The i.MX27/MX27L processors provide three USB ports. The USB module provides high performance USB On-The-Go (OTG) functionality, compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module consists of three independent USB cores, each controlling one USB port.

In addition to the USB cores, the USB module provides for Transceiverless Link (TLL) operation on host Ports 1 and 2, and provides the ability of routing the OTG transceiver interface to Host Port 1 such that this transceiver can be used to communicate with a USB peripheral connected to Host Port 1. The USB module has two connections to the CPU bus—one IP-bus connection for register accesses and one AHB-bus connection for the DMA transfer of data to and from the FIFOs.

The USB module includes the following features:

- Full Speed/Low speed Host only core (HOST 1)
- Transceiverless Link Logic (TLL) for on board connection to a FS/LS USB peripheral

Functional Description and Application Information

- Bypass mode to route Host Port 1 signals to OTG I/O port
- High Speed /Full Speed/Low Speed Host Only core (Host 2)
- Full Speed/Low Speed interface for Serial transceiver
- TLL function for direct connection to USB peripheral in FS/LS (serial) operation
- High-speed OTG core

The USB module has two main modes of operation: Normal mode and Bypass mode. Furthermore, the USB interfaces can be configured for high-speed operation (480 Mbps) and/or full/low speed operation (12/1.5 Mbps). In Normal mode, each USB core controls its corresponding port. In addition to the major operational modes, each port can work in one or more modes, as follows:

PHY mode In PHY mode, an external serial transceiver is connected to the port. This is used for off-board USB connections.

TLL mode In TLL mode, internal logic is enabled to emulate the functionality of two back-to-back connected transceivers. This mode is typically used for on-board USB connections to USB-capable peripherals.

Host Port 2 supports ULPI and Serial Transceivers. The OTG port requires a transceiver and is intended for off-board USB connections.

Serial Interface mode In serial mode, a serial OTG transceiver must be connected. The port does not support dedicated signals for OTG signaling. Instead, a transceiver with built-in OTG registers must be used. Typically, the transceiver registers are accessible over an I²C or SPI interface.

ULPI mode In this mode, a ULPI transceiver is connected to the port pins to support high-speed off board USB connection.

Bypass mode Bypass mode affects the operation of the OTG port and Host Port 1. This mode is only available when a serial transceiver is used on the OTG port, and the peripheral device on Port 1 is using a TLL connection. Bypass mode is activated by setting the bypass bit in the USBCONTROL register. In this mode, the USB OTG port connections are internally routed to the USB Host 1 port, such that the transceiver on the OTG port connects to a peripheral USB device on Host Port 1. The OTG core and the Host 1 core are disconnected from their ports when bypass is active.

Low Power mode Each of the three USB cores has an associated power control module that is controlled by the USB core and clocked on a 32-kHz clock. When a USB bus is idle, the transceiver can be placed in low-power mode (suspend), after which the clocks to the USB core can be stopped. The 32-kHz low power clock must remain active as it is needed for walk-up detection.

2.3.37 Watchdog Timer Module (WDOG)

The Watchdog Timer module (WDOG) protects against system failures by providing a method of escaping from unexpected events or programming errors. Once the WDOG module is activated, it must be serviced by software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the WDOG Timer module either asserts the `wdog` signal or a system reset signal `wdog_rst`, depending on software configuration. The WDOG Timer module also generates a system reset via a software write to

the Watchdog Control Register (WCR) when there is a detection of a clock monitor event, an external reset, an external JTAG reset signal, or if a power-on-reset has occurred.

2.3.38 Wireless External Interface Module (WEIM)

The Wireless External Interface Module (WEIM) handles the interface to devices external to the chip, including generation of chip selects, clocks and controls for external peripherals and memory. It provides asynchronous and synchronous access to devices with an SRAM-like interface.

The WEIM includes six chip selects for external devices, with two CS signals covering a range of 128 Mbytes, and the other four each covering a range of 32 Mbytes. The 128-Mbyte range can be increased to 256 Mbytes when combined with the two signals. The WEIM offers selectable protection for each chip select as well as programmable data port size. There is a programmable wait-state generator for each chip select and support for Big Endian and Little Endian modes of operation per access.

2.3.39 Video Codec

The Video Codec module is the video processing module in the i.MX27 processor. It supports full duplex video codec with 25 fps VGA resolution, supports multi-party calls, and integrates multiple video processing standards, including H.264 BP, MPEG-4 SP, and H.263 P3 (including annex I, J, K, and T), D1 resolution, 30 fps—half-duplex.

NOTE

The Video Codec feature is not available on the i.MX27L.

It has three 64-bit AHB-Lite master bus interfaces connecting to the EMI, which includes two read channels and one write channel. Its 32-bit AHB-Lite master bus is connected to Arm Platform to access system-internal SRAM.

The Video Codec module contains three major architectural components: video codec processing IP, AXI-to-AHB bus protocol transfer module, and a 32-bit to 64-bit AHB master bus protocol transfer module.

The Video Codec module supports following video stream processing features:

- Multi-standard video codec
 - MPEG-4 part-II simple profile encoding/decoding
 - H.264/AVC baseline profile encoding/decoding
 - H.263 P3 encoding/decoding
 - Multi-party call: max processing four image/bitstream encoding and/or decoding simultaneously
 - Multi-format: for example, encodes MPEG-4 bitstream, and decodes H.264 bitstream simultaneously
- Coding tools
 - High-performance motion estimation
 - Single reference frame for both MPEG-4 and H.264 encoding
 - Support 16 reference frame for H.264 decoding

Signal Descriptions

- Quarter-pel and half-pel accuracy motion estimation
- $[\pm 16, \pm 16]$ Search range
- Unrestricted motion vector
- All variable block sizes are supported (in case of encoding, 8×4 , 4×8 , and 4×4 block sizes are not supported).
- MPEG-4 AC/DC prediction and H.264 Intra prediction
- H.263 Annex I, J, K(RS = 0 and ASO =0), and T are supported. In case of encoding, the Annex I and K(RS=1 or ASO=1) are not supported.
- CIR (Cyclic Intra Refresh)/AIR (Adaptive Intra Refresh)
- Error resilience tools
 - MPEG-4 re-synchronize marker and data-partitioning with RVLC (fixed number of bits/macroblocks between macroblocks)
 - H.264/AVC FMO and ASO
 - H.263 slice structured mode
- Bit-rate control (CBR and VBR)
- Pre/post rotation/mirroring
 - 8 rotation/mirroring modes for image to be encoded
 - 8 rotation/mirroring modes for image to be displayed
- Programmability
 - Embeds 16-bit DSP processor that is dedicated to processing bitstream and driving codec hardware
 - General purpose registers and interrupt generation for communication between system and video codec module

3 Signal Descriptions

This section discusses the following:

- Identifies and defines all device signals in text, tables, and (as appropriate) figures. Signals can be organized by group, as applicable.
- Contains pin-assignment/contact-connection diagrams, if the sequence of information in the data sheet requires them to be included here.

Table 3 shows the i.MX27/MX27L signal descriptions.

Table 3. i.MX27/MX27L Signal Descriptions

| Pad Name | Function/Notes |
|---------------------------------------|--|
| External Bus/Chip Select (EMI) | |
| A [13:0] | Address bus signals, shared with SDRAM/MDDR, WEIM and PCMCIA, A[10] for SDRAM/MDDR is not the address but the pre-charge bank select signal. |
| MA10 | Address bus signals for SDRAM/MDDR |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|-----------------------|---|
| A [25:14] | Address bus signals, shared with WEIM and PCMCIA |
| SDBA[1:0] | SDRAM/MDDR bank address signals |
| SD[31:0] | Data bus signals for SDRAM, MDDR |
| SDQS[3:0] | MDDR data sample strobe signals |
| DQM0–DQM3 | SDRAM data mask strobe signals |
| EB0 | Active low external enable byte signal that controls D [15:8], shared with PCMCIA $\overline{PC_REG}$. |
| EB1 | Active low external enable byte signal that controls D [7:0], shared with PCMCIA $\overline{PC_IORD}$. |
| \overline{OE} | Memory Output Enable—Active low output enables external data bus, shared with PCMCIA $\overline{PC_IOWR}$. |
| \overline{CS} [5:0] | Chip Select—The chip select signals \overline{CS} [3:2] are multiplexed with \overline{CSD} [1:0] and are selected by the Function Multiplexing Control Register (FMCR) in the System Control chapter. By default \overline{CSD} [1:0] is selected. \overline{DTACK} is multiplexed with $\overline{CS4}$. \overline{CS} [5:4] are multiplexed with ETMTRACECLK and ETMTRACESYNC; PF22, 21. |
| ECB | Active low input signal sent by flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence. |
| LBA | Active low signal sent by flash device causing external burst device to latch the starting burst address. |
| BCLK | Clock signal sent to external synchronous memories (such as burst flash) during burst mode. |
| \overline{RW} | \overline{RW} signal—Indicates whether external access is a read (high) or write (low) cycle. This signal is also shared with the PCMCIA $\overline{PC_WE}$. |
| RAS | SDRAM/MDDR Row Address Select signal |
| CAS | SDRAM/MDDR Column Address Select signal |
| SDWE | SDRAM Write Enable signal |
| SDCKE0 | SDRAM Clock Enable 0 |
| SDCKE1 | SDRAM Clock Enable 1 |
| SDCLK | SDRAM Clock |
| SDCLK_B | SDRAM Clock_B |
| NFWE_B | NFC Write enable signal, multiplexed with ETMPIPESTAT2; PF6 |
| NFRE_B | NFC Read enable signal, multiplexed with ETMPIPESTAT1; PF5 |
| NFALE | NFC Address latch signal, multiplexed with ETMPIPESTAT0; PF4 |
| NFCLE | NFC Command latch signal, multiplexed with ETMTRACEPKT0; PF1 |
| NFWP_B | NFC Write Permit signal, multiplexed with ETMTRACEPKT1; PF2 |
| NFCE_B | NFC Chip enable signal, multiplexed with ETMTRACEPKT2; PF3 |
| NFRB | NFC read Busy signal, multiplexed with ETMTRACEPKT3; PF0 |
| D[15:0] | Data Bus signal, shared with EMI, PCMCIA, and NFC |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|--------------------------|--|
| PC_CD1_B | PCMCIA card detect signal, multiplexed with ATA ATA_DIOR signal; PF20 |
| PC_CD2_B | PCMCIA card detect signal, multiplexed with ATA ATA_DIOW signal; PF19 |
| PC_WAIT_B | PCMCIA WAIT signal, multiplexed with ATA ATA_CS1 signal; PF18 |
| PC_READY | PCMCIA READY/IRQ signal, multiplexed with ATA ATA_CS0 signal; PF17 |
| PC_PWRON | PCMCIA signal, multiplexed with ATA ATA_DA2 signal; PF16 |
| PC_VS1 | PCMCIA voltage sense signal, multiplexed with ATA ATA_DA1 signal; PF14 |
| PC_VS2 | PCMCIA voltage sense signal, multiplexed with ATA ATA_DAO signal; PF13 |
| PC_BVD1 | PCMCIA Battery voltage detect signal, multiplexed with ATA ATA_DMARQ signal; PF12 |
| PC_BVD2 | PCMCIA Battery voltage detect signal, multiplexed with ATA ATA_DMACK signal; PF11 |
| PC_RST | PCMCIA card reset signal, multiplexed with ATA ATA_RESET_B signal; PF10 |
| IOIS16 | PCMCIA mode signal, multiplexed with ATA ATA_INTRQ signal; PF9 |
| PC_RW_B | PCMCIA read write signal, multiplexed with ATA ATA_IORDY signal; PF8 |
| PC_POE | PCMCIA output enable signal, multiplexed with ATA ATA_BUFFER_EN signal; PF7 |
| Clocks and Resets | |
| CLKO | Clock Out signal selected from internal clock signals. Refer to the clock controller for internal clock selection; PF15. |
| EXT_60M | This is a special factory test signal. To ensure proper operation, connect this signal to ground. |
| EXT_266M | This is a special factory test signal. To ensure proper operation, connect this signal to ground. |
| OSC26M_TEST | This is a special factory test signal. To ensure proper operation, leave this signal as a no connect. |
| RESET_IN | Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset. |
| RESET_OUT | Reset_Out—Output from the internal Hreset_b; and the Hreset can be caused by all reset source: power on reset, system reset (RESET_IN), and watchdog reset. |
| POR | Power On Reset—Active low Schmitt trigger input signal. The $\overline{\text{POR}}$ signal is normally generated by an external RC circuit designed to detect a power-up event. |
| XTAL26M | Oscillator output to external crystal |
| EXTAL26M | Crystal input (26 MHz), or a 16 MHz to 32 MHz oscillator (or square-wave) input when internal oscillator circuit is shut down. |
| CLKMODE[1:0] | These are special factory test signals. To ensure proper operation, do not connect to these signals. |
| EXTAL32K | 32 kHz crystal input (Note: in the RTC power domain) |
| XTAL32K | Oscillator output to 32 kHz crystal (Note: in the RTC power domain) |
| Power_cut | (Note: in the RTC power domain) |
| Power_on_reset | (Note: in the RTC power domain) |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|--|--|
| osc32k_bypass | The signal for osc32k input bypass (Note: in the RTC power domain) |
| Bootstrap | |
| BOOT [3:0] | System Boot Mode Select—The operational system boot mode of the i.MX27/MX27L processor upon system reset is determined by the settings of these pins. BOOT[1:0] are also used as handshake signals to PMIC(VSTBY). |
| JTAG | |
| JTAG_CTRL | JTAG Controller select signal—JTAG_CTRL is sampled during rising edge of TRST. Must be pulled to logic high for proper JTAG interface to debugger. Pulling JTAG_CTRL low is for internal test purposes only. |
| TRST | Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller. |
| TDO | Serial Output for test instructions and data. Changes on the falling edge of TCK. |
| TDI | Serial Input for test instructions and data. Sampled on the rising edge of TCK. |
| TCK | Test Clock to synchronize test logic and control register access through the JTAG port. |
| TMS | Test Mode Select to sequence JTAG test controller's state machine. Sampled on rising edge of TCK. |
| RTCK | JTAG Return Clock used to enhance stability of JTAG debug interface devices. This signal is multiplexed with 1-Wire; thus, utilizing 1-Wire will render RTCK unusable and vice versa; PE16. |
| Secure Digital Interface (X2) | |
| SD1_CMD | SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added. This signal is multiplexed with CSPI3_MOSI; PE22. |
| SD1_CLK | SD Output Clock. This signal is multiplexed with CSPI3_SCLK; PE23. |
| SD1_D[3:0] | SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added. SD1_D[3] is muxed with CSPI3_SS while SD1_D[0] is muxed with CSPI3_MISO PE21–18. |
| SD2_CMD | SD Command bidirectional signal. This signal is multiplexed with MSHC_BS; through GPIO multiplexed with SLCDC1_CS; PB8. |
| SD2_CLK | SD Output Clock signal. This signal is multiplexed with MSHC_SCLK, through GPIO multiplexed with SLCDC1_CLK; PB9. |
| SD2_D[3:0] | SD Data bidirectional signals. SD2_D[3:0] multiplexed with MSHC_DATA[0:3], also through GPIO SD2_1:0] multiplexed with SLCDC1_RS and SLDCD1_D0; PB7–PB4. |
| SD3_CMD | SD Command bidirectional signal. This signal is through GPIO PD0 multiplexed with FEC_TXD0. |
| SD3_CLK | SD Output Clock signal. This signal is multiplexed with ETMTRACEPKT15 and also through GPIO PD1 multiplexed with FEC_TXD1. |
| Note: SD3_DATA is multiplexed with ATA_DATA3–0. | |
| UARTs (X6) | |
| UART1_RTS | Request to Send input signal; PE15 |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|--|---|
| UART1_CTS | Clear to Send output signal; PE14 |
| UART1_RXD | Receive Data input signal; PE13 |
| UART1_TXD | Transmit Data output signal, PE12 |
| UART2_RXD | Receive Data input signal. This signal is multiplexed with KP_ROW6 signal from KPP; PE7. |
| UART2_TXD | Transmit Data output signal. This signal is multiplexed with KP_COL6 signal from KPP; PE6. |
| UART2_RTS | Request to Send input signal. This signal is multiplexed with KP_ROW7 signal from KPP; PE4. |
| UART2_CTS | Clear to Send output signal. This signal is multiplexed with KP_COL7 signal from KPP; PE3. |
| UART3_RTS | Request to Send input signal, PE11 |
| UART3_CTS | Clear to Send output signal; PE10 |
| UART3_RXD | Receive Data input signal; PE9 |
| UART3_TXD | Transmit Data output signal; PE8 |
| Note: UART 4, 5, and 6 are multiplexed with COMS Sensor Interface signals. | |
| Keypad | |
| KP_COL[5:0] | Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2_CTS}}$ and $\overline{\text{UART2_TXD}}$ respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available. |
| KP_ROW[5:0] | Keypad Row selection signals. KP_ROW[7:6] are multiplexed with $\overline{\text{UART2_RTS}}$ and $\overline{\text{UART2_RXD}}$ signals respectively. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signals KP_ROW6 and KP_ROW7 are available. |
| Note: KP_COL[7:6] and KP_ROW[7:6] are multiplexed with UART2 signals as show above, also see UARTs table. | |
| PWM | |
| PWMO | PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module; PE5. |
| CSPI (X3) | |
| CSPI1_MOSI | Master Out/Slave In signal, PD31 |
| CSPI1_MISO | Master In/Slave Out signal, PD30 |
| CSPI1_SS[2:0] | Slave Select (Selectable polarity) signal, the CSPI1_SS2 is multiplexed with $\overline{\text{USBH2_DATA5/RCV}}$; and CSPI1_SS1 is multiplexed with $\overline{\text{EXT_DMAGRANT}}$; PD26–28. |
| CSPI1_SCLK | Serial Clock signal, PD29 |
| CSPI1_RDY | Serial Data Ready signal, shared with Ext_DMAREq_B signal; PD25 |
| CSPI2_MOSI | Master Out/Slave In signal, multiplexed with $\overline{\text{USBH2_DATA1/TXDP}}$; PD24 |
| CSPI2_MISO | Master In/Slave Out signal, multiplexed with $\overline{\text{USBH2_DATA2/TXDm}}$; PD23 |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|---|---|
| CSPI2_SS[2:0] | Slave Select (Selectable polarity) signals, multiplexed with USBH2_DATA4/RXDM, USBH2_DATA3/RXDP, USBH2_DATA6/SPEED; PD19–PD21 |
| CSPI2_SCLK | Serial Clock signal, multiplexed with USBH2_DATA0/OEn; PD22 |
| Note: CSPI3 CSPI3_MOSI, CSPI3_MISO, CSPI3_SS, and CSPI3_SCLK are multiplexed with SD1 signals. | |
| I²C | |
| I2C2_SCL | I ² C2 Clock, through GPIO, multiplexed with SLDCD_data8; PC6 |
| I2C2_SDA | I ² C2 Data, through GPIO, multiplexed with SLDCD_data7; PC5 |
| I2C_CLK | I ² C1 Clock; PD18 |
| I2C_DATA | I ² C1 Data; PD17 |
| CMOS Sensor Interface | |
| CSI_HSYNC | Sensor port horizontal sync, multiplexed with UART5_RTSP; PB21 |
| CSI_VSYNC | Sensor port vertical sync, multiplexed with UART5_CTS; PB20 |
| CSI_D7 | Sensor port data, multiplexed with UART5_RXD; PB19 |
| CSI_D6 | Sensor port data, multiplexed with UART5_TXD; PB18 |
| CSI_D5 | Sensor port data; PB17 |
| CSI_PIXCLK | Sensor port data latch clock; PB16 |
| CSI_MCLK | Sensor port master clock, PB15 |
| CSI_D4 | Sensor port data, PD14 |
| CSI_D3 | Sensor port data, multiplexed with UART6_RTS; PB13 |
| CSI_D2 | Sensor port data, multiplexed with UART6_CTS; PB12 |
| CSI_D1 | Sensor port data, multiplexed with UART6_RXD; PB11 |
| CSI_D0 | Sensor port data, multiplexed with UART6_TXD; PB10 |
| Serial Audio Port—SSI (Configurable to I2S Protocol and AC97) (2 to 4) | |
| SSI1_CLK | Serial clock signal that is output in master or input in slave; PC23 |
| SSI1_TXD | Transmit serial data; PC22 |
| SSI1_RXD | Receive serial data; PC21 |
| SSI1_FS | Frame Sync signal that is output in master and input in slave; PC20 |
| SSI2_CLK | Serial clock signal that is output in master or input in slave, multiplexed with GPT4_TIN. PC27 |
| SSI2_TXD | Transmit serial data signal, multiplexed with GPT4_TOUT; PC26 |
| SSI2_RXD | Receive serial data, multiplexed with GPT5_TIN; PC25 |
| SSI2_FS | Frame Sync signal which is output in master and input in slave, multiplexed with GPT5_TOUT: PC24 |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|--|---|
| SSI3_CLK | Serial clock signal which is output in master or input in slave. This signal is multiplexed with SLCDC2_CLK; through GPIO multiplexed with PC_WAIT_B; PC31. |
| SSI3_TXD | Transmit serial data signal which is multiplexed with SLCDC2_CS, through GPIO multiplexed with PC_READY; PC30 |
| SSI3_RXD | Receive serial data which is multiplexed with SLCDC2_RS; through GPIO multiplexed with PC_VS1; PC29 |
| SSI3_FS | Frame Sync signal which is output in master and input in slave. This signal is multiplexed with SLCDC2_D0; through GPIO multiplexed with PC_VS1; PC28. |
| SSI4_CLK | Serial clock signal which is output in master or input in slave; through GPIO multiplexed with PC_BVD1; PC19 |
| SSI4_TXD | Transmit serial data; through GPIO multiplexed with PC_BVD2; PC18 |
| SSI4_RXD | Receive serial data; through GPIO multiplexed with IOIS16; PC17 |
| SSI4_FS | Frame Sync signal which is output in master and input in slave; PC16 |
| General Purpose Timers (X6) | |
| TIN | Timer Input Capture or Timer Input Clock—The signal on this input is applied to GPT 1–3 simultaneously. This signal is muxed with the Walk-up Guard Mode \overline{WKGD} signal in the PLL, Clock, and Reset Controller module, and is also multiplexed with GPT6_TOUT; PC15. |
| TOUT1 | Timer Output signal from General Purpose Timer1 (GPT1). This signal is multiplexed with SSI1_MCLK and SSI2_MCLK signal of SSI1 and SSI2. The pin name of this signal is simply TOUT, and is also multiplexed with GPT6_TIN; PC14. |
| Note: TOUT2, TOUT3 are multiplexed with PWMO pad; GPT4 and GPT5 signals are multiplexed with SSI2 pads. | |
| USB2.0 | |
| USBOTG_DIR/TXDM | USB OTG direction/Transmit Data Minus signal, multiplexed with KP_ROW7A; PE2 |
| USBOTG_STP/TXDM | USB OTG Stop signal/Transmit Data Minus signal, multiplexed with KP_ROW6A; PE1 |
| USBOTG_NXT/TXDM | USB OTG NEXT/Transmit Data Minus signal, multiplexed with KP_COL6A; PE0 |
| USBOTG_CLK/TXDM | USB OTG Clock/Transmit Data Minus signal, PE24 |
| USBOTG_DATA7/SUSPEND | USB OTG Data7/Suspend signal, PE25 |
| USBH2_STP/TXDM | USB Host2 Stop signal/Transmit Data Minus signal, PA4 |
| USBH2_NXT/TXDM | USB Host2 NEXT/Transmit Data Minus signal, PA3 |
| USBH2_DATA7/SUSPEND | USB Host2 Data7/Suspend signal, PA2 |
| USBH2_DIR/TXDM | USB Host2 Direction/Transmit Data Minus signal, PA1 |
| USBH2_CLK/TXDM | USB Host2 Clock/Transmit Data Minus signal; PA0 |
| USBOTG_DATA3/RXDP | USB OTG data4/Receive Data Plus signal; multiplexed with SLCDC1_DAT15 through PC13 |
| USBOTG_DATA4/RXDM | USB OTG data4/Receive Data Minus signal; multiplexed with SLCDC1_DAT14 through PC12 |
| USBOTG_DATA1/TXDP | USB OTG data1/Transmit Data Plus signal; multiplexed with SLCDC1_DAT13 through PC11 |
| USBOTG_DATA2/TXDm | USB OTG data2/Transmit Data Minus signal; multiplexed with SLCDC1_DAT12 through PC10 |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|--|---|
| USBOTG_DATA0/Oen | USB OTG data0/Output Enable signal; multiplexed with SLCDC1_DAT11 through PC9 |
| USBOTG_DATA6/SPEED | USB OTG data6/Suspend signal; multiplexed with SLCDC1_DAT10 and USBG_TXR_INT_B through PC8 |
| USBOTG_DATA5/RCV | USB OTG data5/RCV signal; multiplexed with SLCDC1_DAT9 through PC7 |
| USBH1_RXDP | USB Host1 Receive Data Plus signal, multiplexed with UART4_RXD; multiplexed with SLCDC1_DAT6 and UART4_RTS_ALT through PB31 |
| USBH1_RXDM | USB Host1 Receive Data Minus signal; multiplexed with SLCDC1_DAT5 and UART4_CTS through PB30 |
| USBH1_TXDP | USB Host1 Transmit Data Plus signal; multiplexed with UART4_CTS, multiplexed with SLCDC1_DAT4 and UART4_RXD_ALT through PB29 |
| USBH1_TXDM | USB Host1 Transmit Data Minus signal; multiplexed with UART4_TXD, multiplexed with SLCDC1_DAT3 through PB28 |
| USBH1_OE_B | USB Host1 Output Enable signal; multiplexed with SLCDC1_DAT2 through PB27 |
| USBH1_FS | USB Host1 Full Speed output signal, multiplexed with UART4_RTS, multiplexed with SLCDC1_DAT1 through PB26 |
| USBH1_RCV | USB Host1 RCV signal; multiplexed with SLCDC1_DAT0 through PB25 |
| USB_OC_B | USB OC signal. PB24 |
| USB_PWR | USB Power signal; PB23 |
| USBH1_SUSP | USB Host1 Suspend signal; PB22 |
| LCD Controller and Smart LCD Controller | |
| OE_ACD | Alternate Crystal Direction/Output Enable; PA31 |
| CONTRAST | This signal is used to control the LCD bias voltage as contrast control; PA30 |
| VSYNC | Frame Sync or Vsync—This signal also serves as the clock signal output for gate; driver (dedicated signal SPS for Sharp panel HR-TFT); PA29. |
| HSYNC | Line Pulse or HSync; PA28 |
| SPL_SPR | Sampling start signal for left and right scanning. Through GPIO, this signal is multiplexed with the SLCDC1_CLK; PA27. |
| PS | Control signal output for source driver (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_CS; PA26. |
| CLS | Start signal output for gate driver. This signal is invert version of PS (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_RS; PA25. |
| REV | Signal for common electrode driving signal preparation (Sharp panel dedicated signal). This signal is multiplexed with SLCDC1_D0; PA24. |
| LD [17:0] | LCD Data Bus—All LCD signals are driven low after reset and when LCD is off. Through GPIO, LD[15:0] signals are multiplexed with SLCDC1_DAT[15:0], SLCDC. PA23–PA6. |
| LSCLK | Shift Clock; PA5 |

Signal Descriptions

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|--|---|
| Note: SLCDC signals are multiplexed with LCDC signals. | |
| ATA (not available on i.MX27L) | |
| ATA_DATA15–0 | ATA Data Bus, [15:0] are multiplexed with ETMTRACEPKT4–12, FEC_MDIO, ETMTRACEPKT13–14 SD3_D3–0; Through GPIO also are multiplexed with SLCDC 15–0, and FEC signals; PF23, PD16–PD2. |
| Noisy I/O Supply Pins | |
| N _{VDD} 1–15, A _{VDD} | Noisy Supply for the I/O pins. There are 16 I/O voltage pads, N _{VDD} 1 through N _{VDD} 15 + A _{VDD} . |
| Analog Supply Pins | |
| FPM _{VDD} MPLL _{VDD} OSC26 _{VDD} UPLL _{VDD} OSC32 _{VDD} OSC32VSS | Supply for analog blocks |
| FPMVSS MPLLVSS OSC26VSS UPLLVSS | Quiet GND for analog blocks |
| Q_{VDD} Internal Power Supply | |
| Q _{VDD} | Power supply pins for silicon internal circuitry |
| QVSS | GND pins for silicon internal circuitry |
| FUSE _{VDD} | For Fuse _{VDD} |
| RTC _{VDD} | For RTC, SCC power supply |
| RTCVSS | For RTC, SCC GND |

Table 3. i.MX27/MX27L Signal Descriptions (continued)

| Pad Name | Function/Notes |
|----------|----------------|
|----------|----------------|

Note: Both 1-Wire and Fast Ethernet Controller signals are multiplexed with other signals. As a result these signal names do not appear in this list. The signals are listed below with the named signal that they are multiplexed.

1-Wire Signals:

The 1-Wire input and output signal is multiplexed with JTAG RTCK pad, PE16.

Fast Ethernet Controller (FEC) Signals on the i.MX27. The ATA module does not exist on the i.MX27L:

FEC_TX_EN: Transmit enable signal, through GPIO multiplexed with ATA_DATA15 pad; PF23

FEC_TX_ER: Transmit Data Error; through GPIO multiplexed with ATA_DATA14 pad; PD16

FEC_COL: Collision signal; through GPIO multiplexed with ATA_DATA13 pad; PD15

FEC_RX_CLK: Receive Clock signal; through GPIO multiplexed with ATA_DATA12 pad; PD14

FEC_RX_DV: Receive data Valid signal; through GPIO multiplexed with ATA_DATA11 pad; PD13

FEC_RXD0: Receive Data0; through GPIO multiplexed with ATA_DATA10 pad; PD12

FEC_TX_CLK: Transmit Clock signal; through GPIO multiplexed with ATA_DATA9 pad; PD11

FEC_CRFS: Carrier Sense enable; through GPIO multiplexed with ATA_DATA8 pad; PD10

FEC_MDC: Management Data Clock; through GPIO multiplexed with ATA_DATA7 pad; PD9

FEC_MDIO: Management Data Input/Output, multiplexed with ATA_DATA6 pad; PD8

FEC_RXD3-1: Receive Data; through GPIO multiplexed with ATA_DATA5-3 pad; PD7-5

FEC_RX_ER: Receive Data Error; through GPIO multiplexed with ATA_DATA2 pad; PD4

FEC_TXD3-2: Transmit Data; through GPIO multiplexed with ATA_DATA1-0; pad; PD3-2

FEC_TXD1: Transmit Data; through GPIO multiplexed with SD3_CLK pad; PD1

FEC_TXD0: Transmit Data; through GPIO multiplexed with SD3_CMD pad; PD0

Note: The Rest ATA signals are multiplexed with PCMCIA Pads.

3.1 Power-Up Sequence

The i.MX27/MX27L processor consists of three major sets for power supply voltage named Q_{VDD} (core logic supply), $FUSE_{VDD}$ (analog supply for FUSEBOX), and $N_{VDD}, VDDA$ (IO supply). The External Voltage Regulators and power-on devices must provide the applications processor with a specific sequence of power and resets to ensure proper operation.

It is important that the applications processor power supplies be powered-up in a certain order to avoid unintentional fuse blown. Q_{VDD} should be powered up before $FUSE_{VDD}$. The recommended order is:

1. Q_{VDD} (1.5 V)
2. $FUSE_{VDD}$ (1.8 V), N_{VDD} (1.8/2.775 V), and Analog Supplies (2.775 V). See [Table 3](#) for signal descriptions.

or

1. Q_{VDD} (1.5 V), N_{VDD} (1.8/2.775 V), and Analog Supplies (2.775 V). See [Table 3](#) for signal descriptions.
2. $FUSE_{VDD}$ (1.8 V).

3.2 EMI Pins Multiplexing

This section discusses the multiplexing of EMI signals. The EMI signals' multiplexing is done inside the EMI. [Table 4](#) lists the i.MX27 pin names, pad types, and the memory devices' equivalent pin names.

Table 4. EMI Multiplexing

| Pin Name | Pad Type | WEIM | SDRAM | PCMCIA | DDR | NFC |
|----------|----------|------|-------|------------------|------|-----|
| A0 | regular | A0 | MA0 | A0 | MA0 | — |
| A1 | regular | A1 | MA1 | A1 | MA1 | — |
| A2 | regular | A2 | MA2 | A2 | MA2 | — |
| A3 | regular | A3 | MA3 | A3 | MA3 | — |
| A4 | regular | A4 | MA4 | A4 | MA4 | — |
| A5 | regular | A5 | MA5 | A5 | MA5 | — |
| A6 | regular | A6 | MA6 | A6 | MA6 | — |
| A7 | regular | A7 | MA7 | A7 | MA7 | — |
| A8 | regular | A8 | MA8 | A8 | MA8 | — |
| A9 | regular | A9 | MA9 | A9 | MA9 | — |
| A10 | regular | A10 | — | A10 | — | — |
| MA10 | regular | — | MA10 | — | MA10 | — |
| A11 | regular | A11 | MA11 | A11 | MA11 | — |
| A12 | regular | A12 | MA12 | A12 | MA12 | — |
| A13 | regular | A13 | MA13 | A13 | MA13 | — |
| A14 | regular | A14 | — | A14 | — | — |
| A15 | regular | A15 | — | A15 | — | — |
| A16 | regular | A16 | — | A16 | — | — |
| A17 | regular | A17 | — | A17 | — | — |
| A18 | regular | A18 | — | A18 | — | — |
| A19 | regular | A19 | — | A19 | — | — |
| A20 | regular | A20 | — | A20 | — | — |
| A21 | regular | A21 | — | A21 | — | — |
| A22 | regular | A22 | — | A22 | — | — |
| A23 | regular | A23 | — | A23 | — | — |
| A24 | regular | A24 | — | A24 | — | — |
| A25 | regular | A25 | — | A25 | — | — |
| SDBA1 | regular | — | SDBA1 | $\overline{CE1}$ | — | — |
| SDBA0 | regular | — | SDBA0 | $\overline{CE2}$ | — | — |
| SD0 | ddr | — | SD0 | — | — | — |
| SD1 | ddr | — | SD1 | — | — | — |
| SD2 | ddr | — | SD2 | — | — | — |
| SD3 | ddr | — | SD3 | — | — | — |
| SD4 | ddr | — | SD4 | — | — | — |
| SD5 | ddr | — | SD5 | — | — | — |

Table 4. EMI Multiplexing (continued)

| Pin Name | Pad Type | WEIM | SDRAM | PCMCIA | DDR | NFC |
|----------|----------|------|-------|--------|-----|-----|
| SD6 | ddr | — | SD6 | — | — | — |
| SD7 | ddr | — | SD7 | — | — | — |
| SD8 | ddr | — | SD8 | — | — | — |
| SD9 | ddr | — | SD9 | — | — | — |
| SD10 | ddr | — | SD10 | — | — | — |
| SD11 | ddr | — | SD11 | — | — | — |
| SD12 | ddr | — | SD12 | — | — | — |
| SD13 | ddr | — | SD13 | — | — | — |
| SD14 | ddr | — | SD14 | — | — | — |
| SD15 | ddr | — | SD15 | — | — | — |
| SD16 | ddr | — | SD16 | — | — | — |
| SD17 | ddr | — | SD17 | — | — | — |
| SD18 | ddr | — | SD18 | — | — | — |
| SD19 | ddr | — | SD19 | — | — | — |
| SD20 | ddr | — | SD20 | — | — | — |
| SD21 | ddr | — | SD21 | — | — | — |
| SD22 | ddr | — | SD22 | — | — | — |
| SD23 | ddr | — | SD23 | — | — | — |
| SD24 | ddr | — | SD24 | — | — | — |
| SD25 | ddr | — | SD25 | — | — | — |
| SD26 | ddr | — | SD26 | — | — | — |
| SD27 | ddr | — | SD27 | — | — | — |
| SD28 | ddr | — | SD28 | — | — | — |
| SD29 | ddr | — | SD29 | — | — | — |
| SD30 | ddr | — | SD30 | — | — | — |
| SD31 | ddr | — | SD31 | — | — | — |
| DQM0 | ddr | — | DQM0 | — | — | — |
| DQM1 | ddr | — | DQM1 | — | — | — |
| DQM2 | ddr | — | DQM2 | — | — | — |
| DQM3 | ddr | — | DQM3 | — | — | — |
| EB0 | regular | EB0 | — | REG | — | — |
| EB1 | regular | EB1 | — | IORD | — | — |
| OE | regular | OE | — | IOWR | — | — |
| CS0 | regular | CS0 | — | — | — | — |
| CS1 | regular | CS1 | — | — | — | — |

Table 4. EMI Multiplexing (continued)

| Pin Name | Pad Type | WEIM | SDRAM | PCMCIA | DDR | NFC |
|--------------------|----------|------|--------|-----------------|-------|-----|
| CS2 | regular | CS2 | CSD0 | — | — | — |
| CS3 | regular | CS3 | CSD1 | — | — | — |
| CS4 | regular | CS4 | — | — | — | — |
| CS5 | regular | CS5 | — | — | — | — |
| ECB | regular | ECB | — | — | — | — |
| LBA | regular | LBA | — | \overline{OE} | — | — |
| BCLK | regular | BCLK | — | — | — | — |
| RW | regular | RW | — | WE | — | — |
| RAS | regular | — | RAS | — | — | — |
| CAS | regular | — | CAS | — | — | — |
| SDWE | regular | — | SDWE | — | — | — |
| SDCKE0 | regular | — | SDCKE0 | — | — | — |
| SDCKE1 | regular | — | SDCKE1 | — | — | — |
| SDCLK | regular | — | SDCLK | — | — | — |
| \overline{SDCLK} | — | — | — | — | — | — |
| SDQS0 | ddr | — | — | — | SDQS0 | — |
| SDQS1 | ddr | — | — | — | SDQS1 | — |
| SDQS2 | ddr | — | — | — | SDQS2 | — |
| SDQS3 | ddr | — | — | — | SDQS3 | — |
| \overline{NFW} | regular | — | — | — | — | WE |
| \overline{NFR} | regular | — | — | — | — | RE |
| NFALE | regular | — | — | — | — | ALE |
| NFCLE | regular | — | — | — | — | CLE |
| \overline{NFWP} | regular | — | — | — | — | WP |
| \overline{NFCE} | regular | — | — | — | — | CE |
| NFRB | regular | — | — | — | — | R/B |
| D15 | regular | D15 | — | D15 | — | D15 |
| D14 | regular | D14 | — | D14 | — | D14 |
| D13 | regular | D13 | — | D13 | — | D13 |
| D12 | regular | D12 | — | D12 | — | D12 |
| D11 | regular | D11 | — | D11 | — | D11 |
| D10 | regular | D10 | — | D10 | — | D10 |
| D9 | regular | D9 | — | D9 | — | D9 |
| D8 | regular | D8 | — | D8 | — | D8 |
| D7 | regular | D7 | — | D7 | — | D7 |

Table 4. EMI Multiplexing (continued)

| Pin Name | Pad Type | WEIM | SDRAM | PCMCIA | DDR | NFC |
|------------------------------|----------|------|-------|--------------------------|-----|-----|
| D6 | regular | D6 | — | D6 | — | D6 |
| D5 | regular | D5 | — | D5 | — | D5 |
| D4 | regular | D4 | — | D4 | — | D4 |
| D3 | regular | D3 | — | D3 | — | D3 |
| D2 | regular | D2 | — | D2 | — | D2 |
| D1 | regular | D1 | — | D1 | — | D1 |
| D0 | regular | D0 | — | D0 | — | D0 |
| $\overline{\text{PC_CD1}}$ | regular | — | — | $\overline{\text{CD1}}$ | — | — |
| $\overline{\text{PC_CD2}}$ | regular | — | — | $\overline{\text{CD2}}$ | — | — |
| $\overline{\text{PC_WAIT}}$ | regular | — | — | $\overline{\text{WAIT}}$ | — | — |
| PC_READY | regular | — | — | READY | — | — |
| PC_PWRON | regular | — | — | PC_PWRON | — | — |
| PC_VS1 | regular | — | — | VS1 | — | — |
| PC_VS2 | regular | — | — | VS2 | — | — |
| PC_BVD1 | regular | — | — | BVD1 | — | — |
| PC_BVD2 | regular | — | — | BVD2 | — | — |
| PC_RST | regular | — | — | RST | — | — |
| IOIS16 | regular | — | — | IOIS16/WP | — | — |
| $\overline{\text{PC_RW}}$ | regular | — | — | $\overline{\text{RW}}$ | — | — |
| PC_POE | regular | — | — | POE | — | — |
| M_REQUEST | regular | — | — | — | — | — |
| M_GRANT | regular | — | — | — | — | — |

4 Electrical Characteristics

This section provides the chip-level and module-level electrical characteristics for the i.MX27/i.MX27L.

4.1 i.MX27/i.MX27L Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC. See [Table 5](#) for a quick reference to the individual tables and sections.

Table 5. i.MX27/i.MX27L Chip-Level Conditions

| For these characteristics... | Topic appears... |
|--|----------------------------|
| Table 6, “DC Absolute Maximum Conditions” | on page 40 |
| Table 7, “DC Operating Conditions” | on page 40 |
| Table 9, “Interface Frequency” | on page 41 |
| Table 10, “Frequency Definition for Power Consumption Measurement” | on page 42 |
| Table 11, “Current Consumption” | on page 42 |
| Section 4.1.3, “Test Conditions and Recommended Settings” | on page 43 |

[Table 6](#) provides the DC absolute maximum operating conditions.

CAUTION

Stresses beyond those listed under [Table 6](#) may cause permanent damage to device. These are stress ratings only. Functional operation of device at these or any other conditions beyond those indicated under “DC operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 6. DC Absolute Maximum Conditions

| Ref. Num | Parameter | Symbol | Min | Max | Units |
|----------|----------------------------------|---------------|------|---------------------------|-------|
| 1 | Supply Voltage | V_{DDmax} | -0.5 | 1.52 | V |
| 2 | Supply Voltage (Level Shift I/O) | $V_{DDIOmax}$ | -0.5 | 3.3 | V |
| 3 | Input Voltage Range | V_{Imax} | -0.5 | $NV_{DD} (1, 5-13) + 0.3$ | V |
| 4 | Storage Temperature Range | $T_{storage}$ | -20 | 125 | °C |

[Table 7](#) provides the DC recommended operating conditions.

Table 7. DC Operating Conditions

| ID | Parameter | Symbol | Min | Typical | Max | Units |
|----|----------------------------------|-------------|------|---------|------|-------|
| 1 | Core Supply Voltage (@266 MHz) | QV_{DD} | 1.2 | 1.3 | 1.52 | V |
| 2 | Core Supply Voltage (@400 MHz) | QV_{DD} | 1.38 | 1.45 | 1.52 | V |
| 3 | RTC, SCC separate Supply Voltage | RTC_{VDD} | 1.2 | — | 1.52 | V |

Table 7. DC Operating Conditions (continued)

| ID | Parameter | Symbol | Min | Typical | Max | Units |
|----|---|---------------------------------------|------|---------|-------|-------|
| 4 | I/O Supply Voltage, Fast (7, 11, 12, 14, 15) ¹ | NV _{DD_FAST} | 1.75 | — | 2.8 | V |
| 5 | I/O Supply Voltage, Slow (5, 6, 8, 9, 10, 13, AV _{DD}) | NV _{DD_SLOW} | 1.75 | — | 3.05 | V |
| | | NV _{DD_SLOW} | 1.75 | — | 3.1 | V |
| 6 | I/O Supply Voltage, DDR (1, 2, 3, 4) ² | NV _{DD_DDR} | 1.75 | — | 1.9 | V |
| 7 | Analog Supply Voltage: FPMV _{DD} , UPLL _{VDD} , MPLLV _{DD} | V _{DD} | 1.35 | 1.4 | 1.6 | V |
| 8 | Fusebox read Supply Voltage | FUSEV _{DD} (read mode) | 1.7 | 1.875 | 1.95 | V |
| 9 | Fusebox Program Supply Voltage | FUSEV _{DD} (program mode) | 3.00 | 3.15 | 3.30 | V |
| 10 | OSC32V _{DD} | V _{OSC32} | 1.1 | — | 1.6 | V |
| 11 | OSC26V _{DD} | V _{OSC26} | 2.68 | — | 2.875 | V |
| 12 | Operating Ambient Temperature (17mm x17mm package) | T _A | -20 | — | 85 | °C |
| 13 | Operating Ambient Temperature (19mm x19mm package) | T _A | -40 | — | 85 | °C |

¹ Segments 11, 14, 15 are mixture of Fast and Slow GPIO.

² Segments 1, 3, 4 are mixture of DDR and Fast GPIO.

4.1.1 DPLL Frequency Specification

Table 8 provides the frequency specifications for the DPLL.

Table 8. DPLL FREQUENCY Specifications

| Parameter | Min | Typical | Max | Unit |
|---|------|---------|------|------|
| Output Duty Cycle (dpdck) | 48.5 | 50.0 | 51.5 | % |
| Output Duty Cycle (dpgdck_2) | 48.5 | 50.0 | 51.5 | % |
| Frequency Lock Time (FOL mode or non-integer MF) | — | — | 80 | μs |
| Phase Lock Time | — | — | 100 | μs |
| Cycle-to-Cycle Jitter | — | — | 0.2 | ns |
| MPLL Operating Frequency ¹ | — | — | 600 | MHz |

¹ A 600 MHz MPLL frequency equals 1.2 GHz at the 2x clock port (see figure 3-2 in MCIMX27 reference manual), so by using the DIV3 divider, it results in an Arm clock frequency of 400 MHz.

Table 9 provides information for interface frequency limits.

Table 9. Interface Frequency

| ID | Parameter | Symbol | Min | Typical | Max | Units |
|----|----------------------------------|-------------------|-----|---------|-------|-------|
| 1 | JTAG: TCK Frequency of Operation | f _{JTAG} | DC | 5 | 33.25 | MHz |

4.1.2 Current Consumption

Table 10 defines the frequency settings used for specifying power consumption in Table 11. All power states are specified. The temperature setting of 25° C is used for specifying the Deep Sleep Mode (DSM) per the temperature range shown in Table 7.

Table 10. Frequency Definition for Power Consumption Measurement

| ID | Parameter | Symbol | Value | Units |
|----|-------------|--------------------|--------|-------|
| 1 | MCU core | $f_{MCUmeas@266}$ | 266 | MHz |
| 2 | MCU core | $f_{MCUmeas@400}$ | 400 | MHz |
| 3 | MCU AHB bus | $f_{MCU-AHBmeas}$ | 133 | MHz |
| 4 | MCU IP bus | $f_{MCU-IPmeas}$ | 66 | MHz |
| 5 | OSC32 | $f_{osc32khzmeas}$ | 32.768 | kHz |

Table 11 shows the power consumption for the i.MX27/i.MX27L device.

Table 11. Current Consumption

| ID | Parameter | Conditions | Symbol | Typical | Max | Units |
|----|--|---|----------------------|---------|------|-------|
| 1 | RUN Current (QV _{DD} current) | RUN Current at 266 MHz QV _{DD} = 1.3 V, T _A = 25°C | I _{ddRUN} | 215 | 260 | mA |
| | | RUN Current at 400 MHz QV _{DD} = 1.45 V, T _A = 25°C | I _{ddRUN} | 366 | 420 | mA |
| 2 | Doze Current | <ul style="list-style-type: none"> QV_{DD} = 1.2 V NV_{DD} = 1.75 V Arm is in wait for interrupt mode. Arm well bias is enabled. MCU PLL is on. SPLL is off. FPM is on. 26MHz oscillator is on. 32 kHz oscillator is on. Other modules are off. T_A = 25° C. | I _{ddDOZE} | 11 | 13.5 | mA |
| 3 | Sleep Current | <ul style="list-style-type: none"> QV_{DD} = 1.2 V. NV_{DD} = 1.75 V. Both PLLs are off. FPM is off. Arm well bias is enabled. 32 kHz oscillator is on. 26MHz oscillator is off. All the modules are off. T_A = 25° C. | I _{ddSLEEP} | 0.9 | 3.5 | mA |
| 4 | Power Gate | <ul style="list-style-type: none"> NV_{DD13} is on. See Table 7 for specific values. RTC_{VDD}, OSC32_{VDD} are on. See Table 7 for specific values. All other V_{DD} = 0 V T_A = 25° C. | I _{ddPG} | 50 | 216 | µA |

4.1.3 Test Conditions and Recommended Settings

Unless specified, AC timing parameters are specified for 15 pF loading on i.MX27/i.MX27L pads. Drive strength has been kept at default/reset values for testing. EMI timing has been verified with high drive strength setting and 25 pF loads. SDHC timing has also been verified with high drive strength setting. Unless otherwise noted, AC/DC parameters are guaranteed at operating conditions shown in [Table 7](#).

4.2 Module-Level Electrical Specifications

This section contains the i.MX27/i.MX27L electrical information including timing specifications, arranged in alphabetical order by module name.

4.2.1 Pads IO (PADIO) Electricals

4.2.1.1 DC Electrical Characteristics

The over-operating characteristics appear in [Table 12](#) for GPIO pads and [Table 13](#) for DDR (Double Data Rate) pads (unless otherwise noted).

Table 12. GPIO Pads DC Electrical Parameters

| Parameter | Symbol | Test Conditions | Min | Typical | Max | Units |
|---|-------------|---|------------------|---------|-----------------|-------|
| High-level output voltage | V_{OH} | $I_{OH} = -1 \text{ mA}$ | $N_{VDD} - 0.15$ | — | — | V |
| | | $I_{OH} = \text{specified Drive}$ | $0.8 * N_{VDD}$ | — | — | V |
| Low-level output voltage | V_{OL} | $I_{OL} = 1 \text{ mA}$ | — | — | 0.15 | V |
| | | $I_{OL} = \text{specified Drive}$ | — | — | $0.2 * N_{VDD}$ | V |
| High-level output current, slow slew rate | I_{OH_S} | $V_{OH} = 0.8 * N_{VDD}$ Normal High Max High ¹ | -2 -4 -8 | — | — | mA |
| High-level output current, fast slew rate | I_{OH_F} | $V_{OH} = 0.8 * N_{VDD}$ Normal High Max High ¹ | -4 -6 -8 | — | — | mA |
| Low-level output current, slow slew rate | I_{OL_S} | $V_{OL} = 0.2 * N_{VDD}$ Normal High Max High ¹ | 2 4 8 | — | — | mA |
| Low-level output current, fast slew rate | I_{OL_F} | $V_{OL} = 0.2 * N_{VDD}$ Normal High Max High ¹ | 4 6 8 | — | — | mA |
| Input Hysteresis | V_{HYS} | Hysteresis enabled | 0.25 | — | — | V |
| Schmitt trigger VT+ | V_{T+} | Hysteresis enabled | $0.5 * Q_{VDD}$ | — | — | V |
| Schmitt trigger VT- | V_{T-} | Hysteresis enabled | — | — | $0.5 * Q_{VDD}$ | V |

Electrical Characteristics

Table 12. GPIO Pads DC Electrical Parameters (continued)

| Parameter | Symbol | Test Conditions | Min | Typical | Max | Units |
|---------------------------------|-----------------|---|-----------------------|---------|-----------------------|----------|
| Pull-up resistor (22 kΩ PU) | R _{PU} | — | 15 | 22 | 59 | kΩ |
| Pull-up resistor (47 kΩ PU) | R _{PU} | — | 30 | 47 | 128 | |
| Pull-up resistor (100 kΩ PU) | R _{PU} | — | 34 | 100 | 268 | |
| Pull-down resistor (100 kΩ PD) | R _{PD} | — | 25 | 100 | 343 | |
| Input current (no PU/PD) | I _{IN} | V _I = 0 V _I = N _{VDD} | — | 0.33 | ±1 | μA |
| Input current (22 kΩ PU) | I _{IN} | V _I = 0 V _I = N _{VDD} | — | — | 115 0.1 | μA μA |
| Input current (47 kΩ PU) | I _{IN} | V _I = 0 V _I = N _{VDD} | — | — | 53 0.1 | μA μA |
| Input current (100 kΩ PU) | I _{IN} | V _I = 0 V _I = N _{VDD} | — | — | 25 0.1 | μA μA |
| Input current (100 kΩ PD) | I _{IN} | V _I = 0 V _I = N _{VDD} | — | — | 0.25 28 | μA μA |
| Tri-state input leakage current | I _Z | V _I = N _{VDD} or 0 I/O = high Z | — | 0.33 | ±2 | μA |
| High Level DC Input Voltage | V _{IH} | — | 0.7*V _{DDIO} | — | V _{DDIO} | V |
| Low-Level DC Input Voltage | V _{IL} | — | 0 | — | 0.3*V _{DDIO} | V |

¹ Maximum High strength should be avoided due to excessive overshoot and ringing.

Table 13. DDR (Double Data Rate) I/O Pads DC Electrical Parameters

| Parameter | Symbol | Test Conditions | Min | Typical | Max | Units |
|---------------------------|-----------------|--|--------------------------------|---------|------------------------------|-------|
| High-level output voltage | V _{OH} | I _{OH} = -1 mA | NV _{DD_DDR} -0.08 | — | — | V |
| | | I _{OH} = specified Drive | 0.8*N _{VDD_} DDR | — | — | V |
| Low-level output voltage | V _{OL} | I _{OL} = 1 mA | — | — | 0.08 | V |
| | | I _{OL} = specified Drive | — | — | 0.2*N _{VDD_} DDR | V |
| High-level output current | I _{OH} | V _{OH} =0.8*N _{VDD_DDR} Normal High Max High ¹ DDR Drive ¹ | -3.6 -7.2 -10.8 -14.4 | — | — | mA |
| Low-level output current | I _{OL} | V _{OL} =0.2*N _{VDD_DDR} Normal High Max High ¹ DDR Drive ¹ | 3.6 7.2 10.8 14.4 | — | — | mA |

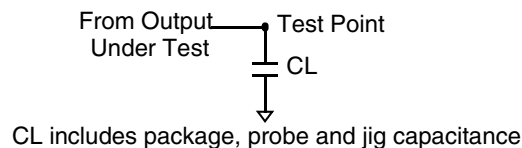
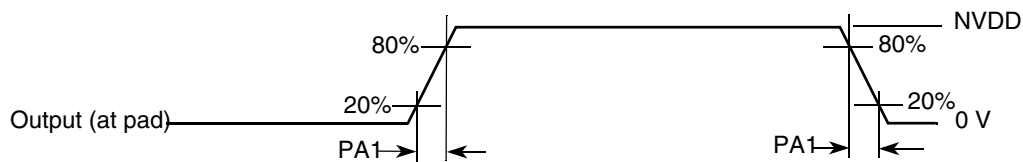
Table 13. DDR (Double Data Rate) I/O Pads DC Electrical Parameters (continued)

| Parameter | Symbol | Test Conditions | Min | Typical | Max | Units |
|--------------------------|----------|---|-----|---------|-----|---------------|
| Low-level input current | I_{IL} | $V_I = 0$ | — | 1.7 | 2 | μA |
| High-level input current | I_{IH} | $V_I = NV_{DD_DDR}$ | — | | 2 | μA |
| Tri-state current | I_Z | $V_I = NV_{DD_DDR}$ or 0 I/O = high Z | — | 1.7 | 2 | μA |

¹ Maximum High and DDR Drive strengths should be avoided due to excessive overshoot and ringing.

4.2.1.2 AC Electrical Characteristics

Figure 2 depicts the load circuit for output pads. Figure 3 depicts the output pad transition time waveform. The range of operating conditions appear in Table 14 for slow general I/O, Table 15 for fast general I/O, and Table 16 for DDR I/O (unless otherwise noted).

**Figure 2. Load Circuit for Output Pad****Figure 3. Output Pad Transition Time Waveform****Table 14. AC Electrical Characteristics of Slow General I/O Pads**

| ID | Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|-----|--|--------|----------------|--------------|------------|-------------|-------|
| PA1 | Output Pad Transition Times (Max High) | tpr | 25 pF 50 pF | 1.25 1.95 | 1.9 2.9 | 3.2 4.75 | ns |
| | Output Pad Transition Times (High) | tpr | 25 pF 50 pF | 1.45 2.6 | — | 4.8 8.4 | ns |
| | Output Pad Transition Times (Standard Drive) | tpr | 25 pF 50 pF | 2.6 5.1 | — | 8.5 16.5 | ns |
| — | Maximum Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 15. AC Electrical Characteristics of Fast General I/O Pads

| ID | Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|-----|---|--------|----------------|-------------|------------|------------|-------|
| PA1 | Output Pad Transition Times (Max High) | tpr | 25 pF 50 pF | 0.9 1.7 | 1.2 2.4 | 2.0 4.0 | ns |
| | Output Pad Transition Times (High) | tpr | 25 pF 50 pF | 1.15 2.3 | 1.6 3.1 | 2.7 5.3 | ns |
| | Output Pad Transition Times (Normal) | tpr | 25 pF 50 pF | 1.7 3.4 | 2.4 4.7 | 4.0 8.0 | ns |
| — | Maximum Input Transition Times ¹ | trm | — | — | — | 25 | ns |

¹ Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 16. AC Electrical Characteristics of DDR I/O Pads

| ID | Parameter | Symbol | Test Condition | Min | Typical | Max | Units |
|-----|---|--------|----------------|-------------|--------------|------------|-------|
| PA1 | Output Pad Transition Times (DDR Drive) | tpr | 25 pF 50 pF | 0.5 1.0 | 0.75 1.45 | 1.2 2.4 | ns |
| | Output Pad Transition Times (Max High) | tpr | 25 pF 50 pF | 0.67 1.3 | 1.0 2.0 | 1.6 3.1 | ns |
| | Output Pad Transition Times (High) | tpr | 25 pF 35 pF | 1.0 1.95 | 1.5 2.9 | 2.4 4.7 | ns |
| | Output Pad Transition Times (Normal) | tpr | 25 pF 50 pF | 2.0 3.9 | 2.9 5.9 | 4.8 8.4 | ns |
| — | Maximum Input Transition Times | trm | — | — | — | 5 | ns |

4.2.2 1-Wire Electrical Specifications

Figure 4 depicts the RPP timing, and Table 17 lists the RPP timing parameters.

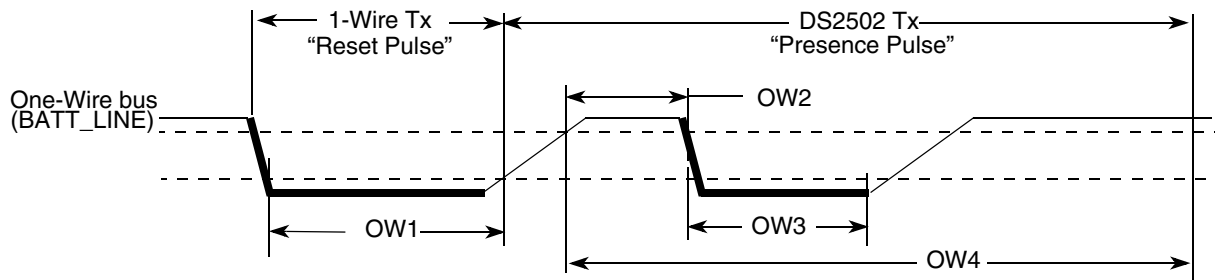


Figure 4. Reset and Presence Pulses (RPP) Timing Diagram

Table 17. RPP Sequence Delay Comparisons Timing Parameters

| ID | Parameters | Symbol | Min | Typical | Max | Units |
|-----|----------------------|-------------------|-----|---------|-----|-------|
| OW1 | Reset Time Low | t _{RSTL} | 480 | 511 | | μs |
| OW2 | Presence Detect High | t _{PDH} | 15 | — | 60 | μs |

Table 17. RPP Sequence Delay Comparisons Timing Parameters (continued)

| ID | Parameters | Symbol | Min | Typical | Max | Units |
|-----|---------------------|------------|-----|---------|-----|---------|
| OW3 | Presence Detect Low | t_{PDL} | 60 | — | 240 | μs |
| OW4 | Reset Time High | t_{RSTH} | 480 | 512 | — | — |

Figure 5 depicts Write 0 Sequence timing, and Table 18 lists the timing parameters.

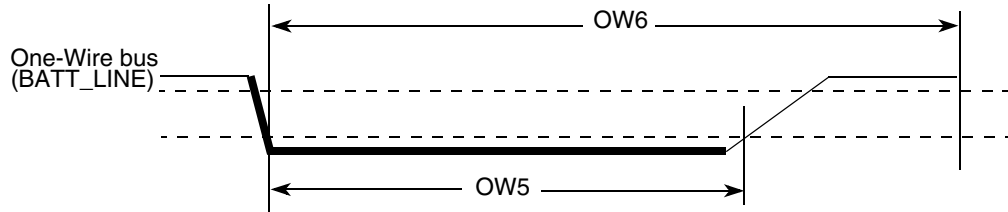


Figure 5. Write 0 Sequence Timing Diagram

Table 18. WR0 Sequence Timing Parameters

| ID | Parameter | Symbol | Min | Typical | Max | Units |
|-----|------------------------|----------------|-----|---------|-----|---------|
| OW5 | Write 0 Low Time | t_{WR0_low} | 60 | 100 | 120 | μs |
| OW6 | Transmission Time Slot | t_{SLOT} | OW5 | 117 | 120 | μs |

Figure 6 depicts Write 1 Sequence timing, Figure 7 depicts the Read Sequence timing, and Table 19 lists the timing parameters.

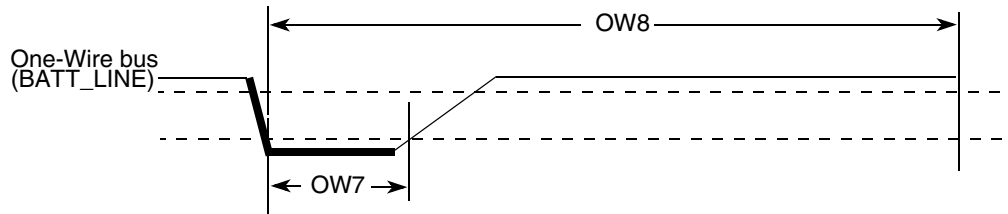


Figure 6. Write 1 Sequence Timing Diagram

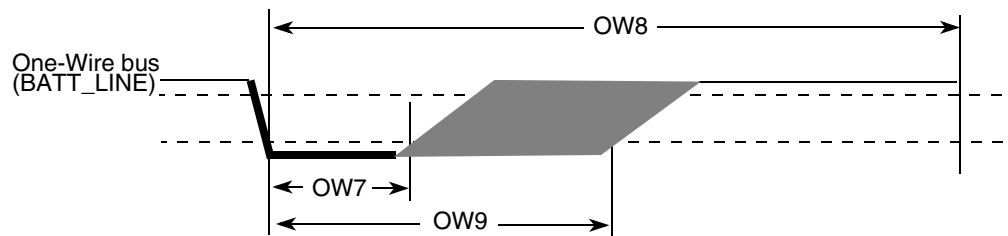


Figure 7. Read Sequence Timing Diagram

Table 19. Write 1/Read Timing Parameters

| ID | Parameter | Symbol | Min | Typical | Max | Units |
|-----|------------------------|---------------|-----|---------|-----|---------------|
| OW7 | Write 1/Read Low Time | t_{LOW1} | 1 | 5 | 15 | μs |
| OW8 | Transmission Time Slot | t_{SLOT} | 60 | 117 | 120 | μs |
| OW9 | Release Time | $t_{RELEASE}$ | 15 | — | 45 | μs |

4.2.3 ATA Electrical Specifications

This section describes the electrical information of the Parallel ATA module compliant with ATA/ATAPI-6 specification.

NOTE

The parallel ATA module is not available on the i.MX27L.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100 MB/s. Parallel ATA module interface consist of a total of 29 pins, Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-6 specification and these requirements are configurable by the ATA module registers.

Below defines the AC characteristics of all the interface signals on all data transfer modes.

4.2.3.1 General Timing Requirements

Table 20 provides the general timing requirements for the ATA interface signals.

Table 20. AC Characteristics of All Interface Signals

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---|------------|-----|------|------|
| S11 | Rising edge slew rate for any signal on ATA interface (see note) | S_{rise} | — | 1.25 | V/ns |
| S12 | Falling edge slew rate for any signal on ATA interface (see note) | S_{fall} | — | 1.25 | V/ns |
| S13 | Host interface signal capacitance at the host connector | C_{host} | — | 20 | pF |

Note: SRISE and SFALL meets this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15 pf through 40 pf where all signals have the same capacitive load value.

ATA Interface Signals

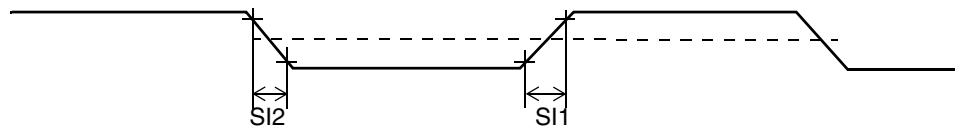


Figure 8. ATA interface Signals Timing Diagram

4.2.4 Digital Audio Mux (AUDMUX)

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI, SAP) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by SSI and SAP modules. Please refer to their respective electrical specifications.

4.2.5 CMOS Sensor Interface (CSI)

This section describes the electrical information (AC timing) of the CSI.

4.2.5.1 Gated Clock Mode Timing

VSYNC, HSYNC, and PIXCLK signals are used in this mode. A frame starts with a rising/falling edge on VSYNC, then HSYNC goes high and holds for the entire line. The pixel clock is valid as long as HSYNC is high. [Figure 9](#) and [Figure 10](#) depict the gated clock mode timings of CSI, and [Table 21](#) lists the timing parameters.

Figure 9 shows sensor output data on the pixel clock falling edge. The CSI latches data on the pixel clock rising edge.

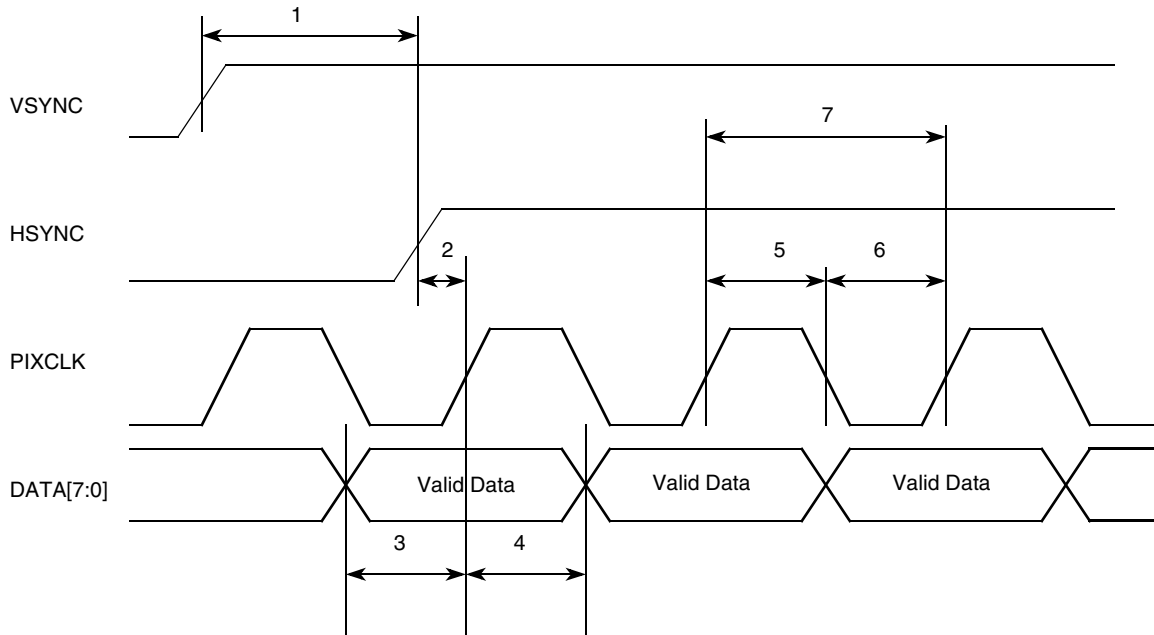


Figure 9. CSI Timing Diagram, Gated, PIXCLK—Sensor Data at Falling Edge, Latch Data at Rising Edge

Figure 10 shows sensor output data on the pixel clock rising edge. The CSI latches data on the pixel clock falling edge.

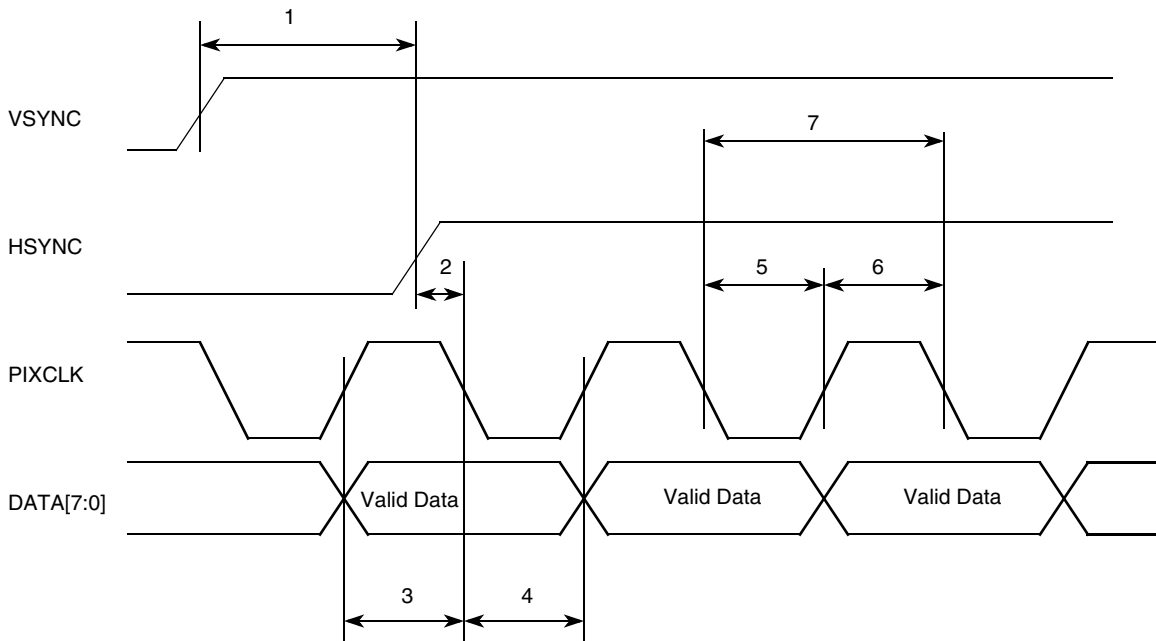


Figure 10. CSI Timing Diagram, Gated, PIXCLK—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 21. Gated Clock Mode Timing Parameters

| Number | Parameter | Minimum | Maximum | Unit |
|--------|-------------------------|--------------------|---------------|------|
| 1 | csi_vsync to csi_hsync | $9 \cdot T_{HCLK}$ | — | ns |
| 2 | csi_hsync to csi_pixclk | 3 | $(T_p/2) - 3$ | ns |
| 3 | csi_d setup time | 1 | — | ns |
| 4 | csi_d hold time | 1 | — | ns |
| 5 | csi_pixclk high time | T_{HCLK} | — | ns |
| 6 | csi_pixclk low time | T_{HCLK} | — | ns |
| 7 | csi_pixclk frequency | 0 | $HCLK/2$ | MHz |

HCLK = AHB System Clock, THCLK = Period for HCLK, Tp = Period of CSI_PIXCLK

The limitation on pixel clock rise time/fall time is not specified. It should be calculated from the hold time and setup time based on the following assumptions:

Rising-edge latch data:

max rise time allowed = (positive duty cycle—hold time)

max fall time allowed = (negative duty cycle—setup time)

In most of case, duty cycle is 50/50, therefore:

max rise time = (period/2—hold time)

max fall time = (period/2—setup time)

For example: Given pixel clock period = 10 ns, duty cycle = 50/50, hold time = 1 ns, setup time = 1 ns.

positive duty cycle = $10/2 = 5$ ns

max rise time allowed = $5 - 1 = 4$ ns

negative duty cycle = $10/2 = 5$ ns

max fall time allowed = $5 - 1 = 4$ ns

Falling-edge latch data:

max fall time allowed = (negative duty cycle—hold time)

max rise time allowed = (positive duty cycle—setup time)

4.2.5.2 Non-Gated Clock Mode Timing

In non-gated mode only, the VSYNC, and PIXCLK signals are used; the HSYNC signal is ignored.

Figure 11 and Figure 12 show the non-gated clock mode timings of CSI, and Table 22 lists the timing parameters.

Figure 11 shows sensor output data on the pixel clock falling edge. The CSI latches data on the pixel clock rising edge.

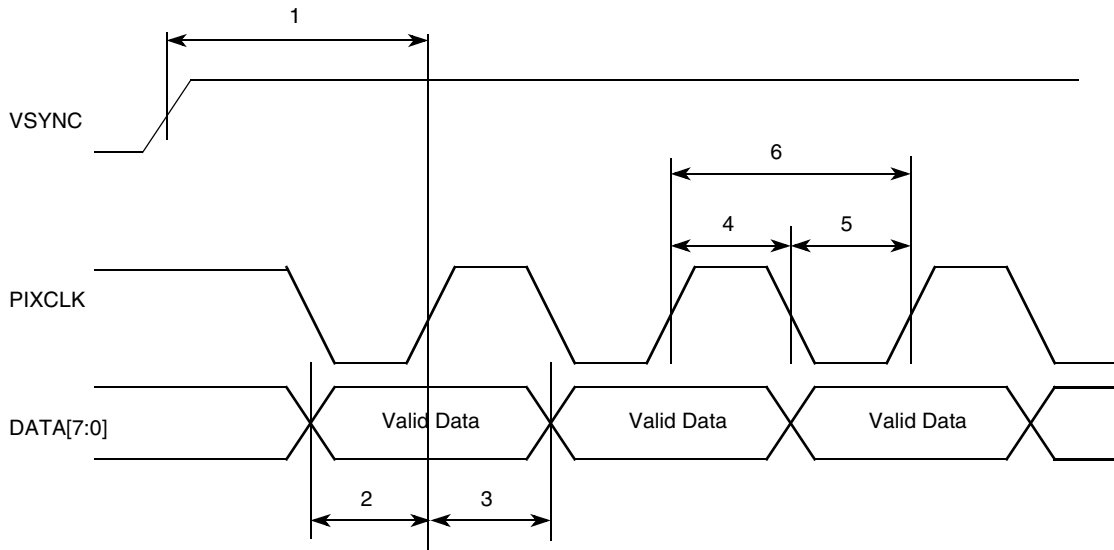


Figure 11. CSI Timing Diagram, Non-Gated, PIXCLK—Sensor Data at Falling Edge, Latch Data at Rising Edge

Figure 12 shows sensor output data on the pixel clock rising edge. The CSI latches data on the pixel clock falling edge.

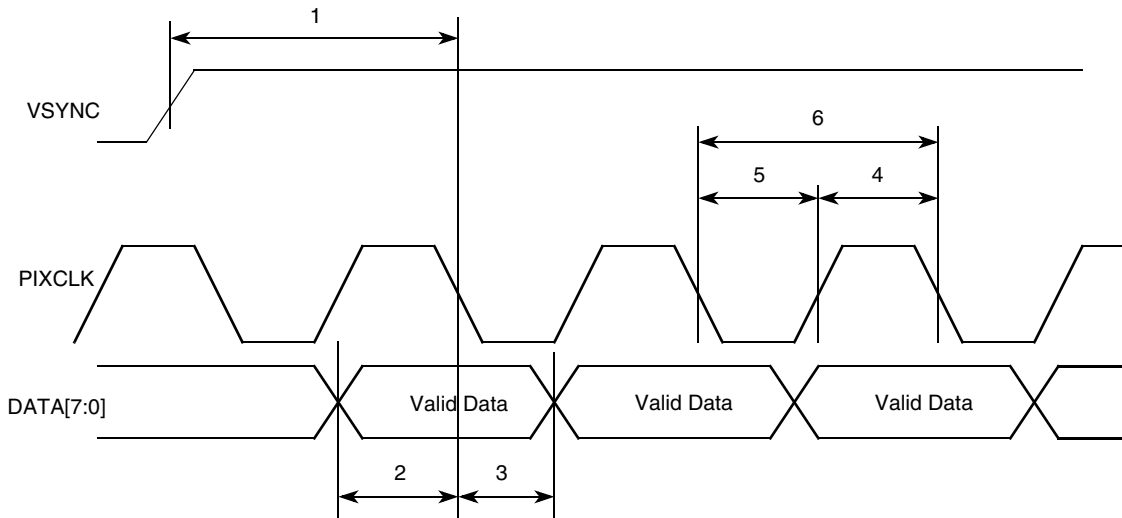


Figure 12. CSI Timing Diagram, Non-Gated, PIXCLK—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 22. Non-Gated Clock Mode Parameters

| Number | Parameter | Minimum | Maximum | Unit |
|--------|-------------------------|--------------------|---------|------|
| — | csi_vsync to csi_pixclk | $9 \cdot T_{HCLK}$ | — | ns |
| — | csi_d setup time | 1 | — | ns |

Table 22. Non-Gated Clock Mode Parameters (continued)

| Number | Parameter | Minimum | Maximum | Unit |
|--------|----------------------|---------|---------|------|
| — | csi_d hold time | 1 | — | ns |
| — | csi_pixclk high time | THCLK | — | ns |
| — | csi_pixclk low time | THCLK | — | ns |
| — | csi_pixclk high time | 0 | HCLK/2 | MHz |

HCLK = AHB System Clock, THCLK = Period of HCLK

4.3 Timing Diagrams

4.3.1 Configurable Serial Peripheral Interface (CSPI)

This section describes the electrical information of the CSPI.

4.3.1.1 CSPI Timing

Figure 13 and Figure 14 depict the master mode and slave mode timing diagrams of the CSPI and Table 23 lists the timing parameters. The values shown in timing diagrams were tested using a worst case core voltage of 1.1 V, slow pad voltage of 2.68 V, and fast pad voltage of 1.65 V.

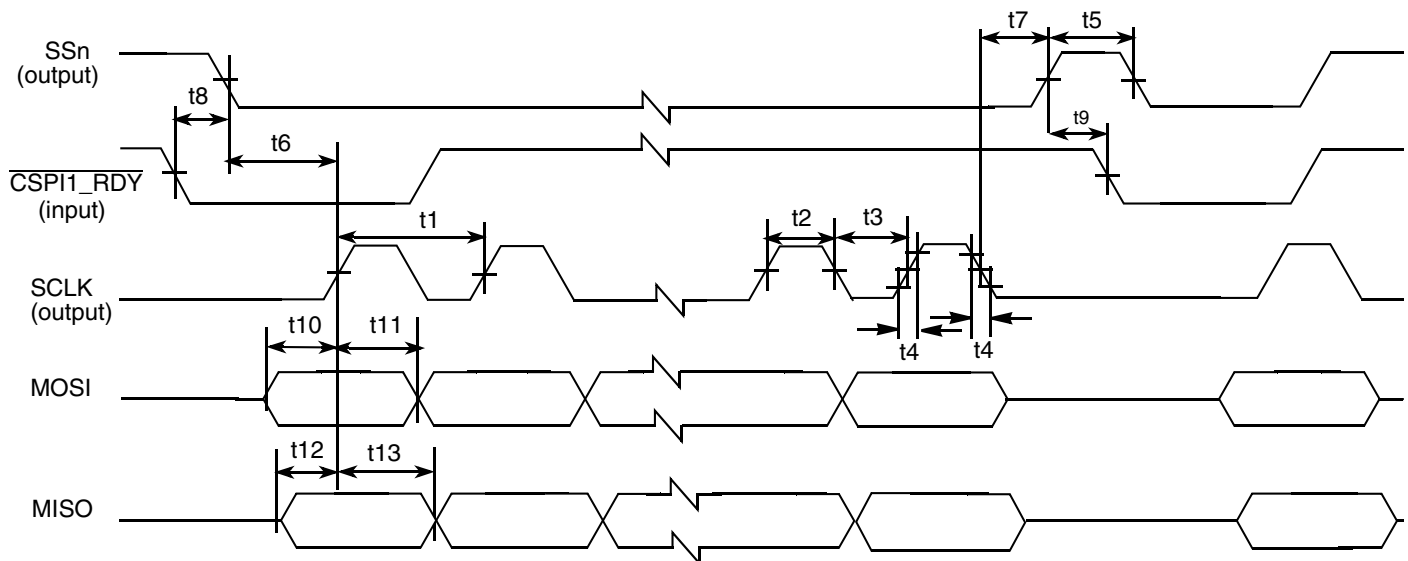


Figure 13. CSPI Master Mode Timing Diagram

Electrical Characteristics

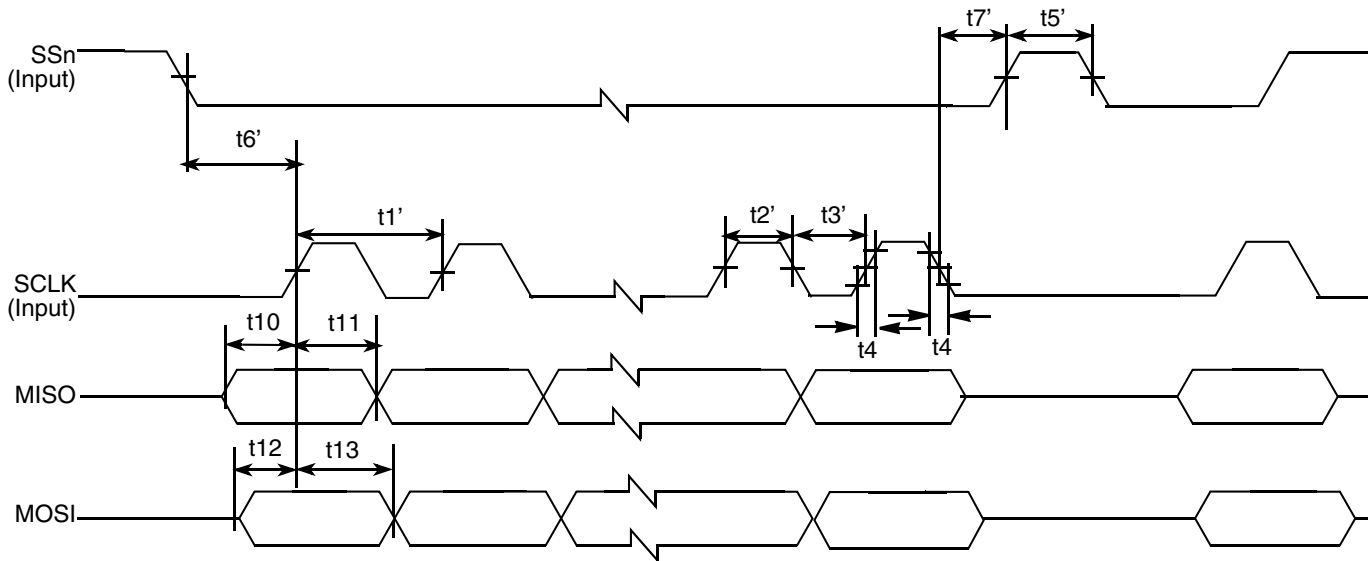


Figure 14. CSPI Slave Mode Timing Diagram

Table 23. CSPI Interface Timing Parameters

| ID Num | Parameter Description | Symbol | Minimum | Maximum | Units |
|--------|---|-------------|----------------------------|------------|-------|
| t1 | CSPI master SCLK cycle time | t_{clko} | 45.12 | — | ns |
| t2 | CSPI master SCLK high time | t_{clkoH} | 22.65 | — | ns |
| t3 | CSPI master SCLK low time | t_{clkoL} | 22.47 | — | ns |
| t1' | CSPI slave SCLK cycle time | t_{clki} | 60.2 | — | ns |
| t2' | CSPI slave SCLK high time | t_{clkiH} | 30.1 | — | ns |
| t3' | CSPI slave SCLK low time | t_{clkiL} | 30.1 | — | ns |
| t4 | CSPI SCLK transition time | t_{pr}^1 | 2.6 | 8.5 | ns |
| t5 | SSn output pulse width | t_{WssO} | $2T_{sclk}^2 + T_{wait}^3$ | — | — |
| t5' | SSn input pulse width | t_{Wssi} | T_{per}^4 | — | — |
| t6 | SSn output asserted to first SCLK edge (SS output setup time) | t_{SssO} | $3T_{sclk}$ | — | — |
| t6' | SSn input asserted to first SCLK edge (SS input setup time) | t_{Sssi} | $T_{per} + 20 \text{ ns}$ | — | — |
| t7 | CSPI master: Last SCLK edge to SSn deasserted (SS output hold time) | t_{HssO} | $2T_{sclk}$ | — | — |
| t7' | CSPI slave: Last SCLK edge to SSn deasserted (SS input hold time) | t_{Hssi} | 30 | — | ns |
| t8 | CSPI master: CSPI1_RDY low to SSn asserted (CSPI1_RDY setup time) | t_{Srdy} | $2T_{per}$ | $5T_{per}$ | — |
| t9 | CSPI master: SSn deasserted to CSPI1_RDY low | t_{Hrdy} | 0 | — | ns |

Table 23. CSPI Interface Timing Parameters (continued)

| ID Num | Parameter Description | Symbol | Minimum | Maximum | Units |
|--------|------------------------|--------------|---|---------|-------|
| t10 | Output data setup time | t_{Sdatao} | $(t_{clkOL} \text{ or } t_{clkOH} \text{ or } t_{clkiL} \text{ or } t_{clkiH}) - T_{ipg}$ | — | — |
| t11 | Output data hold time | t_{Hdatao} | $t_{clkOL} \text{ or } t_{clkOH} \text{ or } t_{clkiL} \text{ or } t_{clkiH}$ | — | — |
| t12 | Input data setup time | t_{Sdatai} | $T_{ipg} + 0.5$ | — | ns |
| t13 | Input data hold time | t_{Hdatai} | 5 | — | ns |

¹ The output SCLK transition time is tested with 25 pF drive.

² T_{sclk} = CSPI clock period.

³ T_{wait} = Wait time as per the Sample Period Control Register value.

⁴ T_{per} = CSPI reference baud rate clock period (PERCLK2).

⁵ T_{ipg} = CSPI main clock IPG_CLOCK period.

4.3.2 Direct Memory Access Controller (DMAC)

After assertion of External DMA Request the DMA burst will start when the corresponding DMA channel becomes the current highest priority channel. The External DMA Request should be kept asserted until it is serviced by the DMAC. One External request will initiate at least one DMA burst.

The output External Grant signal from the DMAC is an active-low signal. This signal will be asserted during the time when a DMA burst is ongoing for an External DMA Request, when the following conditions are true:

- The DMA channel for which the DMA burst is ongoing has requested source as external DMA Request (as per RSSR settings).
- REN and CEN bit of this channel are set.
- External DMA Request is asserted.

Once the grant is asserted the External DMA Request will not be sampled until completion of the DMA burst. The priority of the external request will become low, for the next consecutive burst, if another DMA request signal is asserted.

The waveforms are shown for the worst case—that is, smallest burst (1 byte read/write). Minimum and maximum timings for the External request and External grant signal are present in the data sheet.

Figure 15 shows the minimum time for which the External Grant signal remains asserted if External DMA request is de-asserted immediately after sensing grant signal active.

Electrical Characteristics

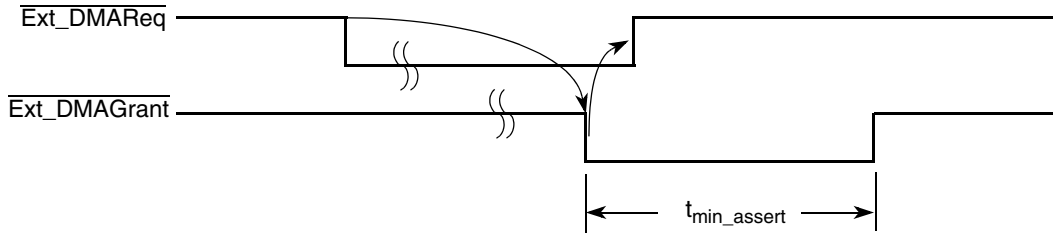
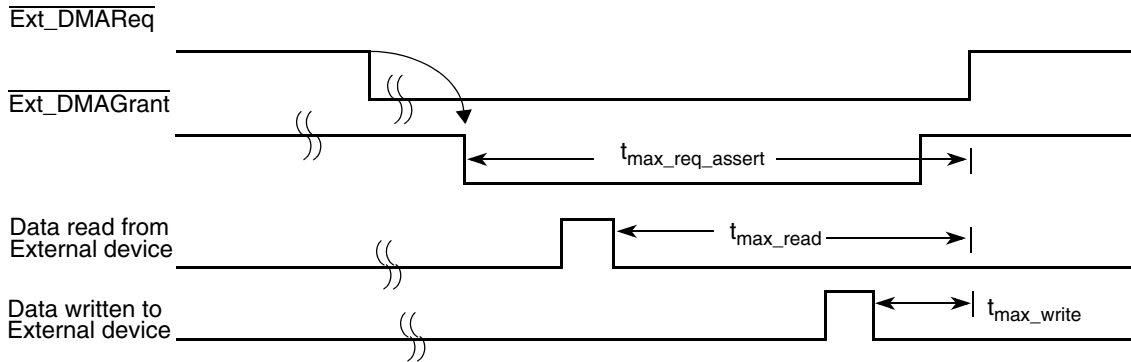


Figure 15. Assertion of DMA External Grant Signal

Figure 16 shows the safe maximum time for which External DMA request can be kept asserted, after sensing grant signal active such that a new burst is not initiated.



NOTE: Assuming worst case that the data is read/written from/to external device as per the above waveform.

Figure 16. Timing Diagram of Safe Maximums for External Request De-Assertion

Table 24. DMAC Timing Parameters

| Parameter | Description | 3.0 V | | 1.8 V | | Unit |
|-----------------------------|---|-------------|------------|-------------|------------|------|
| | | WCS | BCS | WCS | BCS | |
| T _{min_assert} | Minimum assertion time of External Grant signal | 8hclk+8.6 | 8hclk+2.74 | 8hclk+7.17 | 8hclk+3.25 | ns |
| T _{max_req_assert} | Maximum External Request assertion time after assertion of Grant signal | 9hclk-20.66 | 9hclk-6.7 | 9hclk-17.96 | 9hclk-8.16 | ns |
| T _{max_read} | Maximum External Request assertion time after first read completion | 8hclk-6.21 | 8hclk-0.77 | 8hclk-5.84 | 8hclk-0.66 | ns |
| T _{max_write} | Maximum External Request assertion time after first write completion | 3hclk-5.87 | 3hclk-8.83 | 3hclk-15.9 | 3hclkv91.2 | ns |

4.3.3 Fast Ethernet Controller (FEC)

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.3.3.1 MII Receive Signal Timing (FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK)

The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the FEC IPG clock frequency must exceed twice the FEC_RX_CLK frequency.

Figure 17 shows the MII receive signal timings, and Table 25 lists the timing parameters.

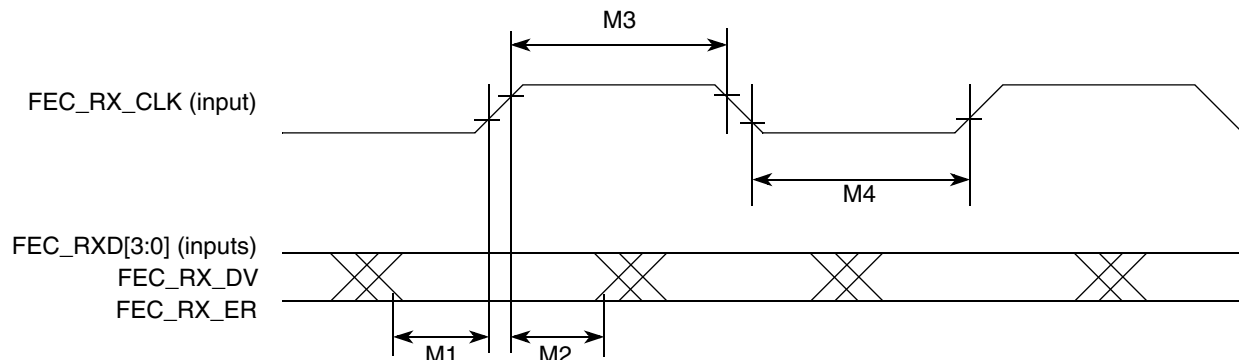


Figure 17. MII Receive Signal Timing Diagram

Table 25. MII Receive Signal Timing Parameters

| ID | Parameter ¹ | Min | Max | Unit |
|----|--|-----|-----|-------------------|
| M1 | FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup | 5 | — | ns |
| M2 | FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold | 5 | — | ns |
| M3 | FEC_RX_CLK pulse width high | 35% | 65% | FEC_RX_CLK period |
| M4 | FEC_RX_CLK pulse width low | 35% | 65% | FEC_RX_CLK period |

¹ FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.3.3.2 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK)

The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the FEC IPG clock frequency must exceed twice the FEC_TX_CLK frequency.

Figure 18 shows the MII transmit signal timings, and Table 26 lists the timing parameters.

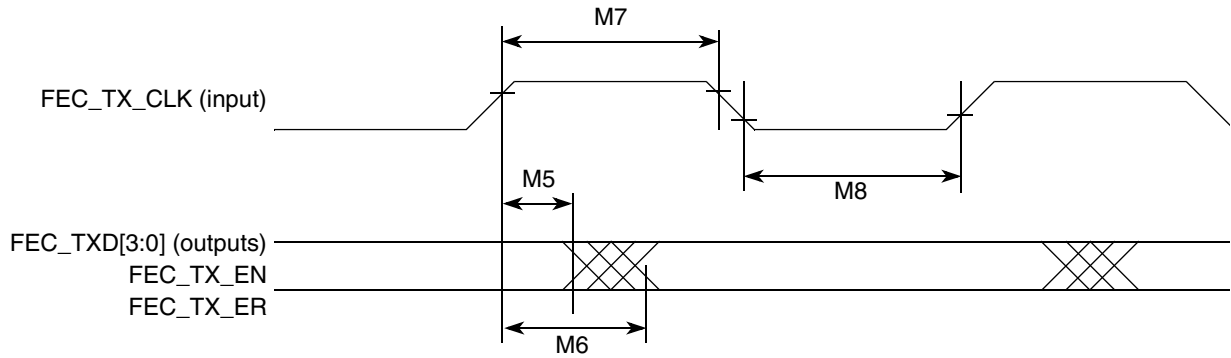


Figure 18. MII Transmit Signal Timing Diagram

Table 26. MII Transmit Signal Timing Parameters

| ID | Parameter ¹ | Min | Max | Unit |
|----|--|-----|-----|-------------------|
| M5 | FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid | 5 | — | ns |
| M6 | FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid | — | 20 | ns |
| M7 | FEC_TX_CLK pulse width high | 35% | 65% | FEC_TX_CLK period |
| M8 | FEC_TX_CLK pulse width low | 35% | 65% | FEC_TX_CLK period |

¹ FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.3.3.3 MII Asynchronous Inputs Signal Timing (FEC_CRIS and FEC_COL)

Figure 19 shows the MII asynchronous input timings, and Table 27 lists the timing parameters.

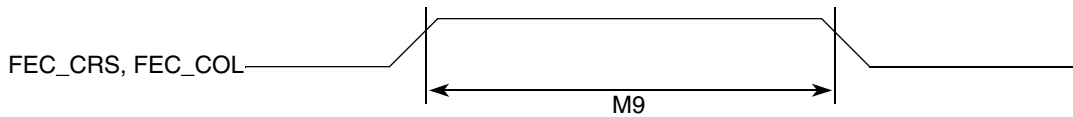


Figure 19. MII Asynchronous Inputs Signal Timing Diagram

Table 27. MII Asynchronous Inputs Signal Timing Parameter

| ID | Parameter | Min | Max | Unit |
|-----------------|---|-----|-----|-------------------|
| M9 ¹ | FEC_CRIS to FEC_COL minimum pulse width | 1.5 | — | FEC_TX_CLK period |

¹ FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

4.3.3.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Figure 20 shows the MII serial management channel timings, and Table 28 lists the timing parameters.

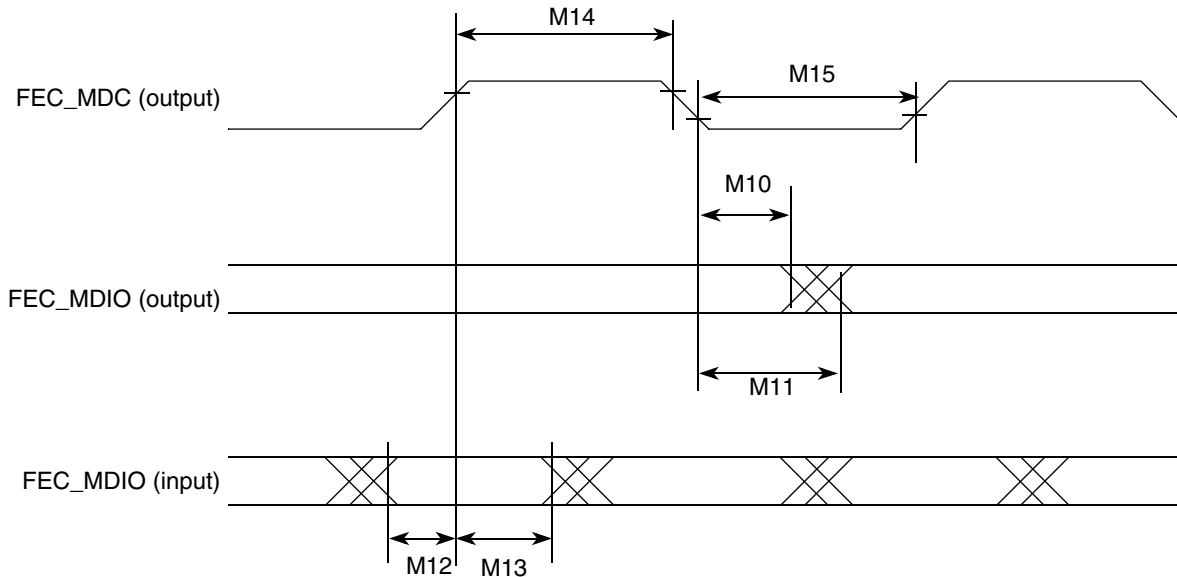


Figure 20. MII Serial Management Channel Timing Diagram

Table 28. MII Serial Management Channel Timing Parameters

| ID | Parameter | Min | Max | Unit |
|-----|---|-----|-----|----------------|
| M10 | FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay) | — | 5 | ns |
| M12 | FEC_MDIO (input) to FEC_MDC rising edge setup | 18 | — | ns |
| M13 | FEC_MDIO (input) to FEC_MDC rising edge hold | 0 | — | ns |
| M14 | FEC_MDC pulse width high | 40% | 60% | FEC_MDC period |
| M15 | FEC_MDC pulse width low | 40% | 60% | FEC_MDC period |

4.3.4 Inter IC Communication (I²C)

This section describes the electrical information of the I²C module.

4.3.4.1 I²C Module Timing

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP. Figure 21 shows the timing of the I²C module. Table 29 lists the I²C module timing parameters.

Electrical Characteristics

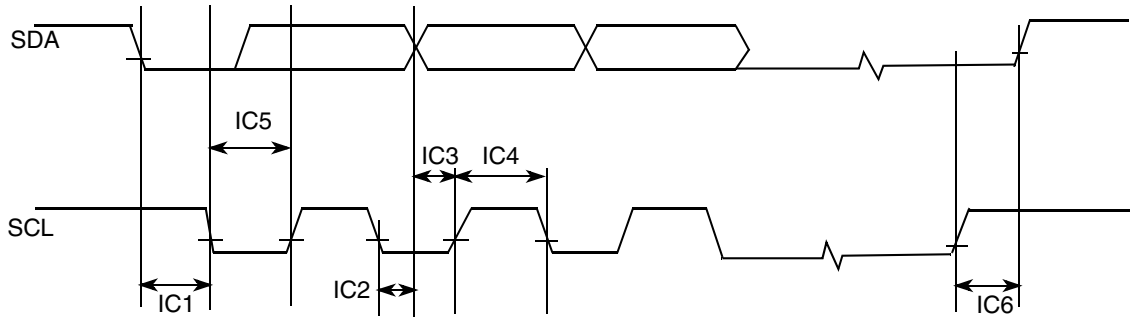


Figure 21. I²C Bus Timing Diagram

Table 29. I²C Module Timing Parameters

| ID | Parameter | 1.8 V \pm 0.10 V | | 3.0 V \pm 0.30 V | | Unit |
|-----|--------------------------------------|--------------------|------|--------------------|------|------|
| | | Min | Max | Min | Max | |
| — | SCL Clock Frequency | 0 | 100 | 0 | 100 | kHz |
| IC1 | Hold time (repeated) START Condition | 114.8 | — | 111.1 | — | ns |
| IC2 | Data Hold Time | 0 | 69.7 | 0 | 72.3 | ns |
| IC3 | Data Setup Time | 3.1 | — | 1.76 | — | ns |
| IC4 | HIGH period of the SCL clock | 69.7 | — | 68.3 | — | ns |
| IC5 | LOW period of the SCL clock | 336.4 | — | 335.1 | — | ns |
| IC6 | Setup Time for STOP condition | 110.5 | — | 111.1 | — | ns |

4.3.5 JTAG Controller (JTAGC)

This section details the electrical characteristics for the JTAGC module. [Figure 22](#) shows the JTAGC test clock input timing; [Figure 23](#) shows the JTAGC boundary scan timing; [Figure 24](#) shows the JTAGC test access port; [Figure 25](#) shows the JTAGC TRST timing; and [Table 30](#) lists the JTAGC timing parameters.

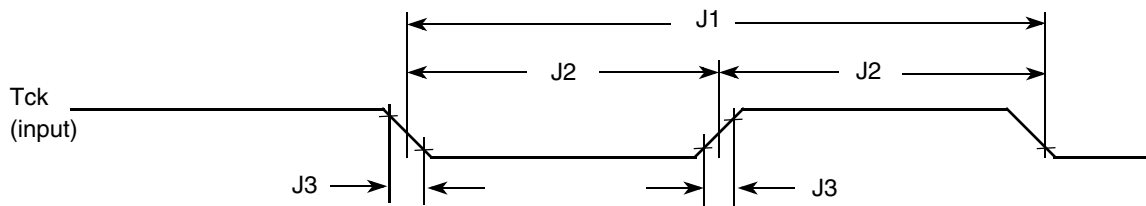


Figure 22. Test Clock Input Timing Diagram

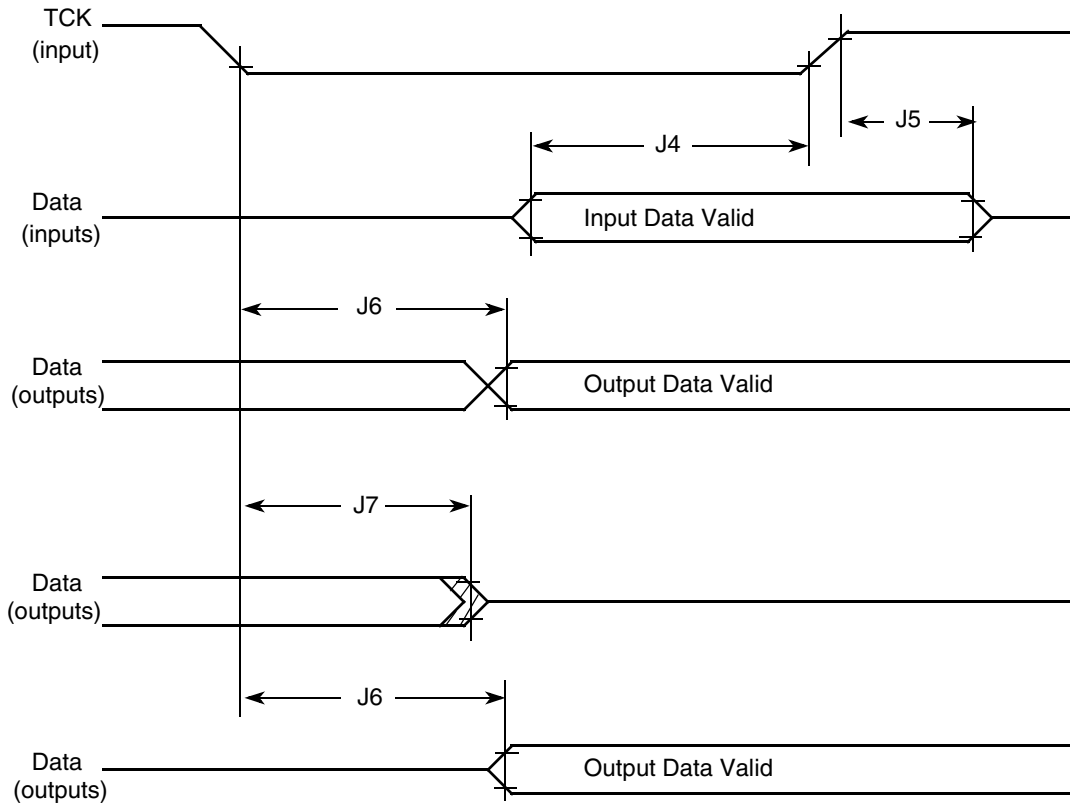


Figure 23. Boundary Scan Timing Diagram

Electrical Characteristics

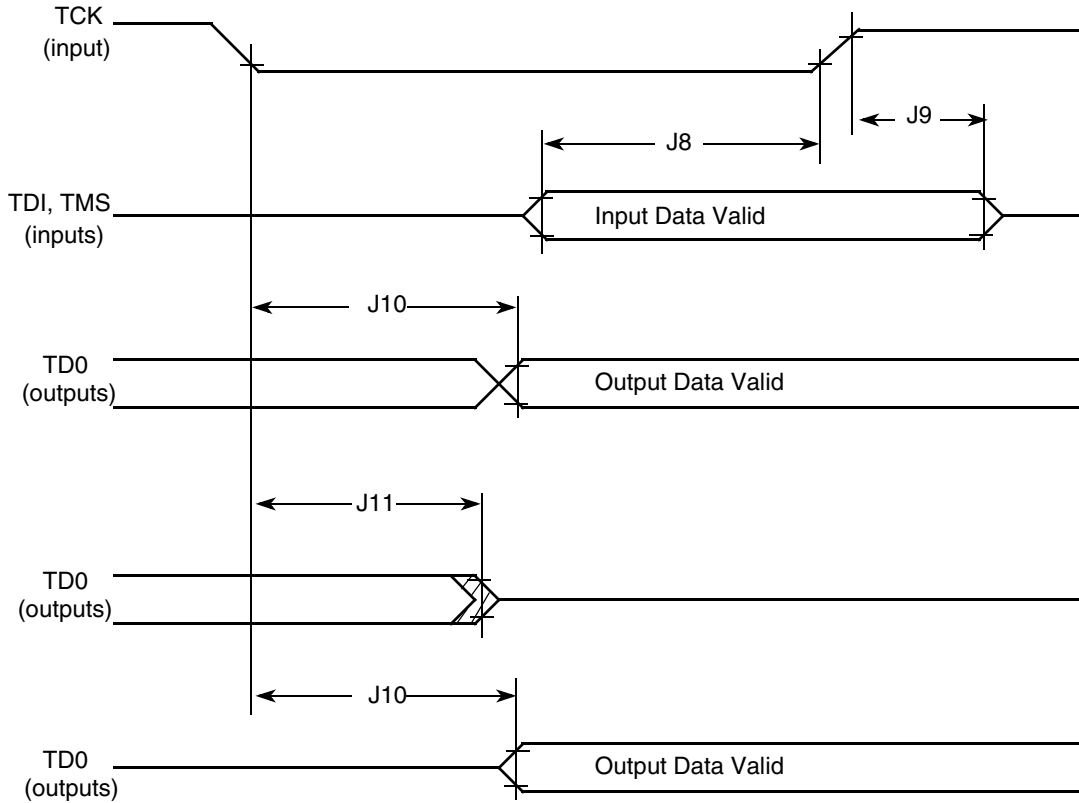


Figure 24. Test Access Port (TAP) Diagram

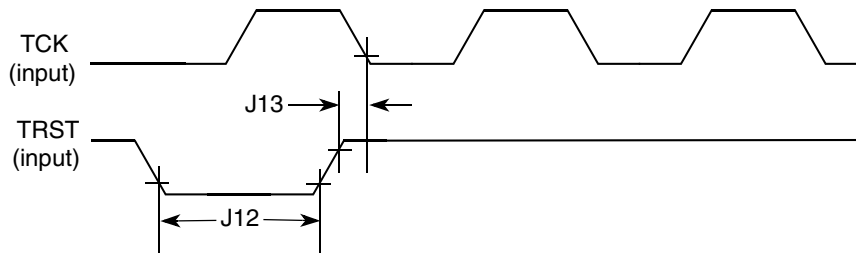


Figure 25. TRST Timing Diagram

Table 30. JTAGC Timing Parameters

| ID | Parameter | All Frequencies | | Unit |
|----|---|-----------------|-----|------|
| | | Min | Max | |
| J1 | TCK cycle time in crystal mode | 30.08 | — | ns |
| J2 | TCK clock pulse width measured at VM ¹ | 15.04 | — | ns |
| J3 | TCK rise and fall times | — | 2.0 | ns |
| J4 | Boundary scan input data set-up time | 3.5 | — | ns |
| J5 | Boundary scan input data hold time | 16.0 | — | ns |

Table 30. JTAGC Timing Parameters (continued)

| ID | Parameter | All Frequencies | | Unit |
|-----|----------------------------------|-----------------|------|------|
| | | Min | Max | |
| J6 | TCK low to output data valid | — | 25.0 | ns |
| J7 | TCK low to output high impedance | — | 25.0 | ns |
| J8 | TMS, TDI data set-up time | 3.5 | — | ns |
| J9 | TMS, TDI data hold time | 20.0 | — | ns |
| J10 | TCK low to TDO data valid | — | 29.0 | ns |
| J11 | TCK low to TDO high impedance | — | 29.0 | ns |
| J12 | TRST assert time | 70.0 | — | ns |
| J13 | TRST set-up time to TCK low | 2.5.0 | — | ns |

¹ Midpoint voltage

4.3.6 Liquid Crystal Display Controller Module (LCDC)

Figure 26 and Figure 27 depict the timings of the LCDC, and Table 31 and Table 32 list the timing parameters.

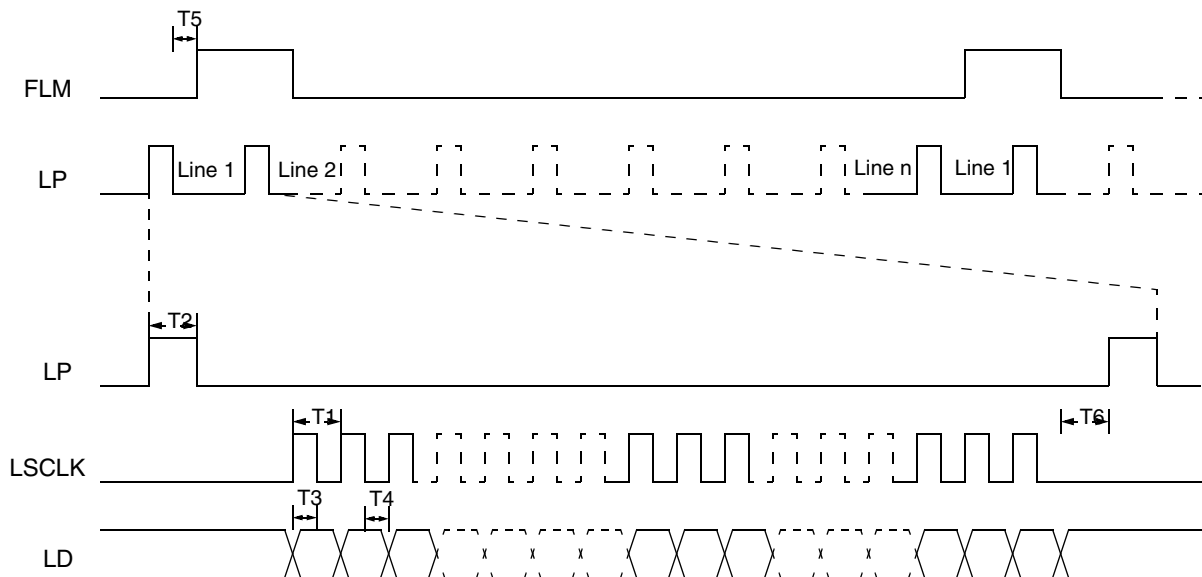


Figure 26. LCDC Non-TFT Mode Timing Diagram

Table 31. LCDC Non-TFT Mode Timing Parameters

| ID | Description | Min | Max | Unit |
|----|--------------------|------|------|----------------|
| T1 | Pixel Clock period | 22.5 | 1000 | ns |
| T2 | LP width | 1 | — | T ¹ |

Table 31. LCDC Non-TFT Mode Timing Parameters (continued)

| ID | Description | Min | Max | Unit |
|----|---|-----|-----|----------------|
| T3 | LD setup time | 5 | — | ns |
| T4 | LD hold time | 5 | — | ns |
| T5 | Wait between LP and FLM rising edge | 2 | — | T ¹ |
| T6 | Wait between last data and LP rising edge | 1 | — | T ¹ |

¹ T is pixel clock period.

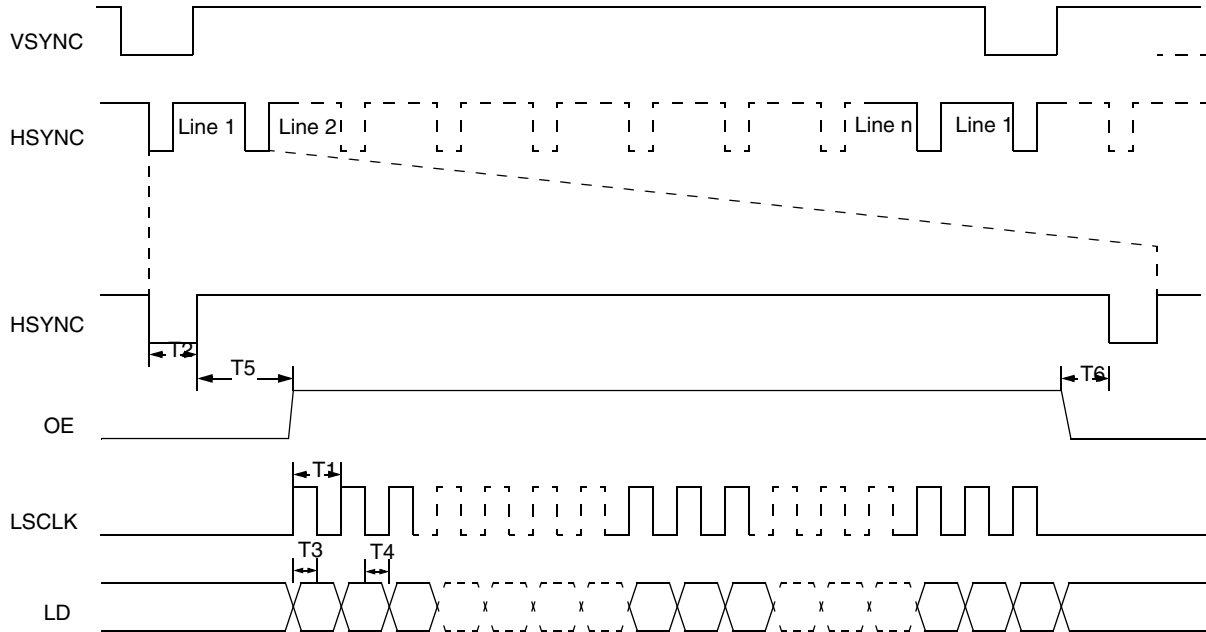


Figure 27. LCDC TFT Mode Timing Diagram

Table 32. LCDC TFT Mode Timing Parameters

| ID | Description | Min | Max | Unit |
|----|---|------|------|----------------|
| T1 | Pixel Clock period | 22.5 | 1000 | ns |
| T2 | HSYNC width | 1 | — | T ¹ |
| T3 | LD setup time | 5 | — | ns |
| T4 | LD hold time | 5 | — | ns |
| T5 | Delay from the end of HSYNC to the beginning of the OE pulse. | 3 | — | T ¹ |
| T6 | Delay from end of OE to the beginning of the HSYNC pulse. | 1 | — | T ¹ |

¹ T is pixel clock period.

4.3.7 Memory Stick Host Controller (MSHC)

Figure 28, Figure 29, and Figure 30, show the MSHC timings. Table 33 and Table 34 list the timing parameters.

NOTE

The i.MX27L does not contain an MSHC module.

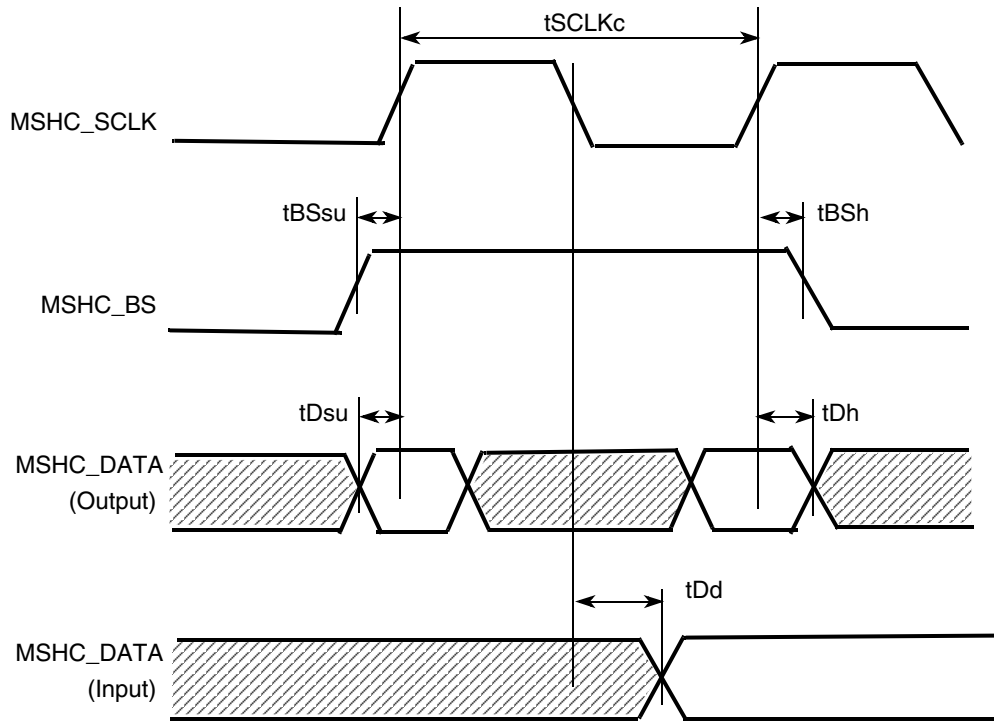


Figure 28. Transfer Operation Timing Diagram (Serial)

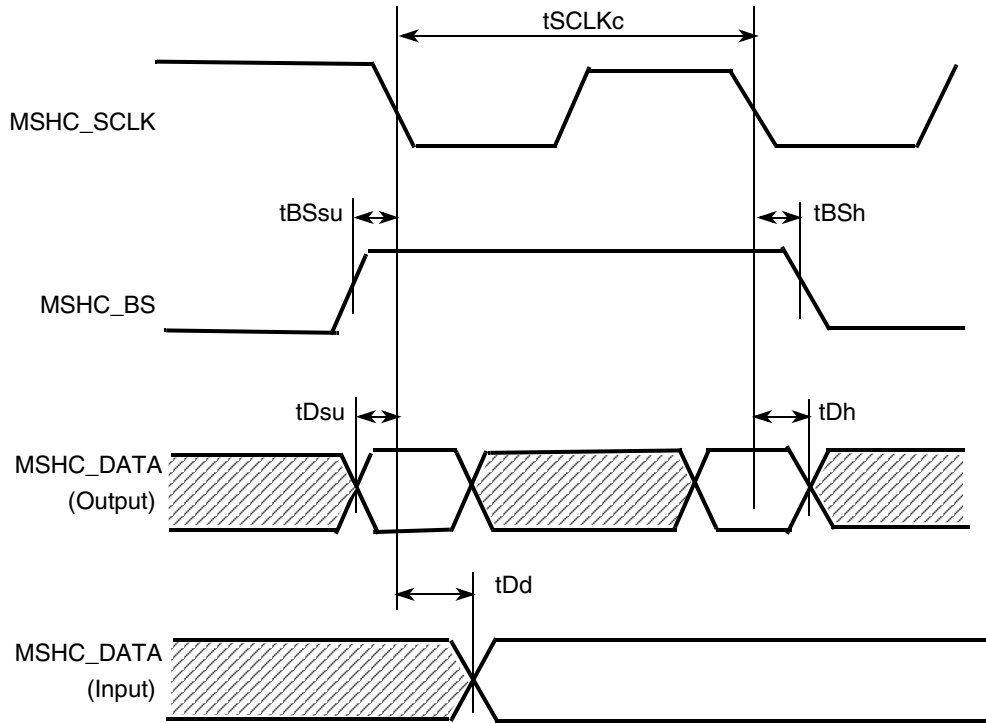


Figure 29. Transfer Operation Timing Diagram (Parallel)

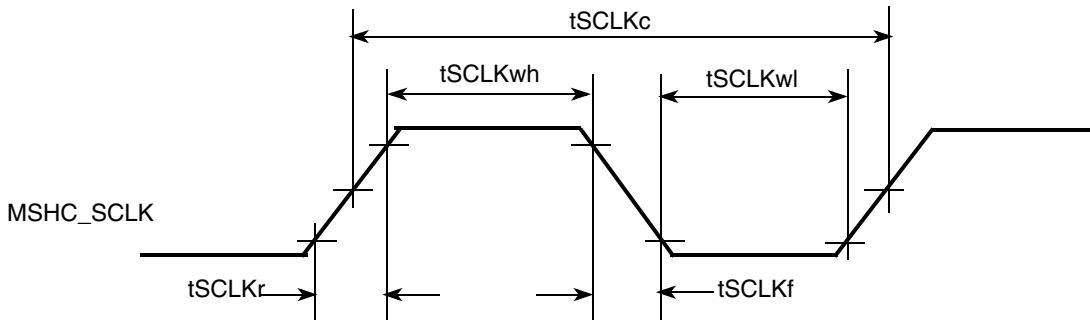


Figure 30. MSHC_CLK Timing Diagram

Table 33. Serial Interface Timing Parameters

| Signal | Parameter | Symbol | Standards | | Unit |
|-----------|----------------|---------|-----------|-----|------|
| | | | Min | Max | |
| MSHC_SCLK | Cycle | tSCLKc | 50 | — | ns |
| | H pulse length | tSCLKwh | 15 | — | ns |
| | L pulse length | tSCLKwl | 15 | — | ns |
| | Rise time | tSCLKr | — | 10 | ns |
| | Fall time | tSCLKf | — | 10 | ns |

Table 33. Serial Interface Timing Parameters (continued)

| Signal | Parameter | Symbol | Standards | | Unit |
|-----------|-------------------|--------|-----------|-----|------|
| | | | Min | Max | |
| MSHC_BS | Setup time | tBSsu | 5 | — | ns |
| | Hold time | tBSh | 5 | — | ns |
| MSHC_DATA | Setup time | tDsu | 5 | — | ns |
| | Hold time | tDh | 5 | — | ns |
| | Output delay time | tDd | — | 15 | ns |

Table 34. Parallel Interface Timing Parameters

| Signal | Parameter | Symbol | Standards | | Unit |
|-----------|-------------------|---------|-----------|-----|------|
| | | | Min | Max | |
| MSHC_SCLK | Cycle | tSCLKc | 25 | — | ns |
| | H pulse length | tSCLKwh | 5 | — | ns |
| | L pulse length | tSCLKwl | 5 | — | ns |
| | Rise time | tSCLKr | — | 10 | ns |
| | Fall time | tSCLKf | — | 10 | ns |
| MSHC_BS | Setup time | tBSsu | 8 | — | ns |
| | Hold time | tBSh | 1 | — | ns |
| MSHC_DATA | Setup time | tDsu | 8 | — | ns |
| | Hold time | tDh | 1 | — | ns |
| | Output delay time | tDd | — | 15 | ns |

4.3.8 NAND Flash Controller Interface (NFC)

Figure 31, Figure 32, Figure 33, and Figure 34 show the relative timing requirements among different signals of the NFC at module level, and Table 35 lists the timing parameters. The NAND Flash Controller (NFC) timing parameters are based on the internal NFC clock generated by the Clock Controller module, where time T is the period of the NFC clock in ns. The relationship between the NFC clock and the external timing parameters of the NFC is provided in Table 35.

Table 35 also provides two examples of external timing parameters with NFC clock frequencies of 22.17 MHz and 33.25 MHz. Assuming a 266 MHz FCLK (CPU clock), NFCDIV should be set to divide-by-12 to generate a 22.17 MHz NFC clock and divide-by-8 to generate a 33.25 MHz NFC clock. The user should compare the parameters of the selected NAND Flash memory with the NFC external timing parameters to determine the proper NFC clock. The maximum NFC clock allowed is 66 MHz. It should also be noted that the default NFC clock on power up is 16.63 MHz.

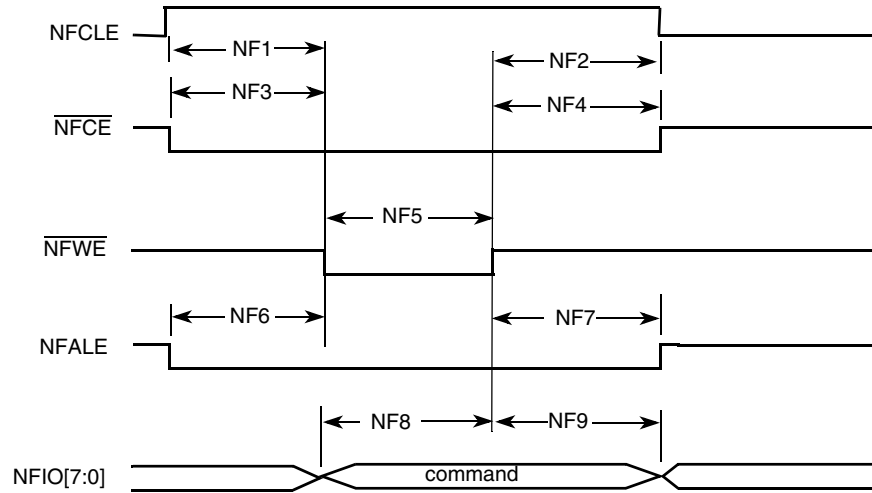


Figure 31. Command Latch Cycle Timing Diagram

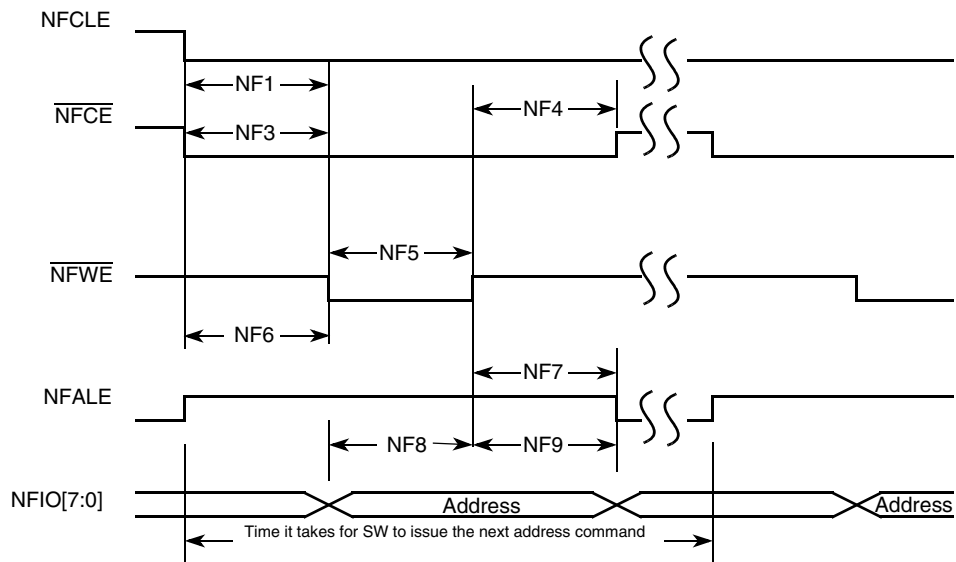


Figure 32. Address Latch Cycle Timing Diagram

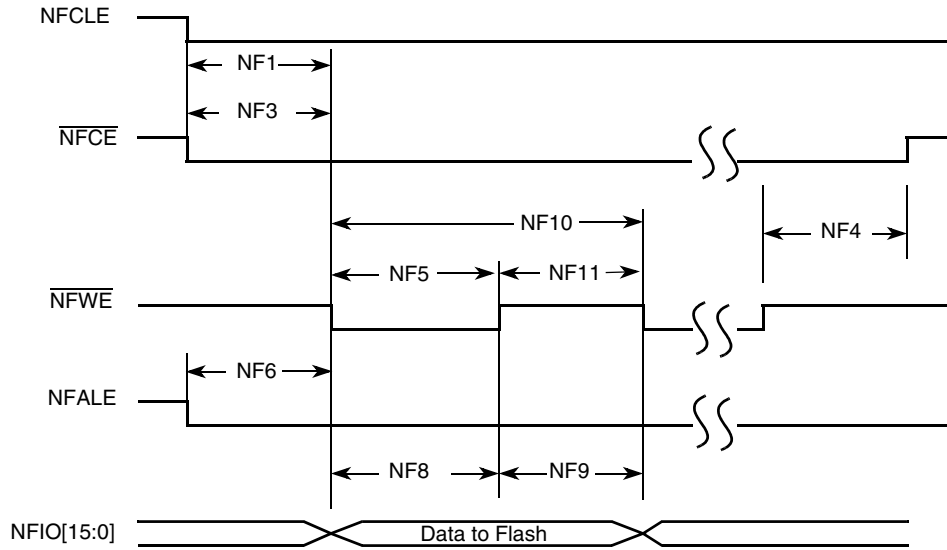


Figure 33. Write Data Latch Timing Diagram

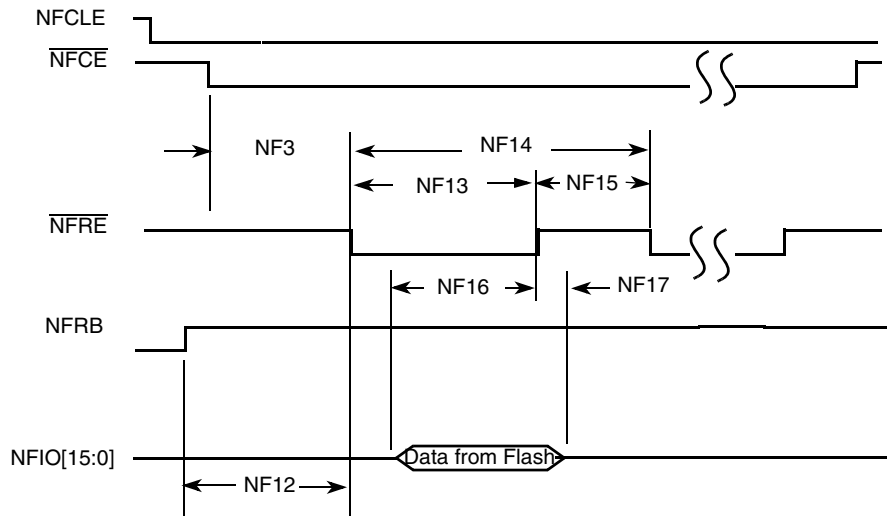


Figure 34. Read Data Latch Timing Diagram

Table 35. NFC Target Timing Parameters

| ID | Parameter | Symbol | Relationship to NFC clock period (T) | | NFC clock 22.17 MHz T = 45 ns | | NFC clock 33.25 MHz T = 30 ns | | Unit |
|-----|--|--------|--------------------------------------|-----|----------------------------------|-----|----------------------------------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| NF1 | NFCLE Setup Time | tCLS | T | — | 45 | — | 30 | — | ns |
| NF2 | NFCLE Hold Time | tCLH | T | — | 45 | — | 30 | — | ns |
| NF3 | $\overline{\text{NFCE}}$ Setup Time | tCS | T | — | 45 | — | 30 | — | ns |
| NF4 | $\overline{\text{NFCE}}$ Hold Time | tCH | T | — | 45 | — | 30 | — | ns |
| NF5 | $\overline{\text{NF_WP}}$ Pulse Width | tWP | T | — | 45 | — | 30 | — | ns |

Table 35. NFC Target Timing Parameters (continued)

| ID | Parameter | Symbol | Relationship to NFC clock period (T) | | NFC clock 22.17 MHz T = 45 ns | | NFC clock 33.25 MHz T = 30 ns | | Unit |
|------|---|--------|--------------------------------------|-----|----------------------------------|-----|----------------------------------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| NF6 | NFALE Setup Time | tALS | T | — | 45 | — | 30 | — | ns |
| NF7 | NFALE Hold Time | tALH | T | — | 45 | — | 30 | — | ns |
| NF8 | Data Setup Time | tDS | T | — | 45 | — | 30 | — | ns |
| NF9 | Data Hold Time | tDH | T | — | 45 | — | 30 | — | ns |
| NF10 | Write Cycle Time | tWC | 2T | — | 90 | — | 60 | — | ns |
| NF11 | $\overline{\text{NFW}}\overline{\text{E}}$ Hold Time | tWH | T | — | 45 | — | 30 | — | ns |
| NF12 | Ready to $\overline{\text{NFR}}\overline{\text{E}}$ Low | tRR | 4T | — | 180 | — | 120 | — | ns |
| NF13 | $\overline{\text{NFR}}\overline{\text{E}}$ Pulse Width | tRP | 1.5T | — | 67.5 | — | 45 | — | ns |
| NF14 | READ Cycle Time | tRC | 2T | — | 90 | — | 60 | — | ns |
| NF15 | $\overline{\text{NFR}}\overline{\text{E}}$ High Hold Time | tREH | 0.5T | — | 22.5 | — | 15 | — | ns |
| NF16 | Data Setup on READ | tDSR | 15 | — | 15 | — | 15 | — | ns |
| NF17 | Data Hold on READ | tDHR | 0 | — | 0 | — | 0 | — | ns |

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value. All timings are listed according to this NFC clock frequency (multiples of NFC clock period) except NF16, which is not NFC clock related.

The read data is generated by the NAND Flash device and sampled with the internal NFC clock.

4.3.9 Personal Computer Memory Card International Association (PCMCIA)

Figure 35 and Figure 36 show the timings pertaining to the PCMCIA module, each of which is an example of one clock of strobe setup time and one clock of strobe hold time. Table 36 lists the timing parameters.

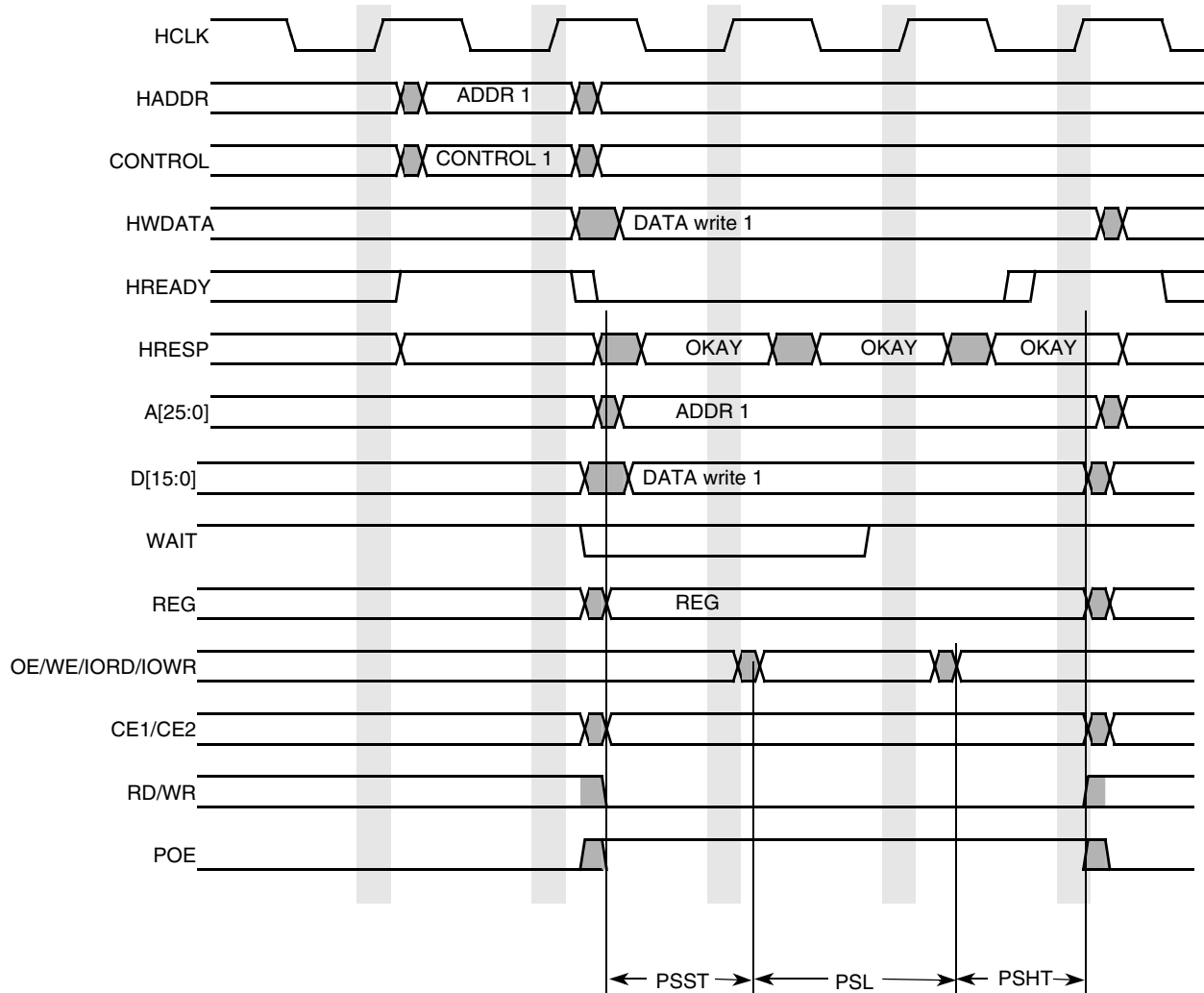


Figure 35. Write Accesses Timing Diagram—PSHT=1, PSST=1

Electrical Characteristics

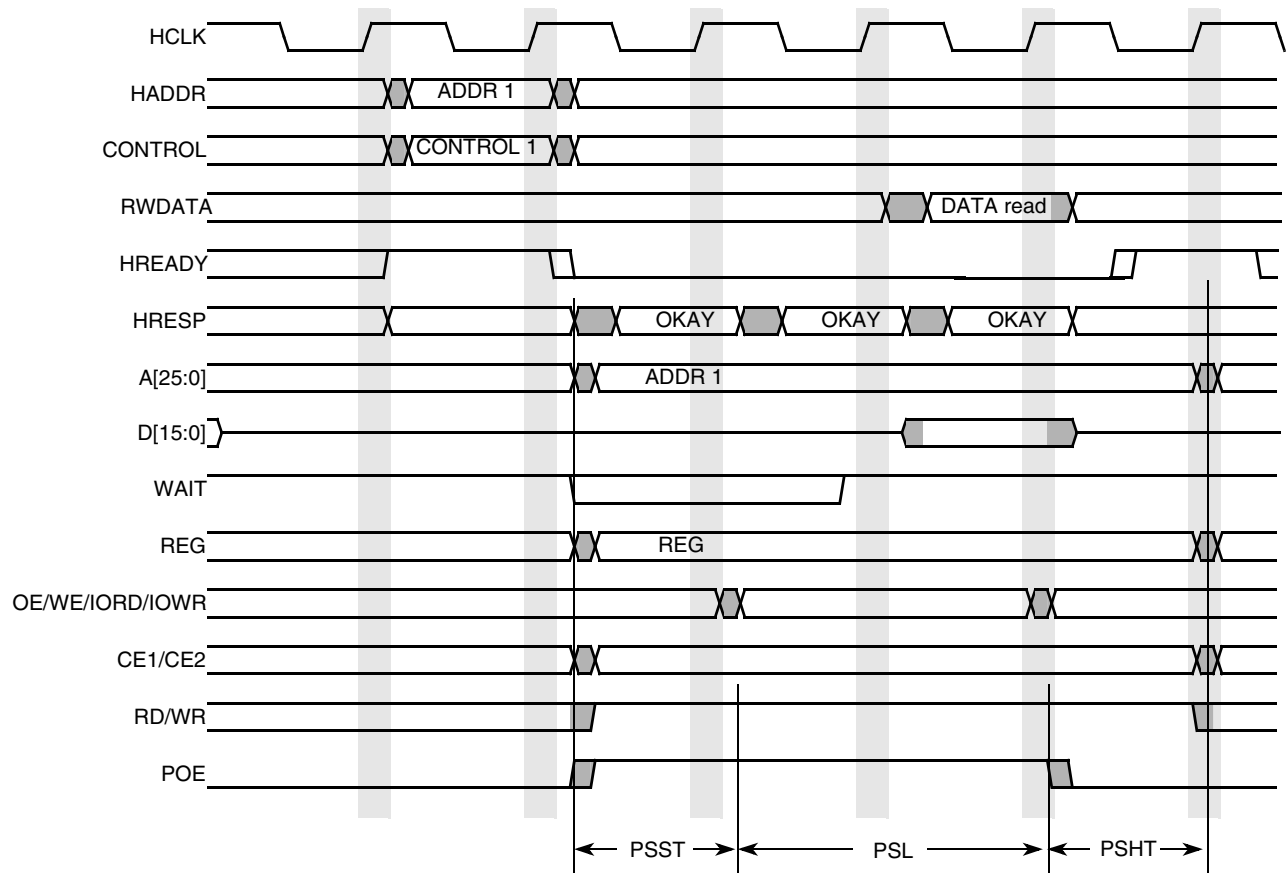


Figure 36. Read Accesses Timing Diagram—PSHT=1, PSST=1

Table 36. PCMCIA Write and Read Timing Parameters

| Symbol | Parameter | Min | Max | Unit |
|--------|---------------------------|-----|-----|-------|
| PSHT | PCMCIA strobe hold time | 0 | 63 | clock |
| PSST | PCMCIA strobe set up time | 1 | 63 | clock |
| PSL | PCMCIA strobe length | 1 | 128 | clock |

4.3.10 SDRAM (DDR and SDR) Memory Controller

Figure 37, Figure 38, Figure 39, Figure 40, Figure 41, and Figure 42 depict the timings pertaining to the ESDCTL module, which interfaces Mobile DDR or SDR SDRAM. Table 37, Table 38, Table 39, Table 40, Table 41, and Table 42 list the timing parameters.

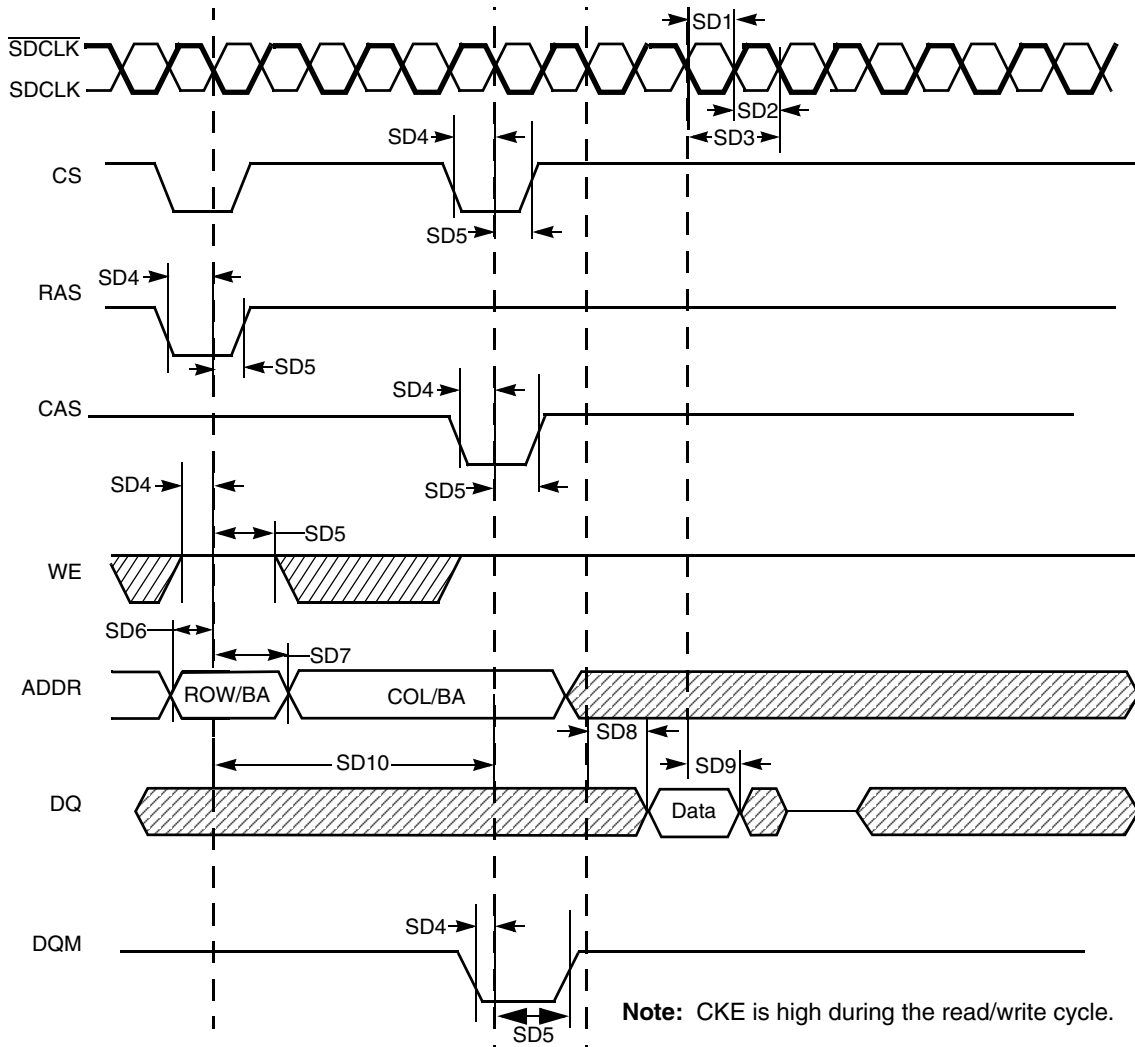


Figure 37. SDRAM Read Cycle Timing Diagram

Table 37. DDR/SDR SDRAM Read Cycle Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---------------------------------------|--------|-----|-----|------|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | SDRAM clock low-level width | tCL | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | tCMS | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | tCMH | 1.8 | — | ns |

Table 37. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

| ID | Parameter | Symbol | Min | Max | Unit |
|------|-------------------------------------|--------|-----|------|-------|
| SD6 | Address setup time | tAS | 2.0 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD8 | SDRAM access time | tAC | — | 6.47 | ns |
| SD9 | Data out hold time ¹ | tOH | 1.8 | — | ns |
| SD10 | Active to read/write command period | tRC | 10 | — | clock |

¹ Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see [Table 41](#) and [Table 42](#).

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, [Table 37](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

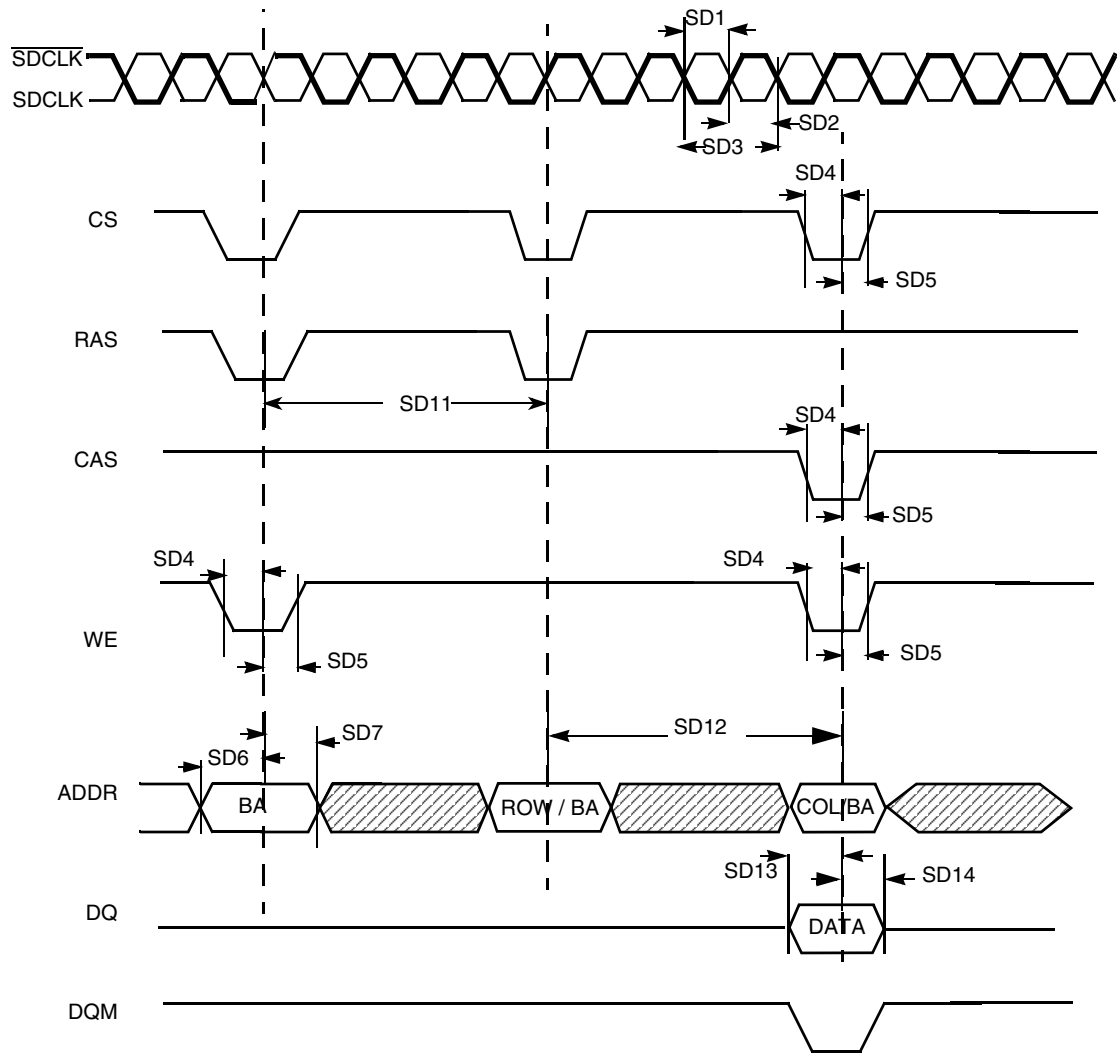


Figure 38. SDR SDRAM Write Cycle Timing Diagram

Table 38. SDR SDRAM Write Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|---|------------------|-----|-----|-------|
| SD1 | SDRAM clock high-level width | t _{CH} | 3.4 | 4.1 | ns |
| SD2 | SDRAM clock low-level width | t _{CL} | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | t _{CK} | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | t _{CMS} | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | t _{CMH} | 1.8 | — | ns |
| SD6 | Address setup time | t _{AS} | 2.0 | — | ns |
| SD7 | Address hold time | t _{AH} | 1.8 | — | ns |
| SD11 | Precharge cycle period ¹ | t _{RP} | 1 | 4 | clock |
| SD12 | Active to read/write command delay ¹ | t _{RCD} | 1 | 8 | clock |

Table 38. SDR SDRAM Write Timing Parameters (continued)

| ID | Parameter | Symbol | Min | Max | Unit |
|------|-----------------|-----------------|-----|-----|------|
| SD13 | Data setup time | t _{DS} | 2.0 | — | ns |
| SD14 | Data hold time | t _{DH} | 1.3 | — | ns |

¹ SD11 and SD12 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 38 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

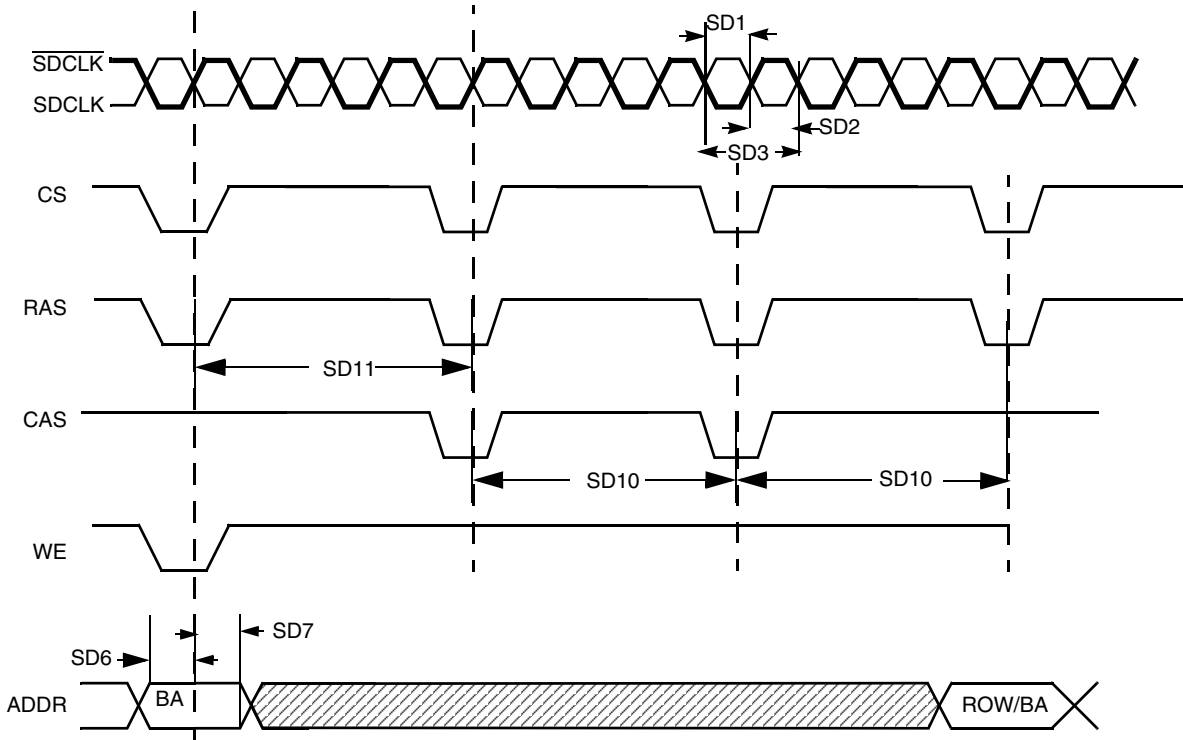


Figure 39. SDRAM Refresh Timing Diagram

Table 39. SDRAM Refresh Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|------------------------------|-----------------|-----|-----|------|
| SD1 | SDRAM clock high-level width | t _{CH} | 3.4 | 4.1 | ns |
| SD2 | SDRAM clock low-level width | t _{CL} | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | t _{CK} | 7.5 | — | ns |

Table 39. SDRAM Refresh Timing Parameters (continued)

| ID | Parameter | Symbol | Min | Max | Unit |
|------|--|--------|-----|-----|-------|
| SD6 | Address setup time | tAS | 1.8 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD10 | Precharge cycle period ¹ | tRP | 1 | 4 | clock |
| SD11 | Auto precharge command period ¹ | tRC | 2 | 20 | clock |

¹ SD10 and SD11 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 39 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

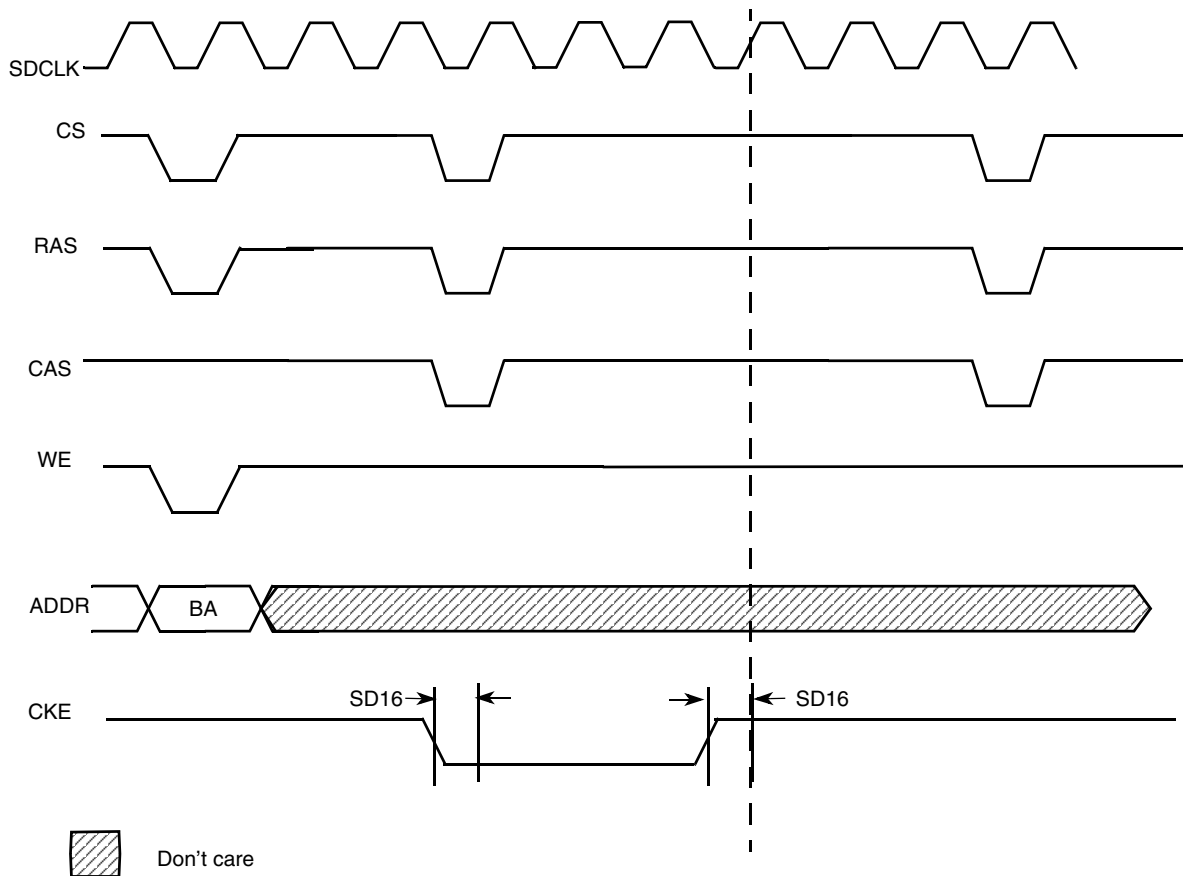


Figure 40. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock continues to run unless both CKEs are low. Then the clock is stopped in low state.

Table 40. SDRAM Self-Refresh Cycle Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|-----------------------|--------|-----|-----|------|
| SD16 | CKE output delay time | tCKS | 1.8 | — | ns |

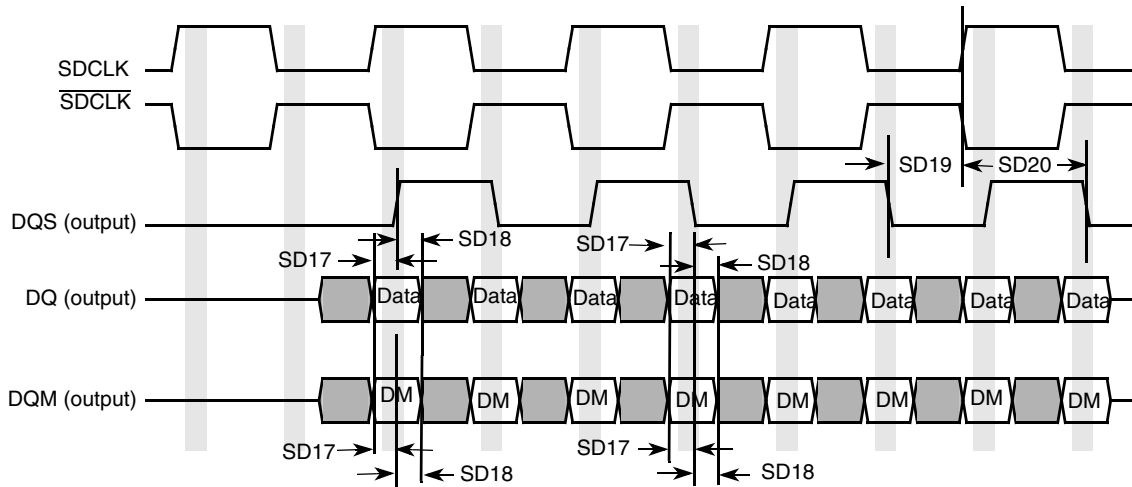


Figure 41. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 41. Mobile DDR SDRAM Write Cycle Timing Parameters¹

| ID | Parameter | Symbol | Min | Max | Unit |
|------|--|--------|------|-----|------|
| SD17 | DQ and DQM setup time to DQS | tDS | 0.95 | — | ns |
| SD18 | DQ and DQM hold time to DQS | tDH | 0.95 | — | ns |
| SD19 | Write cycle DQS falling edge to SDCLK output delay time. | tDSS | 1.8 | — | ns |
| SD20 | Write cycle DQS falling edge to SDCLK output hold time. | tDSH | 1.8 | — | ns |

¹ Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, [Table 41](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

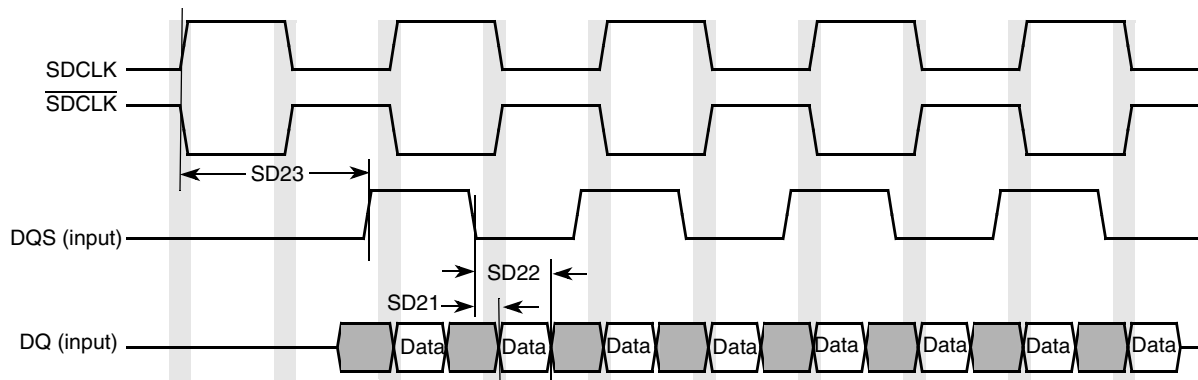


Figure 42. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 42. Mobile DDR SDRAM Read Cycle Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|--|--------|-----|------|------|
| SD21 | DQS–DQ Skew (defines the Data valid window in read cycles related to DQS). | tDQSQ | — | 0.85 | ns |
| SD22 | DQS DQ HOLD time from DQS | tQH | 2.3 | — | ns |
| SD23 | DQS output access time from SDCLK posedge | tDQSK | — | 6.7 | ns |

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, [Table 42](#) indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.10.1 SDHC Electrical DC Characteristics

[Table 43](#) lists the SDHC electrical DC characteristics.

Table 43. SDHC Electrical DC Characteristics

| ID | Parameter | Min | Max | Unit | Comments |
|-------------|---------------------------|------|----------------|---------------|----------|
| General | | | | | |
| SD10 | Peak Voltage on All Lines | –0.3 | $V_{DD} + 0.3$ | V | — |
| All Inputs | | | | | |
| SD11 | Input Leakage Current | –10 | 10 | μA | — |
| All Outputs | | | | | |
| SD12 | Output Leakage Current | –10 | 10 | μA | — |

Table 43. SDHC Electrical DC Characteristics

| ID | Parameter | Min | Max | Unit | Comments |
|--|-------------------------------|-----------------------|-----------------------|------------|-----------------------------------|
| Power Supply | | | | | |
| SD13 | Supply Voltage (low voltage) | 1.65 | 1.95 | V | 1.95 ~2.7 V is not supported. |
| SD14 | Supply Voltage (high voltage) | 2.7 | 3.6 | V | |
| SD15 | Power Up Time | — | 250 | ms | — |
| SD16 | Supply Current | 100 | — | mA | — |
| Bus Signal Line Load | | | | | |
| SD17 | Pull-up Resistance | 10 | 100 | k Ω | Internal PU |
| SD18 | Open Drain Resistance | NA | NA | k Ω | For MMC cards only |
| Open Drain Signal Level | | | | | — |
| SD19 | Output High Voltage | $V_{DD} - 0.2$ | — | V | $I_{OH} = -100$ mA |
| SD20 | Output Low Voltage | — | 0.3 | V | $I_{OL} = 2$ mA |
| Push-Pull Signal Levels (High Voltage) | | | | | |
| SD21 | Output HIGH Voltage | $0.75 \times V_{DD}$ | — | V | $I_{OH} = -100$ mA @ V_{DD} min |
| SD22 | Output LOW Voltage | — | $0.125 \times V_{DD}$ | V | $I_{OL} = 100$ mA @ V_{DD} min |
| SD23 | Input HIGH Voltage | $0.625 \times V_{DD}$ | $V_{DD} + 0.3$ | V | — |
| SD24 | Input LOW Voltage | $V_{SS} - 0.3$ | $0.25 \times V_{DD}$ | V | — |
| Push-Pull Signal Levels (Low Voltage) | | | | | |
| SD25 | Output HIGH Voltage | $V_{DD} - 0.2$ | — | V | $I_{OH} = -100$ mA @ V_{DD} min |
| SD26 | Output LOW Voltage | — | 0.2 | V | $I_{OL} = 100$ mA @ V_{DD} min |
| SD27 | Input HIGH Voltage | $0.7 \times V_{DD}$ | $V_{DD} + 0.3$ | V | — |
| SD28 | Input LOW Voltage | $V_{SS} - 0.3$ | $0.3 \times V_{DD}$ | V | — |

4.3.11 Smart Liquid Crystal Display Controller (SLCDC)

Figure 43 and Figure 44 show the timings of the SLCDC, and Table 44 and Table 45 list the timing parameters.

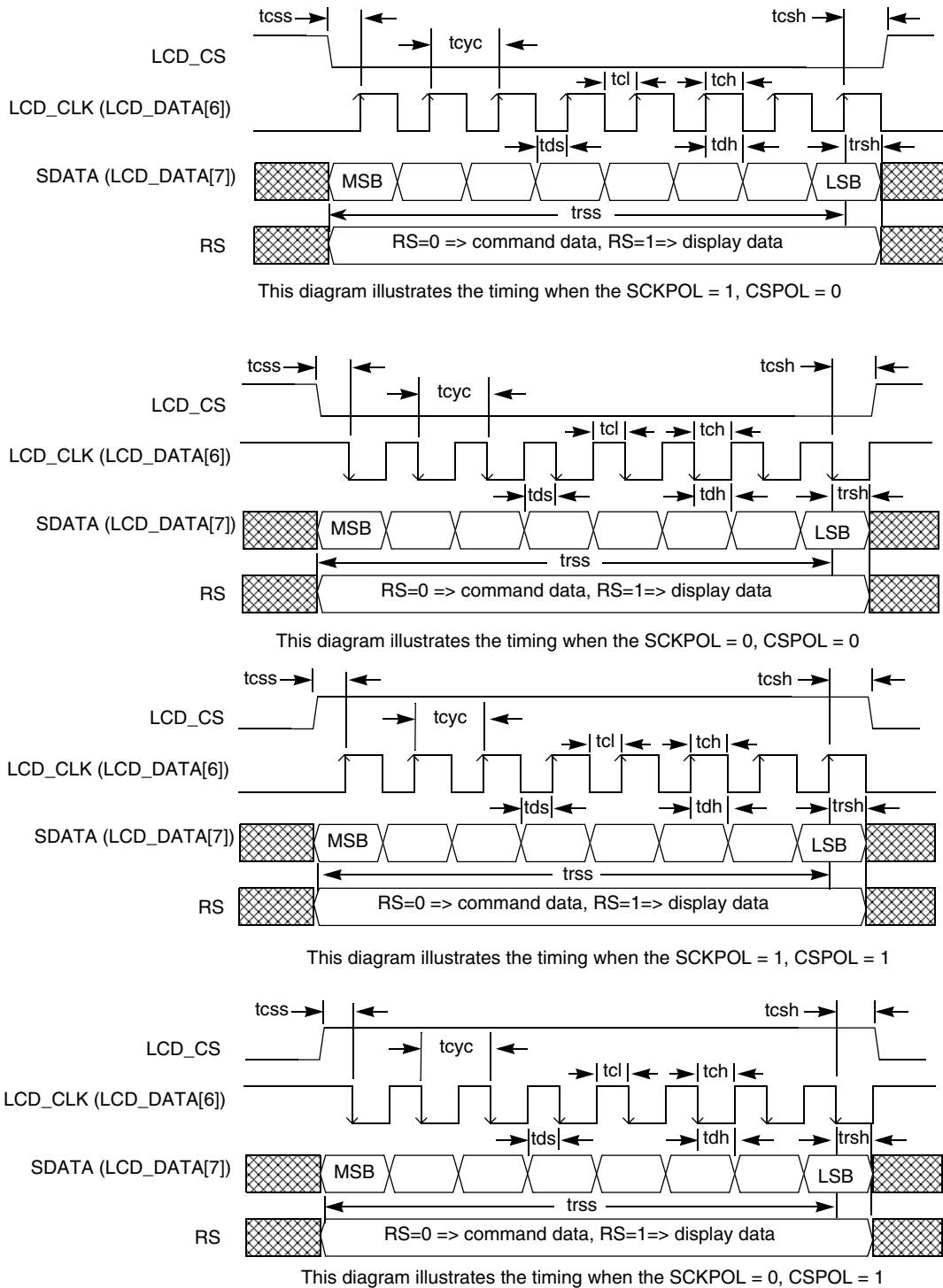
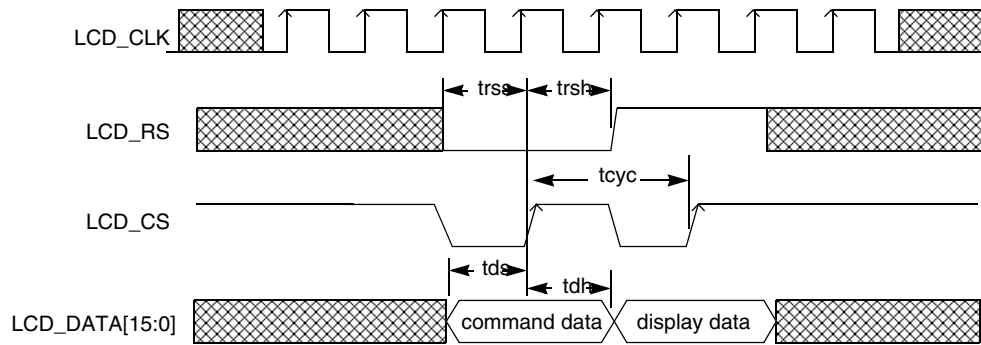


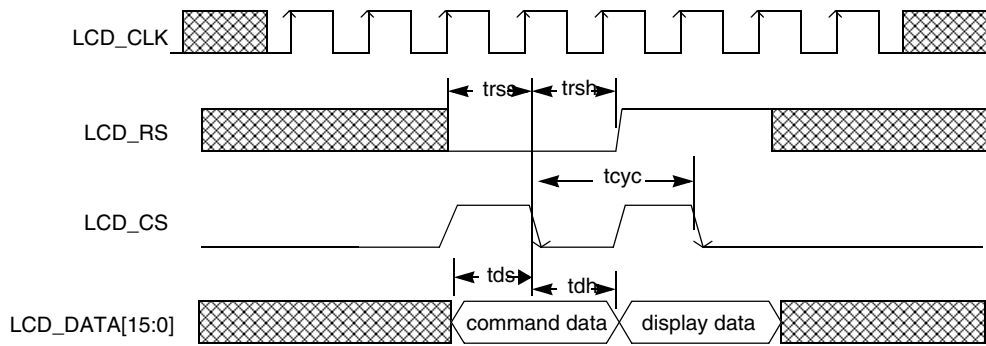
Figure 43. SLCDC Timing Diagram—Serial Transfers to LCD Device

Table 44. SLCDC Serial Interface Timing Parameters

| Symbol | Parameter | Min | Typical | Max | Units |
|-----------|----------------------------|-------------------------------------|---------|------|-------|
| t_{css} | Chip select setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{csh} | Chip select hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{cyc} | Serial clock cycle time | $39 (\pm) t_{prop}$ | — | 2641 | ns |
| t_{cl} | Serial clock low pulse | $18 (\pm) t_{prop}$ | — | — | ns |
| t_{ch} | Serial clock high pulse | $18 (\pm) t_{prop}$ | — | — | ns |
| t_{ds} | Data setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{dh} | Data hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{rss} | Register select setup time | $(15 * t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |
| t_{rsh} | Register select hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | ns |



This diagram illustrates the timing when CSPOL=0



This diagram illustrates the timing when CSPOL=1

Figure 44. SLCDC Timing Diagram—Parallel Transfers to LCD Device

Table 45. SLCDC Parallel Interface Timing Parameters

| Symbol | Parameter | Min | Typical | Max | Units |
|-----------|---------------------------|--------------------------------|---------|------|-------|
| t_{cyc} | Parallel clock cycle time | $78 (\pm) t_{prop}$ | — | 4923 | — |
| t_{ds} | Data setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |
| t_{dh} | Data hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |

Table 45. SLCDC Parallel Interface Timing Parameters (continued)

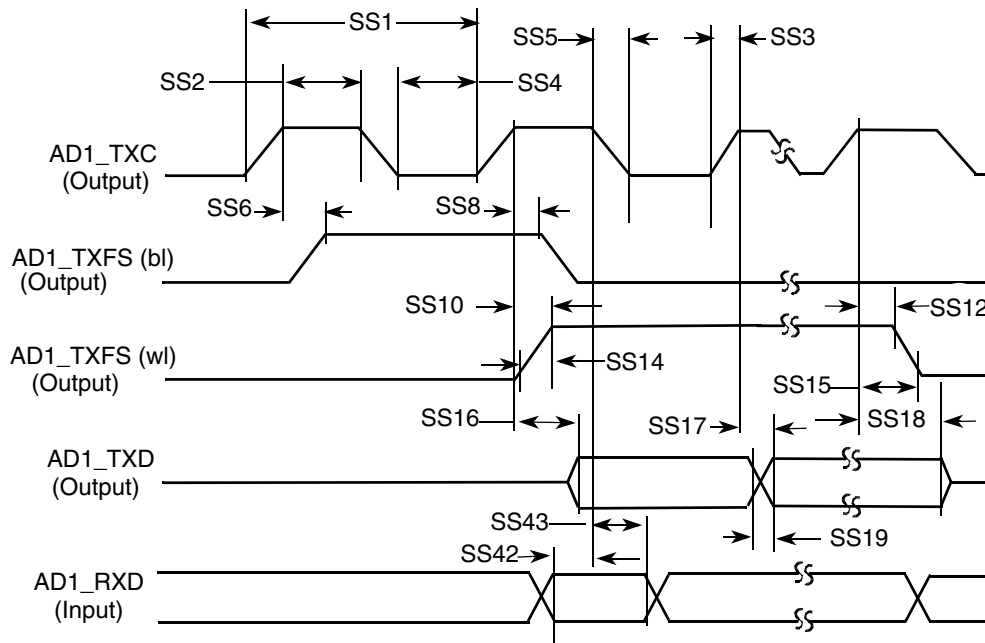
| Symbol | Parameter | Min | Typical | Max | Units |
|-----------|----------------------------|--------------------------------|---------|-----|-------|
| t_{rss} | Register select setup time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |
| t_{rsh} | Register select hold time | $(t_{cyc} / 2) (\pm) t_{prop}$ | — | — | — |

4.3.12 Synchronous Serial Interface (SSI)

This section describes the electrical information of SSI.

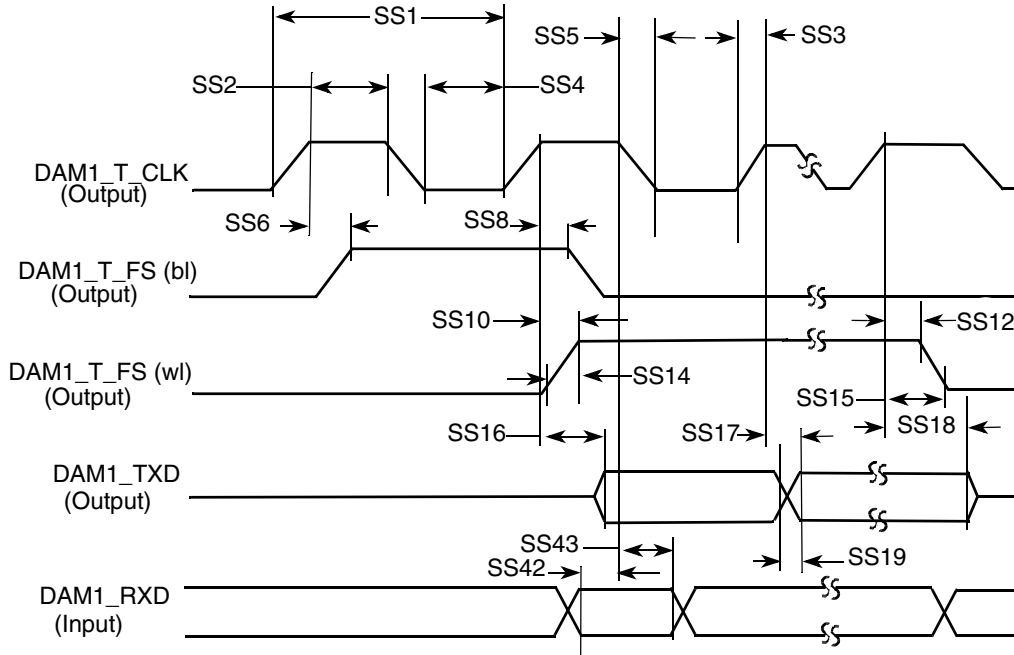
4.3.12.1 SSI Transmitter Timing with Internal Clock

Figure 45 and Figure 46 show the SSI transmitter timing with internal clock, and Table 46 lists the timing parameters.



Note: SRXD Input in Synchronous mode only

Figure 45. SSI Transmitter with Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 46. SSI Transmitter with Internal Clock Timing Diagram

Table 46. SSI Transmitter with Internal Clock Timing Parameters

| ID | Parameter | Min | Max | Unit |
|--------------------------|--|------|------|------|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6 | ns |
| SS6 | (Tx) CK high to FS (bl) high | — | 15.0 | ns |
| SS8 | (Tx) CK high to FS (bl) low | — | 15.0 | ns |
| SS10 | (Tx) CK high to FS (wl) high | — | 15.0 | ns |
| SS12 | (Tx) CK high to FS (wl) low | — | 15.0 | ns |
| SS14 | (Tx/Rx) Internal FS rise time | — | 6 | ns |
| SS15 | (Tx/Rx) Internal FS fall time | — | 6 | ns |
| SS16 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |
| SS17 | (Tx) CK high to STXD high/low | — | 15.0 | ns |
| SS18 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| SS19 | STXD rise/fall time | — | 6 | ns |

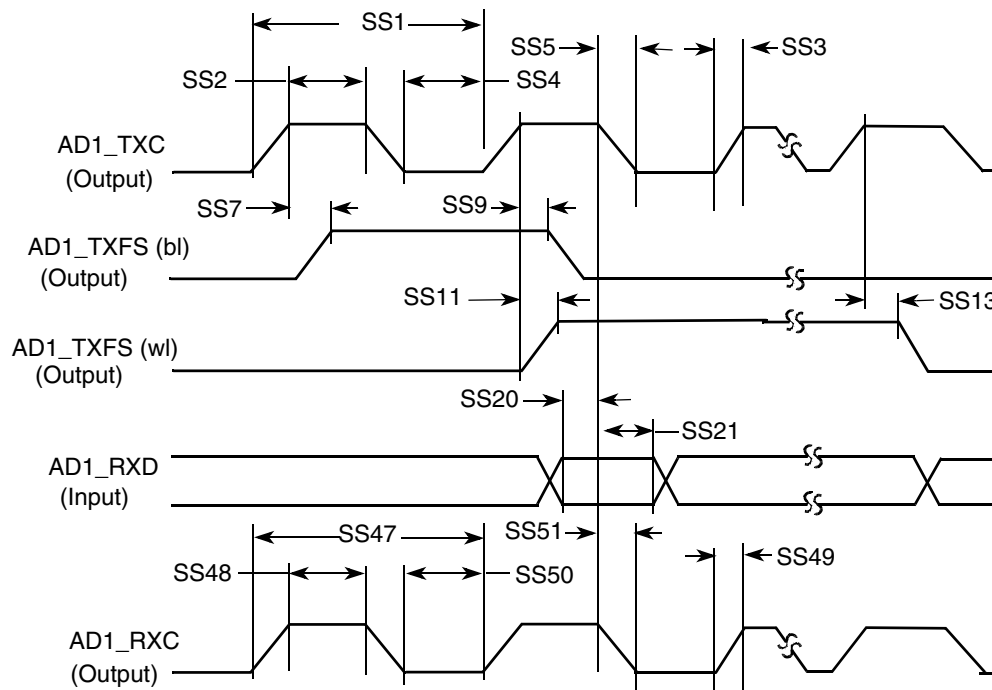
Table 46. SSI Transmitter with Internal Clock Timing Parameters (continued)

| ID | Parameter | Min | Max | Unit |
|--------------------------------------|-----------------------------------|------|-----|------|
| Synchronous Internal Clock Operation | | | | |
| SS42 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS43 | SRXD hold after (Tx) CK falling | 0 | — | ns |
| SS52 | Loading | — | 25 | pF |

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on AUDMUX pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing will be same as that of Tx Data (for example, during AC97 mode of operation).

4.3.12.2 SSI Receiver Timing with Internal Clock

Figure 47 and Figure 48 show the SSI receiver timing with internal clock, and Table 47 lists the timing parameters.

**Figure 47. SSI Receiver with Internal Clock Timing Diagram**

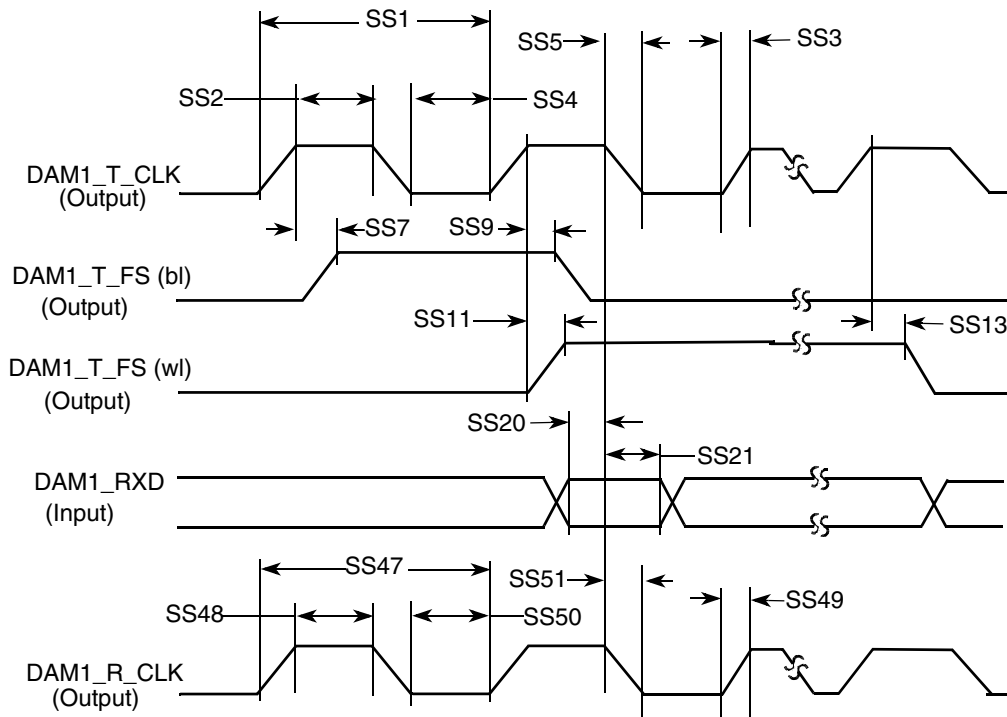


Figure 48. SSI Receiver with Internal Clock Timing Diagram

Table 47. SSI Receiver with Internal Clock Timing Parameters

| ID | Parameter | Min | Max | Unit |
|-------------------------------------|------------------------------------|-------|------|------|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6 | ns |
| SS7 | (Rx) CK high to FS (bl) high | — | 15.0 | ns |
| SS9 | (Rx) CK high to FS (bl) low | — | 15.0 | ns |
| SS11 | (Rx) CK high to FS (wl) high | — | 15.0 | ns |
| SS13 | (Rx) CK high to FS (wl) low | — | 15.0 | ns |
| SS20 | SRXD setup time before (Rx) CK low | 10.0 | — | ns |
| SS21 | SRXD hold time after (Rx) CK low | 0 | — | ns |
| Oversampling Clock Operation | | | | |
| SS47 | Oversampling clock period | 15.04 | — | ns |
| SS48 | Oversampling clock high period | 6 | — | ns |

Table 47. SSI Receiver with Internal Clock Timing Parameters (continued)

| ID | Parameter | Min | Max | Unit |
|------|-------------------------------|-----|-----|------|
| SS49 | Oversampling clock rise time | — | 3 | ns |
| SS50 | Oversampling clock low period | 6 | — | ns |
| SS51 | Oversampling clock fall time | — | 3 | ns |

NOTE

All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

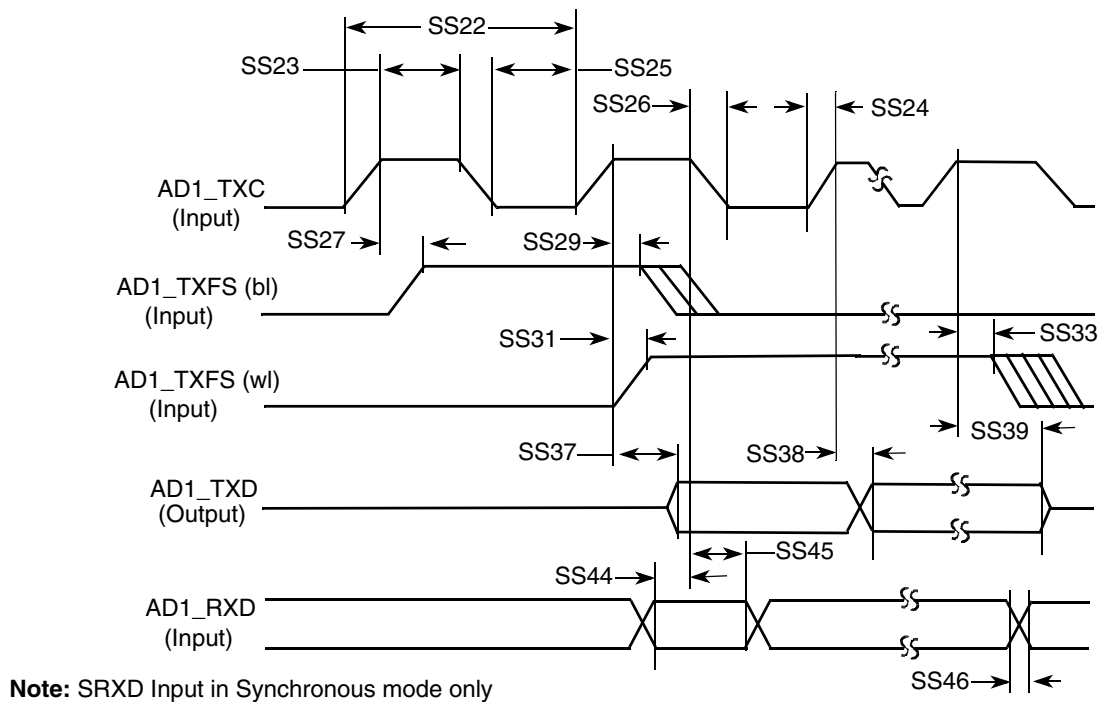
All timings are on AUDMUX pads when SSI is being used for data transfer.

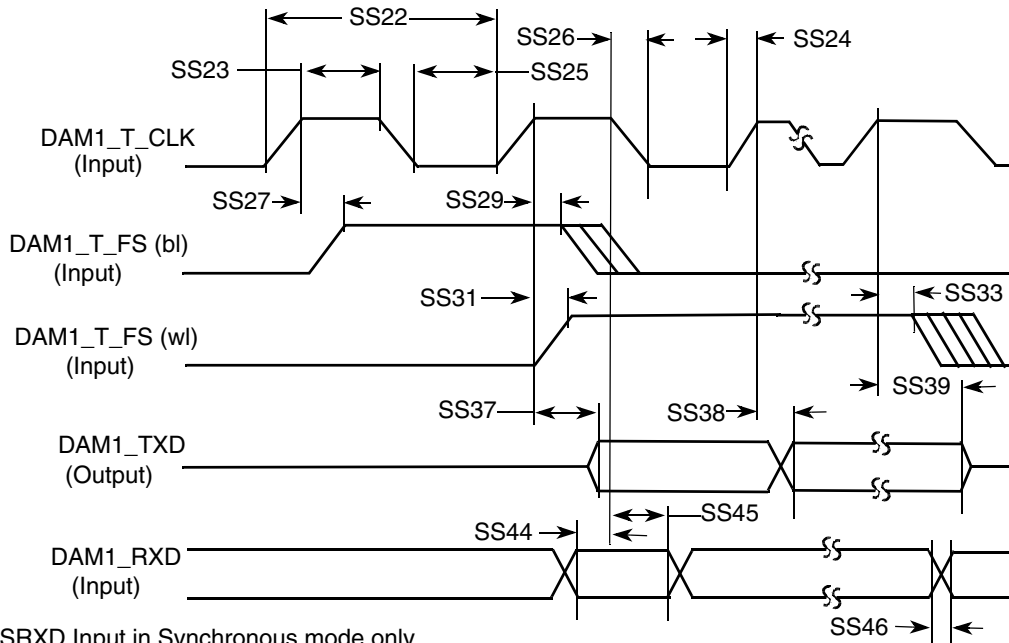
“Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.

For internal Frame Sync operation using external clock, the FS timing is the same as that of Tx Data, for example, during the AC97 mode of operation.

4.3.12.3 SSI Transmitter Timing with External Clock

Figure 49 and Figure 50 show the SSI transmitter timing with external clock, and Table 48 lists the timing parameters.

**Figure 49. SSI Transmitter with External Clock Timing Diagram**



Note: SRXD Input in Synchronous mode only

Figure 50. SSI Transmitter with External Clock Timing Diagram

Table 48. SSI Transmitter with External Clock Timing Parameters

| ID | Parameter | Min | Max | Unit |
|---|--|-------|------|------|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS27 | (Tx) CK high to FS (bl) high | -10.0 | 15.0 | ns |
| SS29 | (Tx) CK high to FS (bl) low | 10.0 | — | ns |
| SS31 | (Tx) CK high to FS (wl) high | -10.0 | 15.0 | ns |
| SS33 | (Tx) CK high to FS (wl) low | 10.0 | — | ns |
| SS37 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |
| SS38 | (Tx) CK high to STXD high/low | — | 15.0 | ns |
| SS39 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| Synchronous External Clock Operation | | | | |
| SS44 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS45 | SRXD hold after (Tx) CK falling | 2.0 | — | ns |
| SS46 | SRXD rise/fall time | — | 6.0 | ns |

NOTE

All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

All timings are on AUDMUX pads when the SSI is being used for data transfer.

“Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.

For internal Frame Sync operation using external clock, the FS timing will be same as that of Tx Data, for example, during the AC97 mode of operation.

4.3.12.4 SSI Receiver Timing with External Clock

Figure 51 and Figure 52 show the SSI receiver timing with external clock, and Table 49 lists the timing parameters.

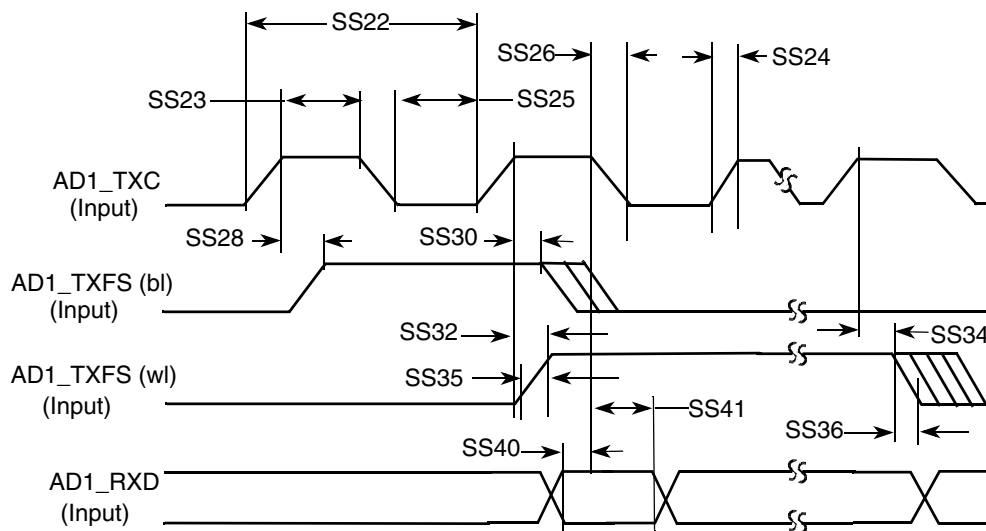


Figure 51. SSI Receiver with External Clock Timing Diagram

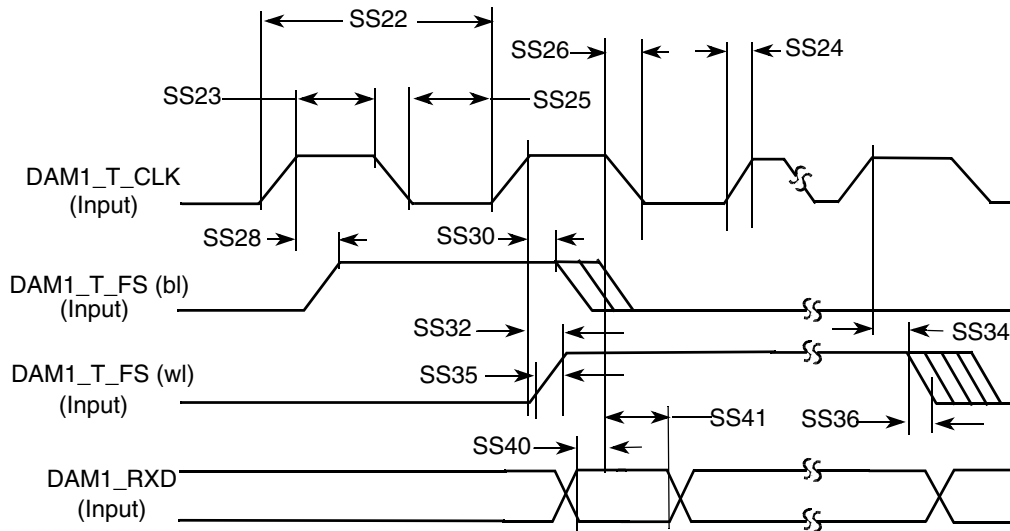


Figure 52. SSI Receiver with External Clock Timing Diagram

Table 49. SSI Receiver with External Clock Timing Parameters

| ID | Parameter | Min | Max | Unit |
|---------------------------------|------------------------------------|-------|------|------|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS28 | (Rx) CK high to FS (bl) high | -10.0 | 15.0 | ns |
| SS30 | (Rx) CK high to FS (bl) low | 10.0 | — | ns |
| SS32 | (Rx) CK high to FS (wl) high | -10.0 | 15.0 | ns |
| SS34 | (Rx) CK high to FS (wl) low | 10.0 | — | ns |
| SS35 | (Tx/Rx) External FS rise time | — | 6.0 | ns |
| SS36 | (Tx/Rx) External FS fall time | — | 6.0 | ns |
| SS40 | SRXD setup time before (Rx) CK low | 10.0 | — | ns |
| SS41 | SRXD hold time after (Rx) CK low | 2.0 | — | ns |

NOTE

All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

All timings are on AUDMUX pads when the SSI is being used for data transfer.

“Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.

For internal Frame Sync operation using external clock, the FS timing will be same as that of Tx Data, for example, during the AC97 mode of operation.

4.3.13 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, \overline{ECB} and \overline{DTACK} all captured according to BCLK rising edge time. [Figure 53](#) shows the timing of the WEIM module, and [Table 50](#) lists the timing parameters.

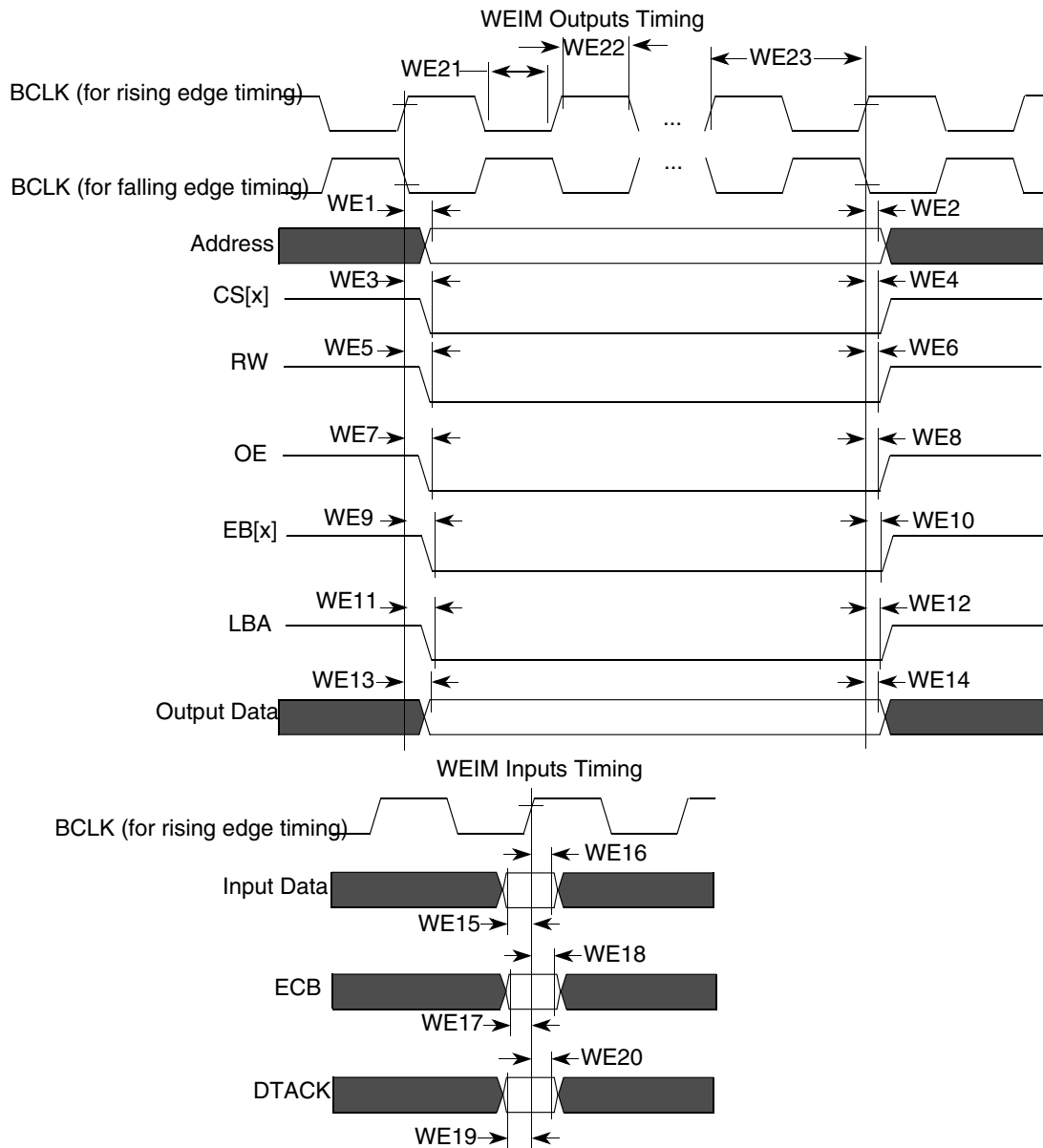


Figure 53. WEIM Bus Timing Diagram

Table 50. WEIM Bus Timing Parameters

| ID | Parameter | 1.8 V | | Unit |
|-----|---|-------|------|------|
| | | Min | Max | |
| WE1 | Clock fall to address valid | 0.68 | 2.05 | ns |
| WE2 | Clock rise/fall to address invalid | 0.68 | 2.49 | ns |
| WE3 | Clock rise/fall to $\overline{CS}[x]$ valid | 0.45 | 2.25 | ns |
| WE4 | Clock rise/fall to $\overline{CS}[x]$ invalid | 0.45 | 2.25 | ns |

Table 50. WEIM Bus Timing Parameters (continued)

| ID | Parameter | 1.8 V | | Unit |
|------|--|-----------------|------|------|
| | | Min | Max | |
| WE5 | Clock rise/fall to \overline{RW} Valid | 0.90 | 2.60 | ns |
| WE6 | Clock rise/fall to \overline{RW} Invalid | 0.90 | 2.60 | ns |
| WE7 | Clock rise/fall to \overline{OE} Valid | 1.17 | 3.57 | ns |
| WE8 | Clock rise/fall to \overline{OE} Invalid | 1.17 | 3.57 | ns |
| WE9 | Clock rise/fall to $\overline{EB[x]}$ Valid | 0.73 | 2.43 | ns |
| WE10 | Clock rise/fall to $\overline{EB[x]}$ Invalid | 0.73 | 2.43 | ns |
| WE11 | Clock rise/fall to \overline{LBA} Valid | 1.03 | 2.84 | ns |
| WE12 | Clock rise/fall to \overline{LBA} Invalid | 1.03 | 2.84 | ns |
| WE13 | Clock rise/fall to Output Data Valid | 1.04 | 4.01 | ns |
| WE14 | Clock rise to Output Data Invalid | 1.04 | 4.01 | ns |
| WE15 | Input Data Valid to Clock rise, FCE=0 (in the case there is ECB_B asserted during access) | 1/2BCLK +3.6 | — | ns |
| WE15 | Input Data Valid to Clock rise, FCE=0 (in the case there is NO ECB_B asserted during access) | 6.95 | — | ns |
| WE16 | Clock rise to Input Data Invalid, FCE=0 | 2.35 | — | ns |
| WE17 | Input Data Valid to Clock rise, FCE=1 | 1.24 | — | ns |
| WE18 | Clock rise to Input Data Invalid, FCE=1 | 0.23 | — | ns |
| WE19 | \overline{ECB} setup time, FCE=0 | 7.23 | — | ns |
| WE20 | \overline{ECB} hold time, FCE=0 | 2.93 | — | ns |
| WE21 | \overline{ECB} setup time, FCE=1 | 1.08 | — | ns |
| WE22 | \overline{ECB} hold time, FCE=1 | 0 | — | ns |
| WE23 | \overline{DTACK} setup time | 5.35 | — | ns |
| WE24 | \overline{DTACK} hold time | 3.19 | — | ns |
| WE25 | BCLK High Level Width ¹ | 3.0 | — | ns |
| WE26 | BCLK Low Level Width ¹ | 3.0 | — | ns |
| WE27 | BCLK Cycle time ¹ | 7.5 | — | ns |

¹ BCLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Electrical Characteristics

Test conditions: pad voltage, 1.7–1.95 V; pad capacitance, 25 pF.
 Recommended drive strength for all controls, address, and BCLK is Max High.

Figure 54, Figure 55, Figure 56, Figure 57, Figure 58, and Figure 59 show examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 50 for specific control parameter settings.

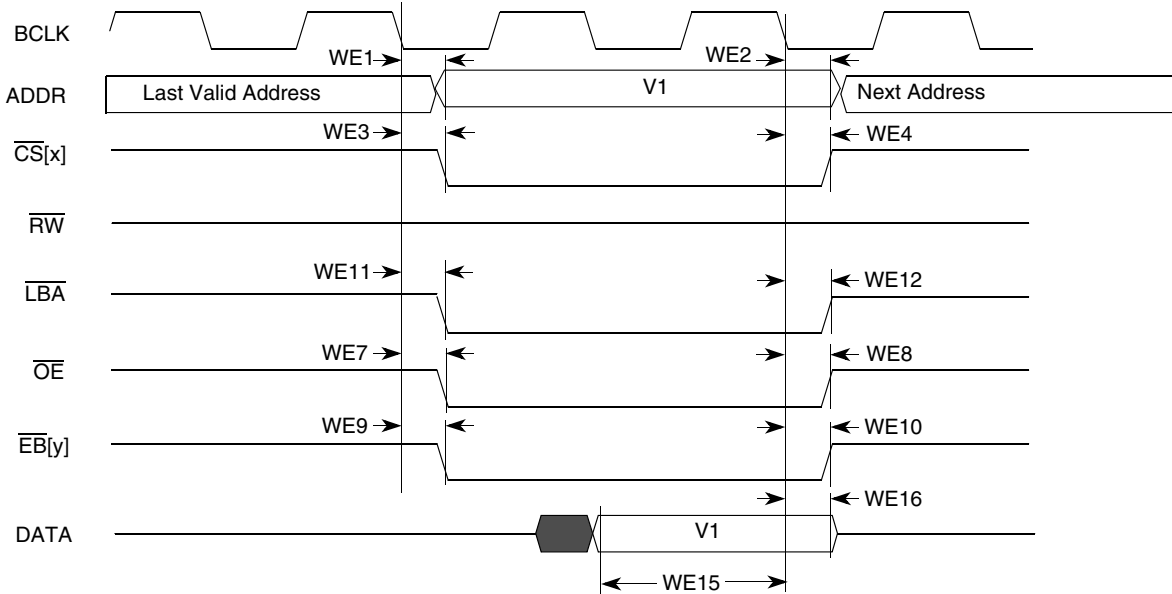


Figure 54. Asynchronous Memory Timing Diagram for Read Access—WSC=1

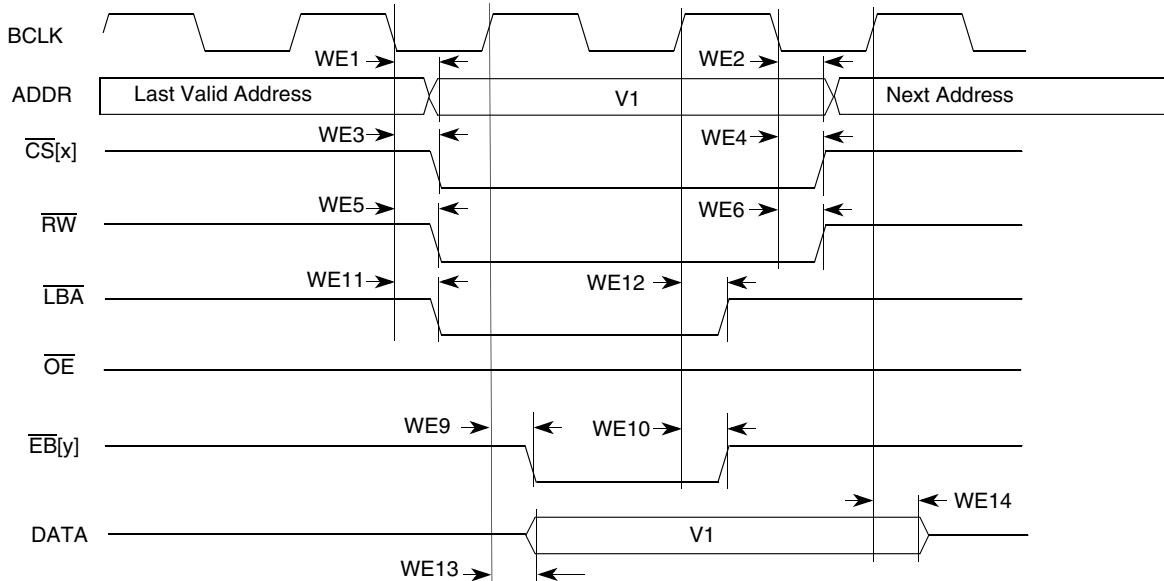


Figure 55. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

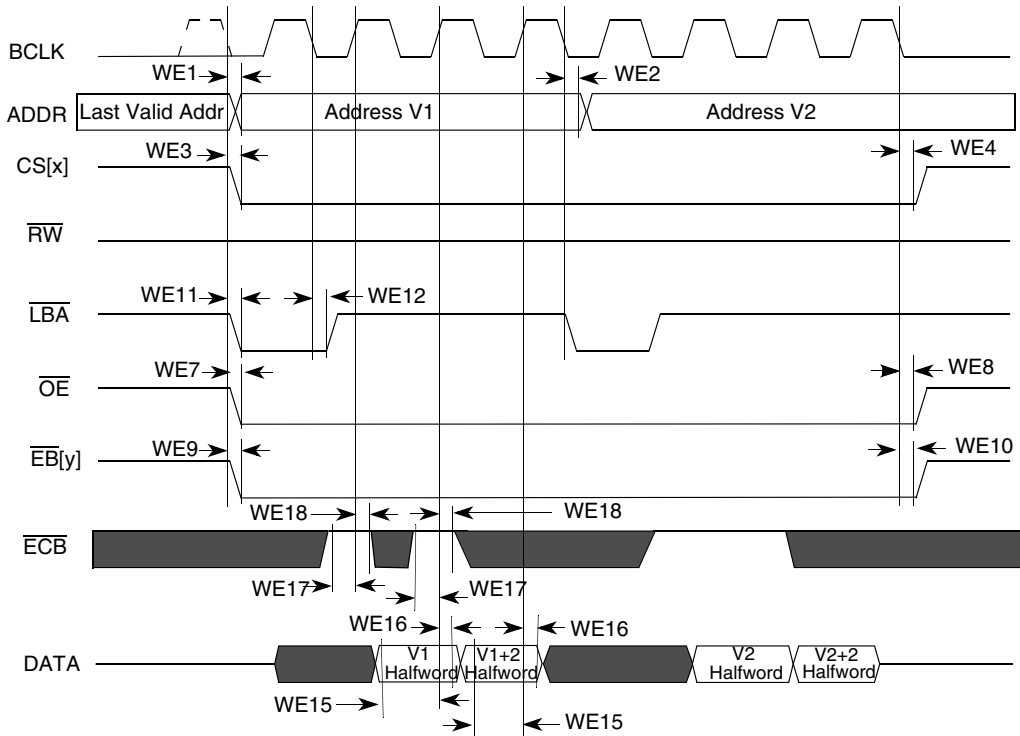


Figure 56. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses: WSC=2, SYNC=1, DOL=0

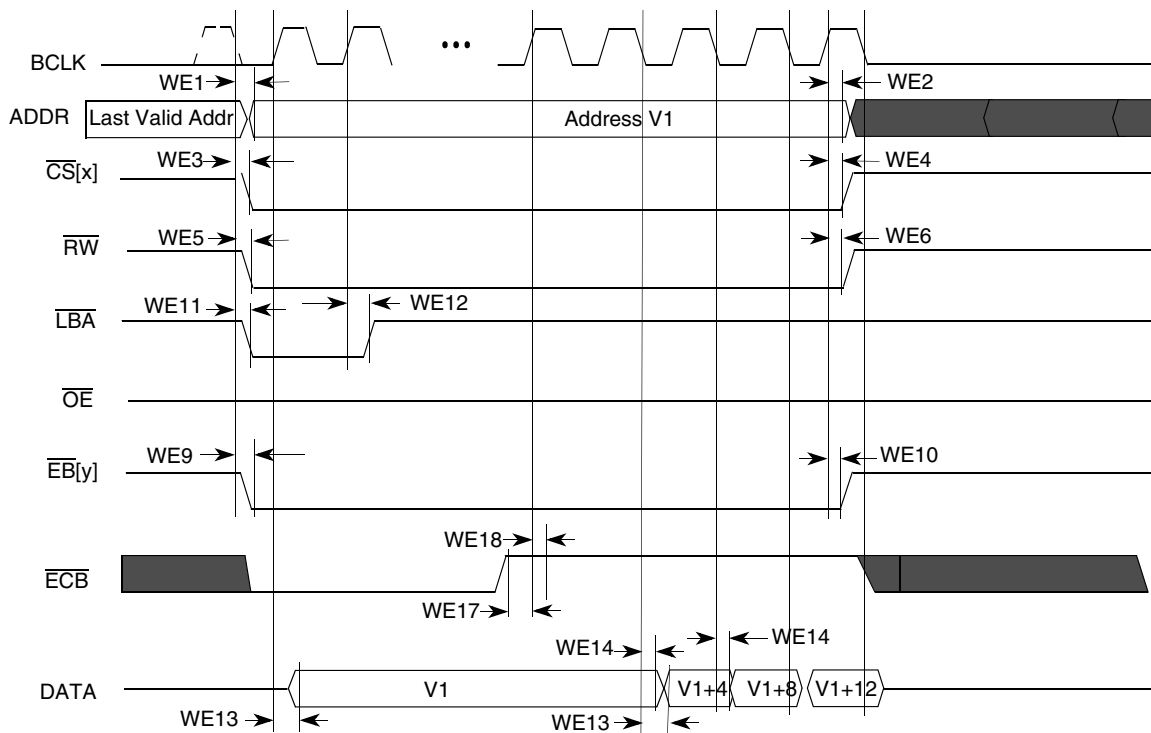


Figure 57. Synchronous Memory Timing Diagram for Burst Write Access—BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1

Electrical Characteristics

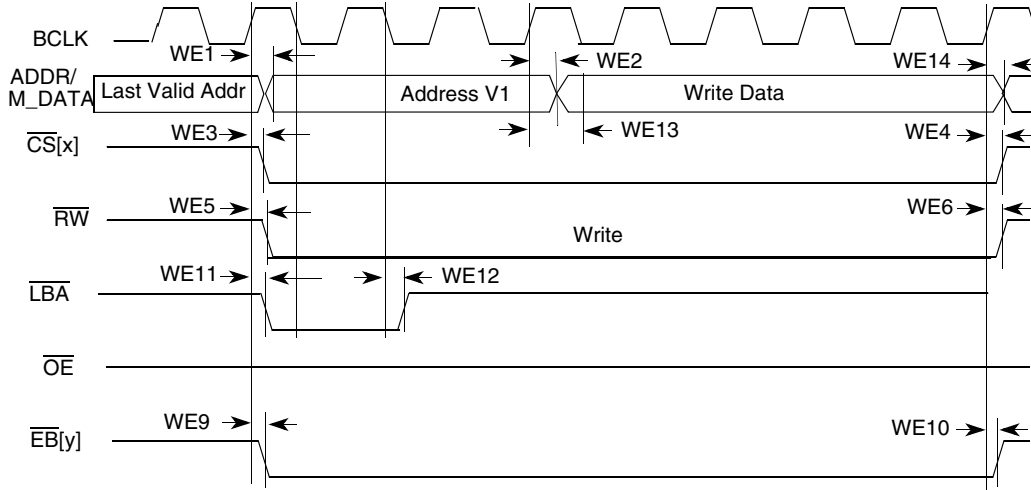


Figure 58. Muxed A/D Mode Timing Diagram for Asynchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1

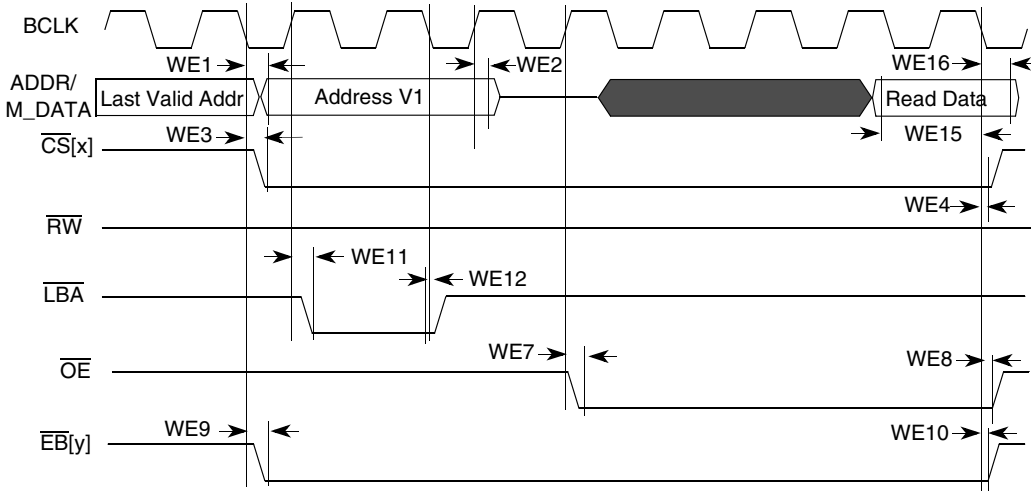


Figure 59. Muxed A/D Mode Timing Diagram for Asynchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7

4.3.13.1 WEIM Synchronous Mode Sample Point

Figure 60 shows that the AHB first sample point is the time marker A.

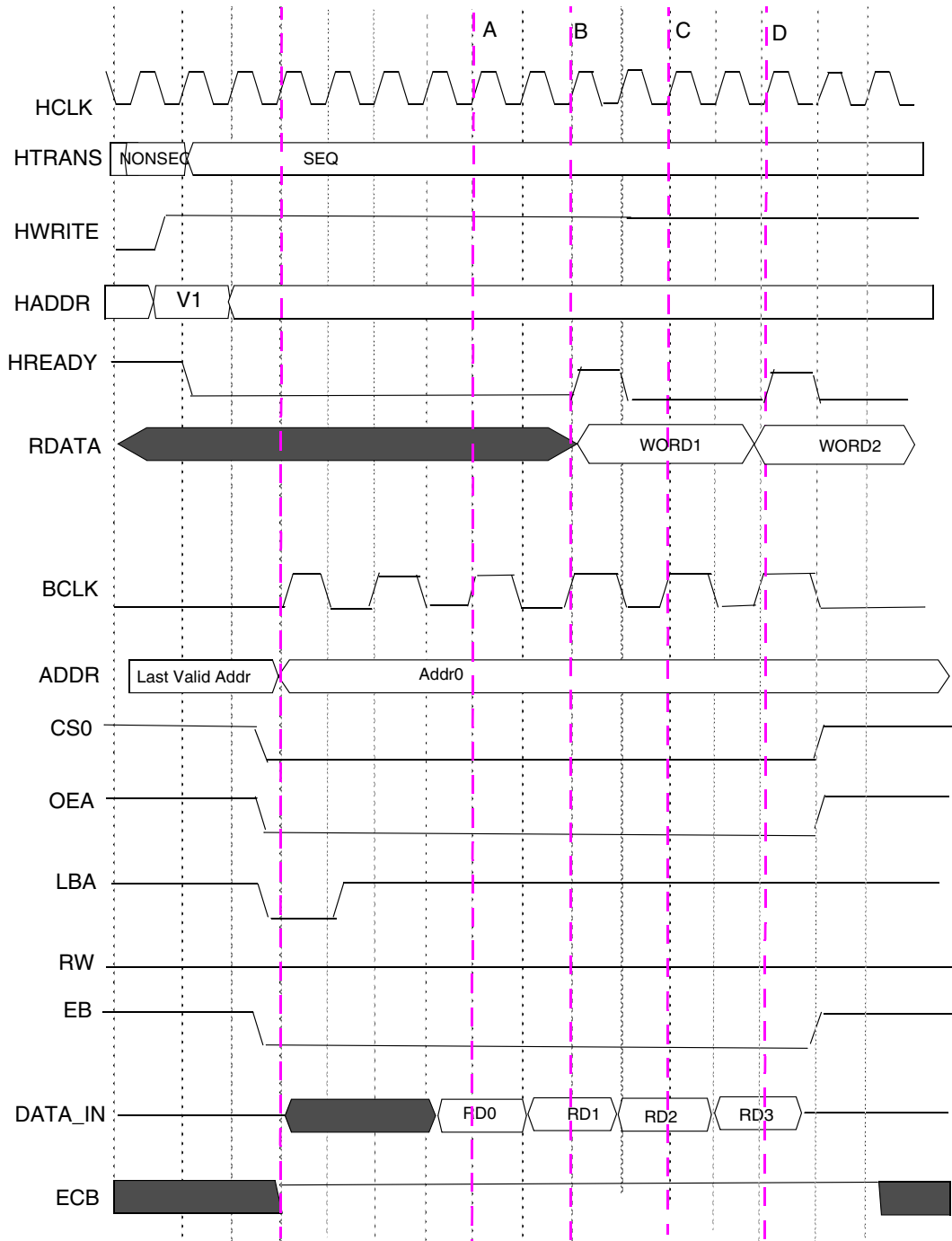


Figure 60. FCE=0,SYNC=1,BCD=1,WSC=4,BCS=0,CSA=0,OEA=0

Figure 61 shows that the AHB first sample point is the time marker A.

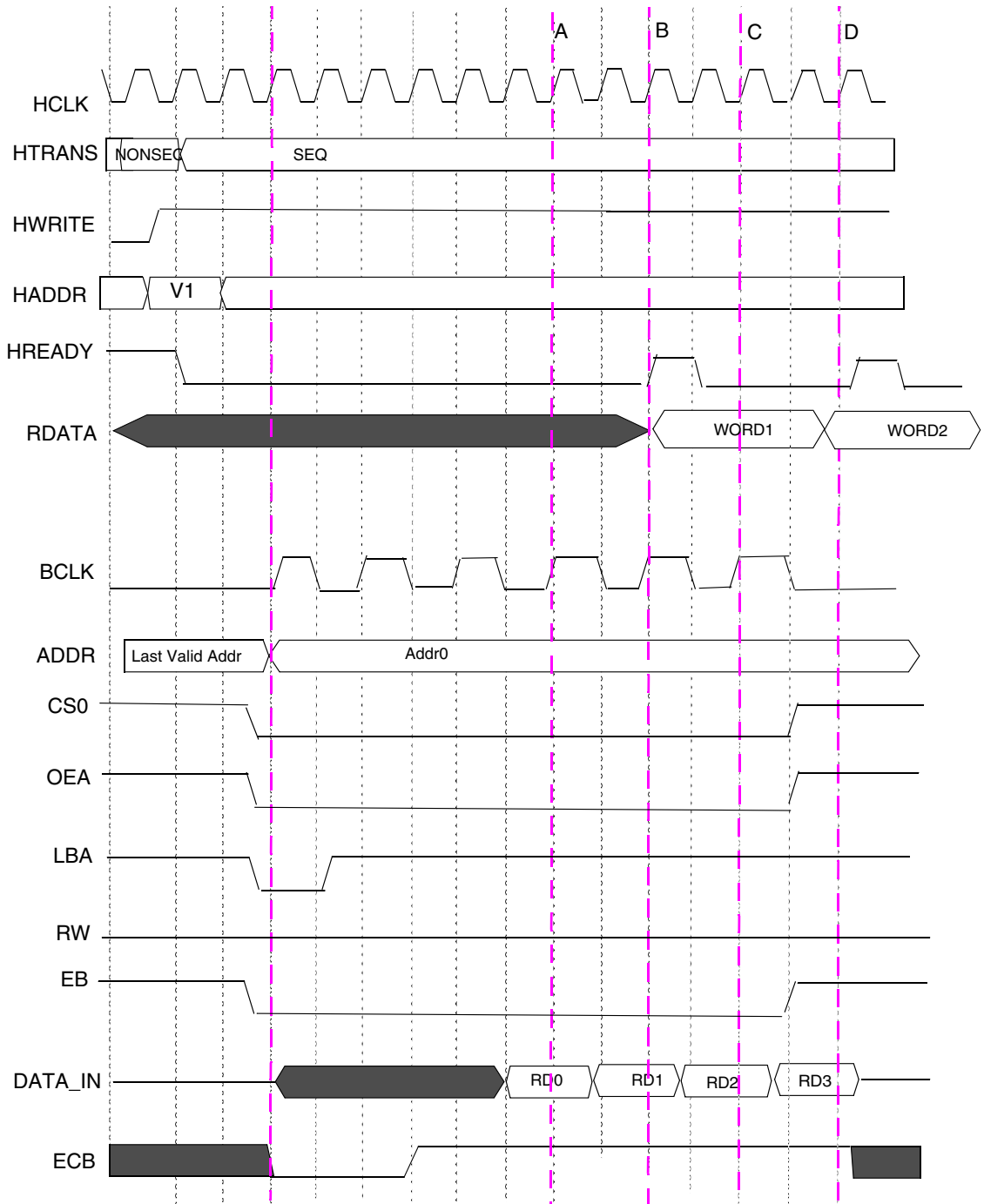


Figure 61. FCE=0,SYNC=1,BCD=1,WSC=6,BCS=0,CSA=0,OEA=0

Figure 62 shows that the AHB first sample point is the time marker A.

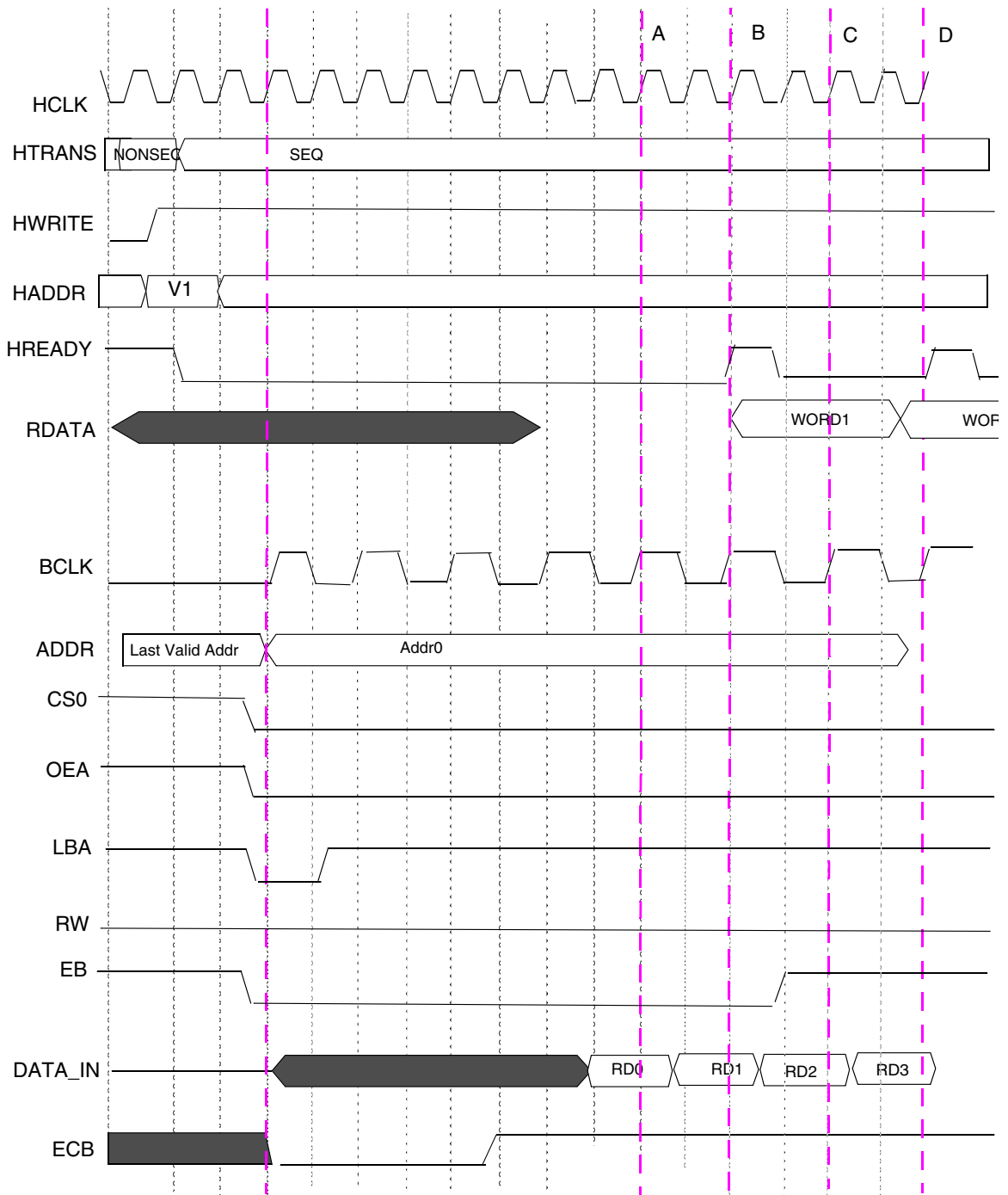


Figure 62. FCE=0,SYNC=1,BCD=1,WSC=8,BCS=0,CSA=0,OEA=0

Figure 63 shows that the AHB first sample point is the time marker A, If ECB is asserted during access, the sample point will be changed to the negative of the BCLK (just like the sample point C&D).

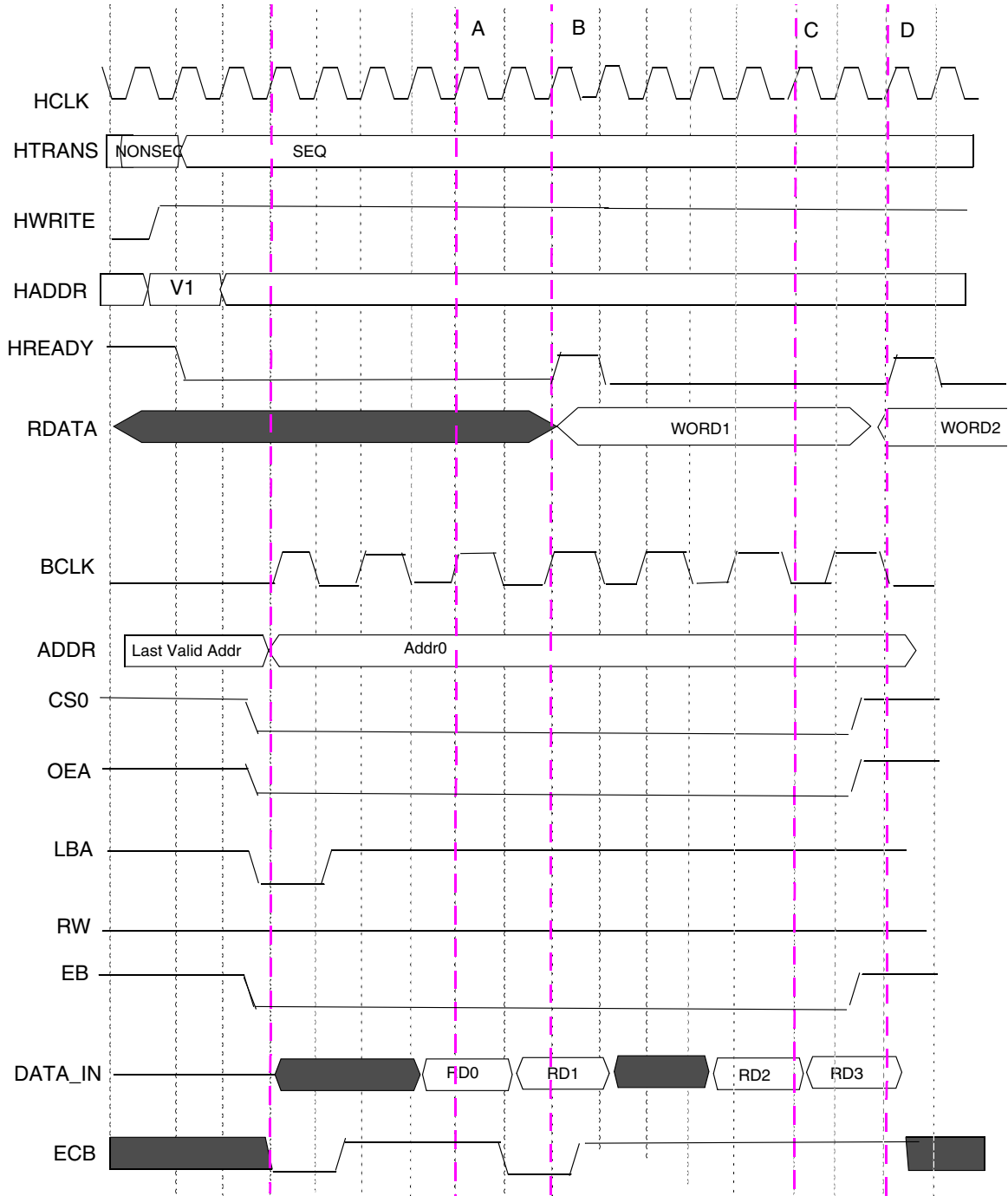


Figure 63. FCE=0,SYNC=1,BCD=1,WSC=4,BCS=0,CSA=0, OEA=0

4.3.14 USBOTG Electricals

This section describes the electrical information of the USB OTG port and host ports.

4.3.15 Serial Interface

In order to support four serial different interfaces, the USBOTG transceiver can be configured to operate in one of the following modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

4.3.15.1 DAT_SE0 Bidirectional Mode

Table 51. Signal Definitions—DAT_SE0 Bidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|--|
| USB_TXOE_B | Out | <ul style="list-style-type: none"> • Transmit enable, active low |
| USB_DAT_VP | Out In | <ul style="list-style-type: none"> • TX data when USB_TXOE_B is low • Differential RX data when USB_TXOE_B is high |
| USB_SE0_VM | Out In | <ul style="list-style-type: none"> • SE0 drive when USB_TXOE_B is low • SE0 RX indicator when USB_TXOE_B is high |

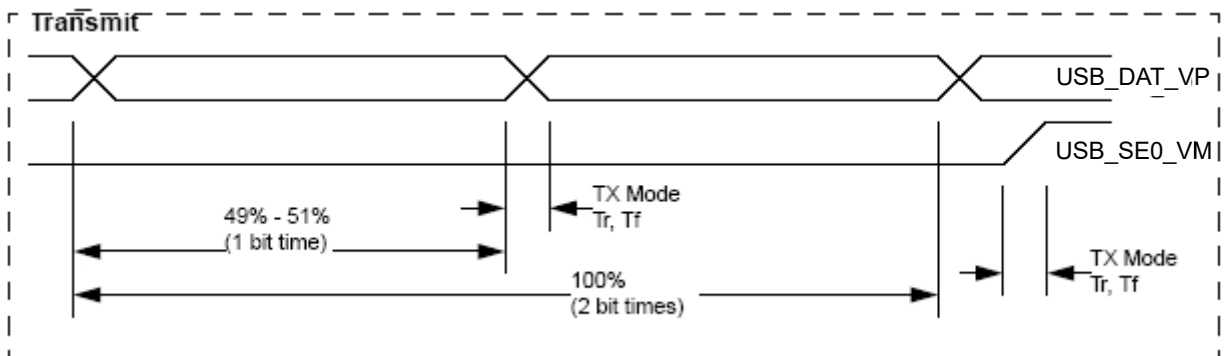


Figure 64. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

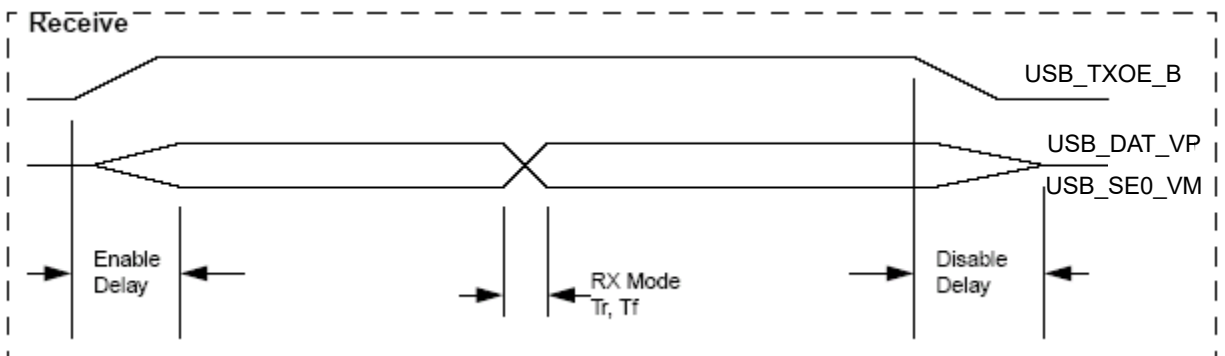


Figure 65. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 52. OTG Port Timing Specification in DAT_SE0 Bidirectional Mode

| Parameter | Signal Name | Direction | Min | Max | Unit | Conditions/ Reference Signal |
|-------------------|--------------------------|-----------|------|------|------|---------------------------------|
| TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| Enable Delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| Disable Delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |
| RX Rise/Fall Time | USB_DAT_VP | In | — | 3.0 | ns | 35 pF |
| RX Rise/Fall Time | USB_SE0_VM | In | — | 3.0 | ns | 35 pF |

4.3.15.2 DAT_SE0 Unidirectional Mode

Table 53. Signal Definitions—DAT_SE0 Unidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|---|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out | TX data when USB_TXOE_B is low. |
| USB_SE0_VM | Out | SE0 drive when USB_TXOE_B is low. |
| USB_VP1 | In | Buffered data on DP when USB_TXOE_B is high. |
| USB_VM1 | In | Buffered data on DM when USB_TXOE_B is high. |
| USB_RCV | In | Differential RX data when USB_TXOE_B is high. |

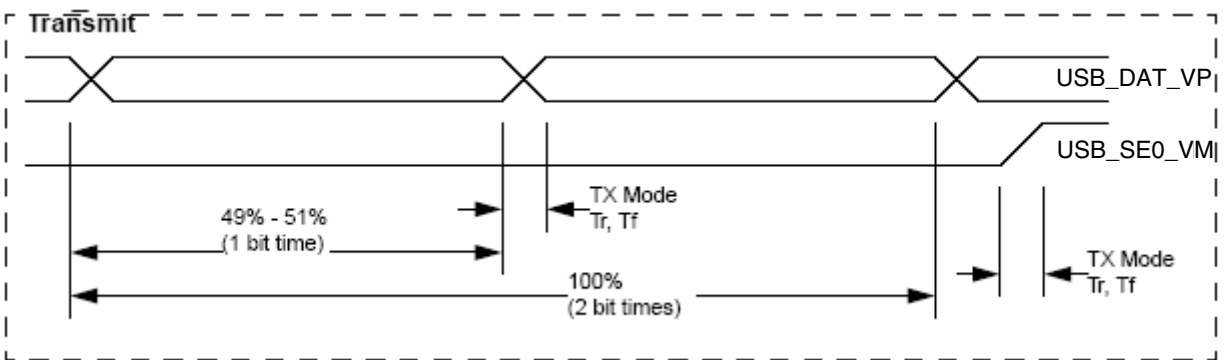


Figure 66. USB Transmit Waveform in DAT_SE0 Unidirectional Mode

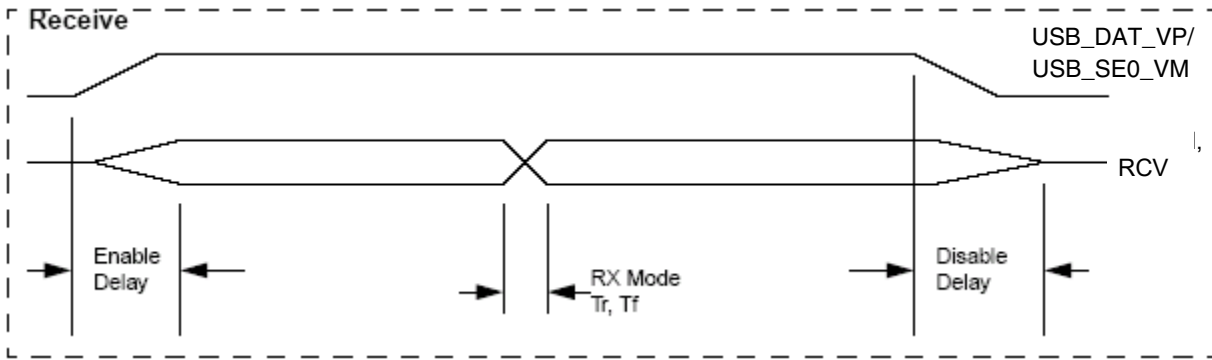


Figure 67. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 54. OTG Port Timing Specification in DAT_SE0 Unidirectional Mode

| Parameter | Signal Name | Signal Source | Min | Max | Unit | Condition/ Reference Signal |
|-------------------|--------------------------|---------------|------|------|------|--------------------------------|
| TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| Enable Delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| Disable Delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |
| RX Rise/Fall Time | USB_VP1 | In | — | 3.0 | ns | 35 pF |
| RX Rise/Fall Time | USB_VM1 | In | — | 3.0 | ns | 35 pF |
| RX Rise/Fall Time | USB_RCV | In | — | 3.0 | ns | 35 pF |

4.3.15.3 VP_VM Bidirectional Mode

Table 55. Signal Definitions—VP_VM Bidirectional Mode

| Name | Direction | Signal Description |
|------------|---------------------|---|
| USB_TXOE_B | Out | • Transmit enable, active low |
| USB_DAT_VP | Out (Tx) In (Rx) | • TX VP data when USB_TXOE_B is low • RX VP data when USB_TXOE_B is high |
| USB_SE0_VM | Out (Tx) In (Rx) | • TX VM data when USB_TXOE_B low • RX VM data when USB_TXOE_B high |
| USB_RCV | In | • Differential RX data |

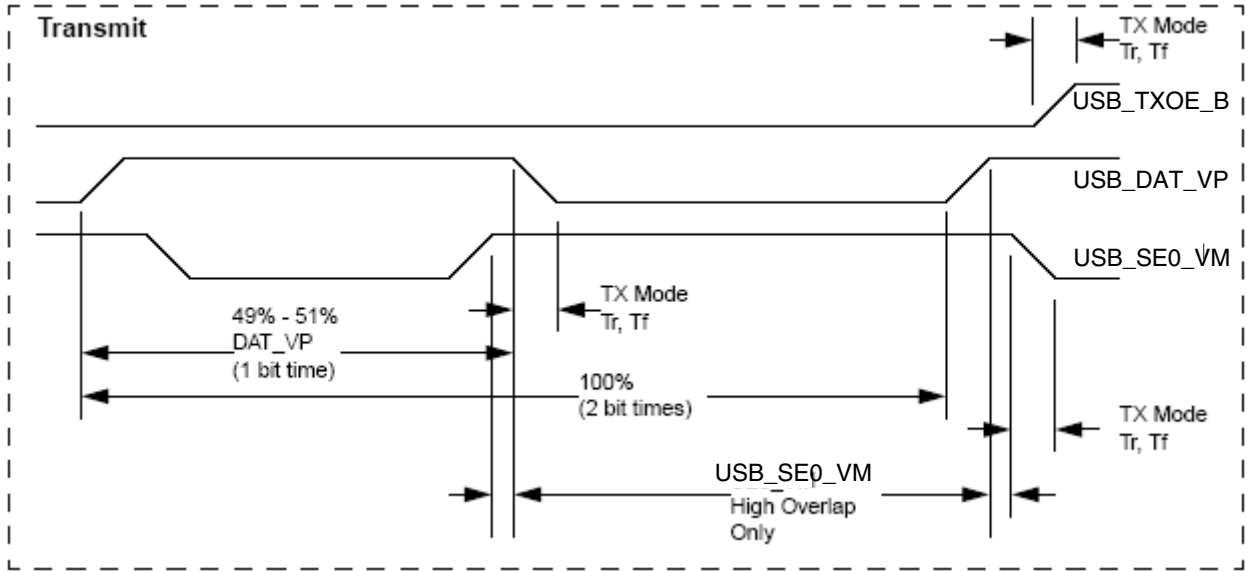


Figure 68. USB Transmit Waveform in VP_VM Bidirectional Mode

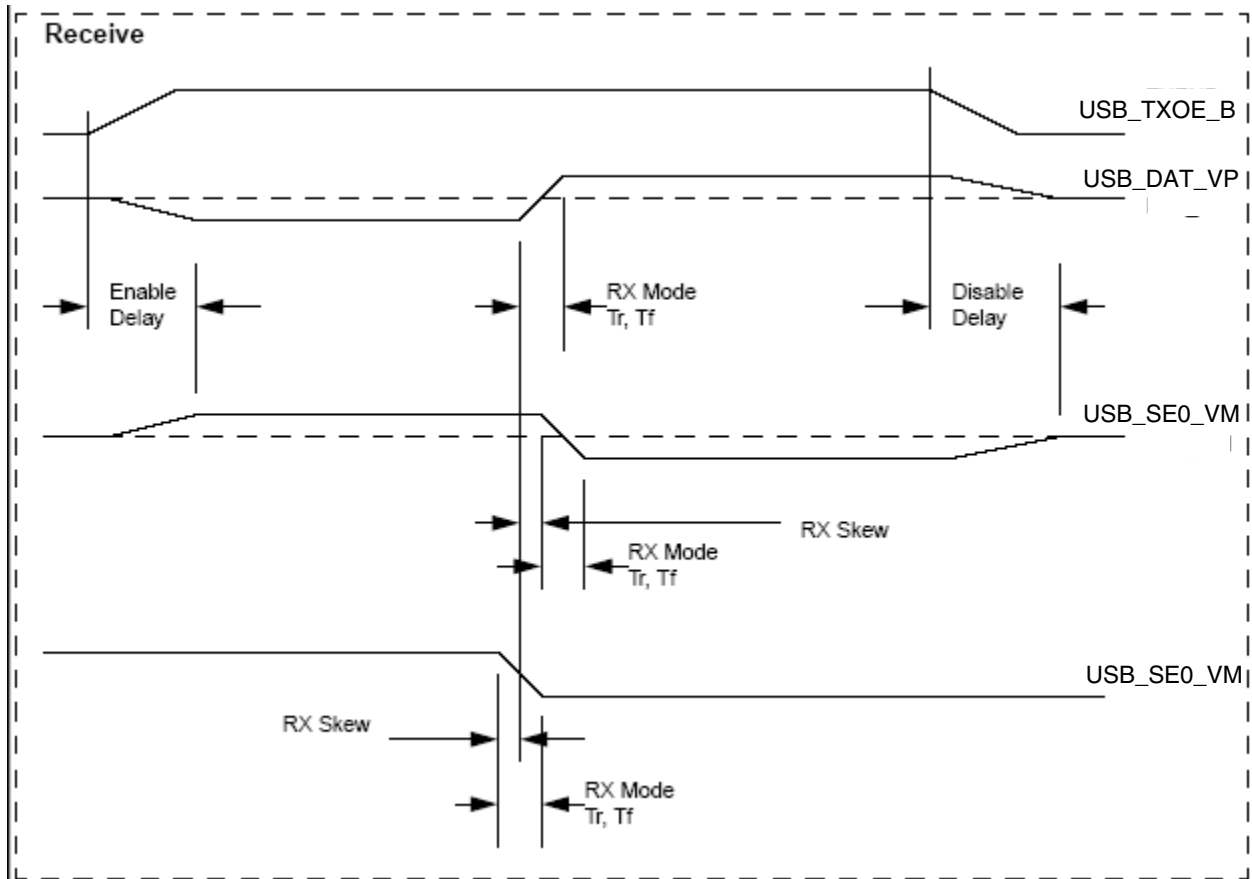


Figure 69. USB Receive Waveform in VP_VM Bidirectional Mode

Table 56. OTG Port Timing Specification in VP_VM Bidirectional Mode

| Parameter | Signal Name | Direction | Min | Max | Unit | Condition/ Reference Signal |
|-------------------|--------------------------|-----------|------|------|------|--------------------------------|
| TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| TX High Overlap | USB_SE0_VM | Out | 0.0 | — | ns | USB_DAT_VP |
| TX Low Overlap | USB_SE0_VM | Out | — | 0.0 | ns | USB_DAT_VP |
| Enable Delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| Disable Delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |
| RX Rise/Fall Time | USB_DAT_VP | In | — | 3.0 | ns | 35 pF |
| RX Rise/Fall Time | USB_SE0_VM | In | — | 3.0 | ns | 35 pF |
| RX Skew | USB_DAT_VP | Out | -4.0 | +4.0 | ns | USB_SE0_VM |
| RX Skew | USB_RCV | Out | -6.0 | +2.0 | ns | USB_DAT_VP |

4.3.15.4 VP_VM Unidirectional Mode

Table 57. Signal Definitions—VP_VM Unidirectional Mode

| Name | Direction | Signal Description |
|------------|-----------|------------------------------------|
| USB_TXOE_B | Out | Transmit enable, active low |
| USB_DAT_VP | Out | TX VP data when USB_TXOE_B is low |
| USB_SE0_VM | Out | TX VM data when USB_TXOE_B is low |
| USB_VP1 | In | RX VP data when USB_TXOE_B is high |
| USB_VM1 | In | RX VM data when USB_TXOE_B is high |
| USB_RCV | In | Differential RX data |

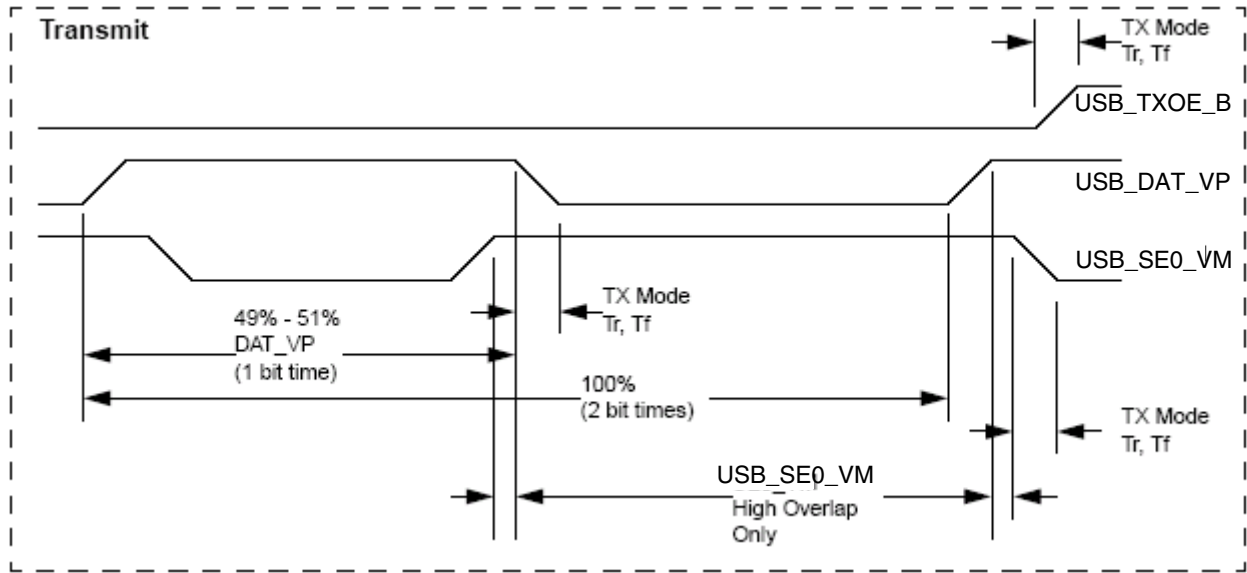


Figure 70. USB Transmit Waveform in VP_VM Unidirectional Mode

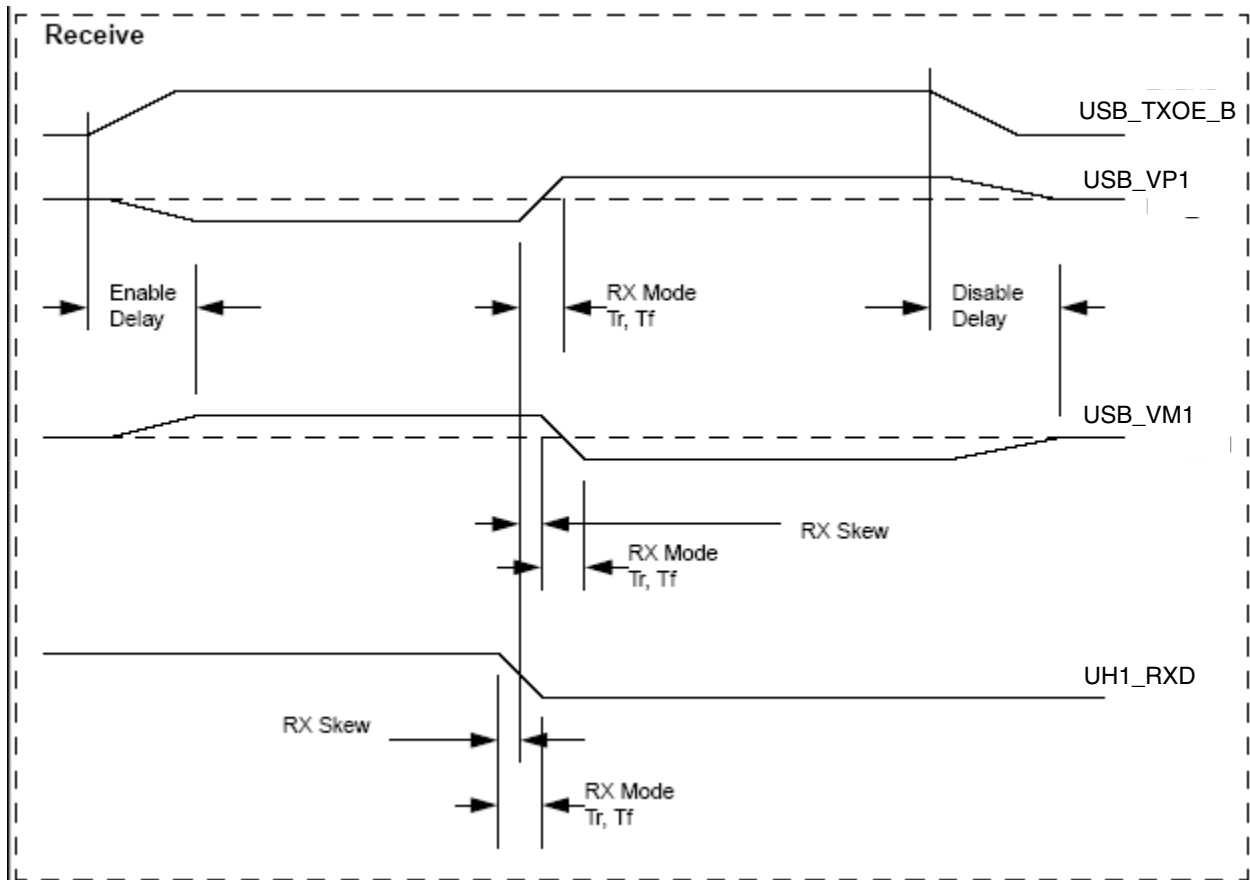


Figure 71. USB Receive Waveform in VP_VM Unidirectional Mode

Table 58. USB Timing Specification in VP_VM Unidirectional Mode

| Parameter | Signal | Direction | Min | Max | Unit | Conditions/ Reference Signal |
|-------------------|--------------------------|-----------|------|------|------|---------------------------------|
| TX Rise/Fall Time | USB_DAT_VP | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_SE0_VM | Out | — | 5.0 | ns | 50 pF |
| TX Rise/Fall Time | USB_TXOE_B | Out | — | 5.0 | ns | 50 pF |
| TX Duty Cycle | USB_DAT_VP | Out | 49.0 | 51.0 | % | — |
| TX High Overlap | USB_SE0_VM | Out | 0.0 | — | ns | USB_DAT_VP |
| TX Low Overlap | USB_SE0_VM | Out | — | 0.0 | ns | USB_DAT_VP |
| Enable Delay | USB_DAT_VP USB_SE0_VM | In | — | 8.0 | ns | USB_TXOE_B |
| Disable Delay | USB_DAT_VP USB_SE0_VM | In | — | 10.0 | ns | USB_TXOE_B |
| RX Rise/Fall Time | USB_VP1 | In | — | 3.0 | ns | 35 pF |
| RX Rise/Fall Time | USB_VM1 | In | — | 3.0 | ns | 35 pF |
| RX Skew | USB_VP1 | Out | -4.0 | +4.0 | ns | USB_SE0_VM |
| RX Skew | USB_RCV | Out | -6.0 | +2.0 | ns | USB_DAT_VP |

5 Package Information and Pinout

The i.MX27/MX27L processor is available in a 17 mm × 17 mm, 0.65 mm pitch, 404-pin MAPBGA package and a 19 mm × 19 mm, 0.8 mm pitch, 473-pin MAPBGA package.

5.1 Package Outline Drawing (17 mm × 17 mm–404 pin)

Figure 72 through Figure 76 show the package drawings and dimensions of the production package.

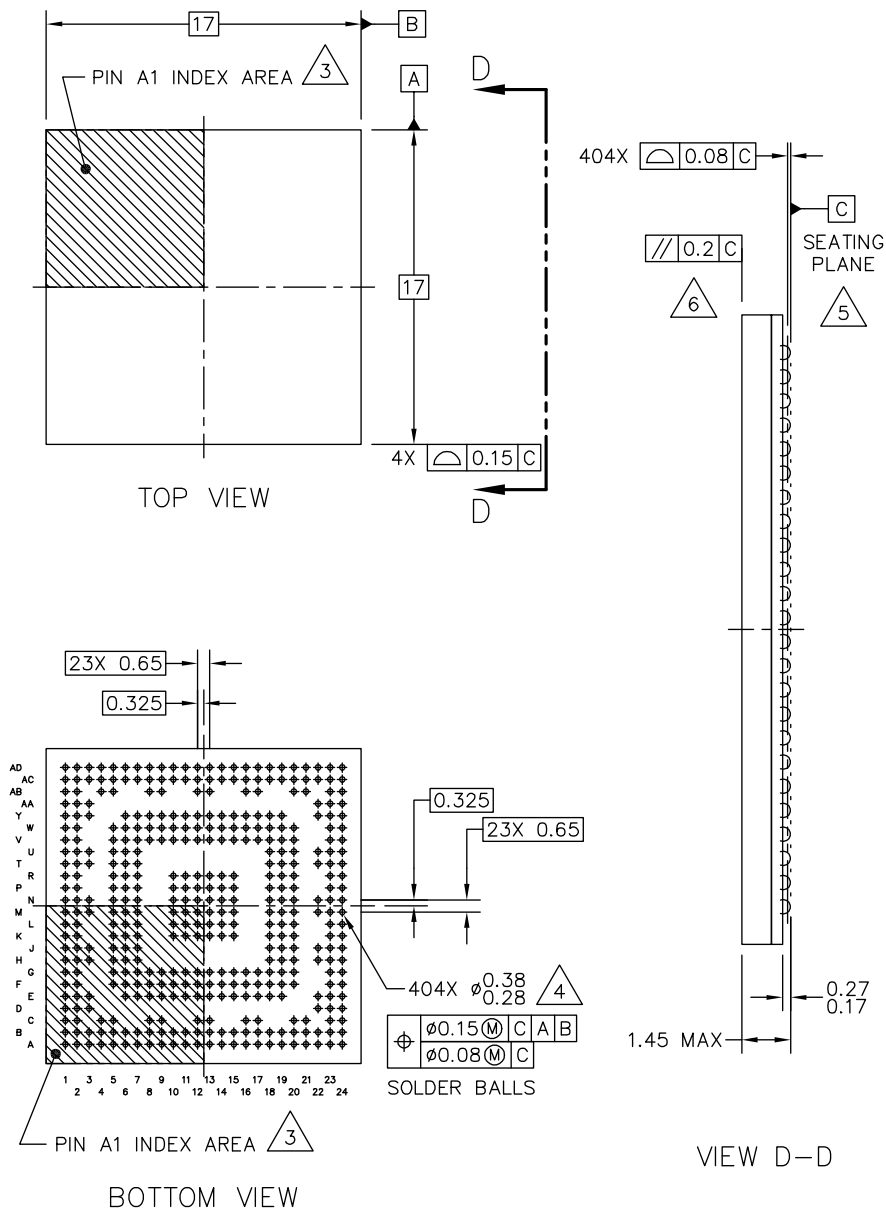
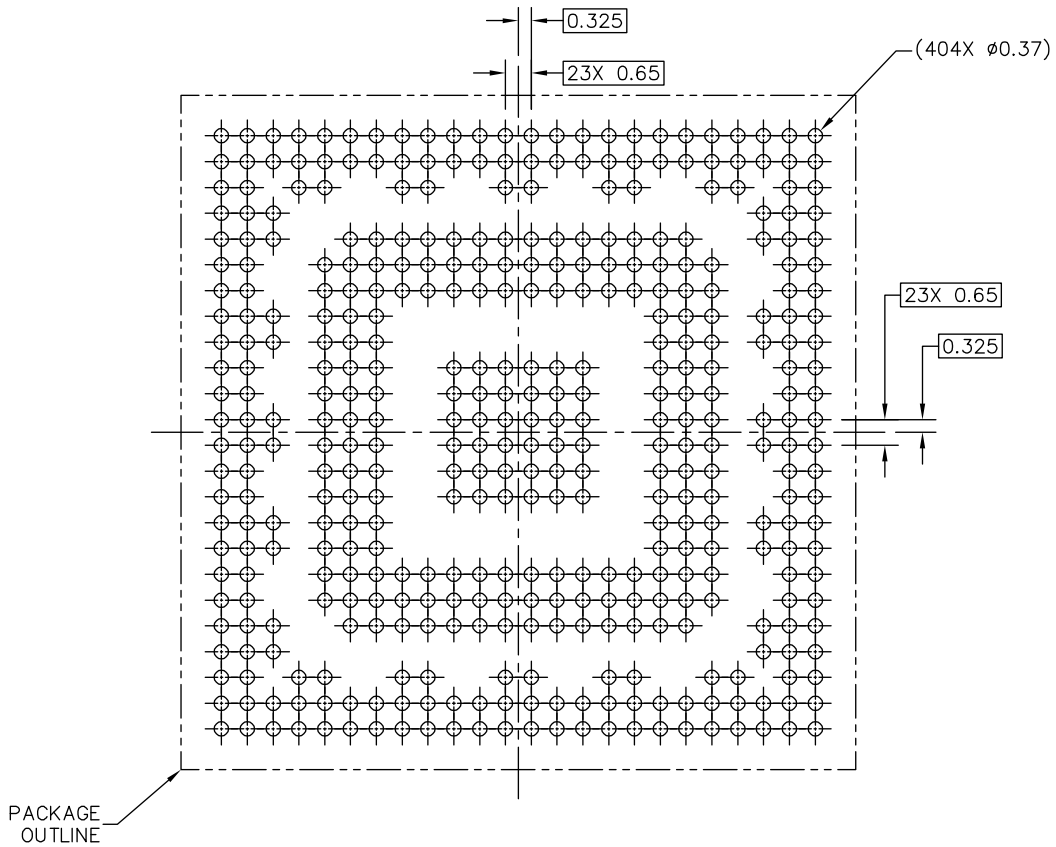


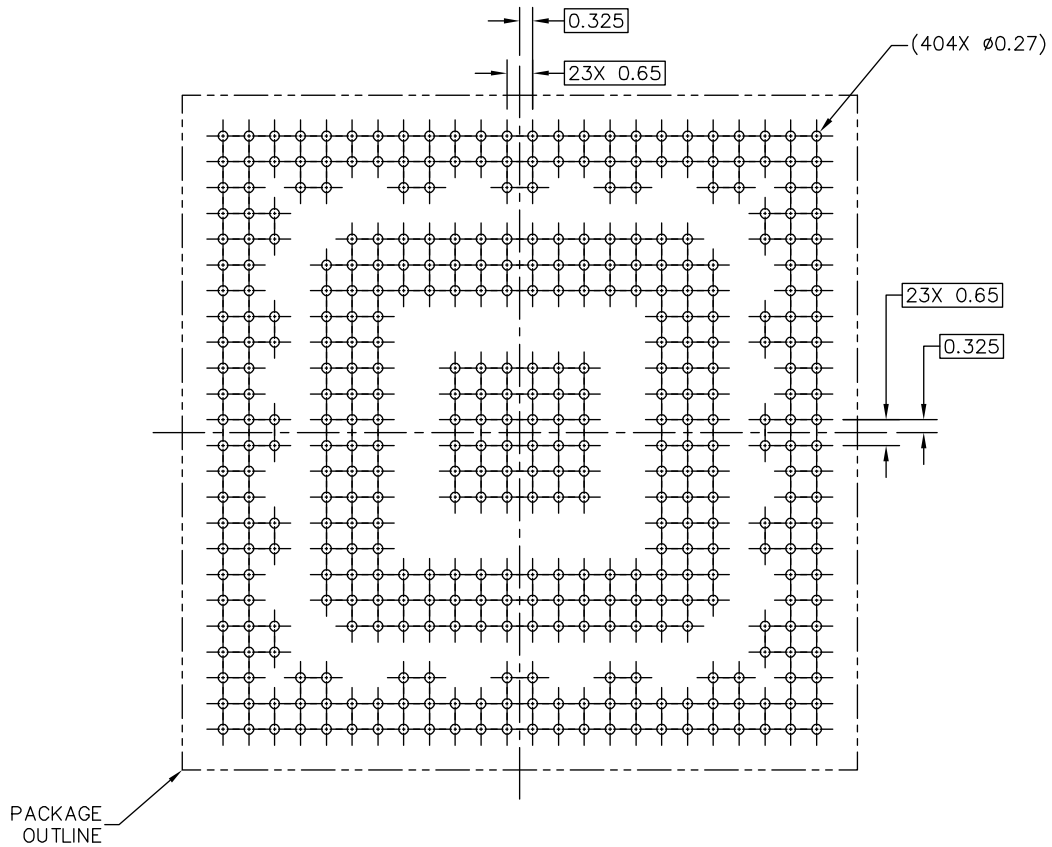
Figure 72. i.MX27/MX27L 17 mm × 17 mm MAPBGA: Mechanical Drawing (sheet 1 of 5)



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

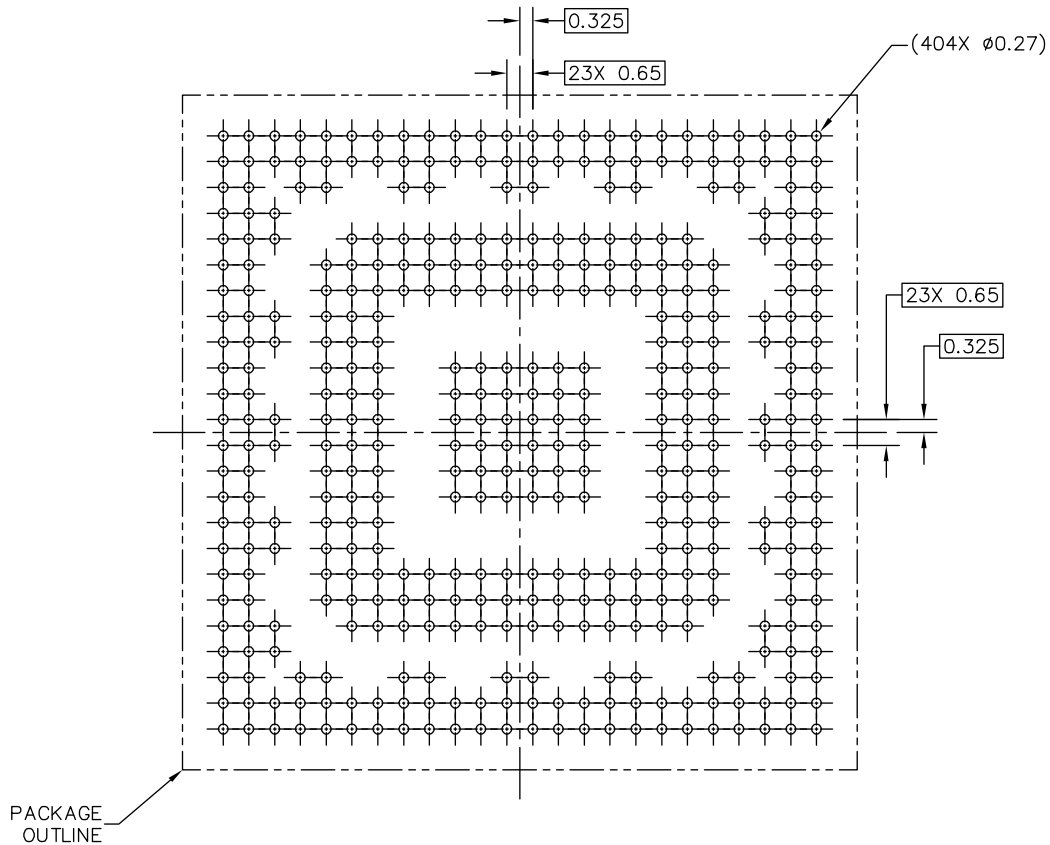
Figure 73. i.MX27/MX27L 17 mm × 17 mm MAPBGA: Mechanical Drawing (Sheet 2 of 5)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

Figure 74. i.MX27/MX27L 17 mm x 17 mm MAPBGA: Mechanical Drawing (Sheet 3 of 5)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

Figure 75. i.MX27/MX27L 17 mm × 17 mm MAPBGA: Mechanical Drawing (Sheet 4 of 5)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 76. i.MX27/MX27L 17 mm × 17 mm MAPBGA: Mechanical Drawing (Sheet 5 of 5)

5.2 Pin Assignments (17 mm × 17 mm–404 pin)

[Table 59](#) identifies the i.MX27 (17 mm × 17 mm) MAPBGA package pin assignments.

[Table 60](#) provides the pin assignments listed by contact name—that is, the list is sorted alphabetically by the name of the contact. The connections of these pins depend solely upon the user application, however there are a few factory test signals that are not used in a normal application. Following is a list of these signals and how they are to be terminated for proper operation of the i.MX27/MX27L processor:

- CLKMODE[1:0]: To ensure proper operation, leave these signals as no connects.
- OSC26M_TEST: To ensure proper operation, leave this signal as no connect.
- EXT_60M: To ensure proper operation, connect this signal to ground.
- EXT_266M: To ensure proper operation, connect this signal to ground.
- Most of the signals shown in [Table 59](#) are multiplexed with other signals. For ease of reference, all of the signals at a particular pad are shown in the form of a compound signal name. Please refer to [Table 3](#) for complete information on the signal multiplexing schemes of these signals.

Table 59. i.MX27 (17 mm × 17 mm) MAPBGA Pin Assignments

| | | | | | | |
|----|--------------------------------|-----------------------------|-------------------------------|-------------|-----------------------------|----|
| 19 | RTCK_OWIRE _PE16 | TMS | | | USBH1_FS_UART4 _RTS_PB26 | 19 |
| 18 | UART1_CTS_PE14 | TDI | | | SD1_D3_CSPI3 _SS_PE21 | 18 |
| 17 | UART3_CTS_ PE10 | UART1_TXD _PE12 | TRST_B | | SD1_D1_PE19 | 17 |
| 16 | UART2_TXD_KP _COL6_PE6 | UART3_TXD _PE8 | UART1_RTS_PE15 | | TDO | 16 |
| 15 | KP_COL2 | KP_COL4 | | | UART3_RTS_PE11 | 15 |
| 14 | UART2_RTS_KP _ROW7_PE4 | KP_COLO | | | UART2_RXD_KP _ROW6_PE7 | 14 |
| 13 | KP_ROW5 | I2C_CLK_PD18 | PWMO_PE5 | | KP_COL3 | 13 |
| 12 | KP_ROW1 | KP_ROW3 | KP_ROW2 | | UART2_CTS_KP _COL7_PE3 | 12 |
| 11 | SSI3_RXDAT_SLDCDC2 _RS_PC29 | SSI3_CLK_ SLCDC2CLK_PC31 | | | KP_ROW4 | 11 |
| 10 | SSI2_RXDAT_GPT5 _TIN_PC25 | SSI2_CLK_GPT4 _TIN_PC27 | | | SSI3_FS_SLDCDC2 _D0_PC28 | 10 |
| 9 | SSI1_RXDAT _PC21 | SSI1_CLK_PC23 | SSI3_TXDAT_ SLCDC2_CS_PC30 | | SSI1_TXDAT_PC22 | 9 |
| 8 | SSI4_RXDAT _PC17 | SSI4_CLK _PC19 | SD2_D2_MSHC _DATA2_PB6 | | TOUT_PC14 | 8 |
| 7 | CSI_HSYNC_ UART5_RTS_PB21 | TIN_PC15 | | | CSI_PIXCLK_PB16 | 7 |
| 6 | CSI_D5_PB17 | CSI_D7_UART5 _RXD_PB19 | | | CSI_D2_UART6 _CTS_PB12 | 6 |
| 5 | CSI_D3_UART6_ RTS_PB13 | CSI_MCLK_PB15 | SD2_CMD_MSHC _BS_PB8 | | | 5 |
| 4 | SD2_CLK_MSHC _SCLK_PB9 | CSI_D1_UART6 _RXD_PB11 | CSI_D0_UART6 _TXD_PB10 | | | 4 |
| 3 | SD2_D3_MSHC _DATA3_PB7 | SPL_SPR_PA27 | | OE_ACD_PA31 | SD2_D1_MSHC _DATA1_PB5 | 3 |
| 2 | GND | GND | CONTRAST _PA30 | PS_PA26 | LD16_PA22 | 2 |
| 1 | GND | GND | SD2_D0_MSHC _DATA0_PB4 | HSYNC_PA28 | REV_PA24 | 1 |
| | A | B | C | D | E | |

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Table 59. i.MX27 (17 mm × 17 mm) MAPBGA Pin Assignments (continued)

| | | | | | | |
|----|---------------------------|--------------------------|-----------------------|-------------------------|-------------------------|----|
| 19 | USBH1_TXDM_UART4_TXD_PB28 | USBH1_SUSP_PB22 | USBOTG_DATA5_PC7 | USBOTG_DATA0_PC9 | RTCVDD | 19 |
| 18 | CSPI1_SCLK_PD29 | USBOTG_DATA1_PC11 | NVDD14 | UPLLVD | RTCVSS | 18 |
| 17 | TCK | SD1_CLK_CSPI3_SCLK_PE23 | | | | 17 |
| 16 | UART1_RXD_PE13 | | | | | 16 |
| 15 | UART3_RXD_PE9 | NVDD8 | | | GND | 15 |
| 14 | KP_COL5 | NVDD9 | | | GND | 14 |
| 13 | KP_COL1 | QVDD | | | GND | 13 |
| 12 | I2C_DATA_PD17 | QVDD | | | GND | 12 |
| 11 | KP_ROW0 | NVDD10 | | | GND | 11 |
| 10 | SSI2_TXDAT_GPT4_TOUT_PC26 | NVDD11 | | | GND | 10 |
| 9 | SSI1_FS_PC20 | SSI2_FS_GPT5_TOUT_PC24 | | | | 9 |
| 8 | SSI4_FS_PC16 | SSI4_TXDAT_PC18 | | | | 8 |
| 7 | CSI_D6_UART5_TXD_PB18 | CSI_VSYNC_UART5_CTS_PB20 | NVDD15 | LD11_PA17 | LD9_PA15 | 7 |
| 6 | CSI_D4_PB14 | CLS_PA25 | LD15_PA21 | LD5_PA11 | LD1_PA7 | 6 |
| 5 | VSYNC_PA29 | LD17_PA23 | LD13_PA19 | LD7_PA13 | LD3_PA9 | 5 |
| 4 | | | | | | 4 |
| 3 | | | LD12_PA18 | LD2_PA8 | | 3 |
| 2 | LD10_PA16 | LD6_PA12 | LD4_PA10 | LD0_PA6 | LSCLK_PA5 | 2 |
| 1 | LD14_PA20 | LD8_PA14 | NFRB_ETMTRACEPKT3_PFO | NFWP_B_ETMTRACEPKT1_PFO | NFALE_ETMPIPE_STATO_PFO | 1 |
| | F | G | H | J | K | |

Table 59. i.MX27 (17 mm × 17 mm) MAPBGA Pin Assignments (continued)

| | | | | | | |
|----|------------------------------|----------|----------------|------------------------|----------|----|
| 19 | NVDD7 | NVDD13 | POWER_ON_RESET | ATA_DATA6_FEC_MDIO_PD8 | FUSEVSS | 19 |
| 18 | NVDD7 | FPMVDD | NVDD6 | NVDD6 | FUSEVDD | 18 |
| 17 | | | | | | 17 |
| 16 | | | | | | 16 |
| 15 | GND | UPLLSS | GND | FPMVSS | MPLLSS | 15 |
| 14 | GND | GND | GND | GND | GND | 14 |
| 13 | GND | GND | GND | GND | GND | 13 |
| 12 | GND | GND | GND | GND | GND | 12 |
| 11 | GND | GND | GND | GND | GND | 11 |
| 10 | GND | GND | GND | GND | GND | 10 |
| 9 | | | | | | 9 |
| 8 | | | | | | 8 |
| 7 | NVDD12 | NVDD1 | NVDD1 | QVDD | NVDD2 | 7 |
| 6 | NFCLE_ETMTRAC EPKT0_PPF1 | D9 | D1 | A12 | A7 | 6 |
| 5 | NFRE_B_ETMPIP ESTAT1_PPF5 | D13 | D3 | A9 | A5 | 5 |
| 4 | | | | | | 4 |
| 3 | | D11 | D5 | | | 3 |
| 2 | NFCE_B_ETMTRACE PKT2_PPF3 | D15 | D7 | D8 | D4 | 2 |
| 1 | NFWE_B_ETMPIP STAT2_PPF6 | D14 | D12 | D10 | D6 | 1 |
| | L | M | N | P | R | |

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Table 59. i.MX27 (17 mm × 17 mm) MAPBGA Pin Assignments (continued)

| | | | | | | |
|----|--------|-------|-------------|---------------------------|---------------------------|----|
| 19 | AVSS | BOOT2 | OSC26M_TEST | PC_VS2_ATA _DA0_P13 | PC_PWRON_ATA _DA2_P16 | 19 |
| 18 | MPLLVD | AVDD | NVDD5 | PC_CD1_B_ATA _DIOR_P20 | PC_WAIT_B_ATA _CS1_P18 | 18 |
| 17 | | | NVDD5 | EXT_60M | OE_B | 17 |
| 16 | | | QVDD | EB0_B | LBA_B | 16 |
| 15 | | | QVDD | CS5_B_ETMTRACE CLK_P22 | CS2_B | 15 |
| 14 | | | QVDD | CS3_B | SDCKE1 | 14 |
| 13 | | | NVDD4 | SDWE_B | DQM2 | 13 |
| 12 | | | NVDD3 | DQM1 | SD2 | 12 |
| 11 | | | NVDD3 | A16 | A15 | 11 |
| 10 | | | NVDD2 | SD6 | SD8 | 10 |
| 9 | | | NVDD2 | SD13 | SD12 | 9 |
| 8 | | | A19 | SDQS1 | SD15 | 8 |
| 7 | NVDD2 | NVDD2 | SD29 | SD25 | SD18 | 7 |
| 6 | A1 | A25 | SD28 | SDQS2 | A20 | 6 |
| 5 | SDBA1 | SD31 | SD26 | SD23 | | 5 |
| 4 | | | | | | 4 |
| 3 | MA10 | A3 | | | SDQS3 | 3 |
| 2 | D0 | A11 | A6 | A2 | SDBA0 | 2 |
| 1 | D2 | A13 | A8 | A4 | A0 | 1 |
| | T | U | V | W | Y | |

Table 59. i.MX27 (17 mm × 17 mm) MAPBGA Pin Assignments (continued)

| | | | | | |
|----|------|-------|----------------------------|-----------------------------|----|
| | AA | AB | AC | AD | |
| 1 | SD30 | A23 | GND | GND | 1 |
| 2 | A24 | SD24 | GND | GND | 2 |
| 3 | SD27 | | A22 | SD22 | 3 |
| 4 | | A21 | SD20 | SD19 | 4 |
| 5 | | SD21 | SD17 | SD16 | 5 |
| 6 | | | A18 | SD14 | 6 |
| 7 | | | A17 | SD11 | 7 |
| 8 | | SD10 | SD9 | SD7 | 8 |
| 9 | | A14 | SD5 | SDQS0 | 9 |
| 10 | | | SD4 | SD3 | 10 |
| 11 | | | SD1 | DQM3 | 11 |
| 12 | | SD0 | A10 | DQM0 | 12 |
| 13 | | RAS_B | CAS_B | SDCLK | 13 |
| 14 | | | SDCKE0 | SDCLK_B | 14 |
| 15 | | | RW_B | CS4_B_ETMTRACE SYNC_PF21 | 15 |
| 16 | | CS1_B | ECB_B | CS0_B | 16 |
| 17 | | BCLK | EB1_B | CLKO_PF15 | 17 |
| 18 | | | JTAG_CTRL | EXT_266M | 18 |
| 19 | | | PC_CD2_B_ATA _DIOW_PF19 | PC_READY_ATA _CS0_PF17 | 19 |

Table 60 shows the device pin list, sorted by signal identification, including pad locations for ground and power supply voltages.

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing

| Contact Name | Location |
|------------------------------|----------|
| A0 | Y1 |
| A1 | T6 |
| A10 | AC12 |
| A11 | U2 |
| A12 | P6 |
| A13 | U1 |
| A14 | AB9 |
| A15 | Y11 |
| A16 | W11 |
| A17 | AC7 |
| A18 | AC6 |
| A19 | V8 |
| A2 | W2 |
| A20 | Y6 |
| A21 | AB4 |
| A22 | AC3 |
| A23 | AB1 |
| A24 | AA2 |
| A25 | U6 |
| A3 | U3 |
| A4 | W1 |
| A5 | R5 |
| A6 | V2 |
| A7 | R6 |
| A8 | V1 |
| A9 | P5 |
| ATA_DATA0_SD3_D0_PD2 | R23 |
| ATA_DATA1_SD3_D1_PD3 | R24 |
| ATA_DATA10_ETMTRACEPKT9_PD12 | R20 |
| ATA_DATA11_ETMTRACEPKT8_PD13 | W23 |
| ATA_DATA12_ETMTRACEPKT7_PD14 | U23 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|------------------------------|----------|
| ATA_DATA13_ETMTRACEPKT6_PD15 | W24 |
| ATA_DATA14_ETMTRACEPKT5_PD16 | T20 |
| ATA_DATA15_ETMTRACEPKT4_PF23 | Y24 |
| ATA_DATA2_SD3_D2_PD4 | P20 |
| ATA_DATA3_SD3_D3_PD5 | T24 |
| ATA_DATA4_ETMTRACEPKT14_PD6 | T22 |
| ATA_DATA5_ETMTRACEPKT13_PD7 | T23 |
| ATA_DATA6_FEC_MDIO_PD8 | P19 |
| ATA_DATA7_ETMTRACEPKT12_PD9 | U24 |
| ATA_DATA8_ETMTRACEPKT11_PD10 | U22 |
| ATA_DATA9_ETMTRACEPKT10_PD11 | V24 |
| AVDD | U18 |
| AVSS | T19 |
| BCLK | AB17 |
| BOOT0 | V23 |
| BOOT1 | Y23 |
| BOOT2 | U19 |
| BOOT3 | Y22 |
| CAS_B | AC13 |
| CLKMODE0 | AB20 |
| CLKMODE1 | AB21 |
| CLKO_PF15 | AD17 |
| CLS_PA25 | G6 |
| CONTRAST_PA30 | C2 |
| CS0_B | AD16 |
| CS1_B | AB16 |
| CS2_B | Y15 |
| CS3_B | W14 |
| CS4_B_ETMTRACESYNC_PF21 | AD15 |
| CS5_B_ETMTRACECLK_PF22 | W15 |
| CSI_D0_UART6_TXD_PB10 | C4 |
| CSI_D1_UART6_RXD_PB11 | B4 |
| CSI_D2_UART6_CTS_PB12 | E6 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|-----------------------------|----------|
| CSI_D3_UART6_RTS_PB13 | A5 |
| CSI_D4_PB14 | F6 |
| CSI_D5_PB17 | A6 |
| CSI_D6_UART5_TXD_PB18 | F7 |
| CSI_D7_UART5_RXD_PB19 | B6 |
| CSI_HSYNC_UART5_RTS_PB21 | A7 |
| CSI_MCLK_PB15 | B5 |
| CSI_PIXCLK_PB16 | E7 |
| CSI_VSYNC_UART5_CTS_PB20 | G7 |
| CSPI1_MISO_PD30 | A22 |
| CSPI1_MOSI_PD31 | C21 |
| CSPI1_RDY_PD25 | B21 |
| CSPI1_SCLK_PD29 | F18 |
| CSPI1_SS0_PD28 | B22 |
| CSPI1_SS1_PD27 | C20 |
| CSPI1_SS2_USBH2_DATA5_PD26 | E22 |
| CSPI2_MISO_USBH2_DATA2_PD23 | G20 |
| CSPI2_MOSI_USBH2_DATA1_PD24 | E23 |
| CSPI2_SCLK_USBH2_DATA0_PD22 | D23 |
| CSPI2_SS0_USBH2_DATA6_PD21 | F20 |
| CSPI2_SS1_USBH2_DATA3_PD20 | C23 |
| CSPI2_SS2_USBH2_DATA4_PD19 | D22 |
| D0 | T2 |
| D1 | N6 |
| D10 | P1 |
| D11 | M3 |
| D12 | N1 |
| D13 | M5 |
| D14 | M1 |
| D15 | M2 |
| D2 | T1 |
| D3 | N5 |
| D4 | R2 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|--------------|----------|
| D5 | N3 |
| D6 | R1 |
| D7 | N2 |
| D8 | P2 |
| D9 | M6 |
| DQM0 | AD12 |
| DQM1 | W12 |
| DQM2 | Y13 |
| DQM3 | AD11 |
| EB0_B | W16 |
| EB1_B | AC17 |
| ECB_B | AC16 |
| EXT_266M | AD18 |
| EXT_60M | W17 |
| EXTAL26M | AB24 |
| EXTAL32K | M24 |
| FPMVDD | M18 |
| FPMVSS | P15 |
| FUSEVDD | R18 |
| FUSEVSS | R19 |
| GND | A1 |
| GND | A2 |
| GND | A23 |
| GND | A24 |
| GND | AC1 |
| GND | AC2 |
| GND | AC23 |
| GND | AC24 |
| GND | AD1 |
| GND | AD2 |
| GND | AD23 |
| GND | AD24 |
| GND | B1 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|--------------|----------|
| GND | B2 |
| GND | B23 |
| GND | B24 |
| GND | K10 |
| GND | K11 |
| GND | K12 |
| GND | K13 |
| GND | K14 |
| GND | K15 |
| GND | L10 |
| GND | L11 |
| GND | L12 |
| GND | L13 |
| GND | L14 |
| GND | L15 |
| GND | M10 |
| GND | M11 |
| GND | M12 |
| GND | M13 |
| GND | M14 |
| GND | N10 |
| GND | N11 |
| GND | N12 |
| GND | N13 |
| GND | N14 |
| GND | N15 |
| GND | P10 |
| GND | P11 |
| GND | P12 |
| GND | P13 |
| GND | P14 |
| GND | R10 |
| GND | R11 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|----------------------|----------|
| GND | R12 |
| GND | R13 |
| GND | R14 |
| HSYNC_PA28 | D1 |
| I2C_CLK_PD18 | B13 |
| I2C_DATA_PD17 | F12 |
| I2C2_SCL_PC6 | F24 |
| I2C2_SDA_PC5 | J22 |
| IOIS16_ATA_INTRQ_PF9 | U20 |
| JTAG_CTRL | AC18 |
| KP_COL0 | B14 |
| KP_COL1 | F13 |
| KP_COL2 | A15 |
| KP_COL3 | E13 |
| KP_COL4 | B15 |
| KP_COL5 | F14 |
| KP_ROW0 | F11 |
| KP_ROW1 | A12 |
| KP_ROW2 | C12 |
| KP_ROW3 | B12 |
| KP_ROW4 | E11 |
| KP_ROW5 | A13 |
| LBA_B | Y16 |
| LD0_PA6 | J2 |
| LD1_PA7 | K6 |
| LD10_PA16 | F2 |
| LD11_PA17 | J7 |
| LD12_PA18 | H3 |
| LD13_PA19 | H5 |
| LD14_PA20 | F1 |
| LD15_PA21 | H6 |
| LD16_PA22 | E2 |
| LD17_PA23 | G5 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|-------------------------|----------|
| LD2_PA8 | J3 |
| LD3_PA9 | K5 |
| LD4_PA10 | H2 |
| LD5_PA11 | J6 |
| LD6_PA12 | G2 |
| LD7_PA13 | J5 |
| LD8_PA14 | G1 |
| LD9_PA15 | K7 |
| LSCLK_PA5 | K2 |
| MA10 | T3 |
| MPLLVDD | T18 |
| MPLLVSS | R15 |
| NFALE_ETMPIPESTAT0_PF4 | K1 |
| NFCE_B_ETMTRACEPKT2_PF3 | L2 |
| NFCLE_ETMTRACEPKT0_PF1 | L6 |
| NFRB_ETMTRACEPKT3_PF0 | H1 |
| NFRE_B_ETMPIPESTAT1_PF5 | L5 |
| NFWE_B_ETMPIPESTAT2_PF6 | L1 |
| NFWP_B_ETMTRACEPKT1_PF2 | J1 |
| NVDD1 | M7 |
| NVDD1 | N7 |
| NVDD10 | G11 |
| NVDD11 | G10 |
| NVDD12 | L7 |
| NVDD13 | M19 |
| NVDD14 | H18 |
| NVDD15 | H7 |
| NVDD2 | R7 |
| NVDD2 | T7 |
| NVDD2 | U7 |
| NVDD2 | V10 |
| NVDD2 | V9 |
| NVDD3 | V11 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|--------------------------|----------|
| NVDD3 | V12 |
| NVDD4 | V13 |
| NVDD5 | V17 |
| NVDD5 | V18 |
| NVDD6 | N18 |
| NVDD6 | P18 |
| NVDD7 | L18 |
| NVDD7 | L19 |
| NVDD8 | G15 |
| NVDD9 | G14 |
| OE_ACD_PA31 | D3 |
| OE_B | Y17 |
| OSC26M_TEST | V19 |
| OSC26VDD | AA23 |
| OSC26VSS | AB23 |
| OSC32K_BYPASS | L24 |
| OSC32VDD | M23 |
| OSC32VSS | N23 |
| PC_BVD1_ATA_DMARQ_PF12 | AD20 |
| PC_BVD2_ATA_DMACK_PF11 | W20 |
| PC_CD1_B_ATA_DIOR_PF20 | W18 |
| PC_CD2_B_ATA_DIOW_PF19 | AC19 |
| PC_POE_ATA_BUFFER_EN_PF7 | V20 |
| PC_PWRON_ATA_DA2_PF16 | Y19 |
| PC_READY_ATA_CS0_PF17 | AD19 |
| PC_RST_ATA_RESET_B_PF10 | AC21 |
| PC_RW_B_ATA_IORDY_PF8 | AD21 |
| PC_VS1_ATA_DA1_PF14 | AC20 |
| PC_VS2_ATA_DA0_PF13 | W19 |
| PC_WAIT_B_ATA_CS1_PF18 | Y18 |
| POR_B | AD22 |
| POWER_CUT | N22 |
| POWER_ON_RESET | N19 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|-------------------------|----------|
| PS_PA26 | D2 |
| PWMO_PE5 | C13 |
| QVDD | G12 |
| QVDD | G13 |
| QVDD | G16 |
| QVDD | P7 |
| QVDD | V14 |
| QVDD | V15 |
| QVDD | V16 |
| RAS_B | AB13 |
| RESET_IN_B | AC22 |
| RESET_OUT_B_PE17 | AA22 |
| REV_PA24 | E1 |
| RTCK_OWIRE_PE16 | A19 |
| RTCVDD | K19 |
| RTCVSS | K18 |
| RW_B | AC15 |
| SD0 | AB12 |
| SD1 | AC11 |
| SD1_CLK_CSPI3_SCLK_PE23 | G17 |
| SD1_CMD_CSPI3_MOSI_PE22 | A21 |
| SD1_D0_CSPI3_MISO_PE18 | A20 |
| SD1_D1_PE19 | E17 |
| SD1_D2_PE20 | B20 |
| SD1_D3_CSPI3_SS_PE21 | E18 |
| SD10 | AB8 |
| SD11 | AD7 |
| SD12 | Y9 |
| SD13 | W9 |
| SD14 | AD6 |
| SD15 | Y8 |
| SD16 | AD5 |
| SD17 | AC5 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|---------------------------|----------|
| SD18 | Y7 |
| SD19 | AD4 |
| SD2 | Y12 |
| SD2_CLK_MSHC_SCLK_PB9 | A4 |
| SD2_CMD_MSHC_BS_PB8 | C5 |
| SD2_D0_MSHC_DATA0_PB4 | C1 |
| SD2_D1_MSHC_DATA1_PB5 | E3 |
| SD2_D2_MSHC_DATA2_PB6 | C8 |
| SD2_D3_MSHC_DATA3_PB7 | A3 |
| SD20 | AC4 |
| SD21 | AB5 |
| SD22 | AD3 |
| SD23 | W5 |
| SD24 | AB2 |
| SD25 | W7 |
| SD26 | V5 |
| SD27 | AA3 |
| SD28 | V6 |
| SD29 | V7 |
| SD3 | AD10 |
| SD3_CLK_ETMTRACEPKT15_PD1 | P24 |
| SD3_CMD_PD0 | P23 |
| SD30 | AA1 |
| SD31 | U5 |
| SD4 | AC10 |
| SD5 | AC9 |
| SD6 | W10 |
| SD7 | AD8 |
| SD8 | Y10 |
| SD9 | AC8 |
| SDBA0 | Y2 |
| SDBA1 | T5 |
| SDCKE0 | AC14 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|---------------------------|----------|
| SDCKE1 | Y14 |
| SDCLK | AD13 |
| SDCLK_B | AD14 |
| SDQS0 | AD9 |
| SDQS1 | W8 |
| SDQS2 | W6 |
| SDQS3 | Y3 |
| SDWE_B | W13 |
| SPL_SPR_PA27 | B3 |
| SSI1_CLK_PC23 | B9 |
| SSI1_FS_PC20 | F9 |
| SSI1_RXDAT_PC21 | A9 |
| SSI1_TXDAT_PC22 | E9 |
| SSI2_CLK_GPT4_TIN_PC27 | B10 |
| SSI2_FS_GPT5_TOUT_PC24 | G9 |
| SSI2_RXDAT_GPT5_TIN_PC25 | A10 |
| SSI2_TXDAT_GPT4_TOUT_PC26 | F10 |
| SSI3_CLK_SLCDC2_CLK_PC31 | B11 |
| SSI3_FS_SLCDC2_D0_PC28 | E10 |
| SSI3_RXDAT_SLCDC2_RS_PC29 | A11 |
| SSI3_TXDAT_SLCDC2_CS_PC30 | C9 |
| SSI4_CLK_PC19 | B8 |
| SSI4_FS_PC16 | F8 |
| SSI4_RXDAT_PC17 | A8 |
| SSI4_TXDAT_PC18 | G8 |
| TCK | F17 |
| TDI | B18 |
| TDO | E16 |
| TIN_PC15 | B7 |
| TMS | B19 |
| TOUT_PC14 | E8 |
| TRST_B | C17 |
| UART1_CTS_PE14 | A18 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|---------------------------|----------|
| UART1_RTS_PE15 | C16 |
| UART1_RXD_PE13 | F16 |
| UART1_TXD_PE12 | B17 |
| UART2_CTS_KP_COL7_PE3 | E12 |
| UART2_RTS_KP_ROW7_PE4 | A14 |
| UART2_RXD_KP_ROW6_PE7 | E14 |
| UART2_TXD_KP_COL6_PE6 | A16 |
| UART3_CTS_PE10 | A17 |
| UART3_RTS_PE11 | E15 |
| UART3_RXD_PE9 | F15 |
| UART3_TXD_PE8 | B16 |
| UPLLVD | J18 |
| UPLLVSS | M15 |
| USB_OC_B_PB24 | H20 |
| USB_PWR_PB23 | F23 |
| USBH1_FS_UART4_RTS_PB26 | E19 |
| USBH1_OE_B_PB27 | C24 |
| USBH1_RCV_PB25 | H22 |
| USBH1_RXDM_PB30 | J20 |
| USBH1_RXDP_UART4_RXD_PB31 | E24 |
| USBH1_SUSP_PB22 | G19 |
| USBH1_TXDM_UART4_TXD_PB28 | F19 |
| USBH1_TXDP_UART4_CTS_PB29 | D24 |
| USBH2_CLK_PA0 | H23 |
| USBH2_DATA7_PA2 | J24 |
| USBH2_DIR_PA1 | K23 |
| USBH2_NXT_PA3 | L20 |
| USBH2_STP_PA4 | J23 |
| USBOTG_CLK_PE24 | K24 |
| USBOTG_DATA0_PC9 | J19 |
| USBOTG_DATA1_PC11 | G18 |
| USBOTG_DATA2_PC10 | G23 |
| USBOTG_DATA3_PC13 | K20 |

Table 60. i.MX27 (17 mm × 17 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|-------------------------|----------|
| USBOTG_DATA4_PC12 | H24 |
| USBOTG_DATA5_PC7 | H19 |
| USBOTG_DATA6_PC8 | G24 |
| USBOTG_DATA7_PE25 | M22 |
| USBOTG_DIR_KP_ROW7A_PE2 | N20 |
| USBOTG_NXT_KP_COL6A_PE0 | M20 |
| USBOTG_STP_KP_ROW6A_PE1 | L23 |
| VSYNC_PA29 | F5 |
| XTAL26M | AA24 |
| XTAL32K | N24 |

5.3 Package Outline Drawing (19 mm × 19 mm–473 pin)

Figure 77 shows the package drawings and dimensions of the production package.

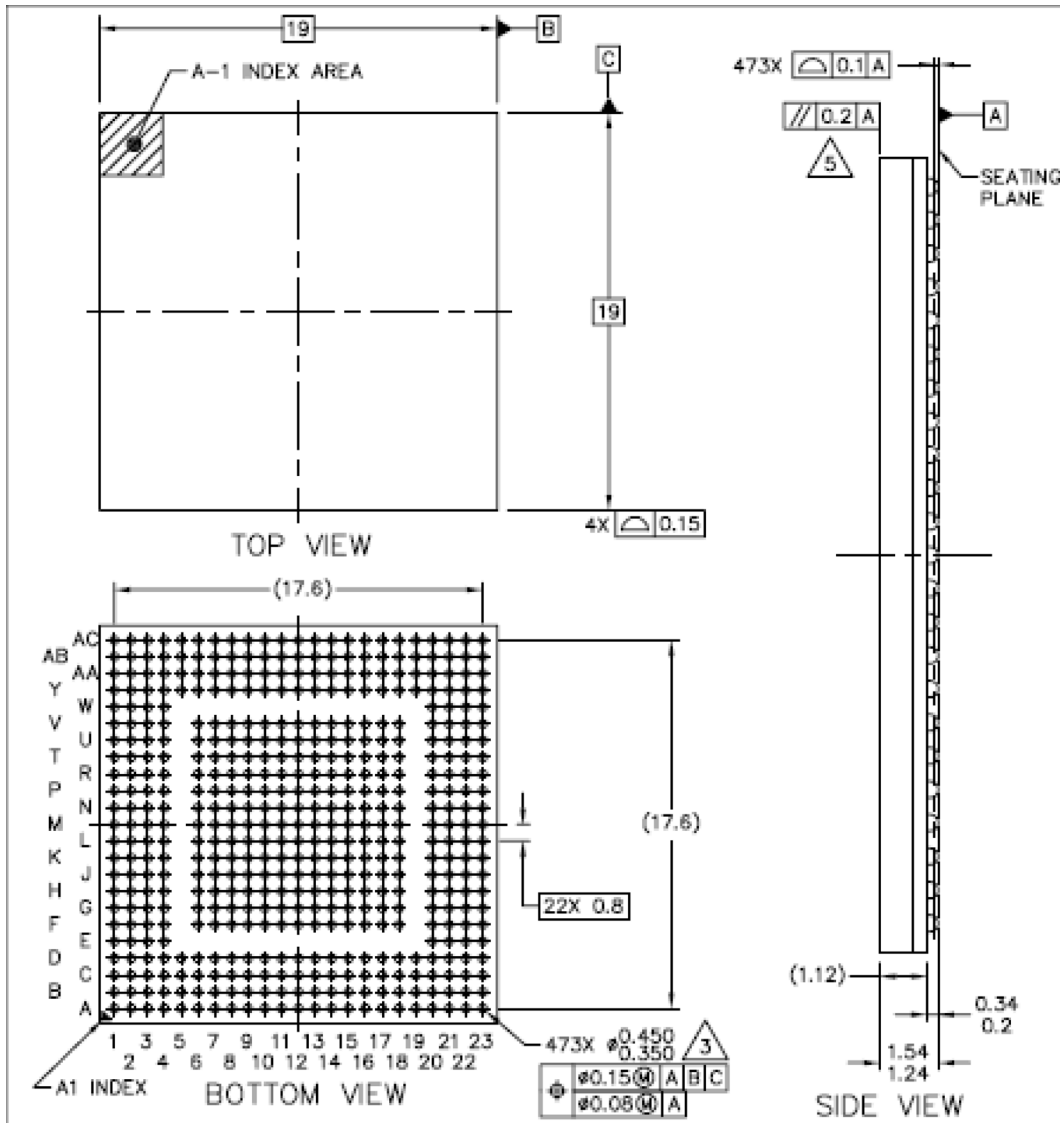


Figure 77. i.MX27/MX27L (19 mm × 19 mm) MAPBGA: Mechanical Drawing

5.4 Pin Assignments (19 mm × 19 mm–473 pin)

[Table 61](#) identifies the i.MX27 (19 mm × 19 mm) MAPBGA package pin assignments.

[Table 62](#) provides the pin assignments listed by contact name—that is, the list is sorted alphabetically by the name of the contact. The connections of these pins depend solely upon the user application, however there are a few factory test signals that are not used in a normal application. Following is a list of these signals and how they are to be terminated for proper operation of the i.MX27/MX27L processor:

- CLKMODE[1:0]: To ensure proper operation, leave these signals as no connects.
- OSC26M_TEST: To ensure proper operation, leave this signal as no connect.
- EXT_60M: To ensure proper operation, connect this signal to ground.
- EXT_266M: To ensure proper operation, connect this signal to ground.
- Most of the signals shown in [Table 62](#) are multiplexed with other signals. For ease of reference, all of the signals at a particular pad are shown in the form of a compound signal name. Refer to [Table 3](#) for complete information on the signal multiplexing schemes of these signals.

Table 61. i.MX27 (19 mm × 19 mm) MAPBGA Pin Assignments

| | | | | | | |
|----|------------------------------|-------------------------------|-------------------------------|----------------------------|-----------|----|
| 18 | RTCK_OWIRE _PE16 | SD1_D0_CSPI3 _MISO_PE18 | TMS | SD1_D3_CSPI3 _SS_PE21 | | 18 |
| 17 | UART1_RXD _PE13 | UART1_CTS _PE14 | UART1_RTS_ PE15 | TDI | | 17 |
| 16 | UART3_TXD _PE8 | UART3_CTS _PE10 | UART3_RTS_ PE11 | TDO | | 16 |
| 15 | KP_COL4 | KP_COL5 | UART2_RXD_KP_ ROW6_PE7 | UART1_TXD_PE12 | | 15 |
| 14 | PWMO_PE5 | KP_COL2 | KP_COL3 | UART2_TXD_KP_ COL6_PE6 | | 14 |
| 13 | UART2_CTS_KP _COL7_PE3 | I2C_CLK_ PD18 | UART2_RTS_KP_ ROW7_PE4 | KP_COL0 | | 13 |
| 12 | KP_ROW3 | KP_ROW2 | KP_ROW4 | KP_ROW5 | | 12 |
| 11 | SSI3_CLK_SLCDC2 _CLK_PC31 | SSI3_RXDAT_SLCDC2 _RS_PC29 | SSI3_TXDAT_SLCDC2_ CS_PC30 | KP_ROW1 | | 11 |
| 10 | SSI3_FS_SLCDC2 _D0_PC28 | SSI2_RXDAT_GPT5 _TIN_PC25 | SSI2_FS_GPT5_TOUT _PC24 | SSI2_CLK_GPT4_ TIN_PC27 | | 10 |
| 9 | SSI1_CLK_ PC23 | SSI1_TXDAT _PC22 | SSI1_FS_PC20 | SSI1_RXDAT _PC21 | | 9 |
| 8 | SSI4_CLK_ PC19 | SSI4_RXDAT _PC17 | TIN_PC15 | SSI4_FS_PC16 | | 8 |
| 7 | TOUT_PC14 | CSI_HSYNC_UART5 _RTS_PB21 | CSI_D7_UART5_ RXD_PB19 | CSI_D6_UART5 _TXD_PB18 | | 7 |
| 6 | CSI_D5_PB17 | CSI_PIXCLK _PB16 | CSI_D4_PB14 | CSI_D3_UART6 _RTS_PB13 | | 6 |
| 5 | CSI_MCLK _PB15 | CSI_D2_UART6_ CTS_PB12 | CSI_D0_UART6_ TXD_PB10 | SD2_CLK_MSHC _SCLK_PB9 | | 5 |
| 4 | CSI_D1_UART6 _RXD_PB11 | SD2_CMD_MSHC _BS_PB8 | SD2_D2_MSHC_ DATA2_PB6 | VSYNC_PA29 | CLS_PA25 | 4 |
| 3 | SD2_D3_MSHC _DATA3_PB7 | SD2_D1_MSHC_ DATA1_PB5 | OE_ACD_ PA31 | SPL_SPR_PA27 | LD17_PA23 | 3 |
| 2 | GND | GND | CONTRAST _PA30 | PS_PA26 | LD16_PA22 | 2 |
| 1 | GND | GND | SD2_D0_MSHC_ DATA0_PB4 | HSYNC_PA28 | LD15_PA21 | 1 |
| | A | B | C | D | E | |

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Table 61. i.MX27 (19 mm × 19 mm) MAPBGA Pin Assignments (continued)

| | | | | | | | |
|----|---------------------------|-----------------|----------|----------|--------------------------|--------------------------|----|
| 18 | GND | USBH1_SUSP_PB22 | NVDD14 | NVDD7 | NVDD7 | NVDD13 | 18 |
| 17 | QVDD | QVDD | QVDD | NVDD14 | UPLLVDD | UPLLVSS | 17 |
| 16 | TRST_B | NVDD8 | QVDD | QVDD | QVDD | QVDD | 16 |
| 15 | TCK | NVDD8 | QVDD | GND | GND | GND | 15 |
| 14 | UART3_RXD_PE9 | NVDD9 | QVDD | GND | GND | GND | 14 |
| 13 | KP_COL1 | NVDD9 | QVDD | GND | GND | GND | 13 |
| 12 | I2C_DATA_PD17 | NVDD10 | QVDD | GND | GND | GND | 12 |
| 11 | KP_ROW0 | NVDD10 | QVDD | GND | GND | GND | 11 |
| 10 | SSI2_TXDAT_GPT4_TOUT_PC26 | NVDD11 | QVDD | GND | GND | GND | 10 |
| 9 | SSI4_TXDAT_PC18 | NVDD11 | QVDD | GND | GND | GND | 9 |
| 8 | CSI_VSYNC_UART5_CTS_PB20 | NVDD11 | QVDD | QVDD | QVDD | QVDD | 8 |
| 7 | GND | GND | QVDD | NVDD12 | NVDD1 | NVDD1 | 7 |
| 6 | GND | NVDD15 | NVDD15 | NVDD12 | NVDD1 | NVDD1 | 6 |
| 5 | | | | | | | 5 |
| 4 | REV_PA24 | LD11_PA17 | LD9_PA15 | LD4_PA10 | LSCLK_PA5 | NFCLE_ETMTRACEPKT0_PPF1 | 4 |
| 3 | LD14_PA20 | LD10_PA16 | LD6_PA12 | LD2_PA8 | NFCE_B_ETMTRACEPKT2_PPF3 | NFRE_B_ETMPIPESTAT1_PPF5 | 3 |
| 2 | LD12_PA18 | LD7_PA13 | LD5_PA11 | LD1_PA7 | NFRB_ETMTRACEPKT3_PPF0 | NFALE_ETMPIPESTAT0_PPF4 | 2 |
| 1 | LD13_PA19 | LD8_PA14 | LD3_PA9 | LD0_PA6 | NFWP_B_ETMTRACEPKT1_PPF2 | NFWE_B_ETMPIPESTAT2_PPF6 | 1 |
| | F | G | H | J | K | L | |

Table 61. i.MX27 (19 mm × 19 mm) MAPBGA Pin Assignments (continued)

| | | | | | | |
|----|----------|----------|----------|----------|----------|----|
| 18 | RTCVD | FPMVD | NVDD6 | FUSEVD | BOOT2 | 18 |
| 17 | RTCVSS | FPMVSS | NVDD6 | FUSEVSS | MPLLSS | 17 |
| 16 | QVDD | QVDD | QVDD | QVDD | QVDD | 16 |
| 15 | GND | GND | GND | GND | QVDD | 15 |
| 14 | GND | GND | GND | GND | QVDD | 14 |
| 13 | GND | GND | GND | GND | QVDD | 13 |
| 12 | GND | GND | GND | GND | QVDD | 12 |
| 11 | GND | GND | GND | GND | QVDD | 11 |
| 10 | GND | GND | GND | GND | QVDD | 10 |
| 9 | GND | GND | GND | GND | QVDD | 9 |
| 8 | QVDD | QVDD | QVDD | QVDD | QVDD | 8 |
| 7 | QVDD | D0 | NVDD2 | NVDD2 | NVDD2 | 7 |
| 6 | D11 | D7 | MA10 | NVDD2 | A1 | 6 |
| 5 | | | | | | 5 |
| 4 | D13 | D8 | NC_P4_1 | A12 | A7 | 4 |
| 3 | D12 | D5 | D3 | A13 | A8 | 3 |
| 2 | D14 | D9 | D4 | D1 | A9 | 2 |
| 1 | D15 | D10 | D6 | D2 | A11 | 1 |
| | M | N | P | R | T | |

Table 61. i.MX27 (19 mm × 19 mm) MAPBGA Pin Assignments (continued)

| | | | | | | |
|----|--------|----------------------------|-------|-----------------------------|----------------------------|----|
| 18 | AVSS | GND | | PC_VS1_ATA_ DA1_PF14 | PC_WAIT_B _ATA_CS1_PF18 | 18 |
| 17 | AVDD | MPLLVD | | PC_CD2_B_ATA_ DIOW_PF19 | EXT_60M | 17 |
| 16 | NVDD4 | NVDD5 | | OE_B | EB0_B | 16 |
| 15 | NVDD4 | NVDD5 | | CS0_B | CS1_B | 15 |
| 14 | NVDD4 | CS5_B_ETM TRACECLK_PF22 | | CS4_B_ETMTRACE SYNC_PF21 | RW_B | 14 |
| 13 | SDCKE1 | SDCKE0 | | SDCLK_B | SDCLK | 13 |
| 12 | NVDD3 | DQM1 | | RAS_B | DQM0 | 12 |
| 11 | NVDD3 | SD2 | | DQM3 | SD0 | 11 |
| 10 | QVDD | SD6 | | SDQS0 | A15 | 10 |
| 9 | NVDD2 | SD12 | | SD9 | SD7 | 9 |
| 8 | NVDD2 | GND | | SD13 | SD11 | 8 |
| 7 | NVDD2 | GND | | A19 | SD15 | 7 |
| 6 | SD29 | A22 | | SD17 | SD16 | 6 |
| 5 | | | | SD20 | A20 | 5 |
| 4 | A3 | SD31 | SD27 | SD26 | SD22 | 4 |
| 3 | A4 | SDBA0 | SDQS3 | SD28 | SD24 | 3 |
| 2 | A5 | A0 | A25 | A24 | A23 | 2 |
| 1 | A6 | A2 | SDBA1 | SD30 | SD25 | 1 |
| | U | V | W | Y | AA | |

Table 61. i.MX27 (19 mm × 19 mm) MAPBGA Pin Assignments (continued)

| | | | | |
|--|----|---------------------------|-----------|----|
| | 18 | PC_CD1_B_ATA _DIOR_P20 | EXT_266M | 18 |
| | 17 | JTAG_CTRL | CLKO_PF15 | 17 |
| | 16 | EB1_B | BCLK | 16 |
| | 15 | ECB_B | LBA_B | 15 |
| | 14 | CS2_B | CS3_B | 14 |
| | 13 | SDWE_B | CAS_B | 13 |
| | 12 | A10 | DQM2 | 12 |
| | 11 | SD1 | SD3 | 11 |
| | 10 | SD4 | A14 | 10 |
| | 9 | SD5 | A16 | 9 |
| | 8 | SD10 | SD8 | 8 |
| | 7 | SD14 | A17 | 7 |
| | 6 | SDQS1 | A18 | 6 |
| | 5 | SD19 | SD18 | 5 |
| | 4 | SD21 | A21 | 4 |
| | 3 | SDQS2 | SD23 | 3 |
| | 2 | GND | GND | 2 |
| | 1 | GND | GND | 1 |
| | | AB | AC | |

Table 62 shows the device pin list, sorted by signal identification, including pad locations for ground and power supply voltages.

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing

| Contact Name | Location |
|------------------------------|----------|
| A0 | V2 |
| A1 | T6 |
| A10 | AB12 |
| A11 | T1 |
| A12 | R4 |
| A13 | R3 |
| A14 | AC10 |
| A15 | AA10 |
| A16 | AC9 |
| A17 | AC7 |
| A18 | AC6 |
| A19 | Y7 |
| A2 | V1 |
| A20 | AA5 |
| A21 | AC4 |
| A22 | V6 |
| A23 | AA2 |
| A24 | Y2 |
| A25 | W2 |
| A3 | U4 |
| A4 | U3 |
| A5 | U2 |
| A6 | U1 |
| A7 | T4 |
| A8 | T3 |
| A9 | T2 |
| ATA_DATA0_SD3_D0_PD2 | P20 |
| ATA_DATA1_SD3_D1_PD3 | P21 |
| ATA_DATA10_ETMTRACEPKT9_PD12 | U23 |
| ATA_DATA11_ETMTRACEPKT8_PD13 | U22 |
| ATA_DATA12_ETMTRACEPKT7_PD14 | U21 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|------------------------------|----------|
| ATA_DATA13_ETMTRACEPKT6_PD15 | U20 |
| ATA_DATA14_ETMTRACEPKT5_PD16 | V23 |
| ATA_DATA15_ETMTRACEPKT4_PF23 | V22 |
| ATA_DATA2_SD3_D2_PD4 | R23 |
| ATA_DATA3_SD3_D3_PD5 | R22 |
| ATA_DATA4_ETMTRACEPKT14_PD6 | R21 |
| ATA_DATA5_ETMTRACEPKT13_PD7 | R20 |
| ATA_DATA6_FEC_MDIO_PD8 | T23 |
| ATA_DATA7_ETMTRACEPKT12_PD9 | T22 |
| ATA_DATA8_ETMTRACEPKT11_PD10 | T20 |
| ATA_DATA9_ETMTRACEPKT10_PD11 | T21 |
| AVDD | U17 |
| AVSS | U18 |
| BCLK | AC16 |
| BOOT0 | V21 |
| BOOT1 | V20 |
| BOOT2 | T18 |
| BOOT3 | W23 |
| CAS_B | AC13 |
| CLKMODE0 | AA22 |
| CLKMODE1 | Y22 |
| CLKO_PF15 | AC17 |
| CLS_PA25 | E4 |
| CONTRAST_PA30 | C2 |
| CS0_B | Y15 |
| CS1_B | AA15 |
| CS2_B | AB14 |
| CS3_B | AC14 |
| CS4_B_ETMTRACESYNC_PF21 | Y14 |
| CS5_B_ETMTRACECLK_PF22 | V14 |
| CSI_D0_UART6_TXD_PB10 | C5 |
| CSI_D1_UART6_RXD_PB11 | A4 |
| CSI_D2_UART6_CTS_PB12 | B5 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|-----------------------------|----------|
| CSI_D3_UART6_RTS_PB13 | D6 |
| CSI_D4_PB14 | C6 |
| CSI_D5_PB17 | A6 |
| CSI_D6_UART5_TXD_PB18 | D7 |
| CSI_D7_UART5_RXD_PB19 | C7 |
| CSI_HSYNC_UART5_RTS_PB21 | B7 |
| CSI_MCLK_PB15 | A5 |
| CSI_PIXCLK_PB16 | B6 |
| CSI_VSYNC_UART5_CTS_PB20 | F8 |
| CSPI1_MISO_PD30 | A21 |
| CSPI1_MOSI_PD31 | C20 |
| CSPI1_RDY_PD25 | B20 |
| CSPI1_SCLK_PD29 | D19 |
| CSPI1_SS0_PD28 | B21 |
| CSPI1_SS1_PD27 | C21 |
| CSPI1_SS2_USBH2_DATA5_PD26 | D20 |
| CSPI2_MISO_USBH2_DATA2_PD23 | E20 |
| CSPI2_MOSI_USBH2_DATA1_PD24 | D23 |
| CSPI2_SCLK_USBH2_DATA0_PD22 | D22 |
| CSPI2_SS0_USBH2_DATA6_PD21 | C23 |
| CSPI2_SS1_USBH2_DATA3_PD20 | C22 |
| CSPI2_SS2_USBH2_DATA4_PD19 | D21 |
| D0 | N7 |
| D1 | R2 |
| D10 | N1 |
| D11 | M6 |
| D12 | M3 |
| D13 | M4 |
| D14 | M2 |
| D15 | M1 |
| D2 | R1 |
| D3 | P3 |
| D4 | P2 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|--------------|----------|
| D5 | N3 |
| D6 | P1 |
| D7 | N6 |
| D8 | N4 |
| D9 | N2 |
| DQM0 | AA12 |
| DQM1 | V12 |
| DQM2 | AC12 |
| DQM3 | Y11 |
| EB0_B | AA16 |
| EB1_B | AB16 |
| ECB_B | AB15 |
| EXT_266M | AC18 |
| EXT_60M | AA17 |
| EXTAL26M | Y23 |
| EXTAL32K | N23 |
| FPMVDD | N18 |
| FPMVSS | N17 |
| FUSEVDD | R18 |
| FUSEVSS | R17 |
| GND | A1 |
| GND | A2 |
| GND | A22 |
| GND | A23 |
| GND | AB1 |
| GND | AB2 |
| GND | AB22 |
| GND | AB23 |
| GND | AC1 |
| GND | AC2 |
| GND | AC22 |
| GND | AC23 |
| GND | B1 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|--------------|----------|
| GND | B2 |
| GND | B22 |
| GND | B23 |
| GND | F6 |
| GND | F7 |
| GND | F18 |
| GND | G7 |
| GND | J9 |
| GND | J10 |
| GND | J11 |
| GND | J12 |
| GND | J13 |
| GND | J14 |
| GND | J15 |
| GND | K9 |
| GND | K10 |
| GND | K11 |
| GND | K12 |
| GND | K13 |
| GND | K14 |
| GND | K15 |
| GND | L9 |
| GND | L10 |
| GND | L11 |
| GND | L12 |
| GND | L13 |
| GND | L14 |
| GND | L15 |
| GND | M9 |
| GND | M10 |
| GND | M11 |
| GND | M12 |
| GND | M13 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|----------------------|----------|
| GND | M14 |
| GND | M15 |
| GND | N9 |
| GND | N10 |
| GND | N11 |
| GND | N12 |
| GND | N13 |
| GND | N14 |
| GND | N15 |
| GND | P9 |
| GND | P10 |
| GND | P11 |
| GND | P12 |
| GND | P13 |
| GND | P14 |
| GND | P15 |
| GND | R9 |
| GND | R10 |
| GND | R11 |
| GND | R12 |
| GND | R13 |
| GND | R14 |
| GND | R15 |
| GND | V7 |
| GND | V8 |
| GND | V18 |
| HSYNC_PA28 | D1 |
| I2C_CLK_PD18 | B13 |
| I2C_DATA_PD17 | F12 |
| I2C2_SCL_PC6 | G23 |
| I2C2_SDA_PC5 | G22 |
| IOIS16_ATA_INTRQ_PF9 | AA20 |
| JTAG_CTRL | AB17 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|--------------|----------|
| KP_COL0 | D13 |
| KP_COL1 | F13 |
| KP_COL2 | B14 |
| KP_COL3 | C14 |
| KP_COL4 | A15 |
| KP_COL5 | B15 |
| KP_ROW0 | F11 |
| KP_ROW1 | D11 |
| KP_ROW2 | B12 |
| KP_ROW3 | A12 |
| KP_ROW4 | C12 |
| KP_ROW5 | D12 |
| LBA_B | AC15 |
| LD0_PA6 | J1 |
| LD1_PA7 | J2 |
| LD10_PA16 | G3 |
| LD11_PA17 | G4 |
| LD12_PA18 | F2 |
| LD13_PA19 | F1 |
| LD14_PA20 | F3 |
| LD15_PA21 | E1 |
| LD16_PA22 | E2 |
| LD17_PA23 | E3 |
| LD2_PA8 | J3 |
| LD3_PA9 | H1 |
| LD4_PA10 | J4 |
| LD5_PA11 | H2 |
| LD6_PA12 | H3 |
| LD7_PA13 | G2 |
| LD8_PA14 | G1 |
| LD9_PA15 | H4 |
| LSCLK_PA5 | K4 |
| MA10 | P6 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|------------------------|----------|
| MPLLVDD | V17 |
| MPLLVSS | T17 |
| NC_P4_1 | P4 |
| NFALE_ETMPIPESTAT0_P4 | L2 |
| NFCE_B_ETMTRACEPKT2_P3 | K3 |
| NFCLE_ETMTRACEPKT0_P1 | L4 |
| NFRB_ETMTRACEPKT3_P0 | K2 |
| NFRE_B_ETMPIPESTAT1_P5 | L3 |
| NFWE_B_ETMPIPESTAT2_P6 | L1 |
| NFWP_B_ETMTRACEPKT1_P2 | K1 |
| NVDD1 | K6 |
| NVDD1 | K7 |
| NVDD1 | L6 |
| NVDD1 | L7 |
| NVDD10 | G11 |
| NVDD10 | G12 |
| NVDD11 | G8 |
| NVDD11 | G9 |
| NVDD11 | G10 |
| NVDD12 | J6 |
| NVDD12 | J7 |
| NVDD13 | L18 |
| NVDD14 | H18 |
| NVDD14 | J17 |
| NVDD15 | G6 |
| NVDD15 | H6 |
| NVDD2 | P7 |
| NVDD2 | R6 |
| NVDD2 | R7 |
| NVDD2 | T7 |
| NVDD2 | U7 |
| NVDD2 | U8 |
| NVDD2 | U9 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|--------------------------|----------|
| NVDD3 | U11 |
| NVDD3 | U12 |
| NVDD4 | U14 |
| NVDD4 | U15 |
| NVDD4 | U16 |
| NVDD5 | V15 |
| NVDD5 | V16 |
| NVDD6 | P17 |
| NVDD6 | P18 |
| NVDD7 | J18 |
| NVDD7 | K18 |
| NVDD8 | G15 |
| NVDD8 | G16 |
| NVDD9 | G13 |
| NVDD9 | G14 |
| OE_ACD_PA31 | C3 |
| OE_B | Y16 |
| OSC26M_TEST | W20 |
| OSC26VDD | W22 |
| OSC26VSS | W21 |
| OSC32K_BYPASS | M21 |
| OSC32VDD | N21 |
| OSC32VSS | N22 |
| PC_BVD1_ATA_DMARQ_PF12 | AA19 |
| PC_BVD2_ATA_DMACK_PF11 | AB20 |
| PC_CD1_B_ATA_DIOR_PF20 | AB18 |
| PC_CD2_B_ATA_DIOW_PF19 | Y17 |
| PC_POE_ATA_BUFFER_EN_PF7 | Y20 |
| PC_PWRON_ATA_DA2_PF16 | AC19 |
| PC_READY_ATA_CS0_PF17 | AB19 |
| PC_RST_ATA_RESET_B_PF10 | Y19 |
| PC_RW_B_ATA_IORDY_PF8 | AB21 |
| PC_VS1_ATA_DA1_PF14 | Y18 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|------------------------|----------|
| PC_VS2_ATA_DA0_PF13 | AC20 |
| PC_WAIT_B_ATA_CS1_PF18 | AA18 |
| POR_B | Y21 |
| POWER_CUT | M23 |
| POWER_ON_RESET | M22 |
| PS_PA26 | D2 |
| PWMO_PE5 | A14 |
| QVDD | F17 |
| QVDD | G17 |
| QVDD | H7 |
| QVDD | H8 |
| QVDD | H9 |
| QVDD | H10 |
| QVDD | H11 |
| QVDD | H12 |
| QVDD | H13 |
| QVDD | H14 |
| QVDD | H15 |
| QVDD | H16 |
| QVDD | H17 |
| QVDD | J8 |
| QVDD | J16 |
| QVDD | K8 |
| QVDD | K16 |
| QVDD | L8 |
| QVDD | L16 |
| QVDD | M7 |
| QVDD | M8 |
| QVDD | M16 |
| QVDD | N8 |
| QVDD | N16 |
| QVDD | P8 |
| QVDD | P16 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|-------------------------|----------|
| QVDD | R8 |
| QVDD | R16 |
| QVDD | T8 |
| QVDD | T9 |
| QVDD | T10 |
| QVDD | T11 |
| QVDD | T12 |
| QVDD | T13 |
| QVDD | T14 |
| QVDD | T15 |
| QVDD | T16 |
| QVDD | U10 |
| RAS_B | Y12 |
| RESET_IN_B | AA21 |
| RESET_OUT_B_PE17 | AC21 |
| REV_PA24 | F4 |
| RTCK_OWIRE_PE16 | A18 |
| RTCVDD | M18 |
| RTCVSS | M17 |
| RW_B | AA14 |
| SD0 | AA11 |
| SD1 | AB11 |
| SD1_CLK_CSPI3_SCLK_PE23 | C19 |
| SD1_CMD_CSPI3_MOSI_PE22 | A20 |
| SD1_D0_CSPI3_MISO_PE18 | B18 |
| SD1_D1_PE19 | A19 |
| SD1_D2_PE20 | B19 |
| SD1_D3_CSPI3_SS_PE21 | D18 |
| SD10 | AB8 |
| SD11 | AA8 |
| SD12 | V9 |
| SD13 | Y8 |
| SD14 | AB7 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|---------------------------|----------|
| SD15 | AA7 |
| SD16 | AA6 |
| SD17 | Y6 |
| SD18 | AC5 |
| SD19 | AB5 |
| SD2 | V11 |
| SD2_CLK_MSHC_SCLK_PB9 | D5 |
| SD2_CMD_MSHC_BS_PB8 | B4 |
| SD2_D0_MSHC_DATA0_PB4 | C1 |
| SD2_D1_MSHC_DATA1_PB5 | B3 |
| SD2_D2_MSHC_DATA2_PB6 | C4 |
| SD2_D3_MSHC_DATA3_PB7 | A3 |
| SD20 | Y5 |
| SD21 | AB4 |
| SD22 | AA4 |
| SD23 | AC3 |
| SD24 | AA3 |
| SD25 | AA1 |
| SD26 | Y4 |
| SD27 | W4 |
| SD28 | Y3 |
| SD29 | U6 |
| SD3 | AC11 |
| SD3_CLK_ETMTRACEPKT15_PD1 | P22 |
| SD3_CMD_PD0 | N20 |
| SD30 | Y1 |
| SD31 | V4 |
| SD4 | AB10 |
| SD5 | AB9 |
| SD6 | V10 |
| SD7 | AA9 |
| SD8 | AC8 |
| SD9 | Y9 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|---------------------------|----------|
| SDBA0 | V3 |
| SDBA1 | W1 |
| SDCKE0 | V13 |
| SDCKE1 | U13 |
| SDCLK | AA13 |
| SDCLK_B | Y13 |
| SDQS0 | Y10 |
| SDQS1 | AB6 |
| SDQS2 | AB3 |
| SDQS3 | W3 |
| SDWE_B | AB13 |
| SPL_SPR_PA27 | D3 |
| SSI1_CLK_PC23 | A9 |
| SSI1_FS_PC20 | C9 |
| SSI1_RXDAT_PC21 | D9 |
| SSI1_TXDAT_PC22 | B9 |
| SSI2_CLK_GPT4_TIN_PC27 | D10 |
| SSI2_FS_GPT5_TOUT_PC24 | C10 |
| SSI2_RXDAT_GPT5_TIN_PC25 | B10 |
| SSI2_TXDAT_GPT4_TOUT_PC26 | F10 |
| SSI3_CLK_SLCDC2_CLK_PC31 | A11 |
| SSI3_FS_SLCDC2_D0_PC28 | A10 |
| SSI3_RXDAT_SLCDC2_RS_PC29 | B11 |
| SSI3_TXDAT_SLCDC2_CS_PC30 | C11 |
| SSI4_CLK_PC19 | A8 |
| SSI4_FS_PC16 | D8 |
| SSI4_RXDAT_PC17 | B8 |
| SSI4_TXDAT_PC18 | F9 |
| TCK | F15 |
| TDI | D17 |
| TDO | D16 |
| TIN_PC15 | C8 |
| TMS | C18 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|---------------------------|----------|
| TOUT_PC14 | A7 |
| TRST_B | F16 |
| UART1_CTS_PE14 | B17 |
| UART1_RTS_PE15 | C17 |
| UART1_RXD_PE13 | A17 |
| UART1_TXD_PE12 | D15 |
| UART2_CTS_KP_COL7_PE3 | A13 |
| UART2_RTS_KP_ROW7_PE4 | C13 |
| UART2_RXD_KP_ROW6_PE7 | C15 |
| UART2_TXD_KP_COL6_PE6 | D14 |
| UART3_CTS_PE10 | B16 |
| UART3_RTS_PE11 | C16 |
| UART3_RXD_PE9 | F14 |
| UART3_TXD_PE8 | A16 |
| UPLLVDD | K17 |
| UPLLVSS | L17 |
| USB_OC_B_PB24 | E22 |
| USB_PWR_PB23 | E21 |
| USBH1_FS_UART4_RTS_PB26 | F20 |
| USBH1_OE_B_PB27 | F21 |
| USBH1_RCV_PB25 | E23 |
| USBH1_RXDM_PB30 | G20 |
| USBH1_RXDP_UART4_RXD_PB31 | G21 |
| USBH1_SUSP_PB22 | G18 |
| USBH1_TXDM_UART4_TXD_PB28 | F22 |
| USBH1_TXDP_UART4_CTS_PB29 | F23 |
| USBH2_CLK_PA0 | J23 |
| USBH2_DATA7_PA2 | K21 |
| USBH2_DIR_PA1 | K20 |
| USBH2_NXT_PA3 | K22 |
| USBH2_STP_PA4 | K23 |
| USBOTG_CLK_PE24 | L22 |
| USBOTG_DATA0_PC9 | H22 |

Table 62. i.MX27 (19 mm × 19 mm) MAPBGA Contact Name Listing (continued)

| Contact Name | Location |
|-------------------------|----------|
| USBOTG_DATA1_PC11 | J20 |
| USBOTG_DATA2_PC10 | H23 |
| USBOTG_DATA3_PC13 | J22 |
| USBOTG_DATA4_PC12 | J21 |
| USBOTG_DATA5_PC7 | H20 |
| USBOTG_DATA6_PC8 | H21 |
| USBOTG_DATA7_PE25 | L20 |
| USBOTG_DIR_KP_ROW7A_PE2 | M20 |
| USBOTG_NXT_KP_COL6A_PE0 | L21 |
| USBOTG_STP_KP_ROW6A_PE1 | L23 |
| VSYNC_PA29 | D4 |
| XTAL26M | AA23 |
| XTAL32K | P23 |

6 Revision History

Table 63 summarizes revisions to this document since the previous release.

Table 63. Document Revision History

| Rev. No. | Date | Significant Change(s) |
|----------|---------|--|
| 2 | 3/2019 | <ul style="list-style-type: none"> Updated Figure 72 through Figure 76. In Section 5, "Package Information and Pinout" standardized section, table and figure titles. |
| 1.8 | 12/2012 | <ul style="list-style-type: none"> In Table 3, "i.MX27/MX27L Signal Descriptions," updated Function/Notes column for SD3_CMD and SD3_CLK. In Table 11, "Current Consumption," for parameter 4, Power Gate, updated maximum power to 216 μA. |
| 1.7 | 05/2011 | In Table 8, "DPLL FREQUENCY Specifications," added the MPLL row along with a footnote. |
| 1.6 | 08/2010 | <ul style="list-style-type: none"> Added a new section- Section 4.3.13.1, "WEIM Synchronous Mode Sample Point." Updated ID WE15 in Table 50. |
| 1.5 | 12/2009 | Updated Table 1, "Ordering Information," to include new part numbers and table footnote. |
| 1.4 | 5/2009 | <ul style="list-style-type: none"> In Table 11, "Current Consumption," a column for Max value was added. In Table 59, "i.MX27 (17 mm \times 17 mm) MAPBGA Pin Assignments," inaccurate pin list information was corrected and the table reformatted. In Table 60, "i.MX27 (17 mm \times 17 mm) MAPBGA Contact Name Listing," inaccurate pin list information was corrected and the table was reformatted. Reformatted Table 62, "i.MX27 (19 mm \times 19 mm) MAPBGA Contact Name Listing." |
| 1.3 | 11/2008 | <ul style="list-style-type: none"> In Table 3, "i.MX27/MX27L Signal Descriptions," switched FEC_TXD0 and FEC_TXD1 for SD3_CMD and SD3_CLK. In Table 23, "CSPI Interface Timing Parameters," updated t6' and t13, and removed t14. In Table 60, "i.MX27 (17 mm \times 17 mm) MAPBGA Contact Name Listing," changed "RW" to "RW_B." Added Table 59, "i.MX27 (17 mm \times 17 mm) MAPBGA Pin Assignments." Updated Table 62, "i.MX27 (19 mm \times 19 mm) MAPBGA Contact Name Listing." |
| 1.2 | 7/2008 | Corrected part number in Section 1.3, "Ordering Information," on p. 4. Part number previously listed as MCIMX27FVOP4A has been corrected to read MCIMX27VOP4A. |
| 1.1 | 7/2008 | Formatting and template work. |

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