



**THE DATASHEET OF
MIC2184YM**



General Description

Micrel's MIC2184 is a high efficiency PWM buck control IC. With its wide input voltage range of 2.9V to 14V, the MIC2184 can be used to efficiently step voltages down in 1- or 2-cell Li Ion battery powered applications, as well as in fixed 3.3V, 5V, or 12V systems.

Efficiencies over 90% are achievable over a wide range of load conditions with the MIC2184's PWM control scheme. The operating frequency can be divided by two by raising the FREQ/2 pin to V_{DD} . This allows the user to optimize efficiency versus board space. It also allows the MIC2184 to be externally synchronized to frequencies below its nominal 400kHz.

The MIC2184 features an oscillator output, FreqOut, which can be used to implement a simple charge pump in low voltage applications. The output of the charge pump can be fed into the gate drive power circuitry via the V_{INP} pin, allowing enhanced gate drive, hence higher efficiencies, despite low input voltages.

MIC2184 features a $1\mu A$ shutdown mode, and a programmable undervoltage lockout, making it well suited for portable applications.

The MIC2184 is available in 16 pin SOP and QSOP package options with a junction temperature range range from $-40^{\circ}C$ to $+125^{\circ}C$.

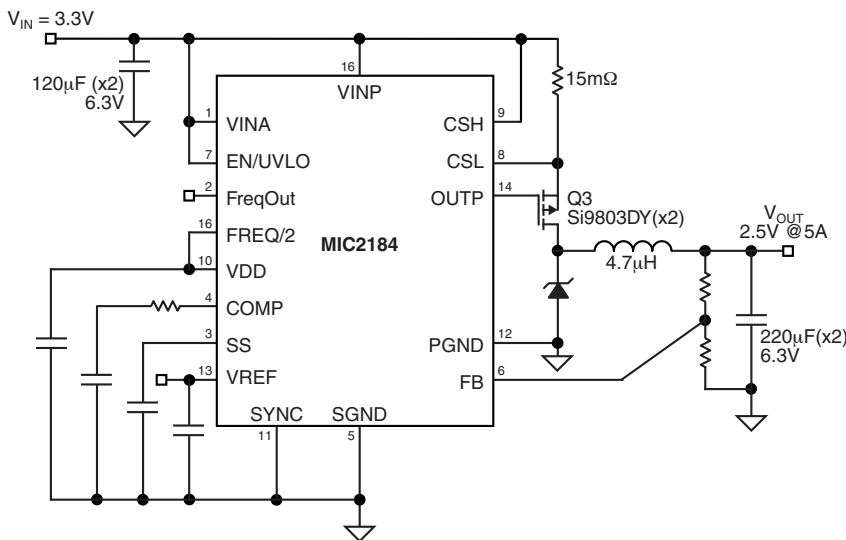
Features

- Input voltage range: 2.9V to 14V
- >90% efficiency
- Oscillator frequency of 400kHz
- Frequency divide-by-two pin
- Frequency sync to 600kHz
- FreqOut oscillator output allows simple charge pump implementation in low voltage systems
- 1.245V reference output
- Front edge blanking
- 5Ω output driver
- Soft start
- PWM current mode control
- $1\mu A$ shutdown current
- Cycle-by-cycle current limiting
- Frequency foldback short circuit protection
- Adjustable under-voltage lockout
- 16 pin narrow-body SOIC and QSOP package options

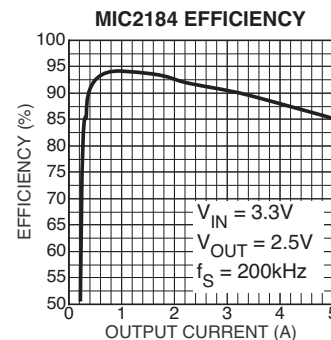
Applications

- 3.3V to 2.5V/1.8V/1.5V conversion
- DC power distribution systems
- Wireless Modems
- ADSL line cards
- 1-and 2-cell Li Ion battery operated equipment
- Satellite Phones

Typical Application



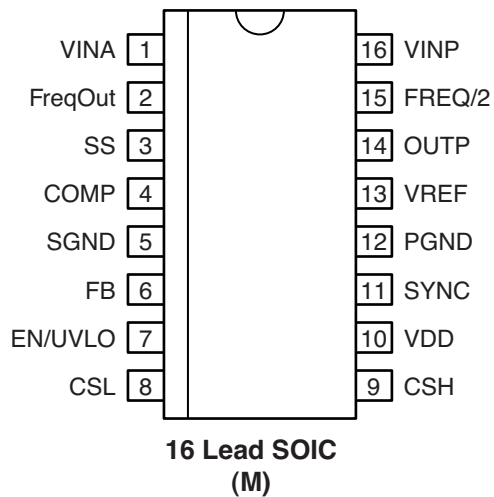
Adjustable Output Buck Converter



Ordering Information

| Part Number | | Output Voltage | Frequency | Junction Temp. Range | Package |
|-------------|------------|----------------|-----------|----------------------|--------------|
| Standard | Pb-Free | | | | |
| MIC2184BM | MIC2184YM | Adj. | 400KHz | -40°C to +125°C | 16-lead SOP |
| MIC2184BQS | MIC2184YQS | Adj. | 400KHz | -40°C to +125°C | 16-lead QSOP |

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|----------|--|
| 1 | VINA | Analog voltage input voltage to the circuit. This powers up the analog sections of the die and does not need to be the same voltage as Pin 16 (V_{INP}). |
| 2 | FreqOut | This provides a digital signal output signal at half the switching frequency. This signal swings from 0 to 3V, and can be used to drive an external capacitive doubler to provide a higher voltage to the V_{INP} input. |
| 3 | SS | Soft start reduces the inrush current and delays and slows the output voltage rise time. A 5 μ A current source will charge the capacitor up to V_{DD} . A 1 μ F capacitor will soft start the switching regulator in 1.5ms. |
| 4 | COMP | Compensation (Output): Internal error amplifier output. Connect to a capacitor or series RC network to compensate the regulator's control loop. |
| 5 | SGND | Small signal ground: must be routed separately from other grounds to the (-) terminal of C_{OUT} . |
| 6 | FB | Feedback Input - the circuit regulates this pin to 1.245V. |
| 7 | EN/UVLO | Enable/UnderVoltage Lockout (input): A low level on this pin will power down the device, reducing the quiescent current to under 5 μ A. This pin has two separate thresholds, below 1.5V the output switching is disabled, and below 0.9V the part is forced into a complete micropower shutdown. The 1.5V threshold functions as an accurate undervoltage lockout (UVLO) with 140mV hysteresis. |
| 8 | CSL | The (-) input to the current limit comparator. A built in offset of 100mV between CSH and CSL in conjunction with the current sense resistor sets the current limit threshold level. This is also the (-) input to the current amplifier. |
| 9 | CSH | The (+) input to the current limit comparator. A built in offset of 100mV between CSH and CSL in conjunction with the current sense resistor sets the current limit threshold level. This is also the (+) input to the current amplifier. |
| 10 | VDD | 3V internal linear-regulator output. V_{DD} is also the supply voltage bus for the chip. Bypass to SGND with 1 μ F. |
| 11 | SYNC | Frequency Synchronization (Input): Connect an external clock signal to synchronize the oscillator. Leading edge of signal above 1.5V starts the switching cycle. Connect to SGND if not used. |
| 12 | PGND | MOSFET driver power ground, connects to source of synchronous MOSFET and the (-) terminal of C_{IN} . |
| 13 | VREF | The 1.245V voltage reference is available on this pin. A 0.1 μ F capacitor should be connected from this pin to ground. |
| 14 | OUTP | High current drive for high side P channel MOSFET. Voltage swing is from ground to V_{INP} . On-resistance is typically 2.5 Ω . |
| 15 | FREQ/2 | When this is low, the oscillator frequency is 400KHz. When this pin is raised to V_{DD} , the oscillator frequency is 200KHz. |
| 16 | VINP | Power Input voltage to the circuit. The output gate drivers are powered from this supply. The current sense resistor R_{CS} should be connected as close as possible to this pin. |

Absolute Maximum Ratings (Note 1)

| | |
|---|----------------------------------|
| Supply Voltage ($V_{IN(A)}$, $V_{IN(P)}$) | 15V |
| Digital Supply Voltage (V_{DD}) | 7V |
| Comp Pin Voltage (V_{COMP}) | -0.3V to +3V |
| Feedback Pin Voltage (V_{FB}) | -0.3V to +3V |
| Enable Pin Voltage ($V_{EN/UVLO}$) | -0.3V to 15V |
| Current Sense Voltage (V_{CSH} - V_{CSL}) | -0.3V to 1V |
| Sync Pin Voltage (V_{SYNC}) | -0.3V to 7V |
| Freq/2 Pin Voltage ($V_{FREQ/2}$) | -0.3V to 7V |
| Power Dissipation (P_D) | |
| 16 lead SOIC | 400mW @ $T_A = 85^\circ\text{C}$ |
| 16 lead QSOP | 245mW @ $T_A = 80^\circ\text{C}$ |
| Ambient Storage Temp | -65°C to +150°C |
| ESD Rating, | Note 3 |

Electrical Characteristics

$V_{IN(A)} = V_{IN(P)} = V_{CSH} = 5\text{V}$, $V_{OUT} = 3.3\text{V}$, $V_{EN/UVLO} = 5\text{V}$, $V_{FREQ/2} = 0\text{V}$, $T_J = 25^\circ\text{C}$, unless otherwise specified. **Bold** values indicate $-40^\circ\text{C} < T_J < +125^\circ\text{C}$.

Operating Ratings (Note 2)

| | |
|--|--|
| Supply Voltage ($V_{IN(A)}$, $V_{IN(P)}$) | +2.9V to +14V |
| Ambient Operating Temperature | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ |
| Junction Temperature | $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| Output Voltage Range | 1.3V to 12V |
| Package Thermal Resistance | |
| θ_{JA} 16-lead SOP | 100°C/W |
| θ_{JA} 16-lead QSOP | 163°C/W |

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|--------------|-------|--------------|---------------|
| Regulation | | | | | |
| Feedback Voltage Reference | ($\pm 1\%$) | 1.233 | 1.245 | 1.257 | V |
| | ($\pm 2\%$) | 1.22 | | 1.27 | V |
| Feedback Bias Current | | | 50 | | nA |
| Output Voltage Line Regulation | $5\text{V} \leq V_{IN} \leq 12\text{V}$ | | 0.04 | | % / V |
| Output Voltage Load Regulation | $0\text{mV} < (V_{CSH} - V_{CSL}) < 75\text{mV}$ | | 0.9 | | % |
| Output Voltage Total Regulation | $5\text{V} \leq V_{IN(A)} \leq 12\text{V}$, $0\text{mV} < (V_{CSH} - V_{CSL}) < 75\text{mV}$ ($\pm 3\%$) | 1.208 | | 1.282 | V |
| Input & V_{DD} Supply | | | | | |
| $V_{IN(A)}$ Input Current | | | 0.7 | | mA |
| $V_{IN(P)}$ Input Current, Note 4 | (Excluding external MOSFET gate current) | | 1.0 | | mA |
| Shutdown Quiescent Current | $V_{EN/UVLO} = 0\text{V}$; ($I_{VINA} + I_{VINP}$) | | 0.5 | 5 | μA |
| Digital Supply Voltage (V_{DD}) | $I_L = 0$ | 2.82 | 3.0 | 3.18 | V |
| Digital Supply load regulation | $I_L = 0$ to 1mA | | 0.03 | | V |
| Undervoltage Lockout | V_{DD} upper threshold (turn on threshold) | | 2.75 | | V |
| UVLO Hysteresis | | | 100 | | mV |
| Reference Output(VREF) | | | | | |
| Reference Voltage | ($\pm 1.5\%$) | 1.226 | 1.245 | 1.264 | V |
| | ($\pm 2.5\%$) | 1.213 | | 1.276 | V |
| Reference Voltage Line Regulation | $5\text{V} < V_{IN(A)} < 12\text{V}$ | | 2 | | mV |
| Reference Voltage Load Regulation | $0 < I_{REF} < 100\mu\text{A}$ | | 1 | | mV |
| Enable/UVLO | | | | | |
| Enable Input Threshold | | 0.6 | 0.9 | 1.2 | V |
| UVLO Threshold | (Turn-on threshold) | 1.4 | 1.5 | 1.6 | V |
| UVLO Hysteresis | | | 140 | | mV |
| Enable Input Current | $V_{EN/UVLO} = 5\text{V}$ | | 0.2 | 5 | μA |

| Parameter | Condition | Min | Typ | Max | Units |
|---------------------------------|--|--------------|-----------|------------|----------|
| Soft Start | | | | | |
| Soft Start Current | | | 5 | | μ A |
| Current Limit | | | | | |
| Current Limit Threshold Voltage | Voltage on CSH-CSL to trip current limit | | 100 | | mV |
| Error Amplifier | | | | | |
| Error Amplifier Gain | | | 20 | | V/V |
| Current Amplifier | | | | | |
| Current Amplifier Gain | | | 3.0 | | V/V |
| Oscillator Section | | | | | |
| Oscillator Frequency (f_O) | | 360 | 400 | 440 | kHz |
| Maximum Duty Cycle | $V_{FB} = 1.0V$ | 100 | | | % |
| Minimum On Time | $V_{FB} = 1.5V$ | | 185 | | ns |
| Freq/2 Frequency (f_O) | $V_{FREQ/2} = 5V$ | 170 | 200 | 230 | kHz |
| Frequency Foldback Threshold | Measured on FB | | 0.3 | | V |
| Frequency Foldback Frequency | | | 90 | | kHz |
| SYNC Threshold Level | | 0.6 | 1.4 | 2.2 | V |
| SYNC Input Current | | | 0.1 | 5 | μ A |
| SYNC Minimum Pulse Width | | 200 | | | ns |
| SYNC Capture Range | Note 5 | $f_O + 15\%$ | | 600 | kHz |
| FreqOut Output | | | | | |
| FreqOut Frequency | Note 6 | | $f_O / 2$ | | kHz |
| FreqOut Current Drive | Sink | | 8 | | mA |
| | Source | | -6 | | mA |
| Gate Drivers | | | | | |
| Rise/Fall Time | $C_L = 3300pF$ | | 50 | | ns |
| Output Driver Impedance | Source; $V_{INP} = 12V$ | | 1.8 | 4 | Ω |
| | Sink; $V_{INP} = 12V$ | | 1.6 | 3.5 | Ω |
| | Source; $V_{INP} = 5V$ | | 2.6 | | Ω |
| | Sink; $V_{INP} = 5V$ | | 2.4 | | Ω |

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(\text{Max})$, the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A .

Note 2: The device is not guaranteed to function outside its operating rating.

Note 3: Devices are ESD sensitive. Handling precautions recommended.

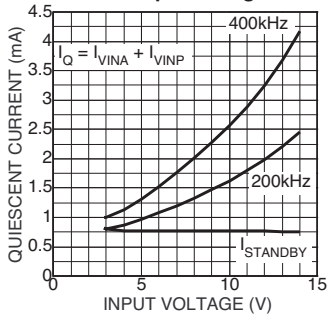
Note 4: See application information for $I(V_{INP})$ vs. V_{INP} .

Note 5: See application information for limitations on maximum operating frequency.

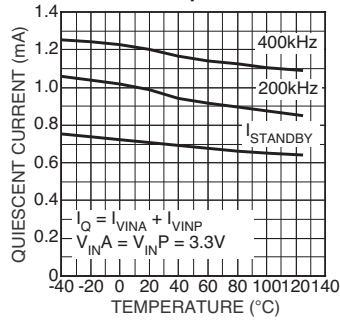
Note 6: The frequency on FreqOut is half the frequency of the oscillator, or half the frequency of the external Sync signal.

Typical Characteristics

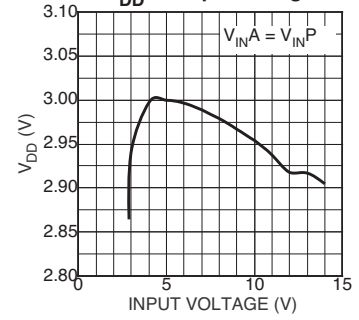
Quiescent Current vs. Input Voltage



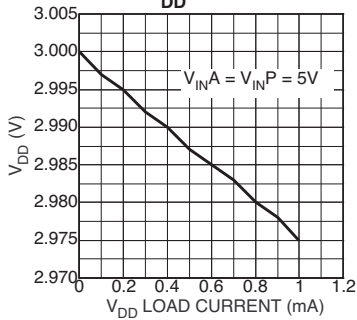
Quiescent Current vs. Temperature



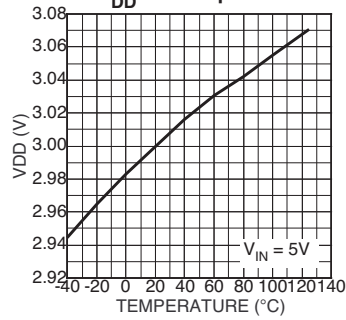
V_{DD} vs. Input Voltage



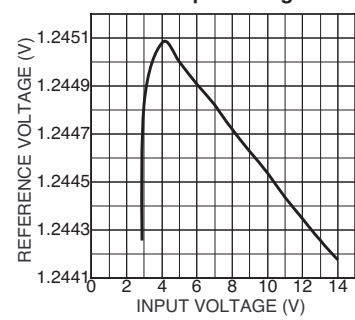
V_{DD} vs. Load



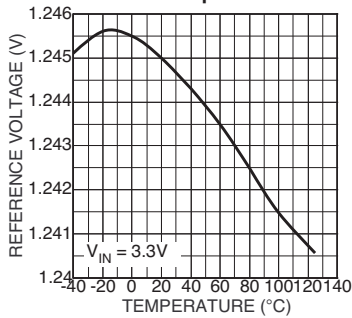
V_{DD} vs. Temperature



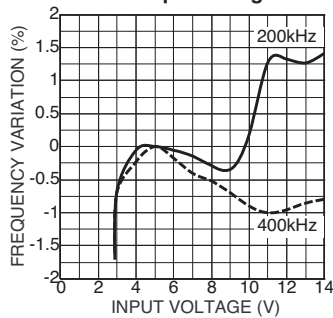
Error Amp Reference Voltage vs. Input Voltage



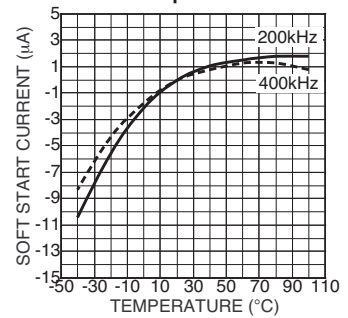
Error Amp Reference Voltage vs. Temperature



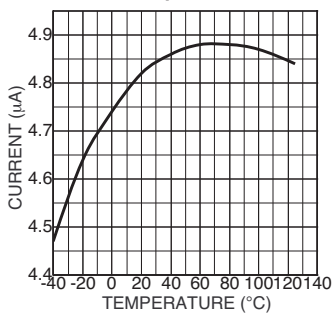
Frequency Variation vs. Input Voltage



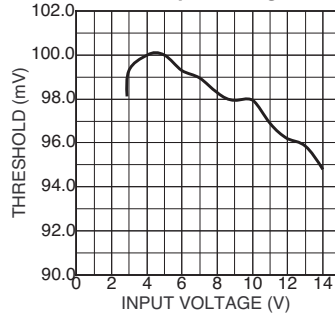
Frequency Variation vs. Temperature



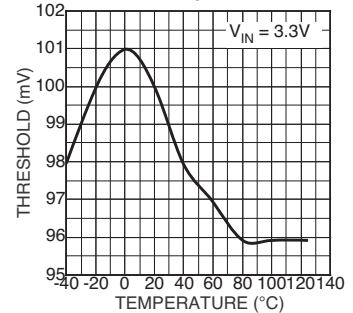
Soft Start Current vs. Temperature

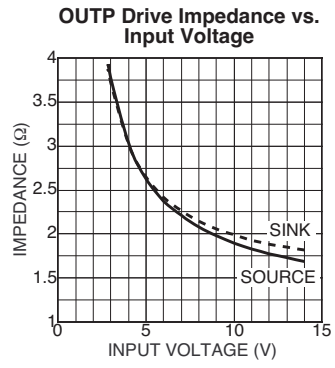


Overcurrent Threshold vs. Input Voltage



Overcurrent Threshold vs. Temperature





Functional Diagram

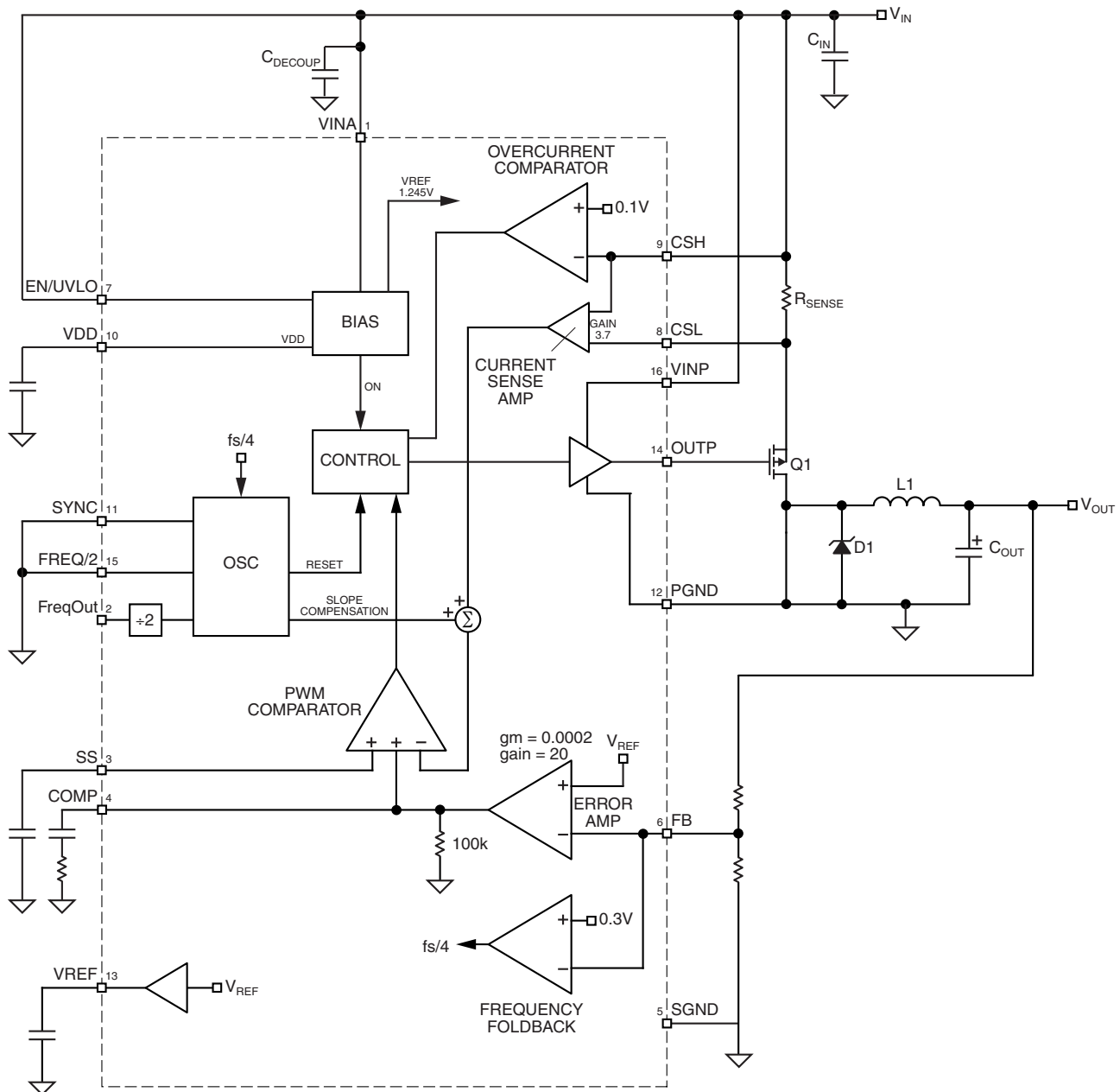


Figure 1. MIC2184 Block Diagram

Functional Characteristics

Controller Overview and Functional Description

The MIC2184 is a BiCMOS, switched mode, synchronous, step down (buck) converter controller. It uses a P-Channel MOSFET, which allows the controller to operate at 100% duty cycle and eliminates the need for a high side drive bootstrap circuit. Current mode control is used to achieve superior transient line and load regulation. An internal corrective ramp provides slope compensation for stable operation above a 50% duty cycle. The controller is optimized for high efficiency, high performance DC-DC converter applications.

Figure 1 is a block diagram of the MIC2184 configured as a synchronous buck converter. At the beginning of the switching cycle, the OUP pin pulls low and turns on the high-side

P-Channel MOSFET, Q1. Current flows from the input to the output through the current sense resistor, MOSFET and inductor. The current amplitude increases, controlled by the inductor. The voltage across the current sense resistor, R_{SENSE} , is amplified inside the MIC2184 and combined with an internal ramp for stability. This signal is compared to the output of the error signal amplifier. When the current signal equals the error voltage signal, the P-channel MOSFET is turned off. The inductor current flows through the diode, D1. At the beginning of the next switching cycle, the P-channel MOSFET is turned on which turns off the diode, D1.

The MIC2184 controller is broken down into 7 functions.

- Control loop
 - PWM operation
 - Current mode control
- Current limit
- Reference, enable and UVLO
- FreqOut
- MOSFET gate drive
- Oscillator and Sync
- Soft-start

Control Loop

PWM Control Loop

The MIC2184 uses current mode control to regulate the output voltage. This dual control loop method (illustrated in Figure 2) senses the output voltage (outer loop) and the inductor current (inner loop). It uses inductor current and output voltage to determine the duty cycle of the buck converter. Sampling the inductor current effectively removes the inductor from the control loop, which simplifies compensation.

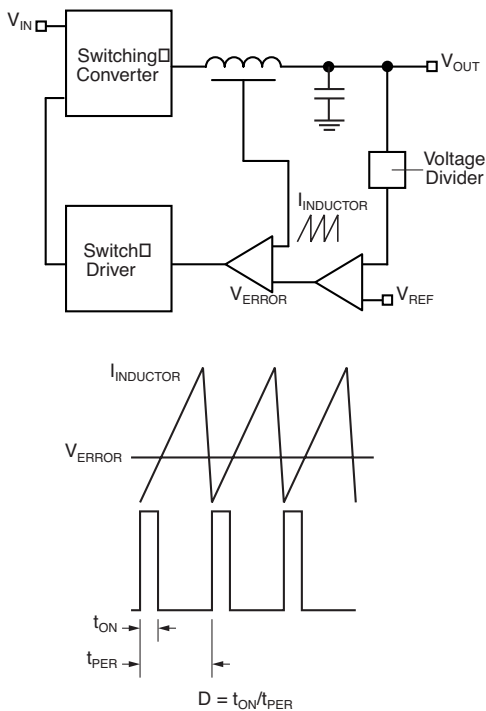


Figure 2. Current Mode Control Example

As shown in Figure 1, the inductor current is sensed by measuring the voltage across the resistor, R_{SENSE} . A ramp is added to the amplified current sense signal to provide slope compensation, which is required to prevent unstable operation at duty cycles greater than 50%.

A transconductance amplifier is used for the error amplifier, which compares an attenuated sample of the output voltage with a reference voltage. The output of the error amplifier is the compensation pin (Comp), which is compared to the current sense waveform in the PWM block. When the current signal becomes greater than the error signal, the comparator turns off the high side drive. The COMP pin provides access to the output of the error amplifier and allows the use of external components to stabilize the voltage loop.

Current Limit

The output current is detected by the voltage drop across the external current sense resistor (R_{SENSE} in Figure 1.). The current sense resistor must be sized using the minimum current limit threshold. The external components must be designed to withstand the maximum current limit. The current sense resistor value is calculated by the equation below:

$$R_{SENSE} = \frac{MIN_CURRENT_SENSE_THRESHOLD}{I_{OUT_MAX}}$$

The maximum output current is:

$$I_{OUT_MAX} = \frac{MAX_CURRENT_SENSE_THRESHOLD}{R_{SENSE}}$$

The current sense pins CSH (pin 9) and CSL (pin 8) are noise sensitive due to the low signal level and high input impedance. The PCB traces should be short and routed close to each other. A small (1nF) capacitor across the pins will attenuate high frequency switching noise.

When the peak inductor current exceeds the current limit threshold, the overcurrent comparator turns off the high side MOSFET for the remainder of the switching cycle, effectively decreasing the duty cycle. The output voltage drops as additional load current is pulled from the converter. When the voltage at the feedback pin (FB) reaches approximately 0.3V, the circuit enters frequency foldback mode and the oscillator frequency will drop to 1/4 of the switching frequency. This limits the maximum output power delivered to the load under a short circuit condition.

Reference, Enable and UVLO Circuits

The output drivers are enabled when the following conditions are satisfied:

- The V_{DD} voltage (pin 10) is greater than its undervoltage threshold.
- The voltage on the enable pin (pin 7) is greater than the enable UVLO threshold.

The enable pin (pin 7) has two threshold levels, allowing the MIC2184 to shut down in a low current mode, or turn off output switching in standby mode. An enable pin voltage lower than the shutdown threshold turns off all the internal circuitry and places the MIC2184 in a micropower shutdown mode.

If the enable pin voltage is between the shutdown and standby thresholds, the internal bias, V_{DD} and reference voltages are turned on. The soft start pin is forced low by an internal discharge MOSFET. The output drivers are inhibited from switching. The OUTP pin is in a high state and the OUTN pin remains in a low state. Raising the enable voltage above the standby threshold allows the soft start capacitor to charge and enables the output drivers. The standby threshold is specified in the electrical characteristics. A resistor divider can be used with the enable pin to prevent the power supply from turning on until a specified input voltage is reached. The circuit in Figure 3 shows how to connect the resistors.

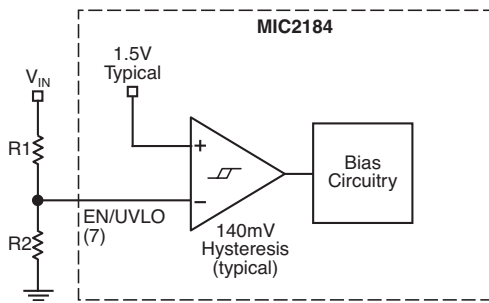


Figure 3. UVLO Circuitry

The line voltage turn on trip point is:

$$V_{\text{INPUT_ENABLE}} = V_{\text{THRESHOLD}} \times \frac{R2}{R1 + R2}$$

where:

$V_{\text{THRESHOLD}}$ is the voltage level of the internal comparator reference, typically 1.5V

The input voltage hysteresis is equal to:

$$V_{\text{INPUT_HYST}} = V_{\text{HYST}} \times \frac{R1 + R2}{R2}$$

where:

V_{HYST} is the internal comparator hysteresis level, typically 140mV.

$V_{\text{INPUT_HYST}}$ is the hysteresis at the input voltage

The MIC2184 will be disabled when the input voltage drops back down to:

$$V_{\text{INPUT_OFF}} = V_{\text{INPUT_ENABLE}} - V_{\text{INPUT_HYST}} = (V_{\text{THRESHOLD}} - V_{\text{HYST}}) \times \frac{R2}{R1 + R2}$$

Either of 2 UVLO conditions will pull the soft start capacitor low.

- When the V_{DD} voltage drops below its undervoltage lockout level.
- When the enable pin drops below its enable threshold

The internal bias circuit generates an internal 1.245V band-gap reference voltage for the voltage error amplifier and a 3V V_{DD} voltage for the internal control circuitry. The V_{REF} pin (pin 13) should be decoupled with a 0.1 μf capacitor placed close to the pin. The V_{DD} pin must be decoupled with a 1 μf ceramic capacitor. The capacitor must be placed close to the V_{DD} pin. The other end of the capacitor must be connected directly to the ground plane.

MOSFET Gate Drive

The MIC2184 is designed to drive a high side P-channel MOSFET. The source pin of the P-channel MOSFET is connected to the input of the power supply. It is turned on when OUTP pulls the gate of the MOSFET low. The advantage of using a P-channel MOSFET is that it does not require a bootstrap circuit to boost the gate voltage higher than the input, as would be required for an N-channel MOSFET.

The V_{INP} pin (pin 16) supplies the drive voltage to the gate drive pin, OUTP. V_{INP} pin is usually connected to the input

supply. The V_{INP} pin and CSH pin must be connected to the same potential.

MOSFET Selection

The P-channel MOSFET must have a V_{GS} threshold voltage equal to or lower than the input voltage when used in a buck converter topology. There is a limit to the maximum gate charge the MIC2184 will drive. Higher gate charge MOSFET will slow down the turn-on and turn-off time of the MOSFET. Slower transition times will cause higher power dissipation in the MOSFET due to higher switching transition losses.

The MOSFET gate charge is also limited by power dissipation in the MIC2184. The power dissipated by the gate drive circuitry is calculated below:

$$P_{\text{GATE_DRIVE}} = Q_{\text{GATE}} \times V_{\text{INP}} \times f_s$$

where: Q_{gate} is the total gate charge of both the N and P-channel MOSFETs.

f_s is the switching frequency

V_{INP} is the gate drive voltage at the V_{INP} pin

The graph in Figure 4 shows the total gate charge that can be driven by the MIC2184 over the input voltage range, for different values of switching frequency.

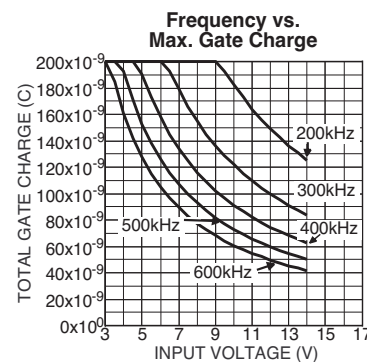


Figure 4. MIC2184 Frequency vs Max. Gate Charge

Oscillator & Sync

The internal oscillator is free running and requires no external components. The $f/2$ pin allows the user to select from two switching frequencies. A low level set the oscillator frequency to 400kHz and a high level set the oscillator frequency to 200kHz. The maximum duty cycle for both frequencies is 100%. This is another advantage of using a P-channel MOSFET for the high-side drive; it can continuously turned on.

A frequency foldback mode is enabled if the voltage on the feedback pin (pin 6) is less than 0.3V. In frequency foldback, the oscillator frequency is reduced by approximately a factor of 4. Frequency foldback is used to limit the energy delivered to the output during a short circuit fault condition.

The SYNC input (pin 11) lets the MIC2184 synchronize with an external clock signal. The rising edge of the sync signal generates a reset signal in the oscillator, which turns off the low side gate drive output. The high side drive then turns on, restarting the switching cycle. The sync signal is inhibited when the controller operates in frequency foldback. The sync signal frequency must be greater than the maximum speci-

fied free running frequency of the MIC2184. If the synchronizing frequency is lower, double pulsing of the gate drive outputs will occur. When not used, the sync pin must be connected to ground.

The maximum recommended output switching frequency is 600kHz. Synchronizing to higher frequencies may be possible, however, higher power dissipation in the internal gate drive circuits will occur. The MOSFET gates require charge to turn on the device. The average current required by the MOSFET gate increases with switching frequency.

Soft Start

Soft start reduces the power supply input surge current at start up by controlling the output voltage risetime. The input surge appears while the output capacitance is charged up. A slower output risetime will draw a lower input surge current. Soft start may also be used for power supply sequencing.

The soft start voltage is applied directly to the PWM comparator. A 5 μ A internal current source is used to charge up the soft start capacitor. The capacitor is discharged when either the enable pin voltage drops below the standby threshold or the V_{DD} voltage drops below its UVLO level.

The part switches at a low duty cycle when the soft start pin voltage is zero. As the soft start voltage rises from 0V to 0.7V, the duty cycle increases from the minimum duty cycle to the operating duty cycle. The oscillator runs at the foldback frequency (1/4 of the switching frequency) until the feedback voltage rises above 0.3V. The risetime of the output is dependent of the soft start capacitor output capacitance, input and output voltage and load current.

Voltage Setting Components

The MIC2184 requires two resistors to set the output voltage as shown in Figure 5.

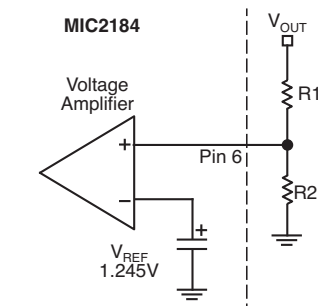


Figure 5

The output voltage is determined by the equation below.

$$V_{OUT} = V_{REF} \times 1 + \frac{R1}{R2}$$

Where: V_{REF} for the MIC2184 is typically 1.245V.

Lower values of R1 are preferred to prevent noise from appearing on the FB pin. A typically recommended value is 10k Ω . If R1 is too small in value it will decrease the efficiency of the power supply, especially at low output loads.

Once R1 is selected, R2 can be calculated with the following formula.

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} \pm V_{REF}}$$

Efficiency Considerations

Efficiency is the ratio of output power to input power. The difference is dissipated as heat in the buck converter. Under light output load, the significant contributors are:

- The V_{IN}A supply current
- The V_{IN}P supply current, which includes the current required to switch the external MOSFET
- Core losses in the output inductor

To maximize efficiency at light loads:

- Use a low gate charge MOSFET or use the smallest MOSFET, which is still adequate for maximum output current.
- Use a ferrite material for the inductor core, which has less core loss than an MPP or iron power core.

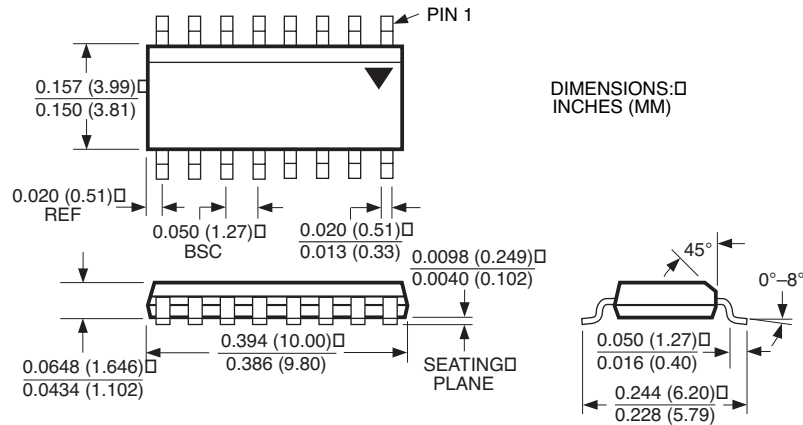
Under heavy output loads the significant contributors to power loss are (in approximate order of magnitude):

- Resistive on time losses in the MOSFET
- Switching transition losses in the MOSFET
- Inductor resistive losses
- Current sense resistor losses
- Input capacitor resistive losses (due to the capacitors ESR)

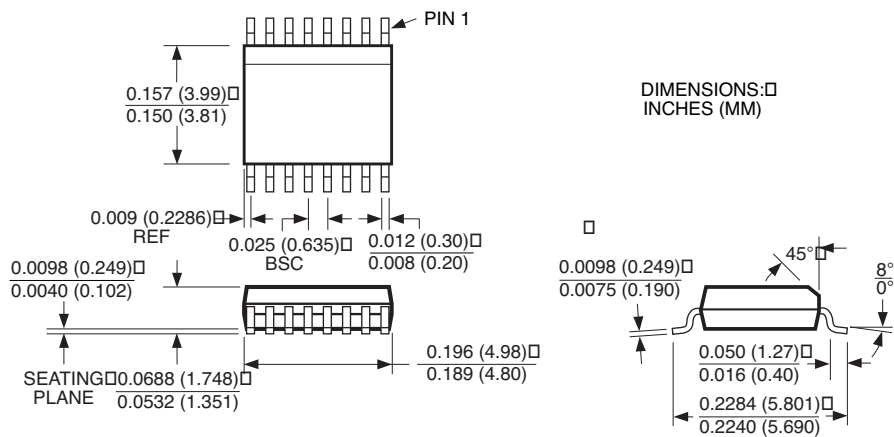
To minimize power loss under heavy loads:

- Use low on resistance MOSFETs. Use low threshold logic level MOSFETs when the input voltage is below 5V. Multiplying the gate charge by the on resistance gives a figure of merit, providing a good balance between low load and high load efficiency.
- Slow transition times and oscillations on the voltage and current waveforms dissipate more power during the turn on and turn off of the MOSFET. A clean layout will minimize parasitic inductance and capacitance in the gate drive and high current paths. This will allow the fastest transition times and waveforms without oscillations. Low gate charge MOSFETs will transition faster than those with higher gate charge requirements.
- For the same size inductor, a lower value will have fewer turns and therefore, lower winding resistance. However, using too small of a value will require more output capacitors to filter the output ripple, which will force a smaller bandwidth, slower transient response and possible instability under certain conditions.
- Lowering the current sense resistor value will decrease the power dissipated in the resistor. However, it will also increase the overcurrent limit and will require larger MOSFETs and inductor components.
- Use low ESR input capacitors to minimize the power dissipated in the capacitors ESR.

Package Information



16-Pin SOP (M)



16-Pin QSOP (QS)

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