



MIC22600

1MHz, 6A Integrated Switch Synchronous Buck Regulator

NOT RECOMMENDED FOR NEW DESIGNS

SEE MIC22705

General Description

The Micrel MIC22600 is a high-efficiency, 6A, integrated switch, synchronous buck (step-down) regulator. The MIC22600 is optimized for highest efficiency and achieves more than 90% efficiency, while still switching at 1MHz over a broad load range with only 1μH inductor and down to 47μF output capacitor. The ultra-high-speed control loop keeps the output voltage within regulation even under extreme transient load swings commonly found in FPGAs and low voltage ASICs. The output voltage can be adjusted down to 0.7V to address all low voltage power needs. The MIC22600 offers a full range of sequencing and tracking options. The EN/DLY pin combined with the Power Good/Power-on-Reset (PG/POR) pin allows multiple outputs to be sequenced in any way during turn-on and turn-off. The RC (Ramp Control™) pin allows the device to be connected to another product in the MIC22xxx and/or MIC68xxx family, to keep the output voltages within a certain ΔV on start-up.

The MIC22600 is available in a 24-pin 4mm x 4mm MLF® and thermally-enhanced 24-pin ePad TSSOP with a junction operating range from -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

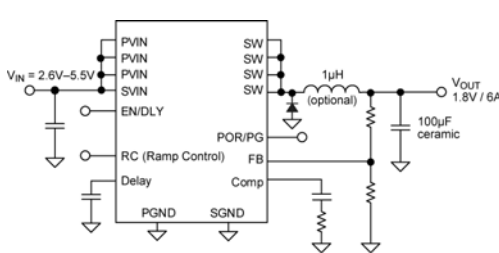
Features

- Input voltage range: 2.6V to 5.5V
- Output voltage adjustable down to 0.7V
- Output current up to 6A
- Full sequencing and tracking ability
- Power-on-Reset/Power Good
- Efficiency > 90% across a broad load range
- Ultra-fast transient response, easy RC compensation
- 100% maximum duty cycle
- Fully-integrated MOSFET switches
- Micropower shutdown
- Thermal-shutdown and current-limit protection
- 24-pin 4mm x 4mm MLF®
- 24-pin ePad TSSOP
- -40°C to +125°C junction temperature range

Applications

- High power density point-of-load conversion
- Servers and routers
- DVD recorders
- Computing peripherals
- Base stations
- FPGAs, DSP and low-voltage ASIC power

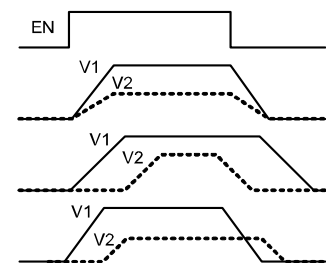
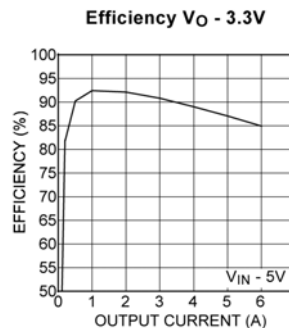
Typical Application



MIC22600 6A 1MHz Synchronous Output Converter

Note:

1. Using a free-wheeling Schottky diode improves efficiency.



Sequencing & Tracking

Ramp Control is a trademark of Micrel, Inc.
MLF and MicroLeadFrame are registered trademarks of Amkor Technology, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • <http://www.micrel.com>

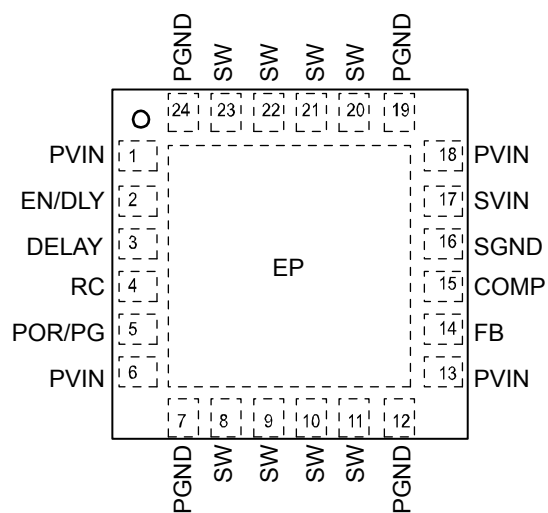
Ordering Information

Part Number	Voltage	Junction Temperature Range	Package	Lead Finish
MIC22600YML	Adjustable	-40° to +125°C	24-Pin 4mm x 4mm MLF®	Pb-Free
MIC22600YTSE	Adjustable	-40° to +125°C	24-pin ePad TSSOP	Pb-Free

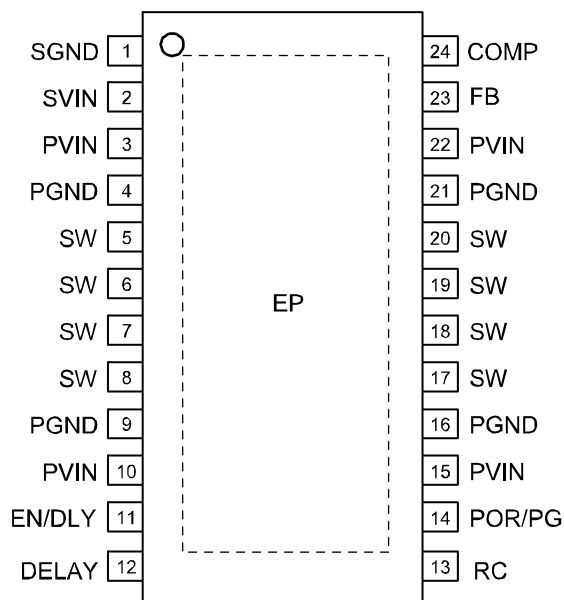
Note:

MLF® is a GREEN RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



24-Pin 4mm x 4mm MLF (ML)



24-pin ePad TSSOP

Pin Description

Pin Number MLF-24	Pin Number TSSOP-24	Pin Name	Description
1, 6, 13, 18	3, 10, 15, 22	PVIN	Power Supply Voltage (Input): Requires bypass capacitor to GND.
17	2	SVIN	Signal Power Supply Voltage (Input): Requires bypass capacitor to GND.
2	11	EN/DLY	EN/DLY (Input): When this pin is pulled higher than the enable threshold, the part will start up. Below this voltage the device is in its low quiescent current mode. The pin has a 1 μ A current source charging it to VIN. By adding a capacitor to this pin a delay may easily be generated. The enable function will not operate with an input voltage lower than the min specified voltage.
4	13	RC	Ramp Control: Capacitor to ground from this pin determines slew rate of output voltage during start-up. This can be used for tracking capability as well as soft start. RC pin cannot be left floating. Use a minimum capacitor value of 220pF or larger.
14	23	FB	Feedback: Input to the error amplifier, connect to the external resistor divider network to set the output voltage.
15	24	COMP	Compensation pin (Input): Place a RC network to GND to compensate the device, see applications section.
5	14	POR/PG	Power On Reset (Output): Open-drain output device indicates when the output is out of regulation and is active after the delay set by the DELAY pin.
7, 12, 19, 24	4, 9, 16, 21	PGND	Power Ground (Signal): Ground
16	1	SGND	Signal Ground (Signal): Ground
3	12	DELAY	DELAY (Input): Capacitor to ground sets internal delay timer. Timer delays power-on reset (POR) output at turn-on and ramp down at turn-off.
8, 9, 10, 11, 20, 21, 22, 23	5, 6, 7, 8, 17, 18 19, 20	SW	Switch (Output): Internal power MOSFET output switches.
EP	EP	GND	Exposed Pad (Power): Must make a full connection to a GND plane for full output power to be realized.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (PVIN, SVIN).....	-0.3V to 6V
Output Switch Voltage (SW)	-0.3V to 6V
Output Switch Current (ISW).....	Internally Limited
Logic Input Voltage (EN, POR, DELAY)	-0.3V to VIN
Control Voltage (RC, COMP, FB)	-0.3V to VIN
Lead Temperature (soldering 10sec.).....	260°C
Storage Temperature (Ts)	-65°C to +150°C
ESD Rating ⁽³⁾	2kV

Operating Ratings⁽²⁾

Supply Voltage (VIN).....	2.6V to 5.5V
Junction Temperature (Tj)	-40°C ≤ Tj ≤ +125°C
Thermal Resistance	
4x4 MLF-24 (θJC)	14°C/W
4x4 MLF-24 (θJA)	40°C/W
24-pin ePad TSSOP (θJC).....	12.9°C/W
24-pin ePad TSSOP (θJA).....	32.2°C/W

Electrical Characteristics⁽⁴⁾

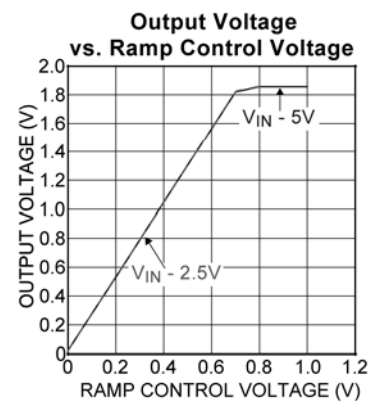
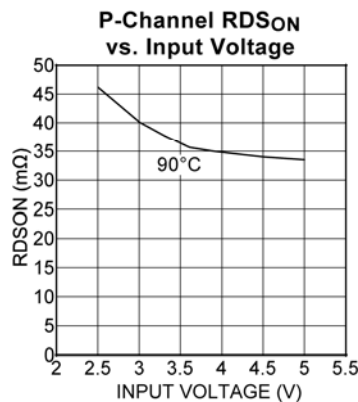
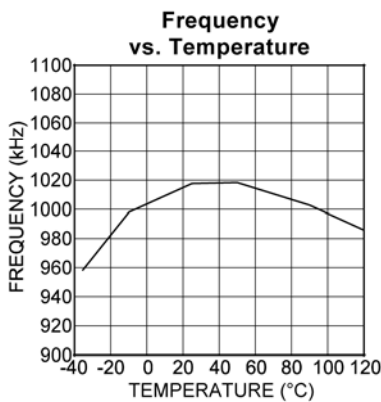
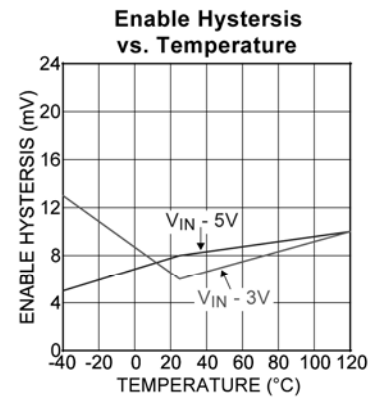
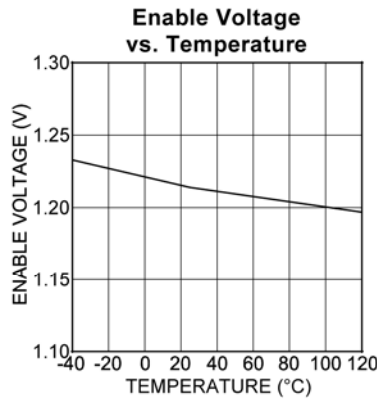
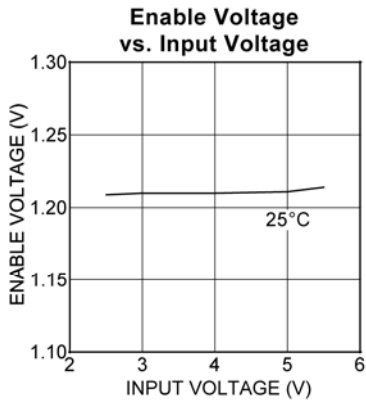
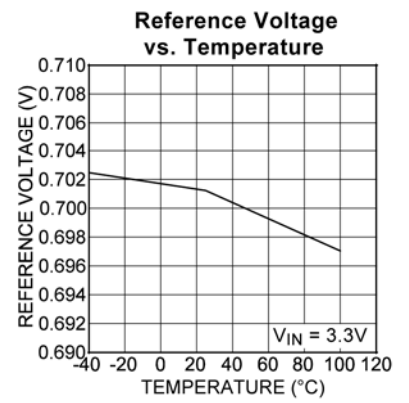
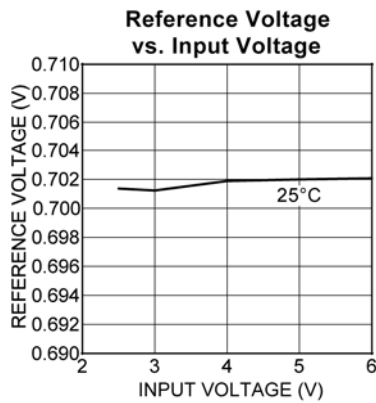
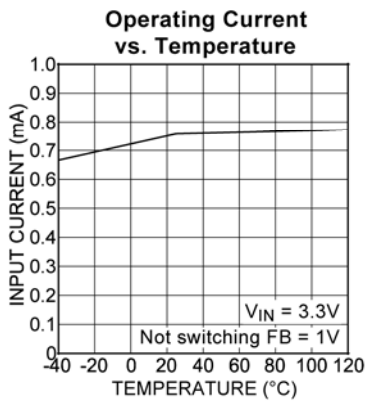
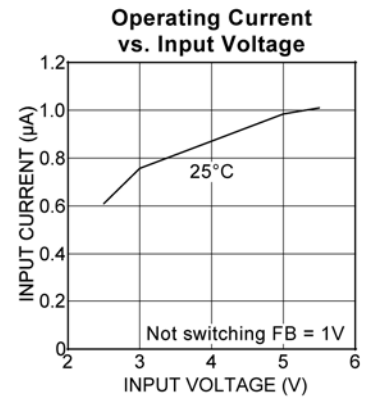
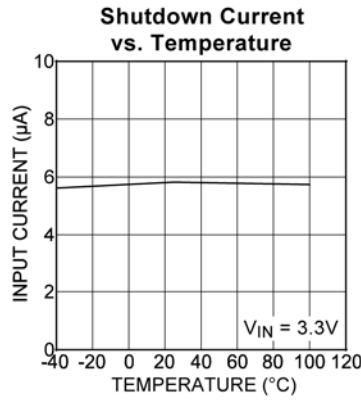
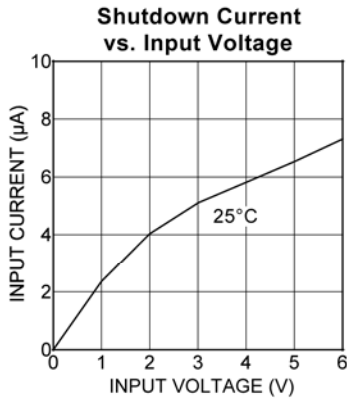
T_A = 25°C with V_{IN} = V_{EN} = 3.3V; V_{OUT} = 1.8V, unless otherwise specified. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		2.6		5.5	V
V _{IN} Turn-On Voltage Threshold	V _{IN} rising	2.4	2.5	2.6	V
UVLO Hysteresis			280		mV
Quiescent Current, PWM Mode	V _{EN} ≥ 1.34V; V _{FB} = 0.9V (not switching)		850	1300	μA
Shutdown Current	V _{EN} = 0V		5	10	μA
Feedback Voltage	± 1% ± 2% (over temperature)	0.693 0.686	0.7	0.707 0.714	V
FB Pin Input Current			1	100	nA
Current Limit in PWM Mode	V _{FB} = 0.5*V _{NOM}	6.5	9	11.5	A
Output Voltage Line Regulation	V _{OUT} 1.8V, V _{IN} = 2.6 to 5.5V, I _{LOAD} = 100mA		0.2		%
Output Voltage Load Regulation	100mA < I _{LOAD} < 6000mA, V _{IN} = 3.3V		0.2		%
Maximum Duty Cycle	V _{FB} ≤ 0.5V	100			%
Switch ON-Resistance PFET	I _{SW} = 1000mA; V _{FB} = 0.5V		0.03		Ω
Switch ON-Resistance NFET	I _{SW} = 1000mA; V _{FB} = 0.9V		0.025		
Oscillator Frequency		0.8	1	1.2	MHz
EN/DLY Threshold Voltage		1.14	1.24	1.34	V
EN/DLY Source Current	V _{IN} = 2.6 to V _{IN} = 5.5V	0.7	1	1.3	μA
RC Pin I _{RAMP}	Ramp Control Current	0.7	1	1.3	μA
Power-on-Reset I _{PG(LEAK)}	V _{PORH} = 5.5V; POR = High			1 2	μA
Power-on-Reset V _{PG(LO)}	Output Logic-Low Voltage (undervoltage condition), I _{POR} = 5mA		130		mV
Power-on-Reset V _{PG}	Threshold, % of V _{OUT} below nominal	7.5	10	12.5	%
	Hysteresis		2		%
Over-Temperature Shutdown			160		°C
Over-Temperature Shutdown Hysteresis			20		°C

Notes:

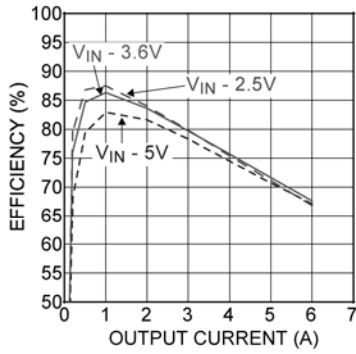
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended.
4. Specification for packaged product only.

Typical Characteristics

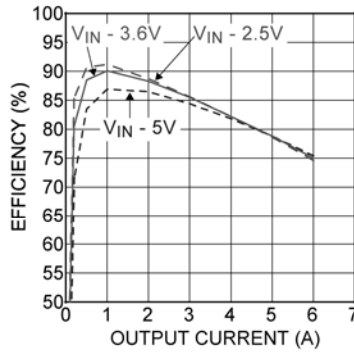


Typical Characteristics (Continued)

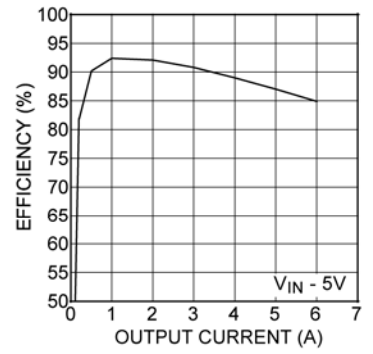
Efficiency V_O - 1.2V



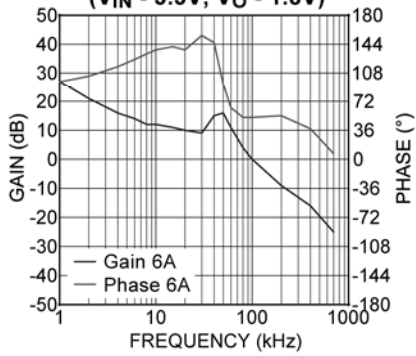
Efficiency V_O - 1.8V



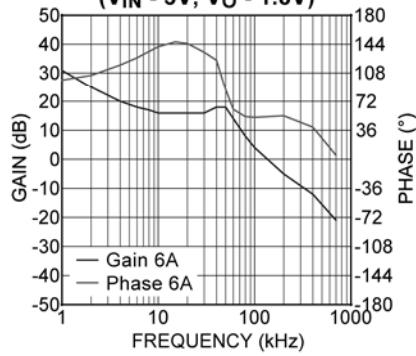
Efficiency V_O - 3.3V



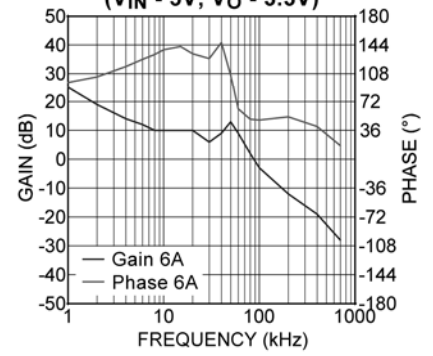
Bode Plot
($V_{IN} - 3.3V, V_O - 1.8V$)



Bode Plot
($V_{IN} - 5V, V_O - 1.8V$)

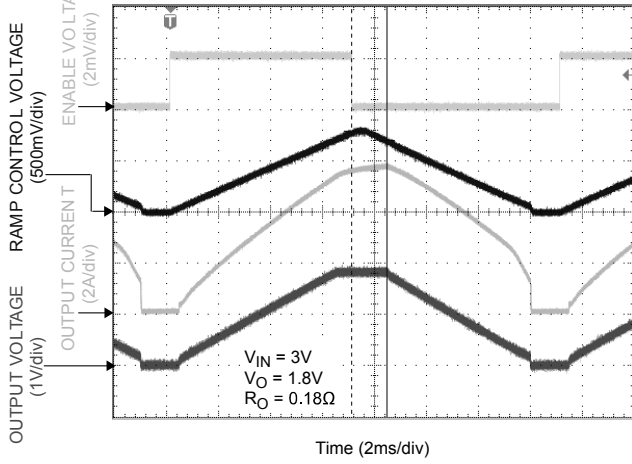


Bode Plot
($V_{IN} - 5V, V_O - 3.3V$)

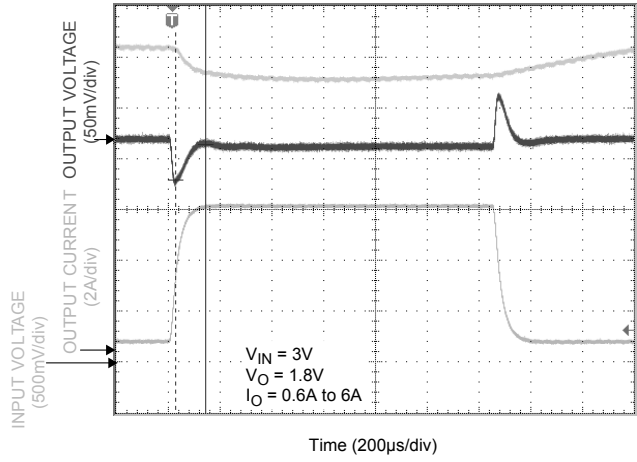


Functional Characteristics

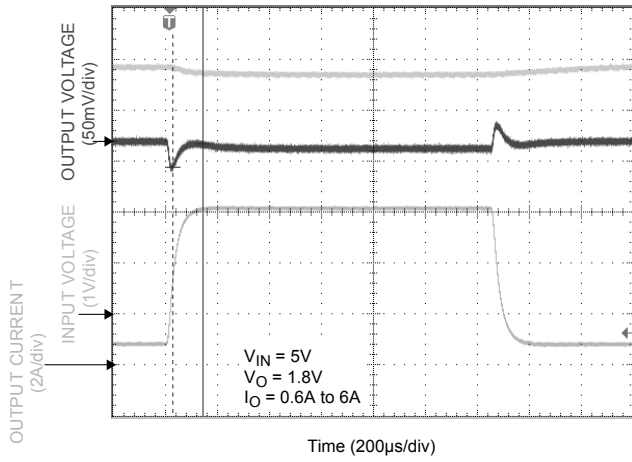
Start-Up/Shutdown ($C_{RC} = 10nF$)



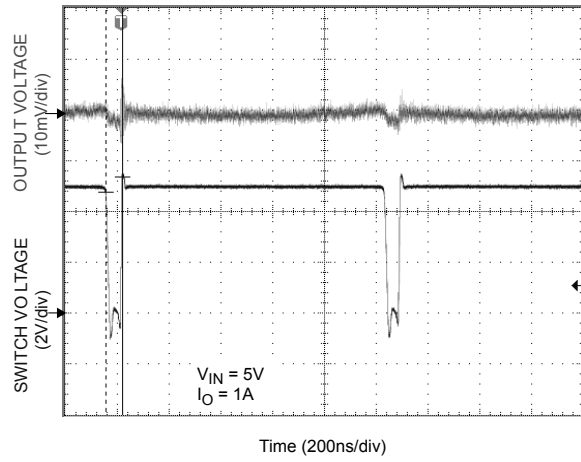
Transient Response



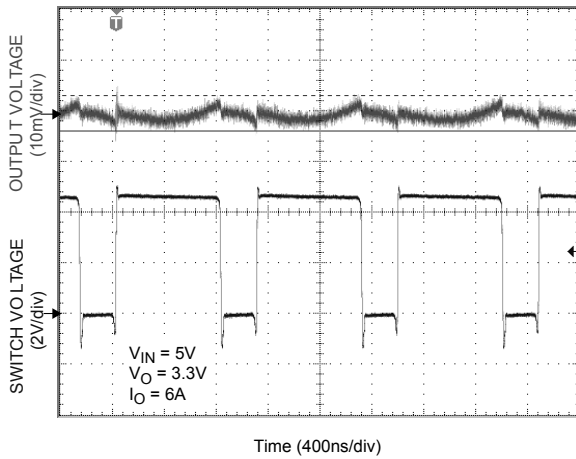
Transient Response



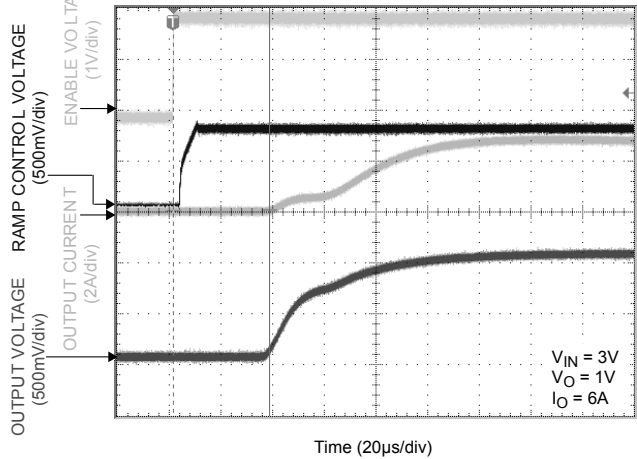
High DC Operation



Output Noise & Ripple

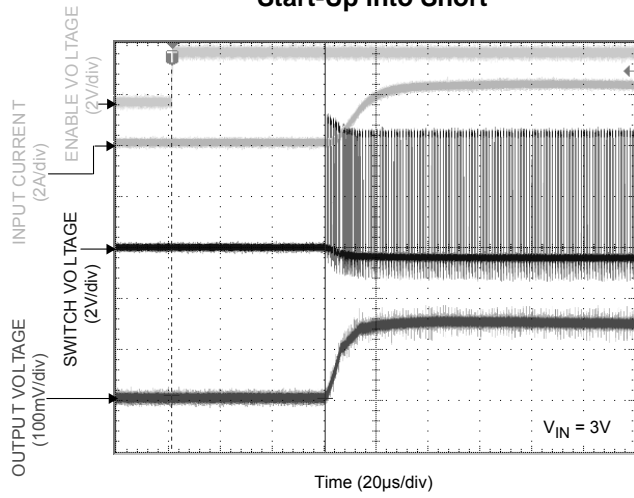


Start-Up ($C_{RC} = 0nF$)

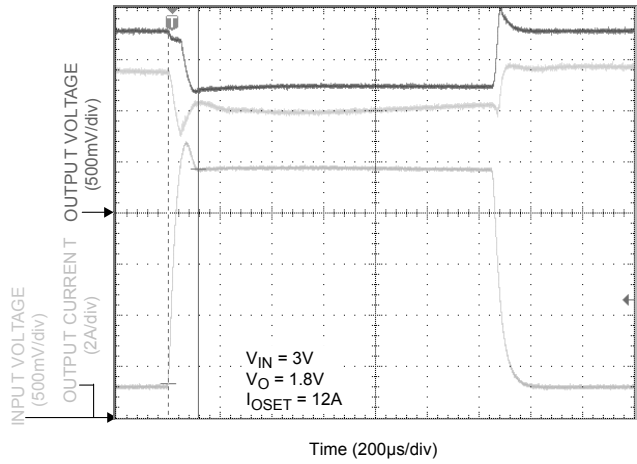


Functional Characteristics (Continued)

Start-Up into Short

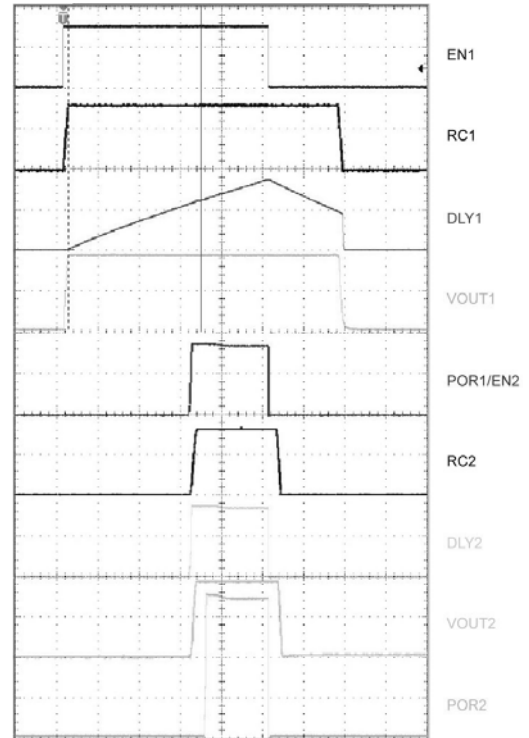
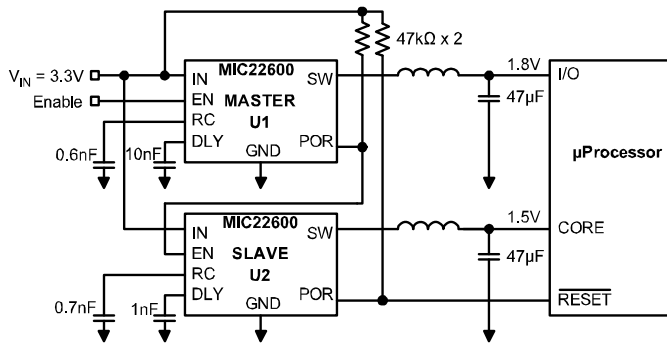


Current Limit Behavior

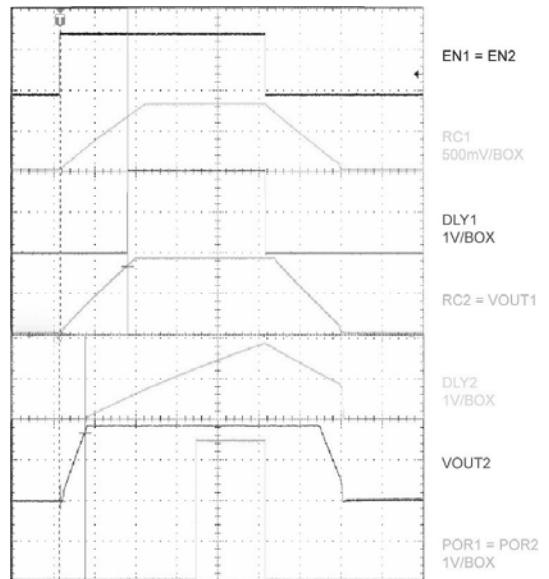
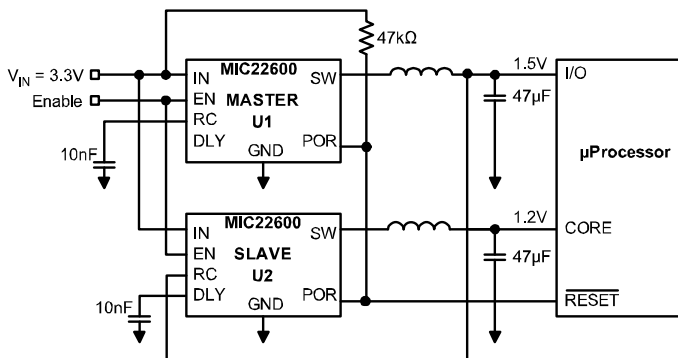


Typical Circuits and Waveforms

Sequencing Circuit and Waveform



Tracking Circuit and Waveform



Functional Diagram

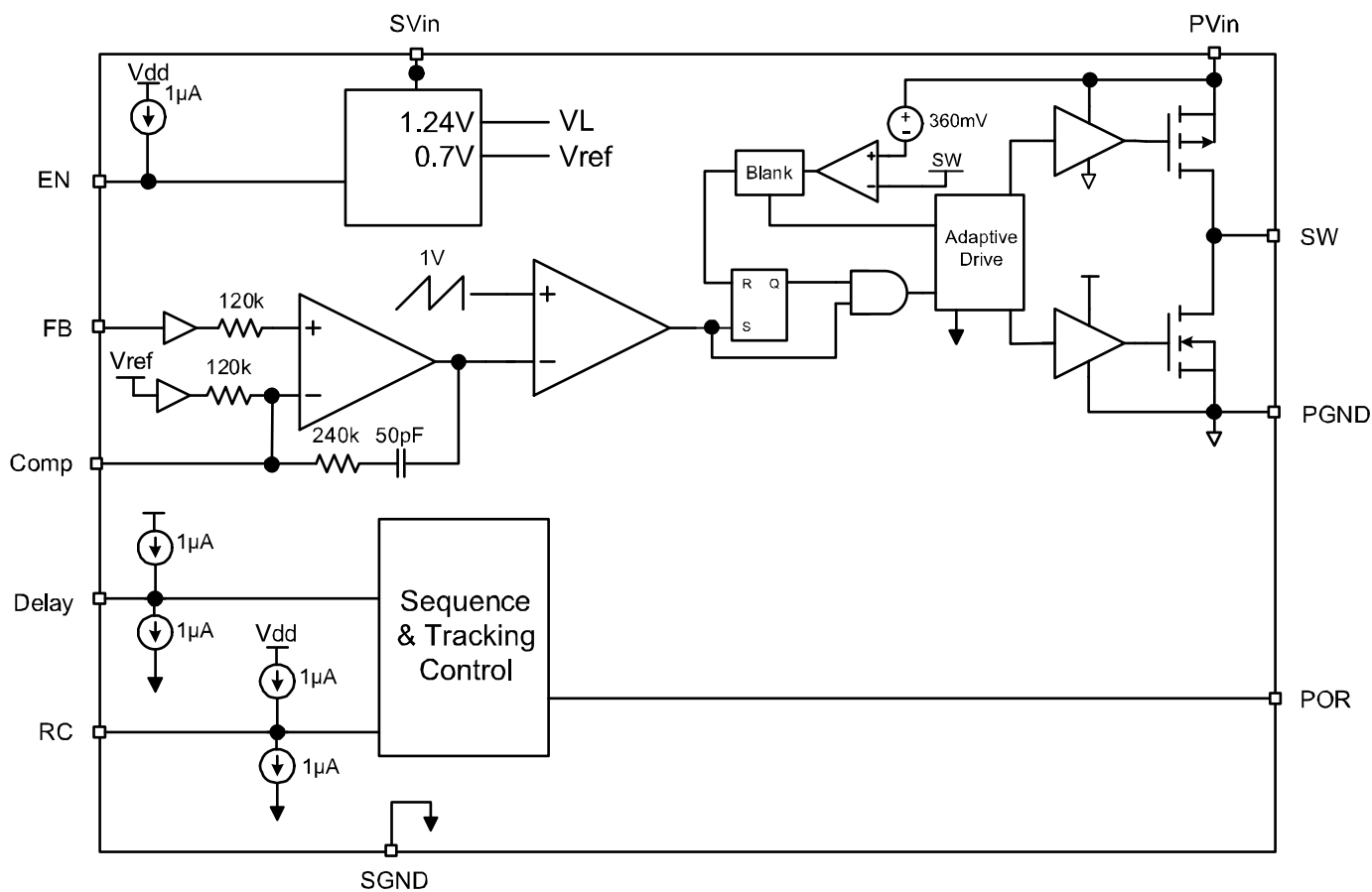


Figure 1. MIC22600 Block Diagram

Functional Description

PVIN, SVIN

PVIN is the input supply to the internal 30mΩ P-Channel Power MOSFET. This should be connected externally to the SVIN pin. The supply voltage range is from 2.6V to 5.5V. A 10μF ceramic is recommended for bypassing each PVIN supply.

EN/DLY

This pin is internally fed with a 1μA current source from VIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V.

RC

RC allows the slew rate of the output voltage to be programmed by the addition of a capacitor from RC to ground. RC is internally fed with a 1μA current source and VOUT slew rate is proportional to the capacitor and the 1μA source. RC pin cannot be left floating. Use a minimum capacitor value of 220pF or larger.

DELAY

Adding a capacitor to this pin allows the delay of the POR signal.

When VOUT reaches 90% of its nominal voltage, the DELAY pin current source (1μA) starts to charge the external capacitor. At 1.24V, POR is asserted high.

COMP

The MIC22600 uses an internal compensation network containing a fixed frequency zero (phase lead response) and pole (phase lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor will add the necessary pole and zero for voltage mode loop stability using low value, low ESR ceramic capacitors.

FB

The feedback pin provides the control path to control the output. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. Refer to the feedback section in the “Applications Information” for more detail.

POR

This is an open drain output. A 47k resistor can be used for a pull up to this pin. POR is asserted high when output voltage reaches 90% of nominal set voltage and after the delay set by C_{DELAY}. POR is asserted low without delay when enable is set low or when the output goes below the -10% threshold. For a Power Good (PG) function, the delay can be set to a minimum. This can be done by removing the DELAY capacitor.

SW

This is the connection to the source of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high frequency high power connection; therefore traces should be kept as short and as wide as practical.

SGND

Internal signal ground for all low power sections.

PGND

Internal ground connection to the source of the internal N-Channel MOSFETs.

Application Information

The MIC22600 is a 6A Synchronous step down regulator IC with a fixed 1 MHz, voltage mode PWM control scheme. The other features include tracking and sequencing control for controlling multiple output power systems, power on reset.

Component Selection

Input Capacitor

A minimum 10 μ F ceramic is recommended on each of the PVIN pins for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics is not recommended.

Output Capacitor

The MIC22600 was designed specifically for the use of ceramic output capacitors and 22 μ F is optimum output capacitor. 22 μ F can be increased to 100 μ F to improve transient performance. Since the MIC22600 is a voltage mode controller, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22600.

Inductor Selection

Inductor selection is determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22600 is designed to use a 0.47 μ H to 4.7 μ H inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the Current Limit of the MIC22600 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC.

It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DCR is inversely proportional to size and can represent a significant efficiency loss. Refer to the "Efficiency Considerations" below for a more detailed description.

EN/DLY Capacitor

EN/DLY sources 1 μ A out of the IC to allow a startup delay to be implemented. The delay time is simply the time it takes 1 μ A to charge CDLY to 1.25V. Therefore:

$$T_{DLY} = \frac{1.24 \times C_{DLY}}{1.10^{-6}}$$

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

$$\text{Efficiency \%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it decreases consumption of current for battery powered applications. Reduced current drawn from a battery increases the devices operating time, particularly in hand held devices.

There are mainly two loss terms in switching converters: conduction losses and switching losses. Conduction losses are simply the power losses due to VI or I^2R . For example, power is dissipated in the high side switch during the on cycle. The power loss is equal to the high side MOSFET $RDS_{(ON)}$ multiplied by the RMS Switch Current squared (I_{SW}^2). During the off cycle, the low side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor's DCR and capacitor's ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The power consumed at 1MHz frequency and power loss due to switching transitions add up to switching losses. A free wheeling schottky diode is recommended to use in parallel with synchronous N-MOSFET to improve the efficiency.

Figure 2 shows an efficiency curve. The portion, from 0A to 1A, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

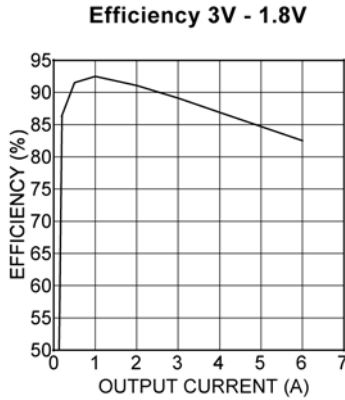


Figure 2. Efficiency Curve

The region, 1A to 6A, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, reducing the internal $R_{DS(ON)}$. This improves efficiency by decreasing conduction loss in the device but the inductor DCR loss is inherent to the device. So inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{(V_{OUT} \times I_{OUT}) + L_{PD}} \right) \right] \times 100$$

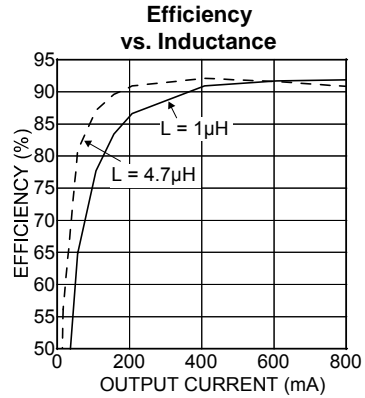


Figure 3. Efficiency vs. Inductance

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductance reduces the peak-to-peak inductor ripple current, which minimize losses. The graph in Figure 3 illustrates the effects of inductance value at light load.

Compensation

The MIC22600 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal 1MHz ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100-200kHz, the MIC22600 is capable of extremely fast transient responses.

The MIC22600 is designed to be stable with a typical application using a 1µH inductor and a 47µF ceramic (X5R) output capacitor. These values can be varied dependant upon the tradeoff between size, cost and efficiency, keeping the LC natural frequency ($\frac{1}{2 \times \pi \times \sqrt{L \cdot C}}$) ideally less than 26 kHz to ensure stability can be achieved. The minimum recommended inductor value is 0.47µH and minimum recommended output capacitor value is 22µF. With a larger inductor, there is a reduced peak-to-peak current which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20k resistor) are shown below.

L	C		
	22-47 μ F	47 μ F- 100 μ F	100 μ F- 470 μ F
0.47 μ H	0*-10pF	22pF	33pF
1 μ H	0 [†] -15pF	15-22pF	33pF
2.2 μ H	15-33pF	33-47pF	100-220pF
* $V_{OUT} > 1.2V$, [†] $V_{OUT} > 1V$			

Table1. Compensation Capacitor Selection

Feedback

The MIC22600 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. The resistor divider network for a desired V_{OUT} is given by:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

where V_{REF} is 0.7V and V_{OUT} is the desired output voltage. A 10k Ω or lower resistor value from the output to the feedback is recommended since large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50pF – 100pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

PWM Operation

The MIC22600 is a voltage mode, pulse width modulation (PWM) controller. By controlling the duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22600 will run at 100% duty cycle.

The MIC22600 provides constant switching at 1MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side P-Channel MOSFET from the input supply to the switch pin and an N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, a freewheeling Schottky diode from the switch node-to-ground is not required.

PWM control provides fixed-frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved.

Sequencing and Tracking

The MIC22600 provides additional pins to provide up/down sequencing and tracking capability for connecting multiple voltage regulators together.

EN/DLY Pin

The EN pin contains a trimmed, 1 μ A current source which can be used with a capacitor to implement a fixed desired delay in some sequenced power systems. The threshold level for power on is 1.24V with a hysteresis of 20mV.

DELAY Pin

The DELAY pin also has a 1 μ A trimmed current source and a 1 μ A current sink which acts with an external capacitor to delay the operation of the Power On Reset (POR) output. This can be used also in sequencing outputs in a sequenced system, but with the addition of a conditional delay between supplies; allowing a first up, last down power sequence.

After EN is driven high, V_{OUT} will start to rise (rate determined by RC capacitor). As the FB voltage goes above 90% of its nominal set voltage, DELAY begins to rise as the 1 μ A source charges the external capacitor. When the threshold of 1.24V is crossed, POR is asserted high and DELAY continues to charge to a voltage SV_{IN} . When FB falls below 90% of nominal, POR is asserted low immediately. However, if EN is driven low, POR will fall immediately to the low state and DELAY will begin to fall as the external capacitor is discharged by the 1 μ A current sink. When the threshold of $((V_{TP}+1.24V)-1.24V)$ is crossed (V_{TP} is the internal voltage clamp, $V_{TP}=0.9V$), V_{OUT} will begin to fall at a rate determined by the RC capacitor. As the voltage change in both cases is 1.24V, both rising and falling delays are matched at $T_{POR} = \frac{1.24 \times C_{DLY}}{1.10^{-6}}$

RC Pin

The RC pin provides a trimmed 1 μ A current source/sink similar to the DELAY Pin for accurate ramp up (soft start) and ramp down control. This allows the MIC22600 to be used in systems requiring voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

1. Externally driven from a voltage source
2. Externally attached capacitor sets output ramp up/down rate

In the first case, driving RC with a voltage from 0V to V_{REF} programs the output voltage between 0 and 100% of the nominal set voltage.

In the second case, the external capacitor sets the ramp up and ramp down time of the output voltage. The time

is given by $T_{RAMP} = \frac{0.7 \cdot C_{RC}}{1.10^{-6}}$ where T_{RAMP} is the time

from 0 to 100% nominal output voltage.

RC pin cannot be left floating. Use a minimum capacitor value of 220pF or larger.

Sequencing and Tracking Examples

There are four distinct variations which are easily implemented using the MIC22600. The two sequencing variations are Delayed and Windowed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22600's to achieve these requirements.

Sequencing:

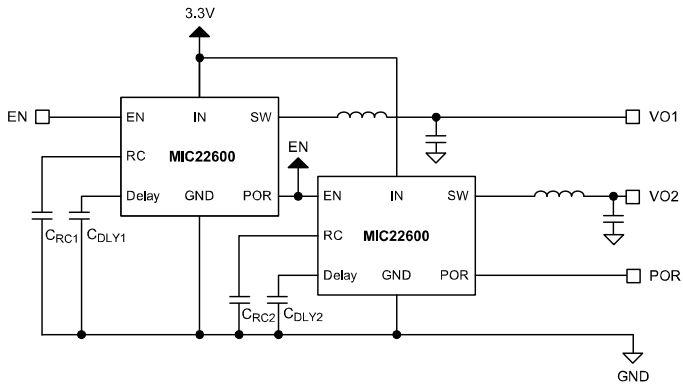


Figure 4. Sequencing MIC22600 Circuit

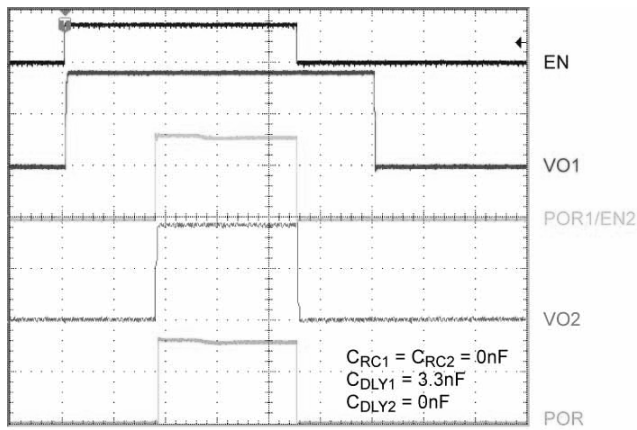


Figure 5. Window Sequencing Example

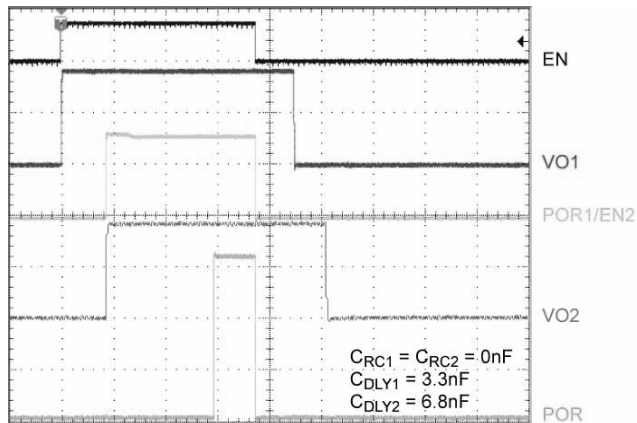


Figure 6. Delayed Sequencing Example

Normal Tracking:

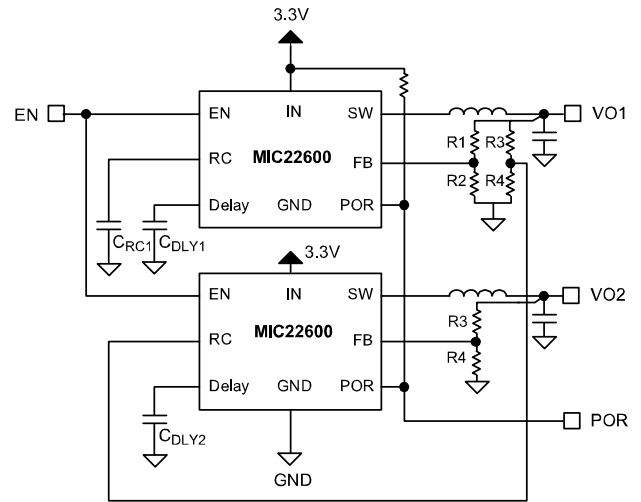


Figure 7. Normal Tracking Circuit

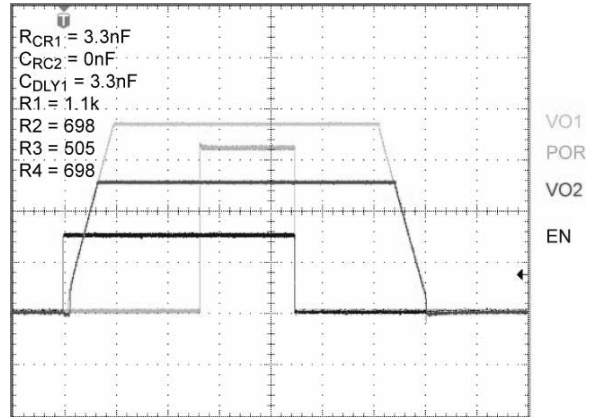


Figure 8. Normal Tracking Example

Ratio Metric Tracking:

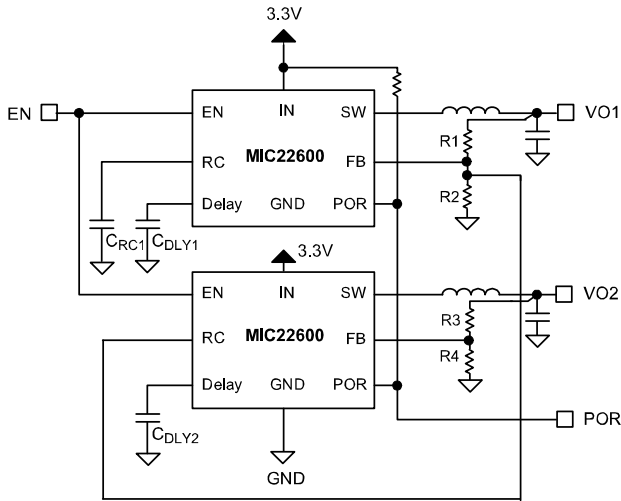


Figure 9. Ratio Metric Tracking Circuit

DDR Memory VDD and VTT Tracking

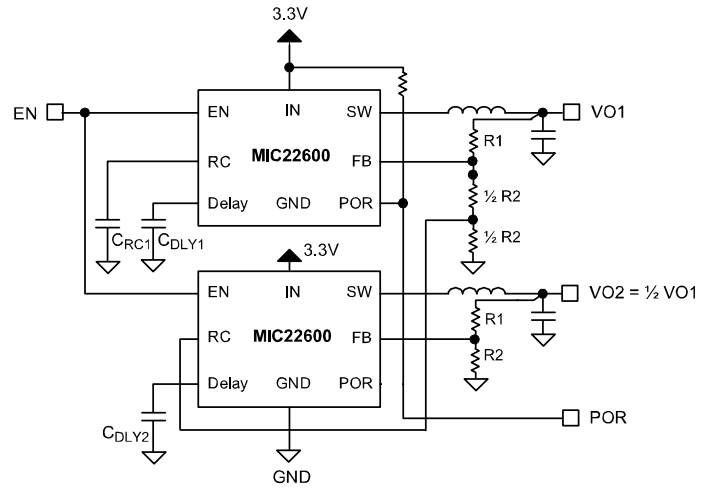


Figure 11. DDR Memory Tracking Circuit

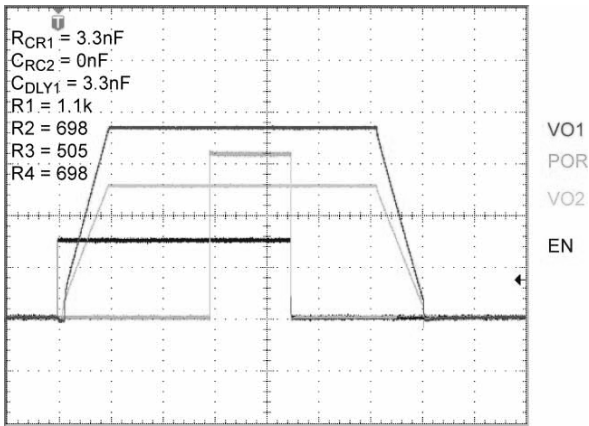


Figure 10. Ratio Metric Tracking Example

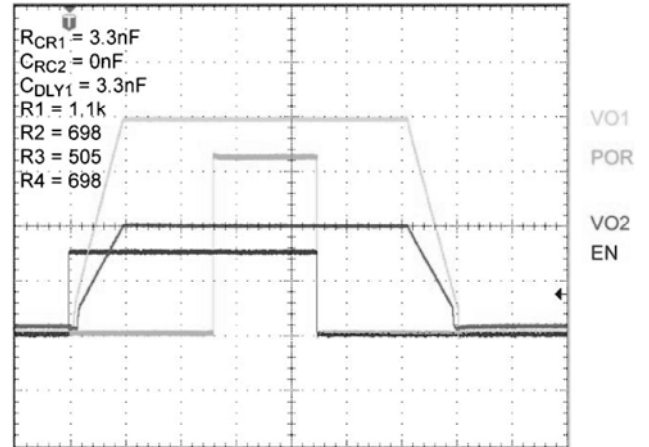


Figure 12. DDR Memory Tracking Example

An alternative method here shows an example of a V_{DDQ} & V_{TT} solution for a DDR memory power supply. Note that POR is taken from Vo_1 as POR_2 will not go high. This is because POR is set high when $FB > 0.9 \cdot V_{REF}$. In this example, FB_2 is regulated to $\frac{1}{2} \cdot V_{REF}$.

Current Limit

The MIC22600 is protected against overload in two stages. The first is to limit the current in the P-channel switch; the second is by over temperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 4 describes the operation of the current-limit circuit. Since the actual $R_{DS_{ON}}$ of the P-Channel MOSFET varies part-to-part, over temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current which is a directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependant upon the $R_{DS_{ON}}$ value. Current limit is set to 9A nominal. Variations in the scale factor K between the Power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

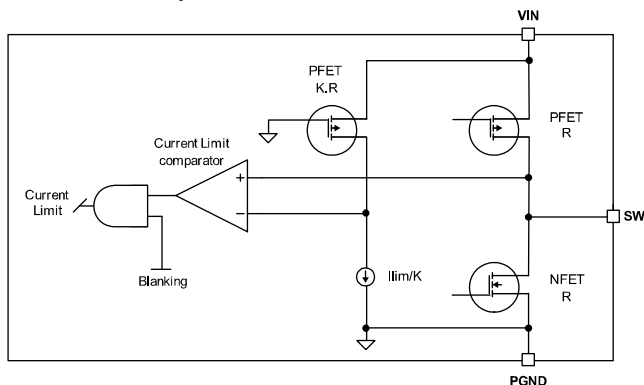


Figure 13. Current-Limit Detail

Thermal Considerations

The MIC22600 is packaged in the MLF® 4mm x 4mm, a package that has excellent thermal performance equaling that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePad) which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

$$T_J = T_{AMB} + P_{DISS} \cdot R\theta_{JA}$$

Where

- P_{DISS} is the power dissipated within the MLF® package and is typically 1.5W at 6A load. This has been calculated for a 1µH inductor and details can be found in Table 1 below for reference.
- $R\theta_{JA}$ is a combination of junction to case thermal resistance ($R\theta_{JC}$) and Case-to-Ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane to ambient, so $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.
- T_{AMB} is the Operating Ambient temperature.

Example:

The Evaluation board has two copper planes contributing to an $R\theta_{JA}$ of approximately 25°C/W. The worst case $R\theta_{JC}$ of the MLF 4x4 is 14°C/W.

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$$

$$R\theta_{JA} = 14 + 25 = 39^\circ\text{C/W}$$

To calculate the junction temperature for a 50°C ambient:

$$T_J = T_{AMB} + P_{DISS} \cdot R\theta_{JA}$$

$$T_J = 50 + (1.5 \times 39)$$

$$T_J = 109^\circ\text{C}$$

This is below the maximum of 125°C.

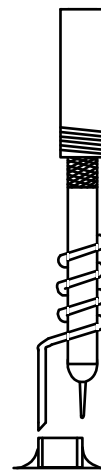
V_{OUT} @6A	V_{IN}				
	3	3.5	4	4.5	5
1	1.47	1.50	1.52	1.54	1.56
1.2	1.45	1.47	1.49	1.51	1.54
1.8	1.46	1.45	1.45	1.47	1.48
2.5	1.61	1.53	1.49	1.47	1.47
3.3	–	1.70	1.62	1.56	1.53

Table 2. Power Dissipation (W) for 6A Output

Ripple Measurements

To properly measure ripple on either input or output of a switching regulator, a proper ring in tip measurement is required. Standard oscilloscope probes come with a grounding clip, or a long wire with an alligator clip. Unfortunately, for high-frequency measurements, this ground clip can pick-up high frequency noise and erroneously inject it into the measured output ripple.

The standard evaluation board accommodates a home made version by providing probe points for both the input and output supplies and their respective grounds. This requires the removing of the oscilloscope probe sheath and ground clip from a standard oscilloscope probe and wrapping a non-shielded bus wire around the oscilloscope probe. If there does not happen to be any non-shielded bus wire immediately available, the leads from axial resistors will work. By maintaining the shortest possible ground lengths on the oscilloscope probe, true ripple measurements can be obtained.



PCB Layout Guideline

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC22602 converter.

IC

- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- The exposed pad (EP) on the bottom of the IC must be connected to the ground.
- Use several vias to connect the EP to the ground plane, layer 2.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Place a 22 μ F/6.3V ceramic bypass capacitor next to each of the 4 PVIN pins.
- Keep both the VIN and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal, but not between the input capacitors and IC pins.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In "Hot-Plug" applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.

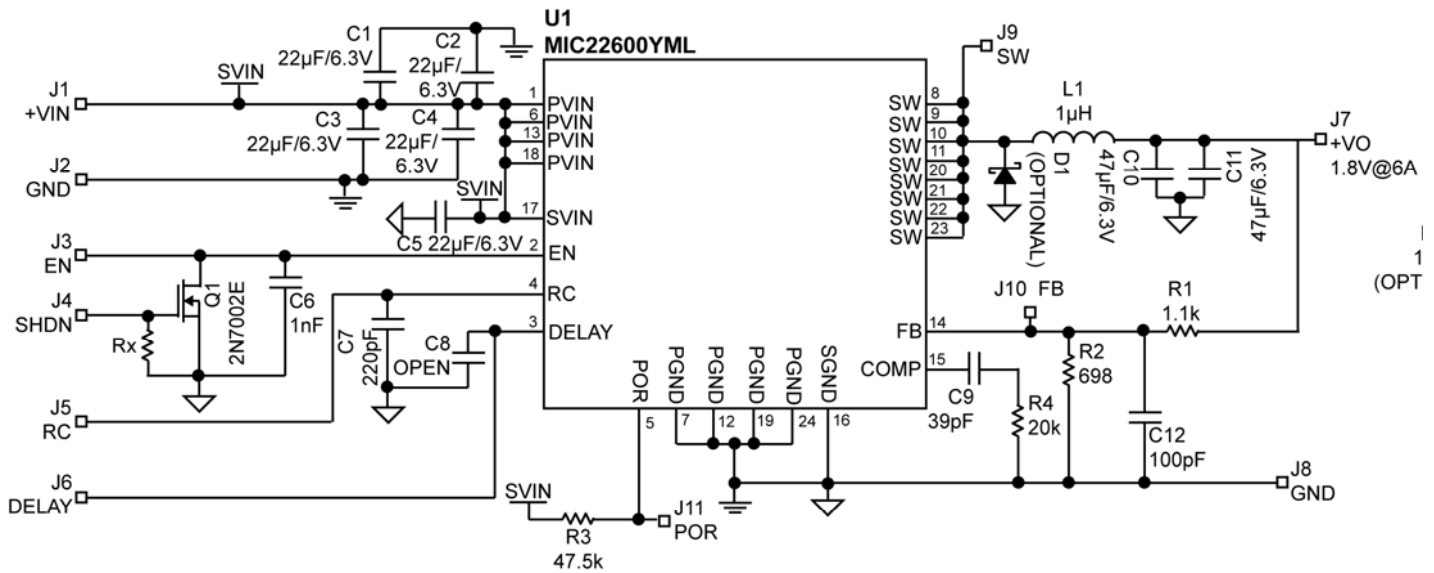
Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Diode

- Place the Schottky diode on the same side of the board as the IC and input capacitor.
- The connection from the Schottky diode's Anode to the input capacitors ground terminal must be as short as possible.
- The diode's Cathode connection to the switch node (SW) must be kept as short as possible.

MIC22600YML Schematic



NOTES:
 1. IF BUCK CAPACITOR ON INPUT RAIL IS AWAY (4 INCHES OR MORE) FROM THE MIC22600, INSTALL THE 470µF BUCK CAPACITOR NEAR VIN.
 2. SOURCE IMPEDANCE SHOULD BE AS LOW AS 10mΩ.

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4, C5	C2012X5R0J226M	TDK ⁽¹⁾	22µF/6.3V, 0805 Ceramic Capacitor	5
	08056D2226MAT	AVX ⁽²⁾		
	GRM21BR60J226ME39L	Murata ⁽³⁾		
C6	OPEN		Open, 0603 Ceramic Capacitor	1
C7	GRM188R71H221KA01D	Murata ⁽³⁾	220pF, 0603 Ceramic Capacitor	1
	VJ0603Y221KXACW1BC	Vishay ⁽⁴⁾		
	C1608X7R1H221K	TDK ⁽¹⁾		
C8	Open (VJ0603Y102KQCW1BC)	Vishay ⁽⁴⁾	1nF, 0603 Ceramic Capacitor	1
	Open (GRM188R71H102KA01D)	Murata ⁽³⁾		
C9	GRM1555C1H390JZ01D	Murata ⁽³⁾	39pF, 0402 Ceramic Capacitor	1
	VJ0402A390KXQCW1BC	Vishay ⁽⁴⁾		
C10, C11	C3216X5R0J476M	TDK ⁽¹⁾	47µF/6V, 1206 Ceramic Capacitor	2
	12066D476KAT	AVX ⁽²⁾		
	GRM31CC80G476ME19L	Murata ⁽³⁾		
C12	VJ0402A101KXQCW1BC	Vishay ⁽⁴⁾	100pF, 0402 Ceramic Capacitor	1
	GRM15551H101JZ01D	Murata ⁽³⁾		
D1	DFLS220L-7	Diodes Inc ⁽⁵⁾	2A, 20V Schottky Diode	1
L1	CDRH8D43NP-1R2NC	Sumida ⁽⁶⁾	1µH, 6A Inductor	1
	FP3-1R0-R	Coiltronics ⁽⁷⁾		
	SPM6530T-1R0M120	TDK ⁽¹⁾		

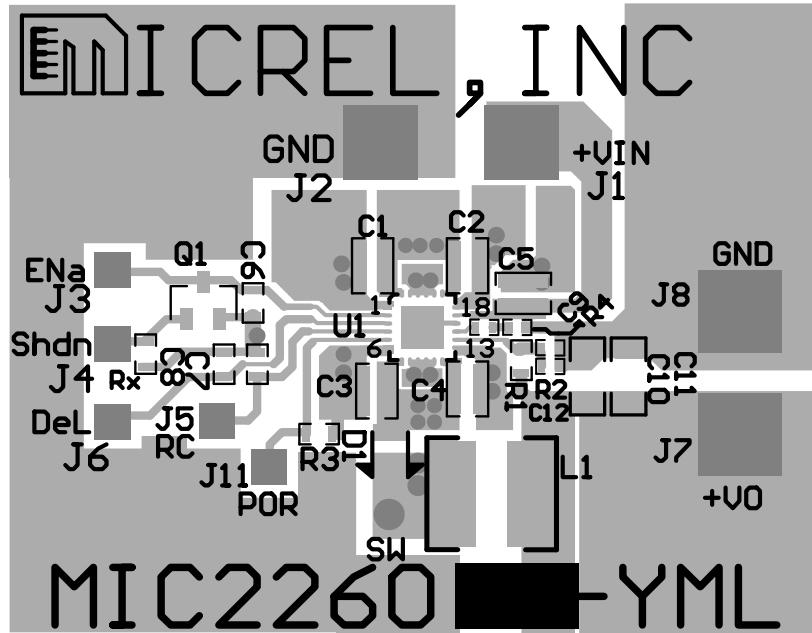
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
R1	CRCW06031101FKEYE3.	Vishay ⁽⁴⁾	1.1k, 0603 Resistor	1
R2	CRCW04026980FKEYE3.	Vishay ⁽⁴⁾	698Ω, 0402 Resistor	1
R3	CRCW06034752FKEYE3.	Vishay ⁽⁴⁾	47.5k, 0603 Resistor	1
R4	CRCW04022002FKEYE3.	Vishay ⁽⁴⁾	20k, 0402 Resistor	1
Rx	OPEN		Open, 0603 Resistor	1
Q1	OPEN		SOT-23	1
U1	MIC22600YML	Micrel⁽⁸⁾	Integrated 6A Synchronous Buck Regulator	1

Notes:

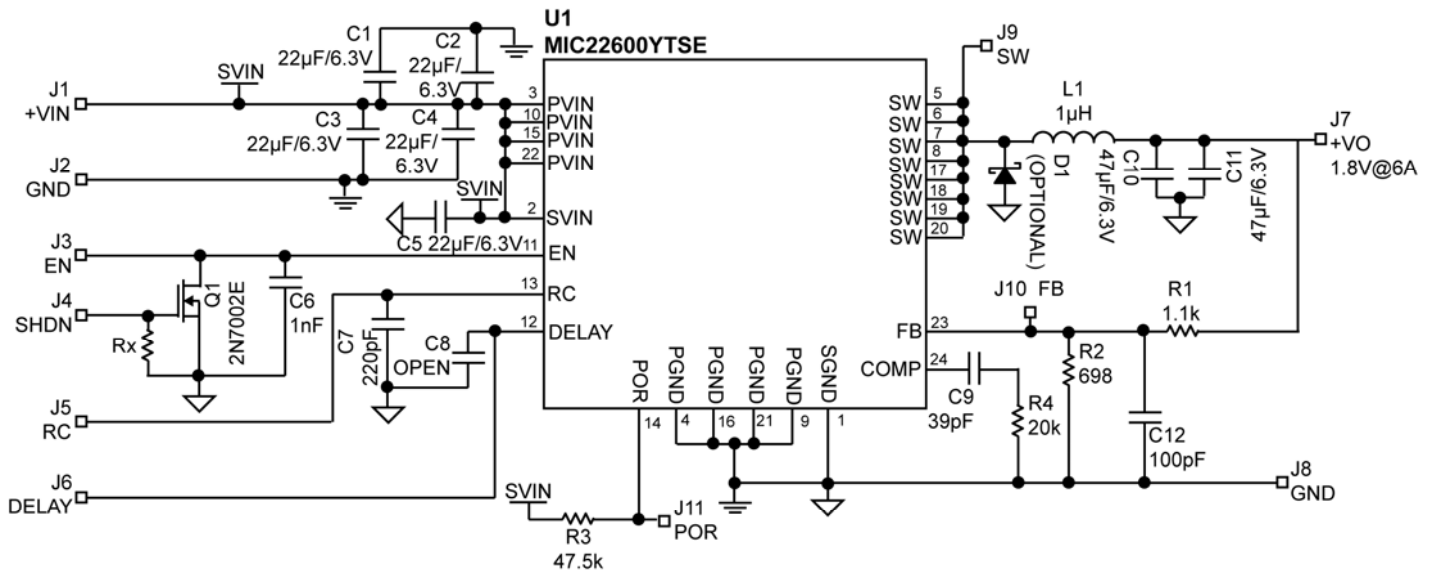
1. TDK: www.tdk.com.
2. AVX: www.avx.com.
3. Murata: www.murata.com.
4. Vishay: www.vishay.com.
5. Diodes Inc.: www.diodes.com.
6. Sumida: www.sumida.com.
7. Coiltronics: www.mouser.com/coiltronics.
8. **Micrel:** www.micrel.com.

PCB Layout Recommendations –YML Package



Top Layer

MIC22600YTSE Schematic



- NOTES:**
 1. IF BUCK CAPACITOR ON INPUT RAIL IS AWAY (4 INCHES OR MORE) FROM THE MIC22600, INSTALL THE 470µF BUCK CAPACITOR NEAR VIN.
 2. SOURCE IMPEDANCE SHOULD BE AS LOW AS 10mΩ.

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
C1, C2, C3, C4, C5	C2012X5R0J226M	TDK ⁽¹⁾	22µF/6.3V, 0805 Ceramic Capacitor	5
	08056D2226MAT	AVX ⁽²⁾		
	GRM21BR60J226ME39L	Murata ⁽³⁾		
C6	OPEN		Open, 0603 Ceramic Capacitor	1
C7	GRM188R71H221KA01D	Murata ⁽³⁾	220pF, 0603 Ceramic Capacitor	1
	VJ0603Y221KXACW1BC	Vishay ⁽⁴⁾		
	C1608X7R1H221K	TDK ⁽¹⁾		
C8	Open (VJ0603Y102KQCW1BC)	Vishay ⁽⁴⁾	1nF, 0603 Ceramic Capacitor	1
	Open (GRM188R71H102KA01D)	Murata ⁽³⁾		
C9	GRM1555C1H390JZ01D	Murata ⁽³⁾	39pF, 0402 Ceramic Capacitor	1
	VJ0402A390KXQCW1BC	Vishay ⁽⁴⁾		
C10, C11	C3216X5R0J476M	TDK ⁽¹⁾	47µF/6V, 1206 Ceramic Capacitor	2
	12066D476KAT	AVX ⁽²⁾		
	GRM31CC80G476ME19L	Murata ⁽³⁾		
C12	VJ0402A101KXQCW1BC	Vishay ⁽⁴⁾	100pF, 0402 Ceramic Capacitor	1
	GRM15551H101JZ01D	Murata ⁽³⁾		
D1	DFLS220L-7	Diodes Inc ⁽⁵⁾	2A, 20V Schottky Diode	1
L1	CDRH8D43NP-1R2NC	Sumida ⁽⁶⁾	1µH, 6A Inductor	1
	FP3-1R0-R	Coiltronics ⁽⁷⁾		
	SPM6530T-1R0M120	TDK ⁽¹⁾		

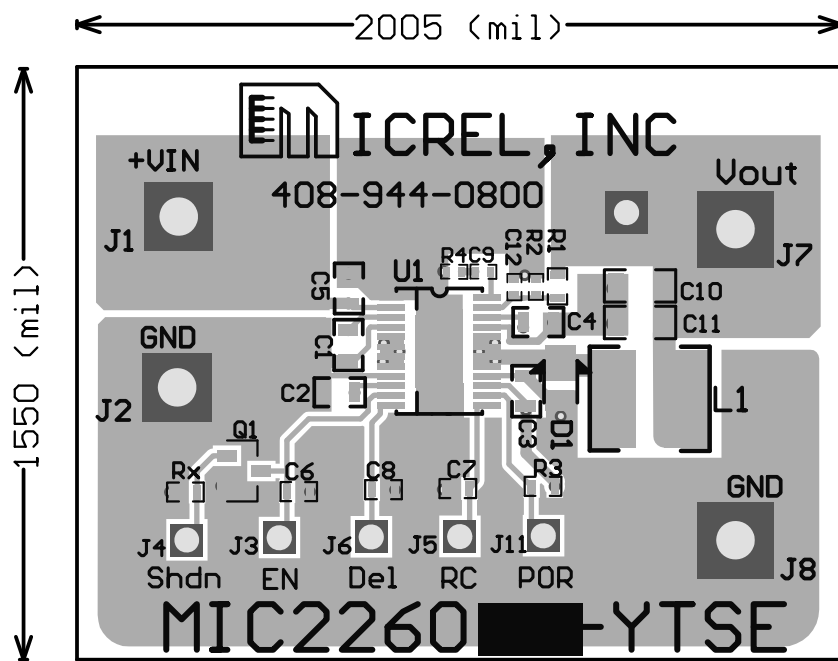
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty
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R2	CRCW04026980FKEYE3.	Vishay ⁽⁴⁾	698Ω, 0402 Resistor	1
R3	CRCW06034752FKEYE3.	Vishay ⁽⁴⁾	47.5k, 0603 Resistor	1
R4	CRCW04022002FKEYE3.	Vishay ⁽⁴⁾	20k, 0402 Resistor	1
Rx	OPEN		Open, 0603 Resistor	1
Q1	OPEN		SOT-23	1
U1	MIC22600YTSE	Micrel⁽⁸⁾	Integrated 6A Synchronous Buck Regulator	1

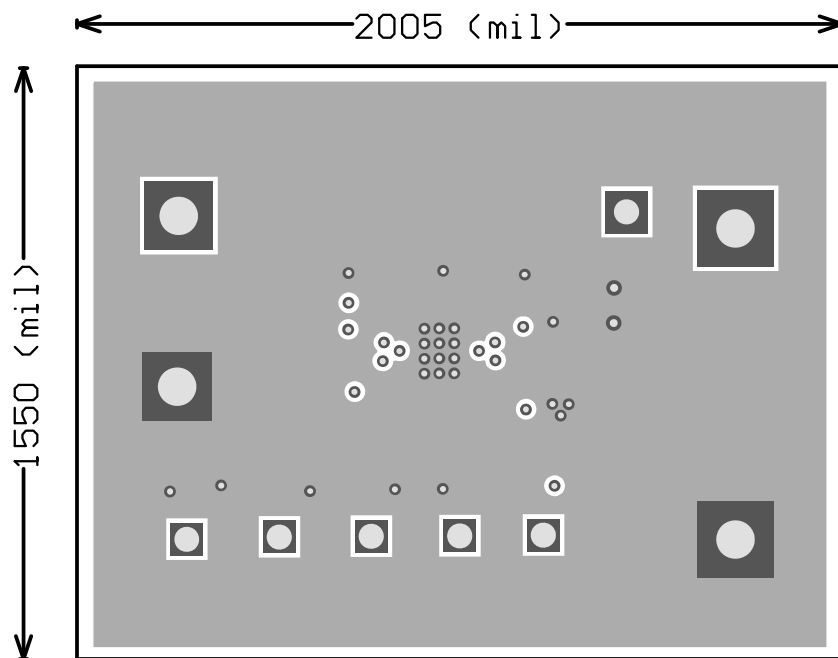
Notes:

1. TDK: www.tdk.com.
2. AVX: www.avx.com.
3. Murata: www.murata.com.
4. Vishay: www.vishay.com.
5. Diodes Inc.: www.diodes.com.
6. Sumida: www.sumida.com.
7. Coiltronics: www.mouser.com/coiltronics.
8. **Micrel:** www.micrel.com.

PCB Layout Recommendations – YTSE Package

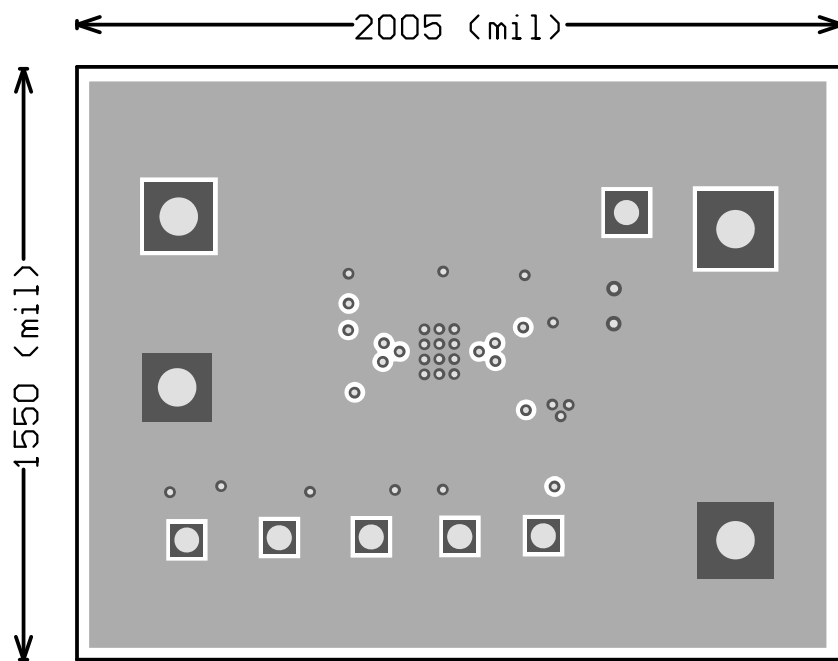


Top Layer

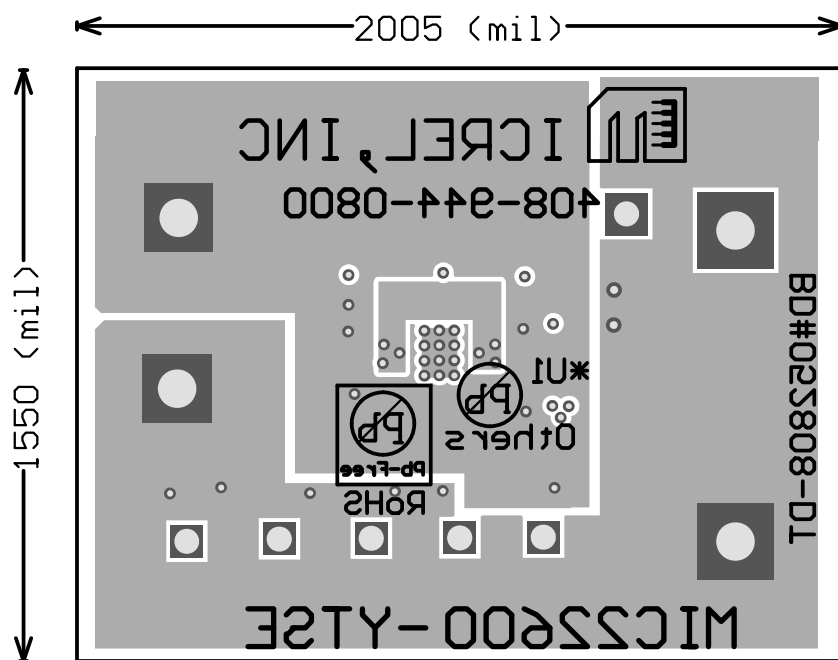


Mid Layer 1

PCB Layout Recommendations – YTSE Package (Continued)

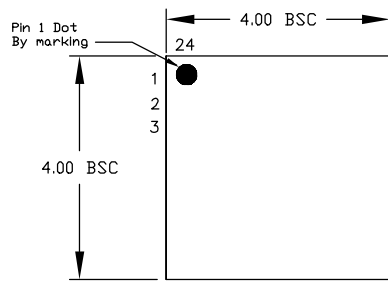


Mid Layer 2

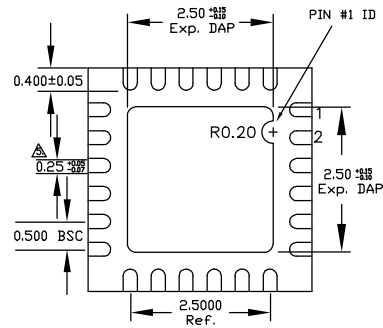


Bottom Layer

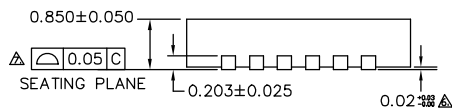
Package Information



TOP VIEW



BOTTOM VIEW



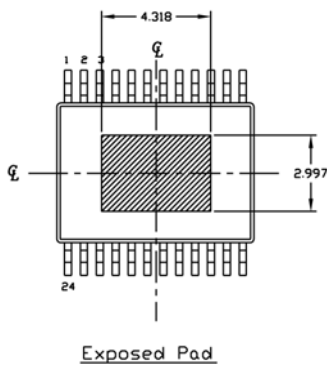
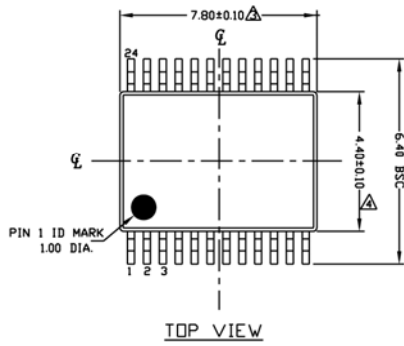
SIDE VIEW

NOTE:

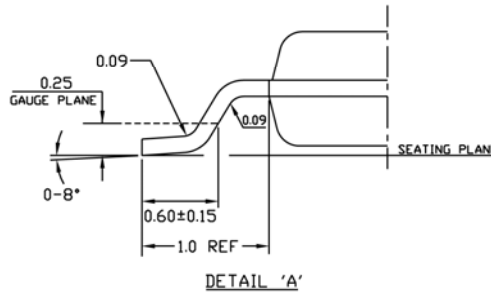
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- △ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- △ APPLIED ONLY FOR TERMINALS.
- △ APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Pin 4mm x 4mm MLF[®] (ML)

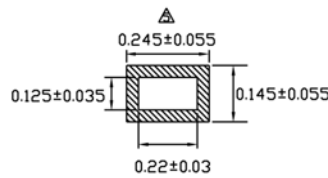
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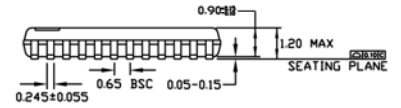
BOTTOM VIEW



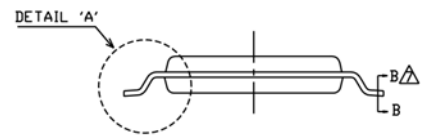
DETAIL 'A'



DETAIL 'B-B'



SIDE VIEW



END VIEW

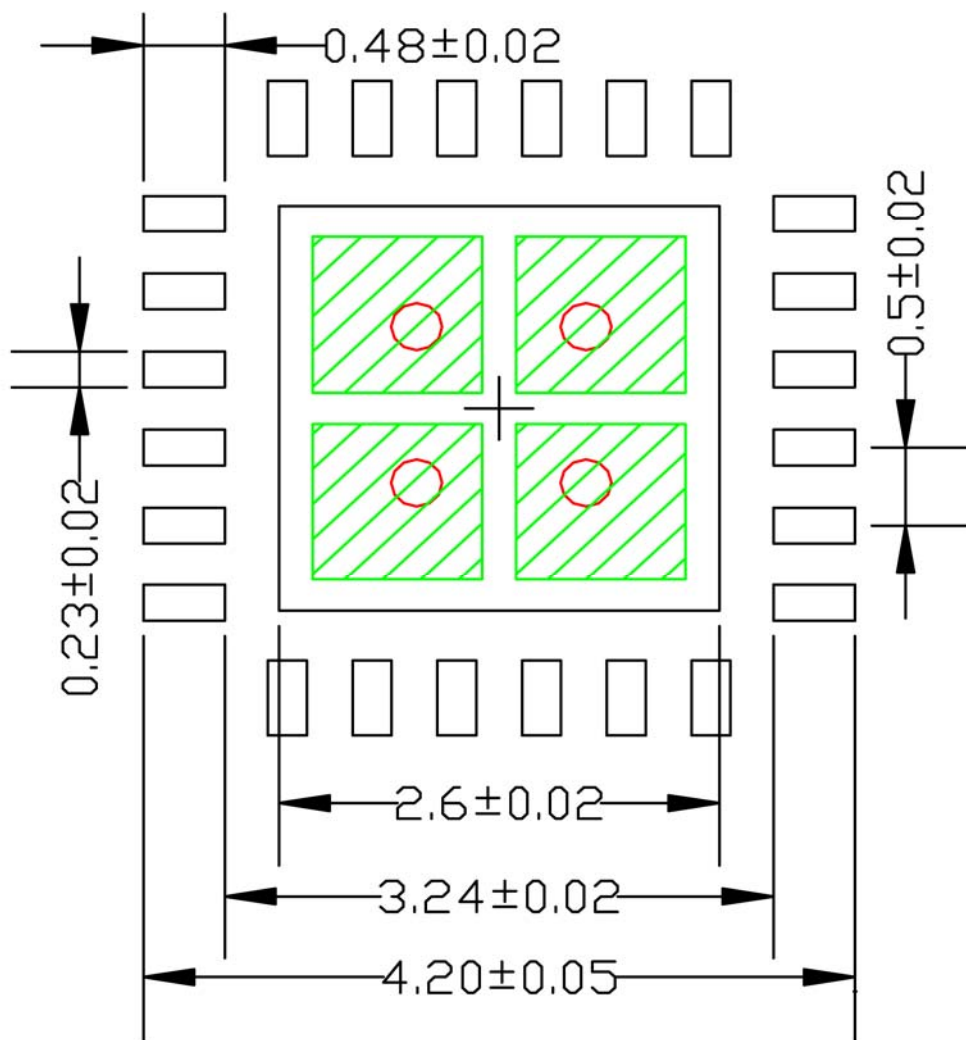
NOTES:

1. DIMENSIONS ARE IN MM.
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1994.
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR.
4. DIMENSION 'E1' DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION.
6. "N" IS THE MAXIMUM NUMBER OF LEAD TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. CROSS SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25mm FROM THE LEAD TIP

24-Pin ePad TSSOP

Recommended Landing Pattern

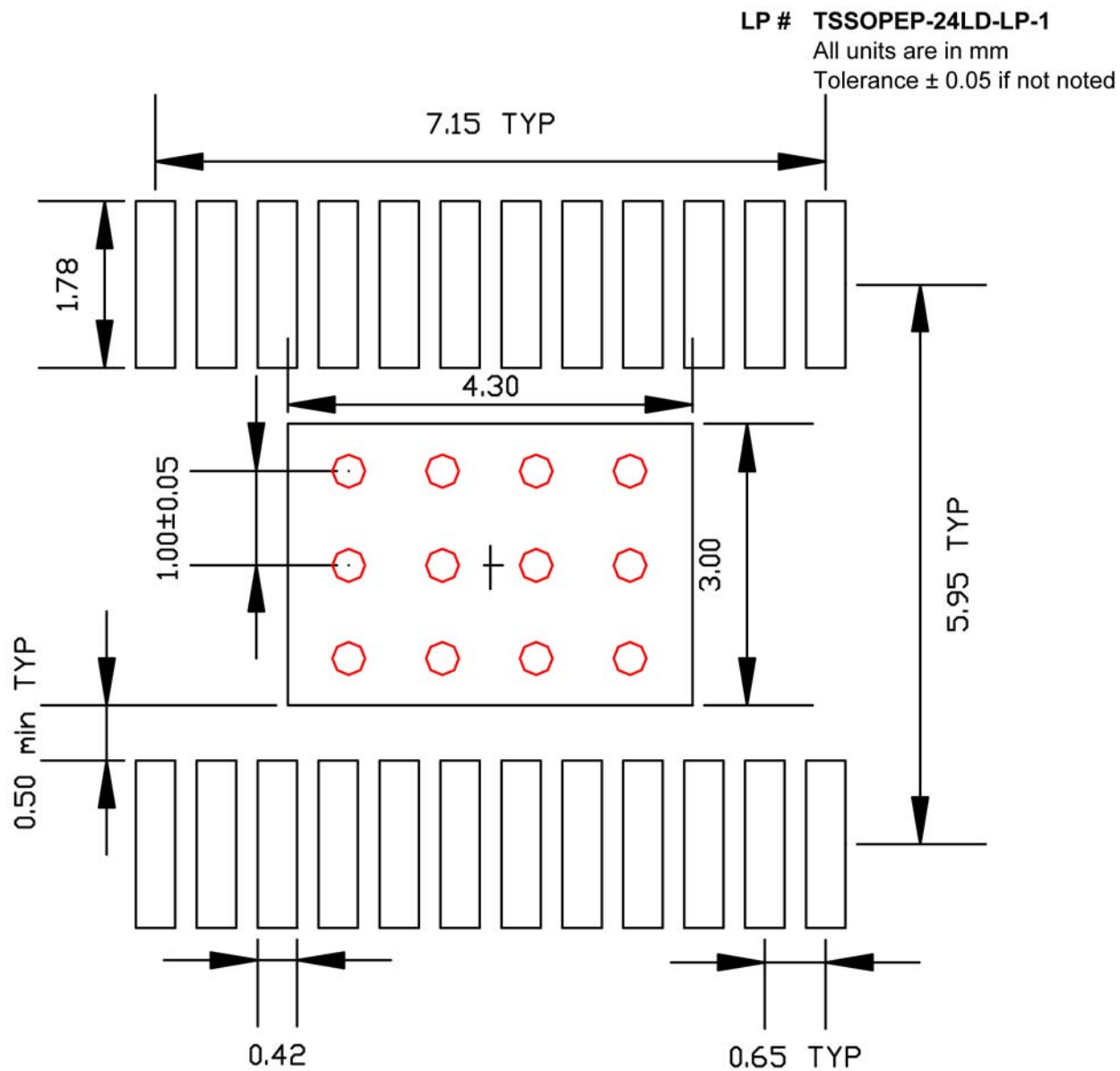
LP # MLF44Q-24LD-LP-1
 All units are in mm
 Tolerance ± 0.05 if not noted



Red circle indicates Thermal Via. Size should be .300mm - .350mm in diameter, 1.00mm pitch, and it should be connected to GND plane for maximum thermal performance.

Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Size should be 1.00mm x 1.00mm in size, 1.20mm pitch.

Recommended Landing Pattern (Continued)



Red circle indicates Thermal Via. Size should be .300mm - .350mm in diameter, and it should be connected to GND plane for maximum thermal performance.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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