MIC22950

10A Integrated Switch Synchronous Buck Regulator with Frequency Programmable to 2MHz

General Description

The Micrel MIC22950 is a high-efficiency 10A integrated switch, synchronous buck (step-down) regulator. The MIC22950 switching frequency is programmable from 400kHz to 2MHz, allowing the customer to optimize designing either for efficiency or for the smallest footprint. The MIC22950 achieves over 95% efficiency while still switching at 2MHz over a broad load range.

The ultra-high-speed control loop keeps the output voltage within regulation, even under extreme transient load swings commonly found in FPGAs and low voltage ASICs.

The output voltage can be adjusted down to 0.7V in order to address all low-voltage power needs.

The MIC22950 features a full range of sequencing and tracking options. The EN/DLY and the DELAY pins, combined with the POR/PG pin, allow multiple outputs to be sequenced in several ways during turn-on and turn-off by using EN pin. The RC (Ramp Control™) pin allows the device to be connected to any another device in the MIC22x00 family of products, to keep the output voltages within a certain delta V during start-up.

The MIC22950 is available in a 32-pin 5mm x 5mm MLF® with a junction operating range from –40°C to +125°C.

Datasheet and supporting documentation can be found on Micrel's web site at: www.micrel.com.

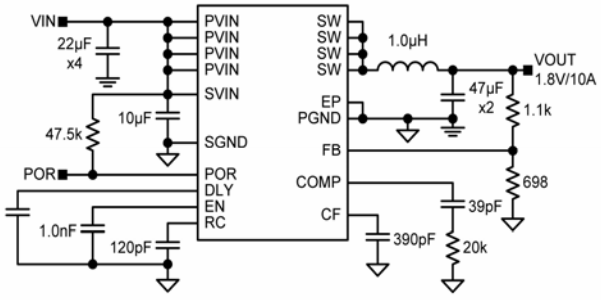
Features

- 2.6V to 5.5V supply voltage
- Fully-integrated MOSFET switches
- Adjustable output voltage option down to 0.7V
- Output load current up to 10A
- Full sequencing and tracking capability
- Power-On Reset
- Efficiency >95% across a broad load range
- Operating frequency programmable: 400kHz to 2MHz
- Ultra-fast transient response
- 100% maximum duty cycle
- Micropower shutdown
- Thermal-shutdown and current-limit protection
- Available in a 32-pin 5mm x 5mm MLF® package
- –40°C to +125°C junction temperature range

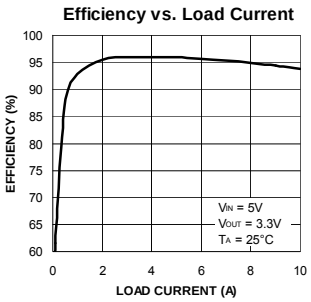
Applications

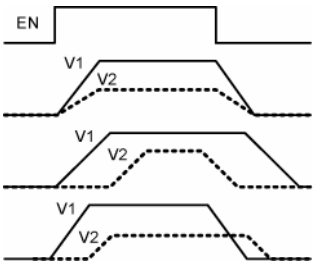
- High-power density point-of-load conversion
- Base stations, Servers and Routers
- Blu-ray players, DVD Recorders
- Computer Peripherals
- FPGAs, DSP, and low-voltage ASIC power

Typical Application



MIC22950 10A Synchronous DC-DC Converter





Sequencing and Tracking

Ramp Control is a trademark of Micrel, Inc

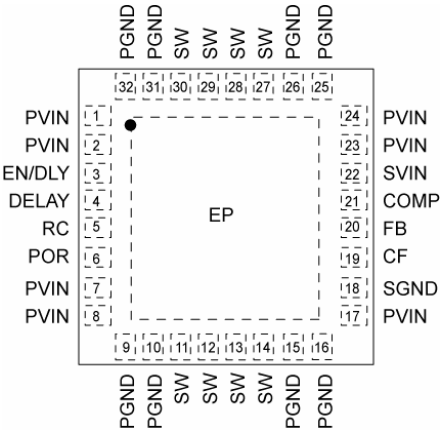
MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

Ordering Information

Part Number	Nominal Output Voltage	Temperature Range	Package	Lead Finish
MIC22950YML	Adjustable	–40° to +125°C	32-Pin 5mm x 5mm MLF®	Lead Free

Note:
MLF® is a GREEN RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



32-Pin 5mm x 5mm MLF® (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1,2,7,8,17,23,24	PVIN	Power Supply Voltage (Input): Requires bypass capacitor to PGND.
3	EN/DLY	Enable/ delay (Input): This pin has a 1.24V band gap reference. When the pin is pulled higher that this the part will start up. Below this voltage the device is in its low quiescent current mode. The pin has a 1µA current source pull-up to VIN. By adding a capacitor to this pin, a delay may be generated. The enable function will not operate with an input voltage lower than UVLO.
4	DELAY	Delay (Input): A capacitor sets the internal delay timer. Timer delays power-on reset (POR) at power-up and power-down.
5	RC	Ramp Control (Input): Capacitor-to-ground from this pin determines slew rate of output voltage during start-up. This can be used for tracking capability as well as soft start. RC pin cannot be left floating. Use a minimum capacitor value of 120pF or larger.
6	POR/PG	Power-On-Reset (Output): Open-drain output device indicates when the output is out of regulation and is active after the delay set by the DELAY pin.
9,10,15,16,25,26, 31,32	PGND	Power Ground (Power): Power Ground.
11,12,13,14,27, 28,29,30	SW	Switch (Output): Internal power MOSFET output switches.
18	SGND	Signal Ground (Signal): Signal Ground.
19	CF	Frequency Set (Input): Adjustable Frequency with external capacitor.
20	FB	Feedback (Input): Input to the error amplifier, connect to the external resistor divider network to set the output voltage.
21	COMP	Compensation pin (Input): Place a RC-to-SGND to compensate the device, see applications section.
22	SVIN	Signal Power Supply Voltage (Input): Requires bypass capacitor-to-SGND.
EP	GND	Center Tab (Power): Must make a full connection to a GND plane for full output power to be realized.

Absolute Maximum Ratings[1]

Supply Voltage (PVIN, SVIN)..... –0.3V to +6V
Output Switch Voltage (V_{SW})..... –0.3V to +6V
Output Switch Current (I_{SW}) .....Internally Limited
Logic Input Voltage (V_{EN}, V_{POR}, V_{DLY}).....–0.3V to V_{IN}
Control Voltage (CF, RC, COMP, FB) .....–0.3V to V_{IN}
Lead Temperature (soldering, 10sec.).....260°C
Storage Temperature (Ts).....–65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN})..... 2.6V to 5.5V
Junction Temperature (T_J) .....–40°C ≤ T_J ≤ +125°C
Thermal Resistance
MLF® (θ_{JC}).....11°C/W
MLF® (θ_{JA}).....30°C/W

Electrical Characteristics[3]

T_A = 25°C with V_{IN} = V_{EN} = 3.3V; V_{OUT} = 1.8V, unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

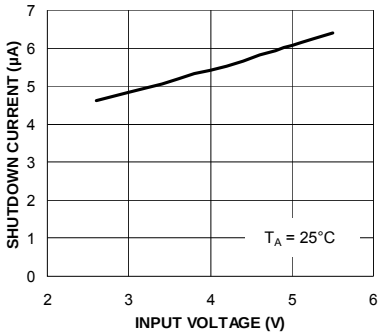
Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		**2.6**		**5.5**	V
V_{IN} Turn On Voltage Threshold	(V_{IN} Rising)	**2.35**	2.5	**2.6**	V
UVLO Hysteresis			260		mV
Quiescent Current (PWM Mode)	V_{EN} = >1.34V; V_{FB} = 1.1*V_{NOM} (not switching)		1	**2**	mA
Shutdown Current	V_{EN} = 0V		5	**10**	µA
[Adjustable] Feedback Voltage	± 2% (over temperature)	**0.686**		**0.714**	V
FB pin input current			1		nA
Current Limit	V_{FB} = 0.9*V_{NOM}	**10**	16.5	**21**	A
Output Voltage Line Regulation	V_{OUT} 1.8V; V_{IN} = 2.6 to 5.5V, I_{LOAD} = 100mA		0.2		%
Output Voltage Load Regulation	100mA < I_{LOAD} < 10A, Vin = 3.3V		0.2		%
Maximum Duty Cycle	V_{FB} ≤ 0.5V	100			%
Switch ON-Resistance PFET Switch ON-Resistance NFET	I_{SW} = 1000mA V_{FB}=0.5V I_{SW} = -1000mA V_{FB}=0.9V		11 8		mΩ mΩ
Oscillator Frequency	CF = 390pF	**325**	510	**610**	kHz
EN/DLY threshold voltage		**1.14**	1.24	**1.34**	V
EN/DLY source current	V_{IN} = 2.6 to V_{IN} = 5.5V	**0.6**	1	**1.8**	µA
RC Pin I_{RAMP}	Ramp Control Current	**0.6**	1	**1.8**	µA
Power On Reset $I_{PG(LEAK)}$	V_{PORH} = 5.5V; POR = High			1 **2**	µA µA
Power On Reset $V_{PG(LO)}$	Output Logic-Low Voltage (undervoltage condition), I_{POR} = 5mA		77		mV
	Hysteresis		2		%
Power On Reset V_{PG}	Threshold, % of V_{OUT} below nominal	**7.5**	10	**12.5**	%
Over-temperature Shutdown			160		°C
Over-temperature Shutdown Hysteresis			20		°C

Notes:

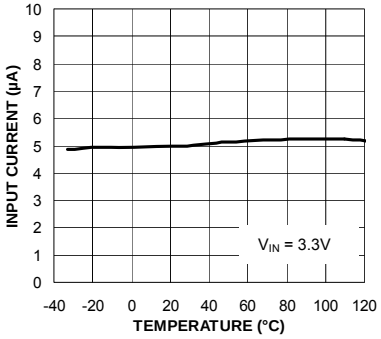
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Specification for packaged product only.

Typical Characteristics

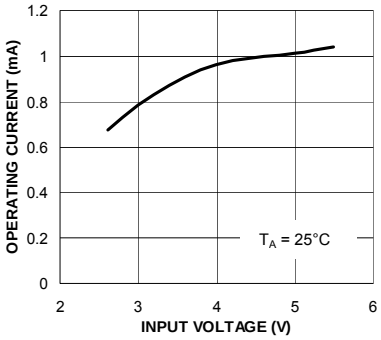
Shutdown Current vs. Input Voltage



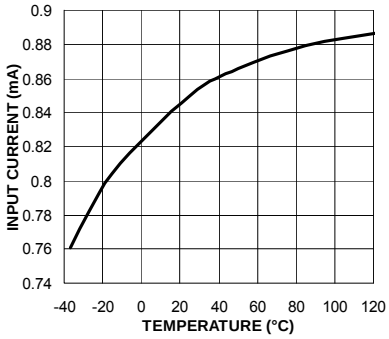
Shutdown Current vs. Temperature



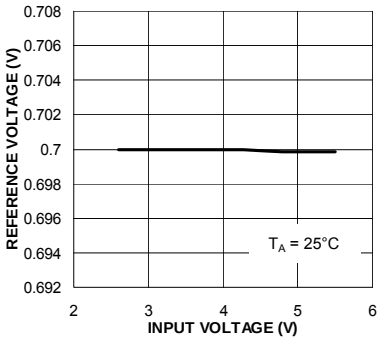
Operating Current (no SW) vs. Input Voltage



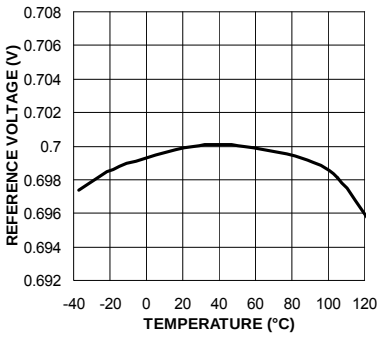
Input Current (no SW) vs. Temperature



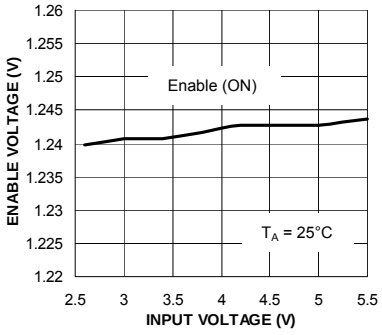
Reference Voltage vs. Input Voltage



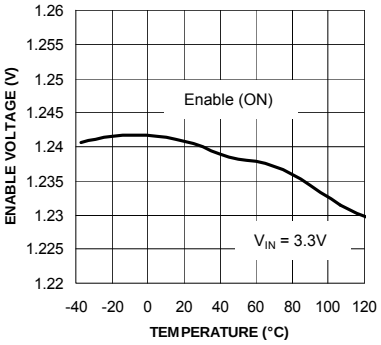
Reference Voltage vs. Temperature



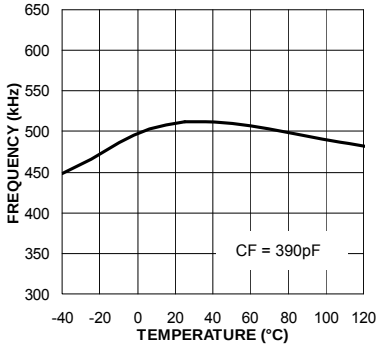
Enable Threshold vs. Input Voltage



Enable Threshold vs. Temperature

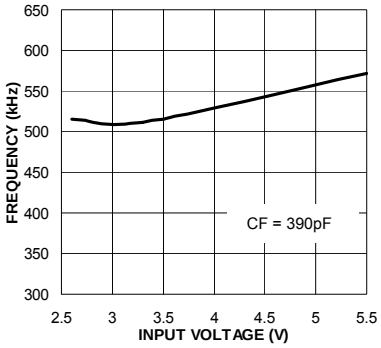


Switching Frequency vs. Temperature

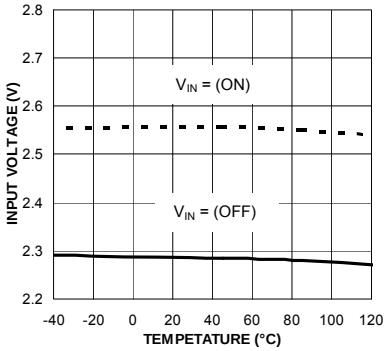


Typical Characteristics (Continued)

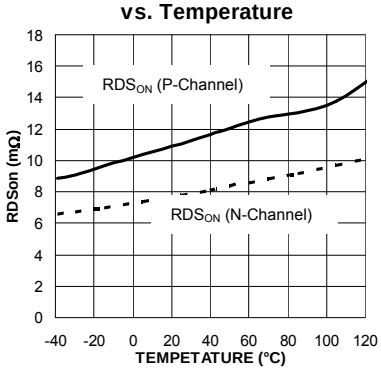
Switching Frequency vs. Input Voltage



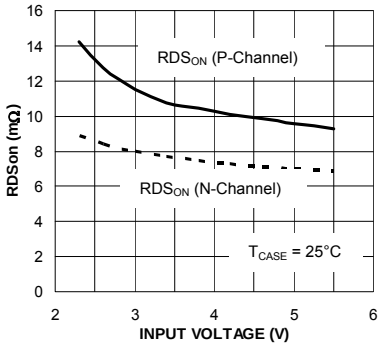
Input Voltage UVLO vs. Temperature



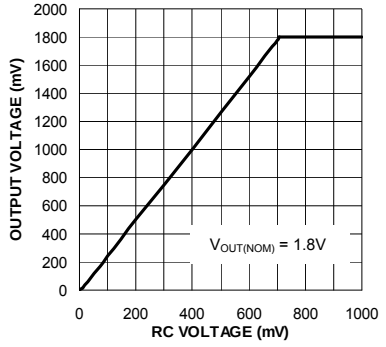
RDSon vs. Temperature



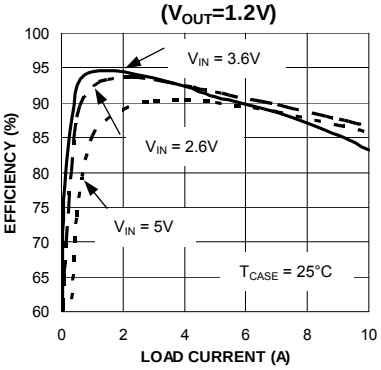
RDSon vs. Input Voltage



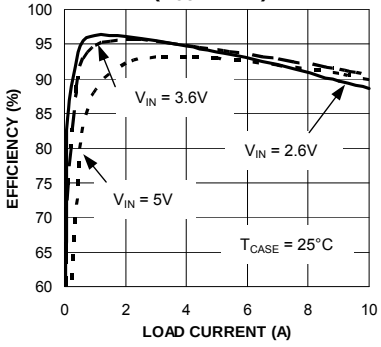
Output Voltage vs. RC Voltage



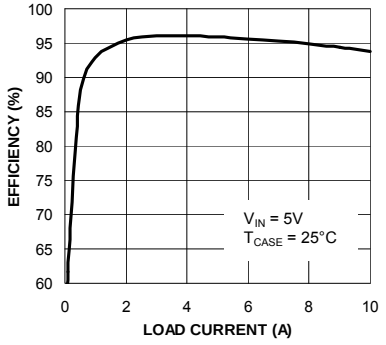
Efficiency vs. Load Current (V_{OUT}=1.2V)



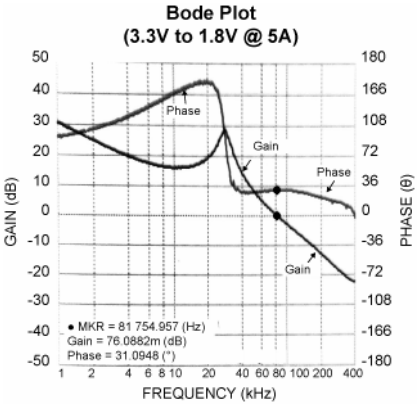
Efficiency vs. Load Current (V_{OUT}=1.8V)

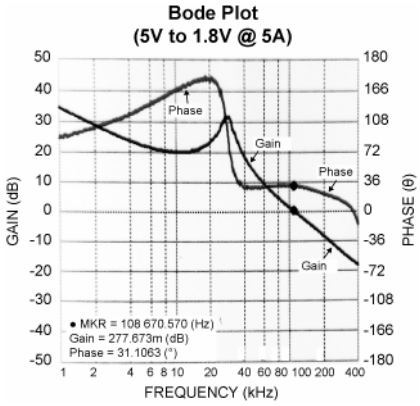


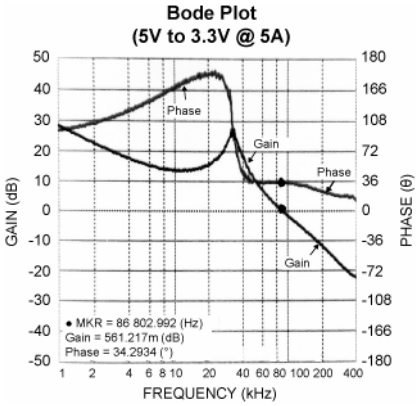
Efficiency vs. Load Current (V_{OUT}=3.3V)



Bode Plots

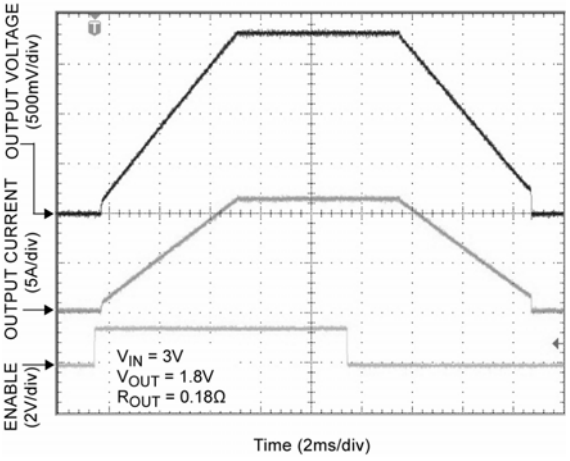

Bode Plot
(3.3V to 1.8V @ 5A)
GAIN (dB)
PHASE (θ)
FREQUENCY (kHz)
Phase
Gain
Phase
Gain
• MKR = 81 754.957 (Hz)
Gain = 76.0882m (dB)
Phase = 31.0948 (°)


Bode Plot
(5V to 1.8V @ 5A)
GAIN (dB)
PHASE (θ)
FREQUENCY (kHz)
Phase
Gain
Phase
Gain
• MKR = 108 670.570 (Hz)
Gain = 277.673m (dB)
Phase = 31.1063 (°)

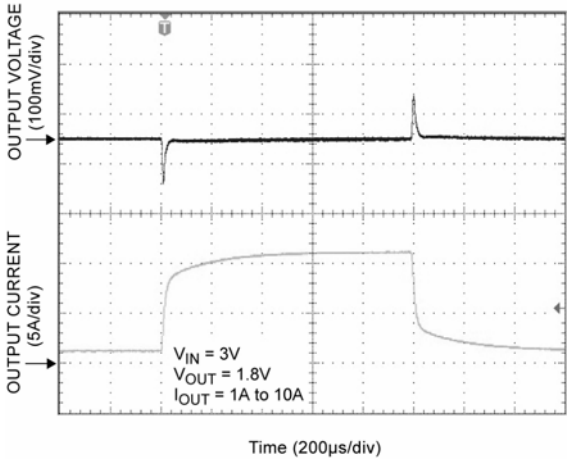

Bode Plot
(5V to 3.3V @ 5A)
GAIN (dB)
PHASE (θ)
FREQUENCY (kHz)
Phase
Gain
Phase
Gain
• MKR = 86 802.992 (Hz)
Gain = 561.217m (dB)
Phase = 34.2934 (°)

Functional Characteristics

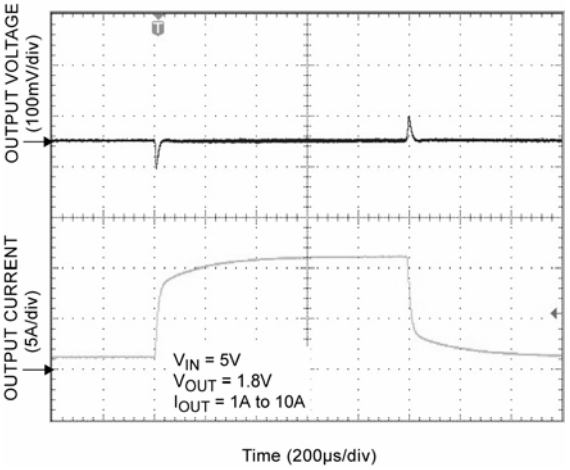
Start-Up/Shutdown (C_{RC} - 10nF)



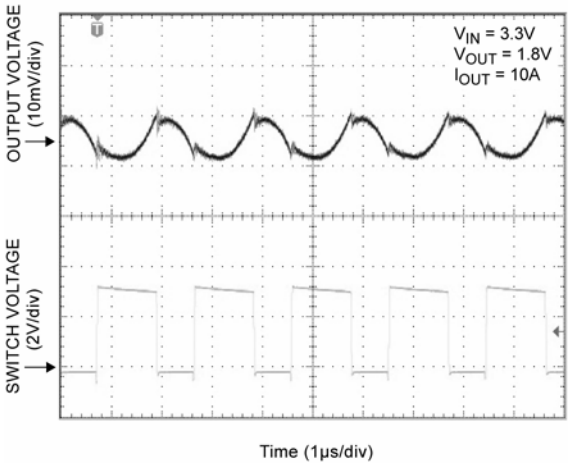
Transient Response



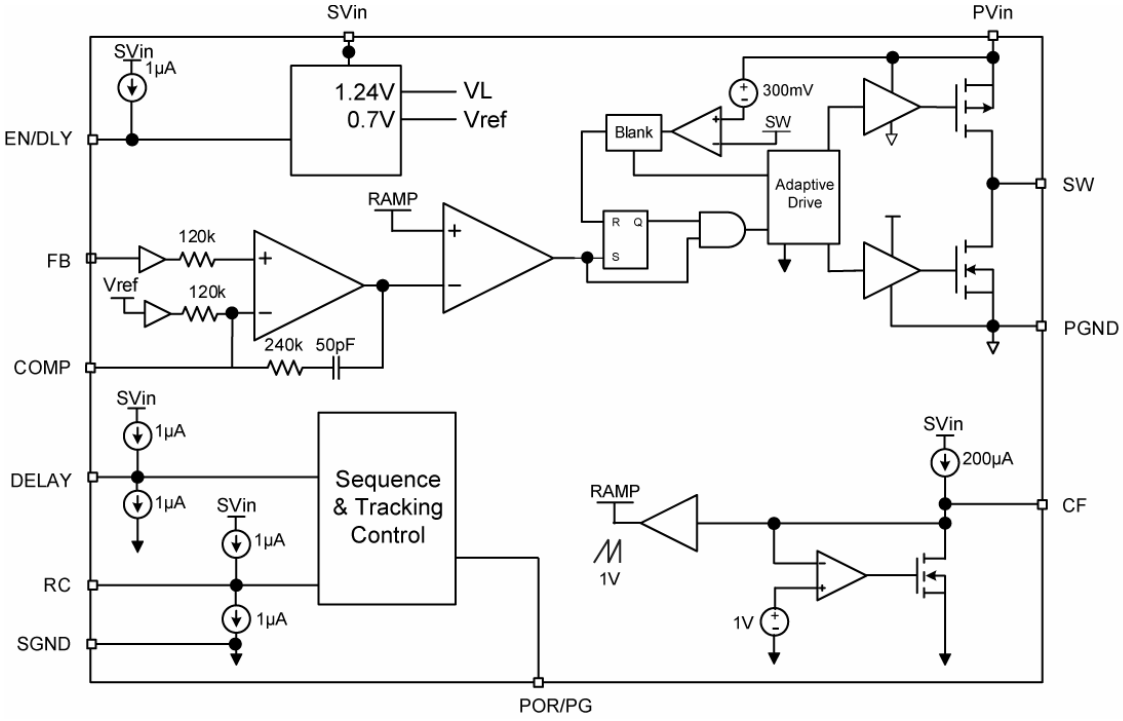
Transient Response



Operating Waveforms



Functional Block Diagram



Functional Description

PVIN, SVIN

PVIN is the input supply to the internal 11mΩ P-Channel Power MOSFET. This should be connected externally to the SVIN pin. The supply voltage range is from 2.6V to 5.5V. A 22µF ceramic is recommended for bypassing each PVIN supply and 10µF capacitor for SVIN pin.

EN/DLY

This pin is internally fed with a 1µA current source to SVIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V.

RC

RC pin allows the slew rate of the output voltage to be programmed by the addition of a capacitor from RC pin to ground. RC pin is internally fed with a 1µA current source and V_{OUT} slew rate is proportional to the capacitor and the 1µA source. The RC pin cannot be left floating. Use a minimum capacitor value of 120pF or longer.

DELAY

Adding a capacitor to this pin allows the delay of the POR signal.

When V_{OUT} reaches 90% of its nominal voltage, the DELAY pin current source (1µA) starts to charge the external capacitor. At 1.24V, POR is asserted high.

COMP

The MIC22950 uses an internal-compensation network containing a fixed-frequency zero (phase-lead response) and pole (phase-lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor will add the necessary pole and zero for voltage-mode loop stability using low-value, low-ESR ceramic capacitors.

FB

The FB pin provides the control path to control the output. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. Refer to the feedback section in *Applications Information* of this data sheet for more detail.

POR/PG

This is an open drain output. A 47k resistor can be used for a pull-up to this pin. POR/PG is asserted high when output voltage reaches 90% of nominal set voltage and after the delay set by C_{DELAY}. POR/PG is asserted low without delay when enable is set low or when the output goes below the −10% threshold. For a power-good (PG) function, the delay can be set to a minimum. This can be done by removing the DELAY pin capacitor.

CF

This pin allows the setting of the switching frequency. A 200µA source current charges the capacitor on this pin up to a voltage of 1V. At this point, CF pin capacitor is then discharged with an internal N-Channel MOSFET marking the end of the switching period. The capacitor should be connected very close to the IC and grounded directly to the SGND pin.

SW

This is the connection to the source of the internal P-channel MOSFET and drain of the N-Channel MOSFET. This is a high-frequency, high-power connection; therefore, traces should be kept as short and as wide as practical.

SGND

Internal signal ground for all low-power sections.

PGND

Internal ground connection to the source of the internal N-Channel MOSFETs.

Application Information

The MIC22950 is a 10A synchronous stepdown regulator IC with a programmable 400kHz to 2MHz switching frequency. The control loop is a voltage-mode PWM control scheme. Other features include tracking and sequencing control for controlling multiple output power systems with POR/PG output.

Component Selection

Input Capacitor

A minimum 22µF ceramic capacitor (preferable) is recommended on each of the PVIN pins for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Do not use Y5V dielectrics, aside from losing most of their capacitance over temperature and voltage, they also become resistive at high frequencies. This reduces their ability to localize high-frequency noise.

Output Capacitor

The MIC22950 was designed specifically for the use of ceramic output capacitors. It is designed to work with 100µF output capacitor. This output capacitor can be increased to improve transient performance. Since the MIC22950 is voltage mode control loop, it relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Do not use Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22950.

Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22950 is designed for use with a 0.39µH to 2.2µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When the saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple can add as much as 2A to the output current level. The RMS rating should be chosen to be equal or greater than the current limit of the MIC22950 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC. For this reason, the heat of the inductor is somewhat coupled to the IC, which offers some level of protection if the inductor gets too hot. It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DC resistance is also important. While DCR is typically inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the *Efficiency Considerations* section for a more detailed description.

EN/DLY Capacitor

EN/DLY sources 1µA out of the IC to allow a start-up delay to be implemented. The delay time is simply the time it takes 1µA to charge $C_{EN/DLY}$ to 1.24V. Therefore:

$$T_{DLY} = \frac{1.24 \times C_{EN/DLY}}{1 \times 10^{-6}}$$

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed:

$$\text{Efficiency \%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal-design considerations and it reduces consumption of current for battery-powered applications. Reduced current draw from a battery increases the devices operating time, critical in hand held devices.

There are mainly two loss terms in switching converters: Static losses and switching losses. Static losses are simply the power losses due to V.I or I^2R. For example, power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET $RDS_{(ON)}$ multiplied by the RMS Switch Current squared (I_{SW}^2). During the off cycle, the low-side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor's DCR and capacitor's ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to

drive the gates on and off at a constant 400kHz to 2MHz frequency and the switching transitions make up the switching losses.

Figure 2 shows an efficiency curve. The non-shaded portion, from 0A to 1A, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

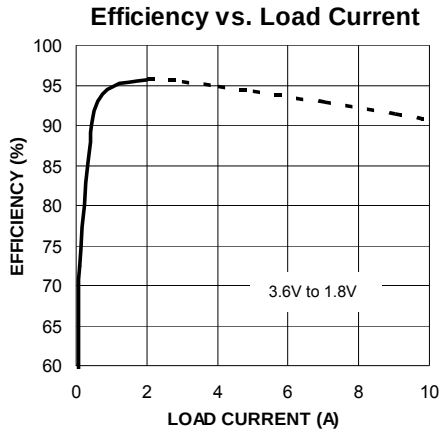


Figure 1. Efficiency Curve

The dashed region, 1A to 6A, efficiency loss is dominated by MOSFET $RDS_{(ON)}$ and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, thus reducing the internal $RDS_{(ON)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1-\left(\frac{V_{OUT}\cdot I_{OUT}}{(V_{OUT}\cdot I_{OUT})+L_{PD}}\right)\right]\times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value maybe desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimize losses. The following graph, in Figure 2, illustrates the effects of inductance value at light load.

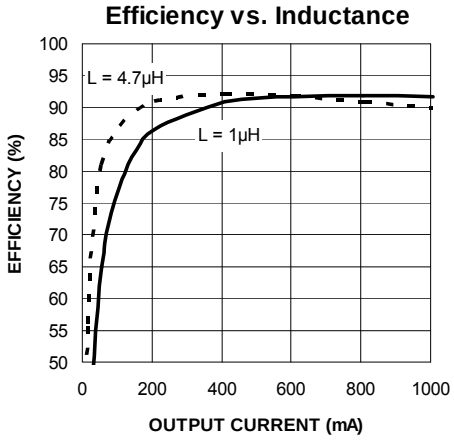


Figure 2. Efficiency vs. Inductance

Compensation

The MIC22950 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal ramp signal which is derived from the CF current charging an external capacitor. This ramp is compared to the output of the error amplifier to modulate the pulse width of the switch node, maintaining output voltage regulation. With a typical gain bandwidth of 100 – 200kHz, the MIC22950 is capable of fast transient responses.

The MIC22950 is designed to be stable with a typical application using a 1µH inductor and a 100µF ceramic (X5R) output capacitor. These values can be varied dependant upon the tradeoff between size, cost and efficiency, keeping the LC natural frequency ($\frac{1}{2\times\pi\times\sqrt{L\times C}}$) ideally less than $F_{SW}/17$ to ensure stability can be achieved. The minimum recommended inductor value is 0.39µH and minimum recommended output capacitor value is 10µF.

The tradeoff between changing these values is that with a larger inductor, there is a reduced peak-to-peak current which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 1k resistor) are shown below:

C→ / L↓	10-22µF	47-100µF	120-470µF
0.39 - 0.47µH	NA	10*-20pF†	25-47pF
0.56 – 1.0µH	10‡-15pF*	22†-39pF	56-100pF
1.2 – 2.2µH	10-22pF	22-68pF	NA
† V_{OUT} > 1V; * V_{OUT} > 1.4V; ‡ V_{OUT} > 1.8V			

Feedback

The MIC22950 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. To calculate the resistor divider network for the desired output is as follows:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

Where V_{REF} is 0.7V and V_{OUT} is the desired output voltage. A 10kΩ or lower resistor value from the output to the feedback is recommended since large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small decoupling capacitor (22pF – 100pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

PWM Operation

The MIC22950 is a voltage-mode, pulse-width modulation (PWM) controller. By controlling the ratio of on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22950 will run at 100% duty cycle.

The MIC22950 provides switching frequency at 400kHz to 2MHz with synchronous internal MOSFETs. The internal MOSFETs include a high-side 11mΩ P-Channel MOSFET from the input supply to the switch pin and an 8mΩ N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, a freewheeling Schottky diode from the switch node-to-ground is not required.

PWM control provides fixed-frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

CF Pin

Each switching cycle begins immediately following the discharge of the CF pin capacitor. From this point, a current source of 200µA flows from CF pin into the external capacitor connected to the CF pin. This creates a linear voltage ramp rising towards a threshold voltage of 1V. When this capacitor reaches the 1V threshold, it triggers the end of the switching cycle by discharging CF pin to ground via an internal N-Channel; at which point, the next cycle begins. The actual switching frequency can be approximated by using the following equation which accounts for internal delays and capacitance:

$$F_{SW} = \frac{1}{T_{DELAY} + \left(V_{RAMP} \cdot \frac{(C_{CF} + C_{PIN})}{I_{CF}}\right)}$$

Where:

F_{SW} = Switching Frequency

T_{DELAY} = CF pin Discharge time ~ 85ns

V_{RAMP} = Voltage ramp amplitude ~ 0.9V

C_{CF} = External CF capacitor = 68pF to 560pF

C_{PIN} = Internal Pin capacitance ~ 15pF

I_{CF} = CF current source = 200µA

Alternatively, the Figure 3 can be used as a visual guide:

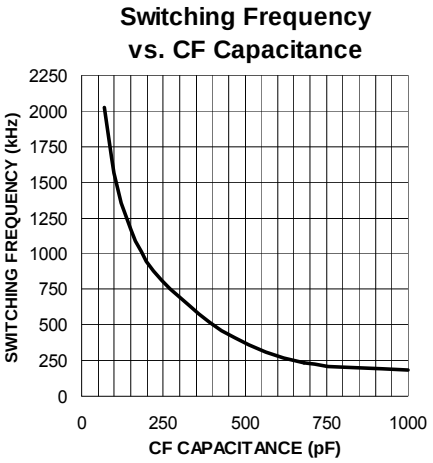


Figure 3. Switching Frequency vs. CF Capacitance

This pin should not be over-ridden using an external clock because the trigger pulses generated when the CF pin reaches 1V are utilized internally.

Sequencing and Tracking

The MIC22950 provides additional pins to provide up/down sequencing and tracking capability for connecting multiple voltage regulators together.

EN/DLY Pin

The EN/DLY pin contains a trimmed, 1µA current source which can be used with a capacitor to implement a fixed desired delay in some sequenced power systems. The threshold level for power on is 1.24V with a hysteresis of 20mV.

DELAY Pin

The DELAY pin also has a 1µA trimmed current source and a 1µA current sink which acts with an external capacitor to delay the operation of the Power On Reset (POR/PG) output. This can be used also in sequencing outputs in a sequenced system, but with the addition of a conditional delay between supplies; allowing a first up, last down power sequence.

After EN pin is driven high, V_{OUT} will start to rise (rate determined by RC pin capacitor). As the FB pin voltage goes above 90% of its nominal set voltage, DELAY pin begins to rise as the 1µA source charges the external capacitor. When the threshold of 1.24V is crossed, POR/PG is asserted high and DELAY continues to charge to a voltage SVIN. When FB falls below 90% of nominal, POR/PG is asserted low immediately.

However, if EN pin is driven low, POR/PG will fall immediately to the low state and DELAY pin will begin to fall as the external capacitor is discharged by the 1µA current sink. When the threshold of (V_{TP} +1.24V)-1.24V is crossed (V_{TP} is internal voltage clamp, $V_{TP} \cong 0.9V$), V_{OUT} will begin to fall at a rate determined by the RC pin capacitor. As the voltage change in both cases is 1.24V, both rising and falling delays are matched at:

$$T_{POR} = \frac{1.24 \times C_{DELAY}}{1 \times 10^{-6}}$$

RC Pin

The RC pin provides a trimmed 1µA current source/sink similar to the DELAY Pin for accurate ramp up (soft start) and ramp down control. This allows the MIC22950 to be used in systems requiring voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

1. Externally driven from a voltage source
2. Externally attached capacitor sets output ramp up/down rate

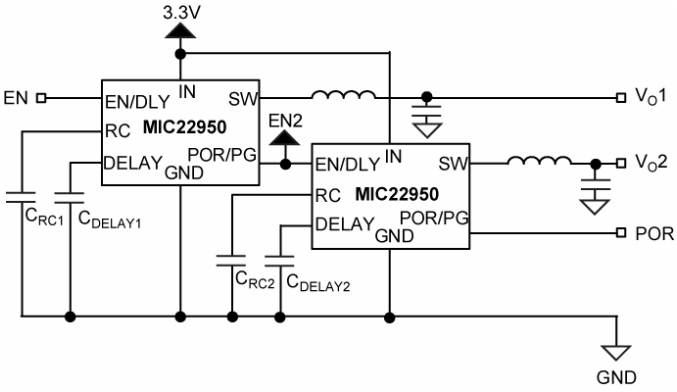
In the first case, driving RC pin with a voltage from 0V to V_{REF} will program the output voltage between 0% and 100% of the nominal set voltage.

In the second case, the external capacitor sets the ramp up and ramp down rate of the output voltage. The rate is given by $T_{RAMP} = \frac{0.7 \times C_{RC}}{1 \times 10^{-6}}$ where T_{RAMP} is the time from 0% to 100% nominal output voltage. RC pin cannot be left floating. Use a minimum capacitor value of 120p for larger.

Tracking and Sequencing Examples

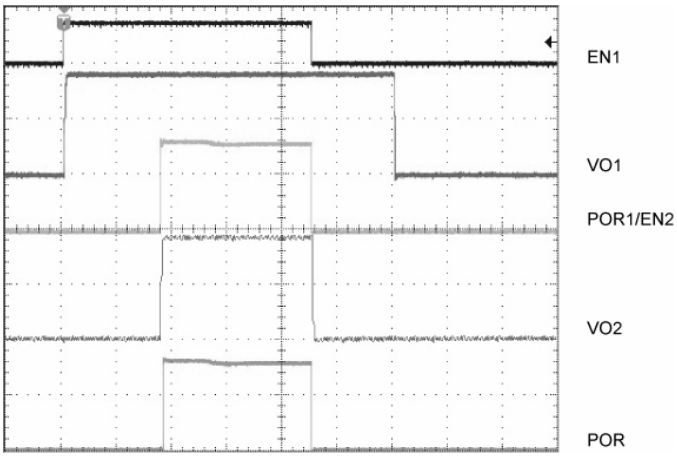
There are four distinct variations which are easily implemented using the MIC22950. The two Sequencing variations are Delayed and windowed. The two tracking variants are ratio Metric and Normal. The following diagrams illustrate methods for connecting two MIC22950's to achieve these requirements.

Sequencing



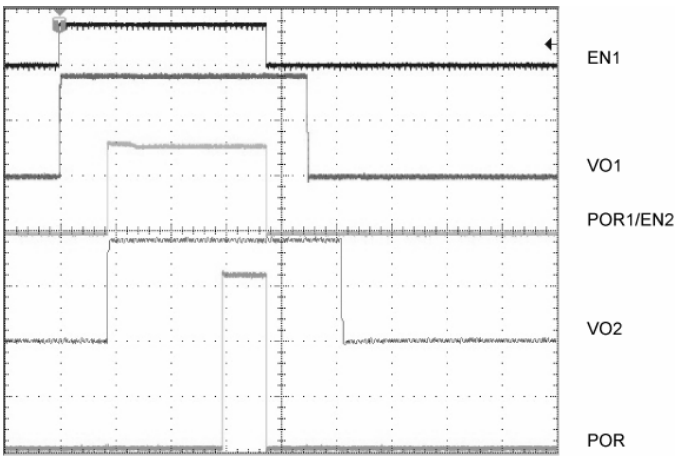
Window Sequencing

$C_{RC1} = C_{RC2} = 0nF, C_{DELAY1} = 3.3nF, C_{DELAY2} = 0nF$

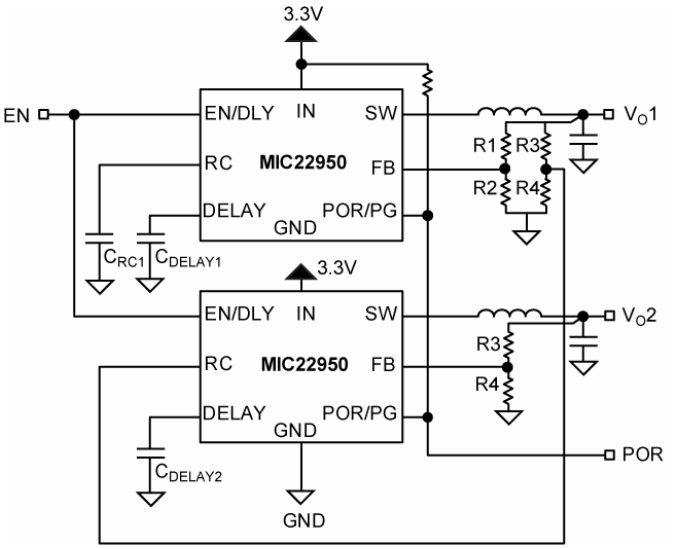


Delayed Sequencing

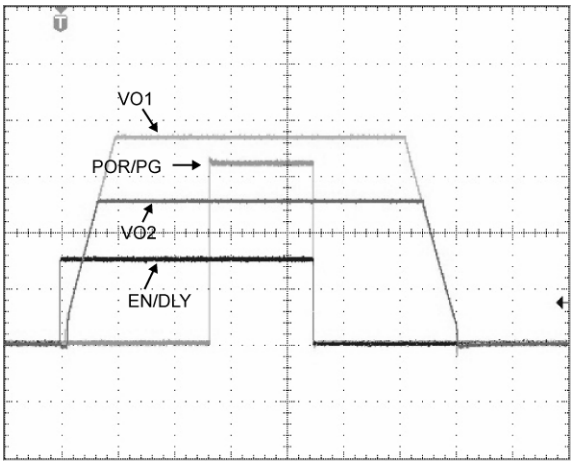
$C_{RC1} = C_{RC2} = 0nF, C_{DELAY1} = 3.3nF, C_{DELAY2} = 6.8nF$



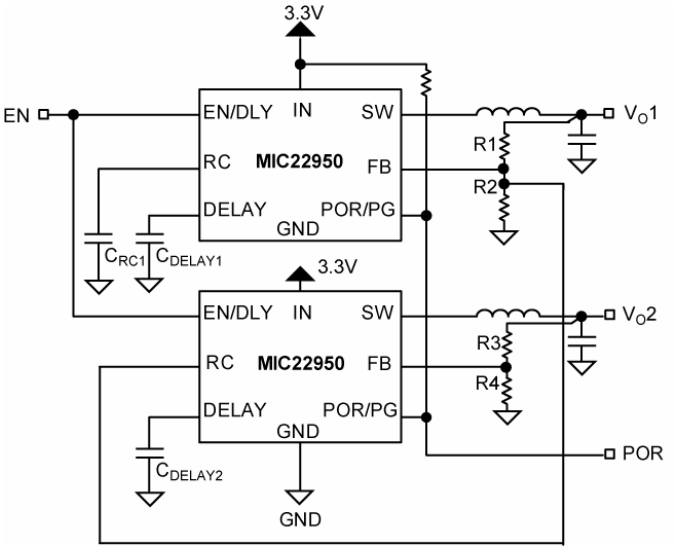
Normal Tracking



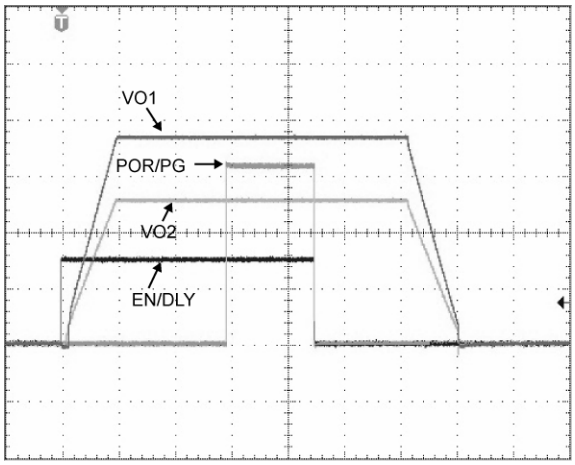
C_{CR1} = 3.3nF, C_{RC2} = 0nF, C_{DELAY1} = C_{DELAY2} = 3.3nF
R1 = 1.1k, R2 = 698, R3 = 505, R4 = 698



Ratio Metric Tracking



C_{CR1} = 3.3nF, C_{RC2} = 0nF, C_{DELAY1} = C_{DELAY2} = 3.3nF
R1 = 1.1k, R2 = 698, R3 = 505, R4 = 698



Current Limit

The MIC22950 is protected against overload in two stages. The first is to limit the current in the P-Channel switch; the second is over- temperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 4 describes the operation of the current-limit circuit. Since the actual RDS_{ON} of the P-Channel MOSFET varies part-to-part, over-temperature and with input voltage, simple I.R voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current which is a directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependant upon the RDS_{ON} value. Current limit is set to nominal value. Variations in the scale factor K between the Power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

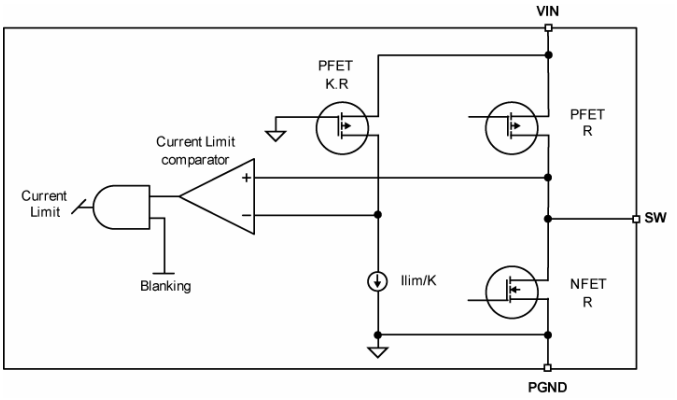


Figure 4. Current Limit Detail

Thermal Considerations

The MIC22950 is packaged in the MLF® 5mm x 5mm, a package that has excellent thermal performance equaling that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePAD) which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

$$T_J = T_A + P_{DISS} \times R\theta_{JA}$$

Where:

P_{DISS} is the power dissipated within the MLF® package and is typically 1.5W at 10A load. This has been calculated for a 1µH inductor and details can be found in Table 1.

$R\theta_{JA}$ is a combination of junction-to-case thermal resistance ($R\theta_{JC}$) and case-to-ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane to ambient. So $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.

T_A is the Operating Ambient temperature.

V_{OUT} @ 10A \ V_{IN}	3	3.5	4	4.5	5
1	1.66	1.67	1.68	1.7	1.73
1.2	1.68	1.69	1.71	1.72	1.74
1.8	1.76	1.76	1.77	1.78	1.8
2.5	1.85	1.84	1.84	1.85	1.86
3.3	-	1.92	1.91	1.91	1.92

Table 1. Power Dissipation (W) for 10A Output

Example

The Evaluation board has two copper planes contributing to an $R\theta_{JA}$ of approximately 25°C/W. The worst case $R\theta_{JC}$ of the MLF® is 11°C/W. If we look at a typical application of 3.6V to 1.8V @ 10A, the estimated Power dissipation in the MLF® package taken from Table 1 will be 1.76W:

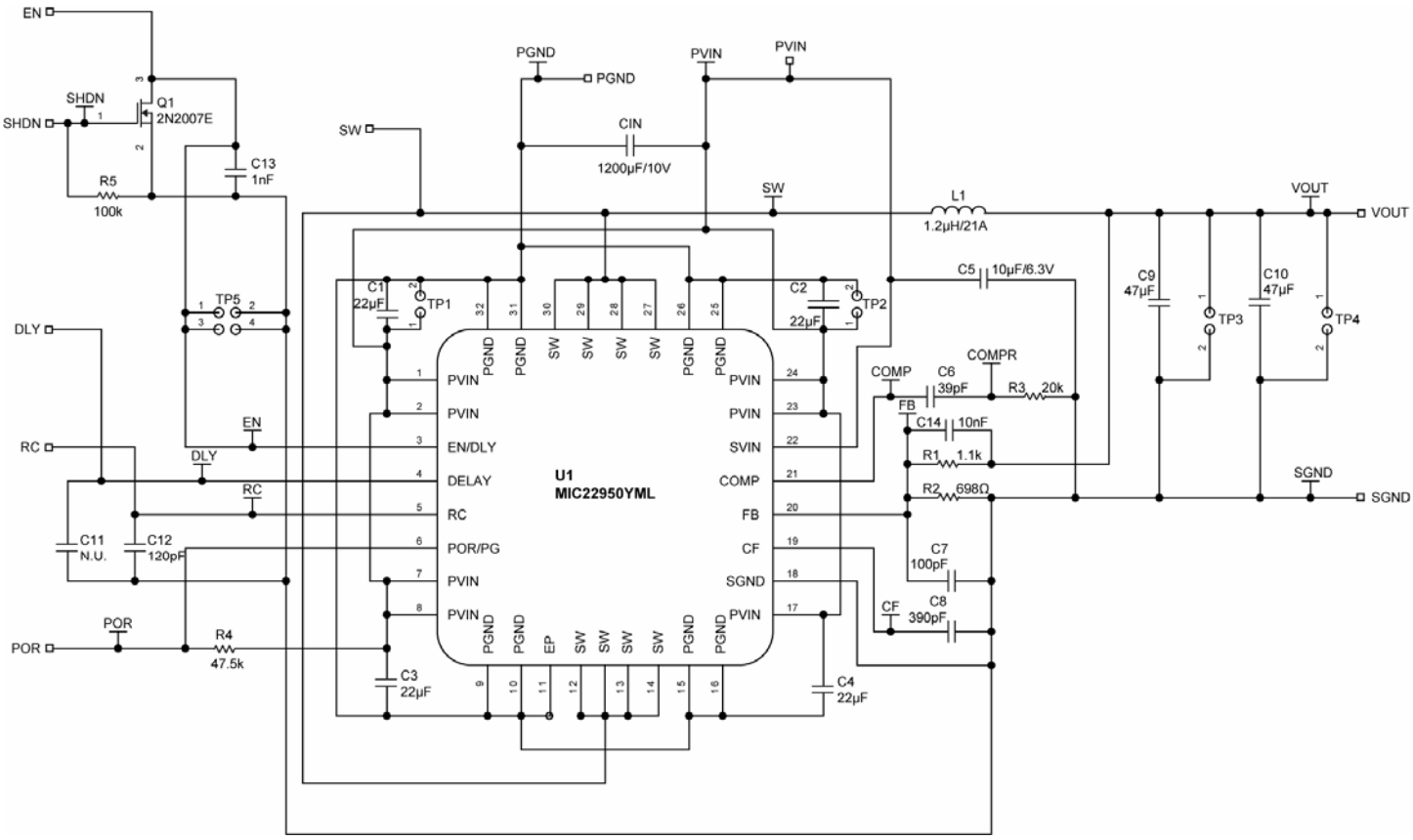
$$R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$$
$$R\theta_{JA} = 11 + 25 = 36^oC/W$$

To calculate the junction temperature for a 50°C ambient:

$$T_J = T_A + P_{DISS}. R\theta_{JA}$$
$$T_J = 50 + (1.76 \times 36)$$
$$\underline{T_J = 113^oC}$$

This is below our maximum of 125°C.

MIC22950 Schematic



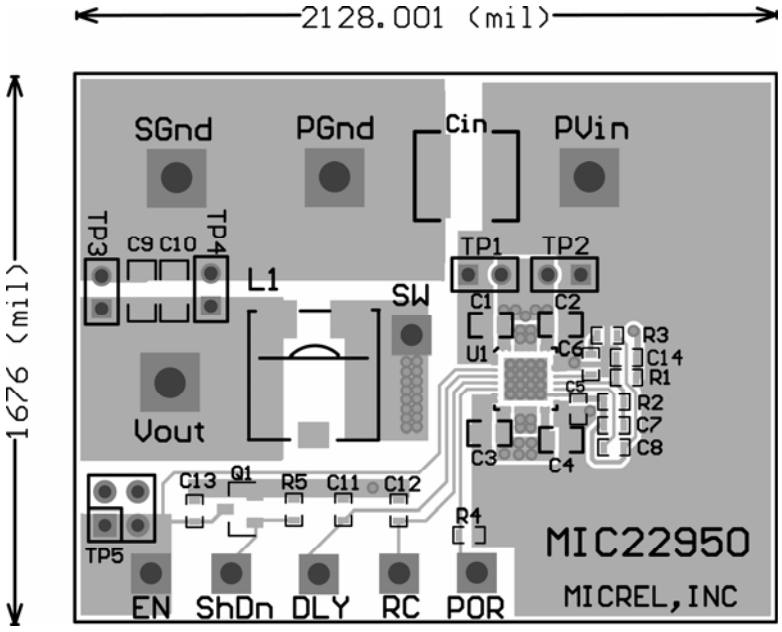
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4	GRM21BR60J226ME39L	muRata[1]	Capacitor, 22µF, 6.3V, X5R, 0805	4
	C2012X5R0J226K	TDK[2]		
	08056D226MAT2A	AVX[3]		
C5	GRM188R60J106ME47D	muRata	Capacitor, 10µF, 6.3V, X5R 0603	1
	C1608X5R0J106K	TDK		
	06036D106MAT2A	AVX		
C6	VJ0603Y390KXXMB	Vitramon[4]	Capacitor, 39pF, 25V, X7R, 0603	1
	06033A390FAT2A	AVX		
	C1608C0G1H390J	TDK		
C7	VJ0603Y101KXAAT	Vitramon	Ceramic Capacitor, 100pF, 50V, 0603	1
	06025A101KAT2A	AVX		
	C1608C0G1H101J	TDK		
C8	VJ0603Y391KXAAT	Vitramon	Ceramic Capacitor, 390pF, 50V, 0603	1
	06035A391JAT2A	AVX		
	C1608C0G1H391J	TDK		
C9, C10	GRM31CR60J476ME19L	muRata	Capacitor, 47µF, 6.3V, 1206	2
	C3216X5R0J476M	TDK		
	12066D476MAT2A	AVX		
C11				
C13	VJ0603Y102KXXMB	Vitramon	Ceramic Capacitor, 1nf, 50V, 0603	2
C14	VJ0603Y103KXXMB	Vitramon	Ceramic Capacitor, 10nf, 50V, 0603	1
C12	06035A121JAT2A	AVX	Capacitor, 120pF, 50V, COG, 0603	
	C1608COG1H121J	TDK		
	GRM1885C1H121JA01D	muRata		
CIN	EEE-FPA122UAP	Panasonic[5]	1200uF, 10V, 10x10.2-Case	1
L1	CDEP105ME-1R2MC	Sumida[6]	1.2µH, 21A , Inductor	1
R1	CRCW06031101FRT1	Vishay Dale[4]	Resistor, 1.1k, 1%, 0603	1
R2	CRCW0603698RFRT1	Vishay Dale	Resistor, 698Ω, 1%, 0603	1
R3	CRCW06032002FRT1	Vishay Dale	Resistor, 20k, 1%, 0603	1
R4	CRCW06034752FRT1	Vishay Dale	Resistor, 47.5k 1%, 0603	1
R5	CRCW06031003FRT1	Vishay Dale	Resistor, 100k 1%, 0603	1
Q1	2N7002E(SOT-23)	Vishay Corp	Signal MOSFET-SOT-236	1
	CMDPM7002A	Central Semiconductor[7]		
U1	**MIC22950YML**	**Micrel[8]**	**10A Integrated Switch Synchronous Buck Regulator with Frequency Programmable to 2MHz**	**1**

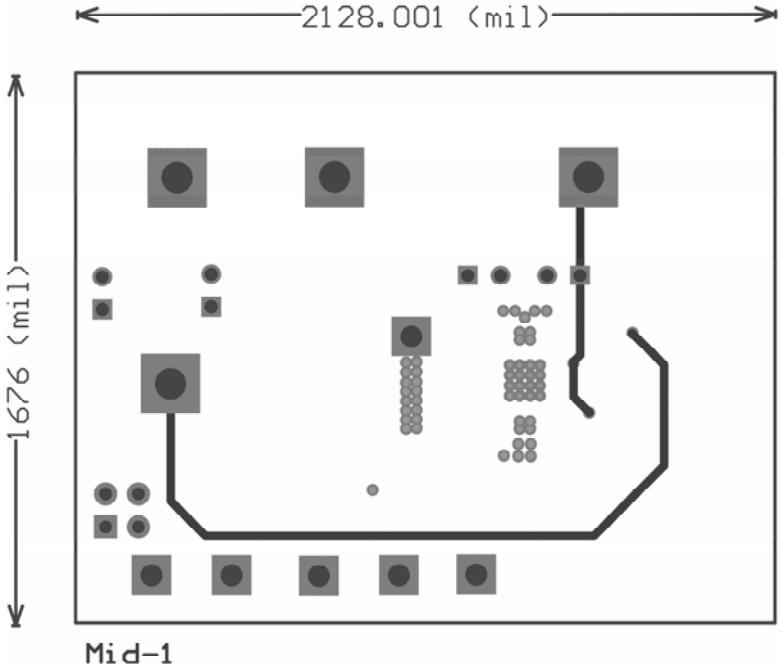
Notes:

1. muRata: www.murata.com
2. TDK: www.tdk.com
3. AVX: www.avx.com
4. Vishay: www.vishay.com
5. Panasonic: www.panasonic.com
6. Sumida: www.sumida.com
7. Central Semiconductor: www.centralsemi.com
8. **Micrel, Inc.: www.micrel.com**

PCB Layout Recommendation

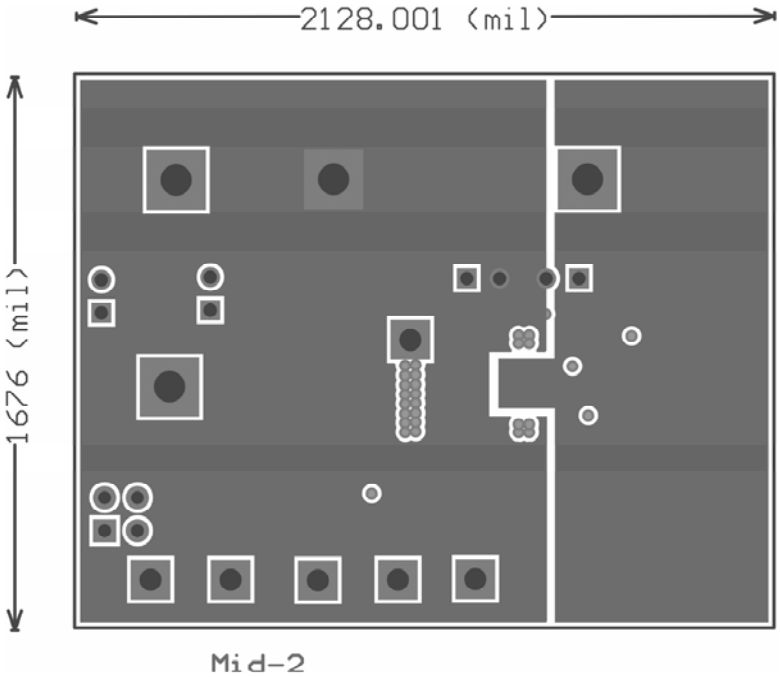


Top Assembly

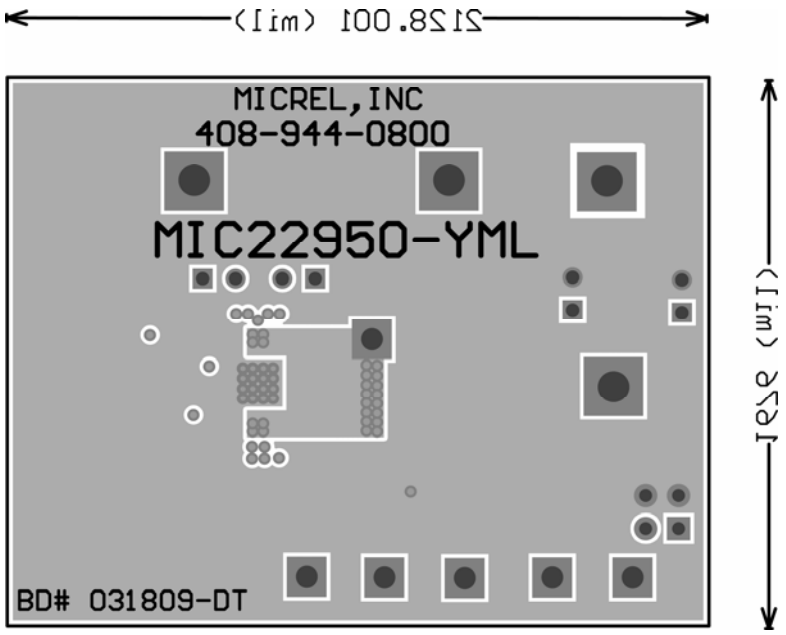


Middle Layer 1

PCB Layout Recommendation (Continued)

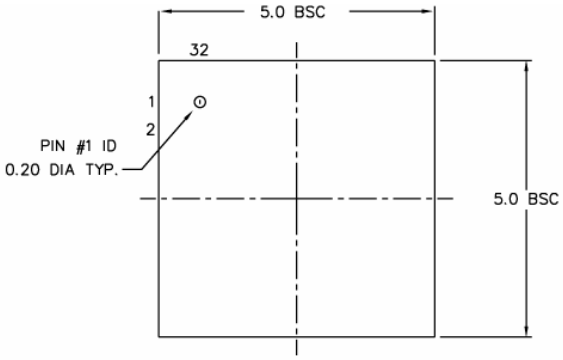


Middle Layer 2

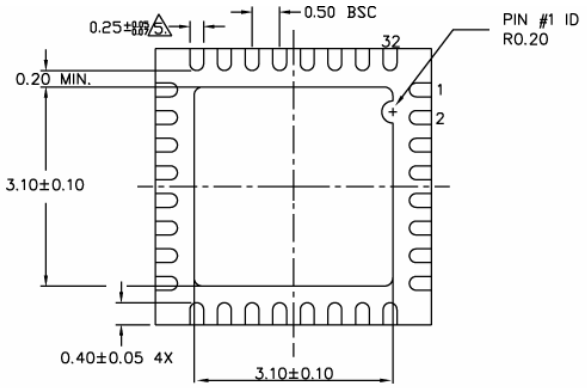


Top Layer

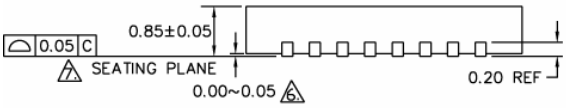
Package Information



TOP VIEW



BOTTOM VIEW

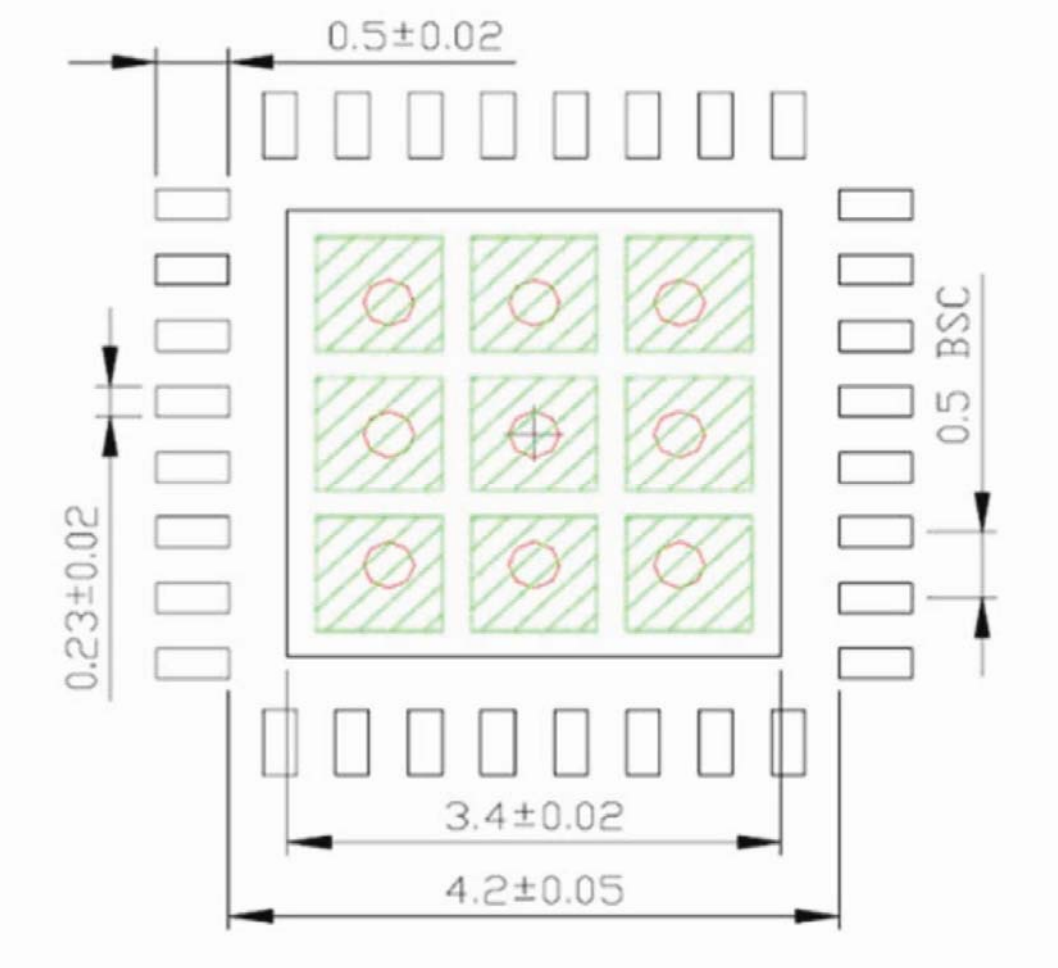


SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin 5mm x 5mm MLF® (ML)

Recommended Land Pattern for 32-Pin 5mm x 5mm MLF®



Red circle indicates Thermal Via. Size should be 300 – 350mm in diameter, 1.00mm pitch, and it should be connected to GND plane for maximum thermal performance.

Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Size should be 0.87 x 0.87mm in size, 1.07mm pitch.

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TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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- Shortage Management
- Alternative Solution
- Excess Inventory Management