



**THE DATASHEET OF  
2SK1399-T2B-A**







These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)</sup>

|                                    |                           |                        |
|------------------------------------|---------------------------|------------------------|
| Supply Voltage                     |                           | -0.5V to 3.6V          |
| Input Voltage (all inputs)         |                           | -0.3V to $V_{CC}+0.3V$ |
| Storage Temperature Range          |                           | -65°C to +150°C        |
| Junction Temperature               |                           | +150°C                 |
| Lead Temperature (Soldering 4 Sec) |                           | +260°C                 |
| Package Thermal Resistance         | $\theta_{JA}$ 16-pin SOIC | +115°C/W               |
|                                    | $\theta_{JC}$ 16-pin SOIC | +105°C/W               |
| ESD Rating (HBM)                   |                           | 8 kV                   |
| ESD Rating (MM)                    |                           | 250V                   |

- (1) Absolute Maximum Ratings are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of [Electrical Characteristics](#) specifies acceptable device operating conditions.

### Recommended Operating Conditions

|   |                |
|---|----------------|
| Supply Voltage ( $V_{CC} - V_{EE}$ )            | 3.3V $\pm 5\%$ |
| Input Coupling Capacitance                      | 1.0 $\mu F$    |
| AEC Capacitor (Connected between AEC+ and AEC-) | 1.0 $\mu F$    |
| Operating Free Air Temperature ( $T_A$ )        | 0°C to +85°C   |

### DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)(2)</sup>.

| Symbol      | Parameter                                 | Conditions                         | Reference             | Min | Typ                  | Max | Units             |
|-------------|---|------------------------------------|-----------------------|-----|----------------------|-----|-------------------|
| $V_{CMIN}$  | Input Common Mode Voltage                 |                                    | SDI, $\overline{SDI}$ |     | 1.9                  |     | V                 |
| $V_{SDI}$   | Input Voltage Swing                       | At LMH0034 input <sup>(3)(4)</sup> |                       | 720 | 800                  | 950 | mV <sub>P-P</sub> |
| $V_{CMOUT}$ | Output Common Mode Voltage                |                                    | SDO, $\overline{SDO}$ |     | $V_{CC} - V_{SDO}/2$ |     | V                 |
| $V_{SDO}$   | Output Voltage Swing                      | 50 $\Omega$ load, differential     |                       |     | 750                  |     | mV <sub>P-P</sub> |
|             | CLI DC Voltage                            | 0m cable <sup>(5)</sup>            | CLI                   |     | 2.5                  |     | V                 |
|             |   | Max cable <sup>(5)</sup>           |                       |     | 1.9                  |     | V                 |
|             | MUTE <sub>REF</sub> DC Voltage (floating) |                                    | MUTE <sub>REF</sub>   |     | 1.3                  |     | V                 |
|             | MUTE <sub>REF</sub> Range                 |                                    |                       |     | 0.7                  |     | V                 |
|             | $\overline{CD}$ /MUTE Output Voltage      | Carrier not present                | $\overline{CD}$ /MUTE | 2.6 |                      |     | V                 |
|             |   | Carrier present                    |                       |     |                      | 0.4 | V                 |
|             | $\overline{CD}$ /MUTE Input Voltage       | Min to mute outputs                |                       | 3.0 |                      |     | V                 |
|             |   | Max to force outputs active        |                       |     |                      | 2.0 | V                 |
| $I_{CC}$    | Supply Current                            | <sup>(6)</sup>                     |                       |     | 63                   | 77  | mA                |

- (1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to  $V_{EE} = 0$  Volts.
- (2) Typical values are stated for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .
- (3) Specification is ensured by characterization.
- (4) The maximum input voltage swing assumes a nonstressing, DC-balance signal; specifically, the SMPTE-recommended color bar test signal. Pathological or other stressing signals may not be used. This specification is for 0m cable only.
- (5) Input signal must be present for valid CLI. Refer to [Figure 2](#) for typical results.
- (6) Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. Refer to [Figure 3](#) and [Figure 4](#).

## AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)</sup>.

| Symbol                          | Parameter   | Conditions   | Reference                    | Min | Typ   | Max  | Units |    |
|---------------------------------|---|--|------------------------------|-----|-------|------|-------|----|
| BR <sub>MIN</sub>               | Minimum Input Data Rate   |  | SDI, $\overline{\text{SDI}}$ |     | 125   |      | Mbps  |    |
| BR <sub>MAX</sub>               | Maximum Input Data Rate   |  |                              |     |       | 1485 | Mbps  |    |
|                                 | Jitter for various cable lengths<br>(with equalizer pathological) | 270 Mbps, Belden 1694A,<br>400 meters <sup>(2)</sup>   |                              |     | 0.2   |      | UI    |    |
|                                 |   | 270 Mbps, Belden 8281,<br>280 meters <sup>(2)</sup>    |                              |     | 0.2   |      | UI    |    |
|                                 |   | 1.485 Gbps, Belden 1694A,<br>140 meters <sup>(2)</sup> |                              |     |       | 0.25 |       | UI |
|                                 |   | 1.485 Gbps, Belden 8281,<br>100 meters <sup>(2)</sup>  |                              |     |       | 0.25 |       | UI |
|                                 |   | 1.485 Gbps, Belden 1694A,<br>200 meters <sup>(2)</sup> |                              |     |       | 0.3  |       | UI |
| t <sub>r</sub> , t <sub>f</sub> | Output Rise Time, Fall Time                                       | 20% – 80% <sup>(2)</sup>                               | SDO, $\overline{\text{SDO}}$ |     | 100   | 220  | ps    |    |
|                                 | Mismatch in Rise/Fall Time  | <sup>(2)</sup>   |                              |     | 2     | 15   | ps    |    |
| t <sub>OS</sub>                 | Output Overshoot  | <sup>(2)</sup>   |                              |     | 1     | 5    | %     |    |
| R <sub>OUT</sub>                | Output Resistance   | single-ended <sup>(3)</sup>                            |                              |     | 50    |      | Ω     |    |
| RL <sub>IN</sub>                | Input Return Loss   | <sup>(4)</sup>   | SDI, $\overline{\text{SDI}}$ | 15  | 18-20 |      | dB    |    |
| R <sub>IN</sub>                 | Input Resistance  | single-ended   |                              |     | 1.3   |      | kΩ    |    |
| C <sub>IN</sub>                 | Input Capacitance   | single-ended <sup>(3)</sup>                            |                              |     | 1     |      | pF    |    |

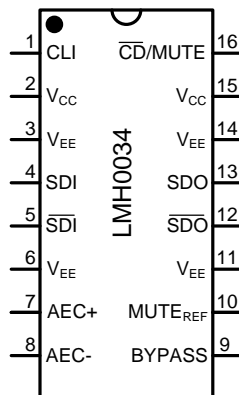
(1) Typical values are stated for V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C.

(2) Specification is ensured by characterization.

(3) Specification is ensured by design.

(4) Input return loss is dependent on board design. The LMH0034 meets this specification on the SD034 evaluation board from 5MHz to 1.5GHz.

## Connection Diagram

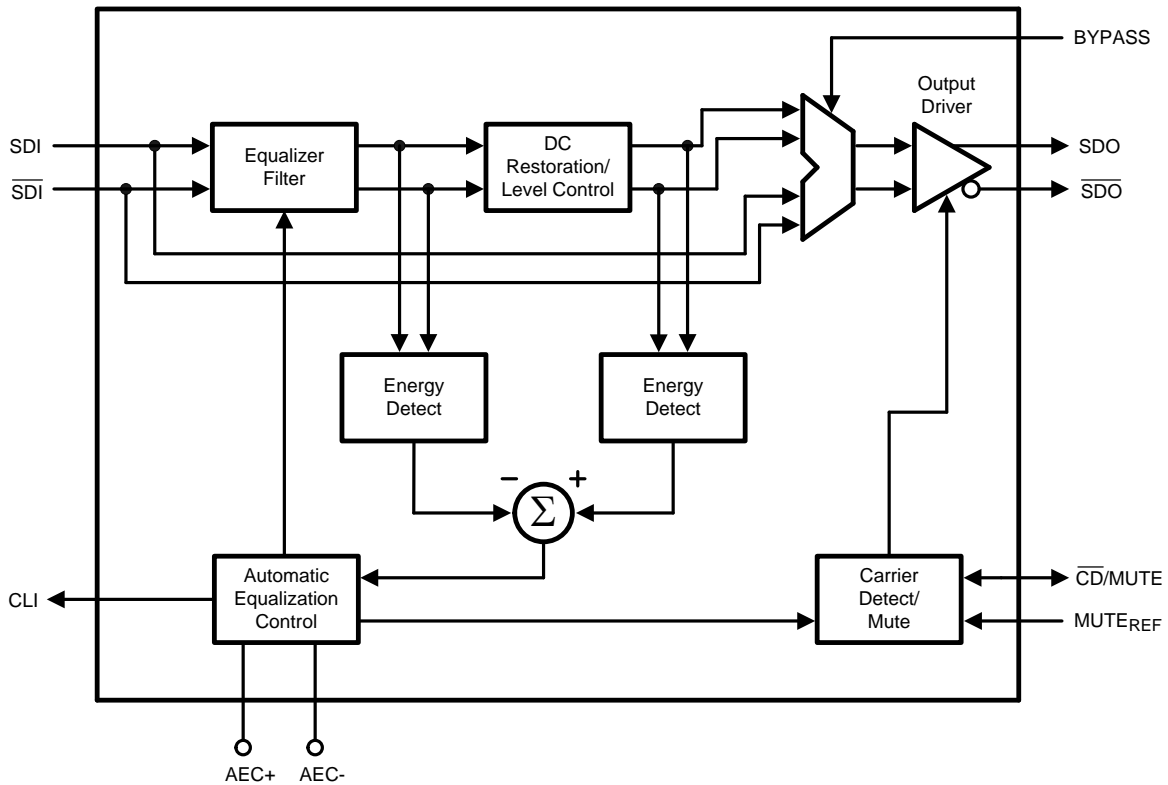


**Figure 1. 16-Pin SOIC  
See D Package**

**PIN DESCRIPTIONS**

| Pin # | Name                        | Description   |
|-------|-----------------------------|---|
| 1     | CLI                         | Cable length indicator. Provides a voltage inversely proportional to the cable length being equalized.  |
| 2     | V <sub>CC</sub>             | Positive power supply (+3.3V).  |
| 3     | V <sub>EE</sub>             | Negative power supply (ground).   |
| 4     | SDI                         | Serial data true input.   |
| 5     | $\overline{\text{SDI}}$     | Serial data complement input.   |
| 6     | V <sub>EE</sub>             | Negative power supply (ground).   |
| 7     | AEC+                        | AEC loop filter external capacitor (1 $\mu$ F) positive connection.   |
| 8     | AEC-                        | AEC loop filter external capacitor (1 $\mu$ F) negative connection.   |
| 9     | BYPASS                      | Bypasses equalization and DC restoration when high. No equalization occurs in this mode.  |
| 10    | MUTE <sub>REF</sub>         | Mute reference. Determines the maximum cable to be equalized before muting. May be unconnected for maximum equalization.  |
| 11    | V <sub>EE</sub>             | Negative power supply (ground).   |
| 12    | $\overline{\text{SDO}}$     | Serial data complement output.  |
| 13    | SDO                         | Serial data true output.  |
| 14    | V <sub>EE</sub>             | Negative power supply (ground).   |
| 15    | V <sub>CC</sub>             | Positive power supply (+3.3V).  |
| 16    | $\overline{\text{CD/MUTE}}$ | Bi-directional carrier detect and output mute. $\overline{\text{CD/MUTE}}$ is high when no signal is present. If unconnected, MUTE is controlled automatically by carrier detect. To force MUTE on, tie to V <sub>CC</sub> . To disable MUTE, tie to GND. $\overline{\text{CD/MUTE}}$ has no function in BYPASS mode. |

**Block Diagram**



## DEVICE OPERATION

### BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1 $\mu$ F capacitor placed across the AEC+ and AEC- pins. **Cable Length Indicator (CLI)** is derived from this block.

The **Carrier Detect / Mute** block generates the carrier detect signal and controls the mute function of the output. This block utilizes the bi-directional  $\overline{\text{CD/MUTE}}$  signal along with **Mute Reference (MUTE<sub>REF</sub>)**.

The **Output Driver** produces SDO and  $\overline{\text{SDO}}$ .

### CABLE LENGTH INDICATOR (CLI)

The cable length indicator provides a voltage to indicate the length of cable being equalized. The CLI voltage decreases as the cable length increases. [Figure 2](#) shows the typical CLI voltage vs. Belden 1694A cable length. Note: CLI is only valid when an input signal is present.

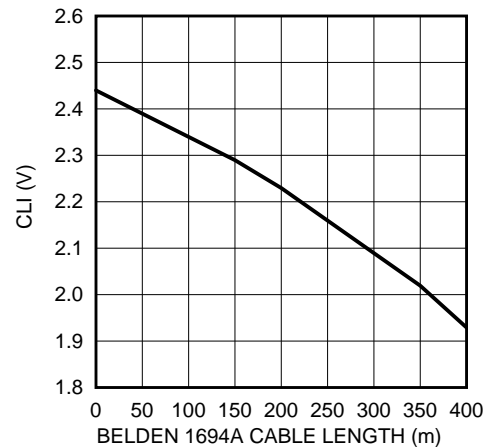


Figure 2. CLI vs. Belden 1694A Cable Length

### MUTE REFERENCE (MUTE<sub>REF</sub>)

The mute reference determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. As the applied MUTE<sub>REF</sub> voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. MUTE<sub>REF</sub> may be left unconnected for maximum equalization before muting.

### CARRIER DETECT / MUTE ( $\overline{\text{CD/MUTE}}$ )

Carrier Detect / Mute is bi-directional, serving as both a carrier detect (output function) and mute (input function).

When used as an output,  $\overline{\text{CD/MUTE}}$  determines if a valid signal is present at the LMH0034 input. If MUTE<sub>REF</sub> is used, the carrier detect threshold will be altered accordingly.  $\overline{\text{CD/MUTE}}$  provides a high voltage when no signal is present at the LMH0034 input, and the outputs are automatically muted.  $\overline{\text{CD/MUTE}}$  is low when a valid input signal has been detected, and the outputs are automatically enabled.

As an input,  $\overline{\text{CD/MUTE}}$  can be used to override the carrier detect and manually mute or enable the LMH0034 outputs. Applying a high input to  $\overline{\text{CD/MUTE}}$  will mute the LMH0034 outputs. Applying a low input will force the outputs to be active regardless of the length of cable or the state of MUTE<sub>REF</sub>.

## INPUT INTERFACING

The LMH0034 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported.

The LMH0034 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

## OUTPUT INTERFACING

The SDO and  $\overline{\text{SDO}}$  outputs are internally loaded with  $50\Omega$ . They produce a  $750\text{ mV}_{\text{P-P}}$  differential output, or a  $375\text{ mV}_{\text{P-P}}$  single-ended output.

## APPLICATION INFORMATION

### PCB LAYOUT RECOMMENDATIONS

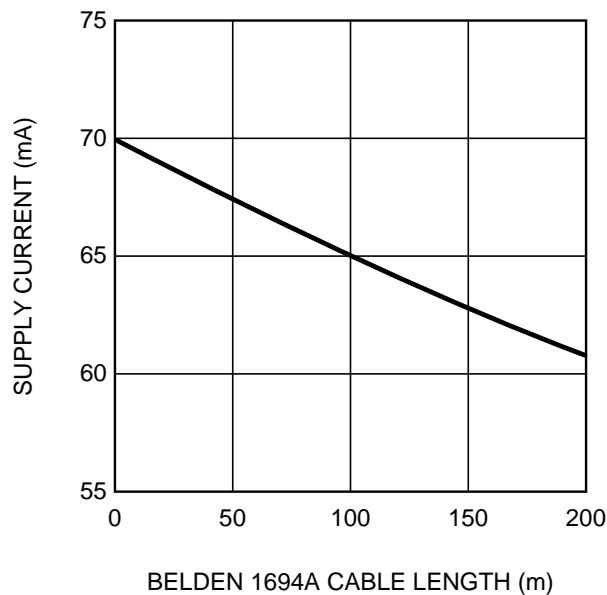
Please refer to the following Application Note: AN-1372 ([SNLA071](#)) “LMH0034 PCB Layout Techniques.”

### REPLACING THE GENNUM GS1524

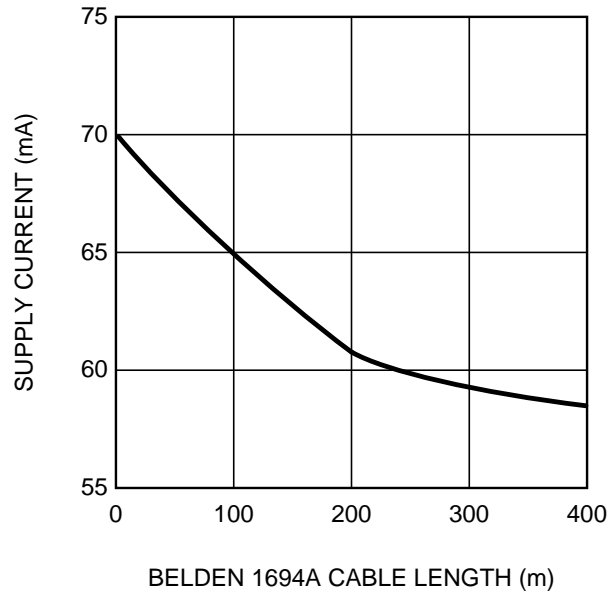
The LMH0034 is form-fit-function compatible with the Gennum GS1524 and GS1524A.

### SUPPLY CURRENT VS. CABLE LENGTH

The supply current ( $I_{\text{CC}}$ ) depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. [Figure 3](#) shows supply current vs. Belden 1694A cable length for 1.485 Gbps data and [Figure 4](#) shows supply current vs. Belden 1694A cable length for 270 Mbps data.



**Figure 3. Supply Current vs. Belden 1694A Cable Length, 1.485 Gbps**



**Figure 4. Supply Current vs. Belden 1694A Cable Length, 270 Mbps**

## REVISION HISTORY

| Changes from Revision G (April 2013) to Revision H         | Page              |
|--|-------------------|
| • Changed layout of National Data Sheet to TI format ..... | <a href="#">7</a> |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMH0034MA/NOPB   | ACTIVE        | SOIC         | D               | 16   | 48          | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | 0 to 85      | L034                    | <a href="#">Samples</a> |
| LMH0034MAX/NOPB  | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | 0 to 85      | L034                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMH0034MAX/NOPB | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.3     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMH0034MAX/NOPB | SOIC         | D               | 16   | 2500 | 367.0       | 367.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LMH0034MA/NOPB | D            | SOIC         | 16   | 48  | 495    | 8      | 4064   | 3.05   |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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