



**THE DATASHEET OF
MP6232DN-LF-Z**



DESCRIPTION

The MP6231/MP6232 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP6231/MP6232 analog switch has 85mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with guaranteed current limits, making it ideal for load switching applications. The MP6231/MP6232 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, then the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP6231/MP6232 is available in 8-pin MSOP, SOIC package with exposed pad and 8-pin SOIC w/o exposed pad.

FEATURES

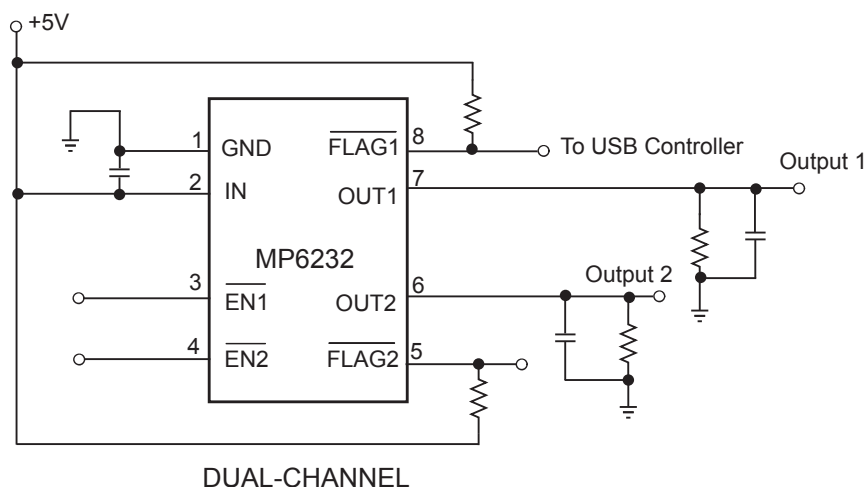
- 500mA Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 140μA Quiescent Current
- 85mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options
- UL File # E322138

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

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TYPICAL APPLICATION



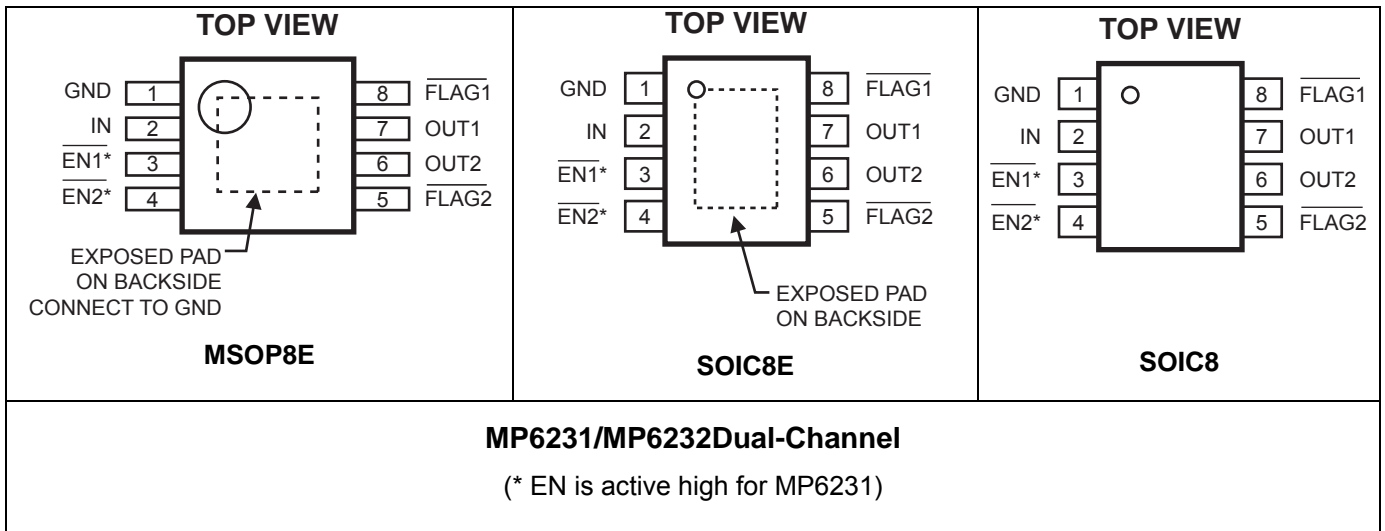
UL Recognized Component

ORDERING INFORMATION

Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T _A =25°C	Package	Top Marking	Free Air Temperature (T _A)
MP6231DN*	Active High	Dual	0.5A	750mA	SOIC8E	MP6231DN	-40°C to +85°C
MP6231DH					MSOP8E	6231D	
MP6231DS					SOIC8		
MP6232DN	Active Low				SOIC8E	MP6232DN	
MP6232DH					MSOP8E	6232D	
MP6232DS					SOIC8		

* For Tape & Reel, add suffix -Z (e.g. MP6231DN-Z).
 For RoHS compliant packaging, add suffix -LF (e.g. MP6231DN-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN	-0.3V to +6.0V
EN, FLAG, OUT to GND	-0.3V to +6.0V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	
SOIC8E	2.5W
MSOP8E	2.27W
SOIC8	1.4W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C
Operating Junct. Temp.	-40°C to +125°C

Thermal Resistance ⁽³⁾	θ_{JA}	θ_{JC}
SOIC8E	50	10... °C/W
MSOP8E	55	12... °C/W
SOIC8	90	42... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (4)
 $V_{IN}=5V$, $T_A=+25^{\circ}C$, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	One Channel Enabled, $I_{OUT}=0$, One Switch ON		90	120	μA
Supply Current	Both Channels Enabled, $I_{OUT}=0$, Both Switches ON		140	160	μA
Shutdown Current	Device Disable, $V_{OUT}=float$, $V_{IN}=5.5V$		1		μA
Off Switch Leakage	Device Disable, $V_{IN}=5.5V$		1		μA
Current Limit		550		1100	mA
Trip Current	Current Ramp (slew rate $\leq 100A/s$) on Output		1.2	1.6	A
Under-voltage Lockout	Rising Edge	1.95		2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	$I_{OUT}=100mA$, and $-40^{\circ}C < T_A < 85^{\circ}C$		85	130	m Ω
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.8	V
FLAG Output Logic Low Voltage	$I_{SINK}=5mA$			0.4	V
FLAG Output High Leakage Current	$V_{IN}=V_{FLAG}=5.5V$			1	μA
Thermal Shutdown			140		$^{\circ}C$
Thermal Shutdown Hysteresis			20		$^{\circ}C$
V_{OUT} Rising Time, T_r	$V_{IN}=5.5V$, $C_L=1\mu F$, $R_L=11\Omega$		0.9		ms
	$V_{IN}=2.7V$, $C_L=1\mu F$, $R_L=11\Omega$		1.7		ms
V_{OUT} Falling Time, T_f	$V_{IN}=5.5V$, $C_L=1\mu F$, $R_L=11\Omega$			0.5	ms
	$V_{IN}=2.7V$, $C_L=1\mu F$, $R_L=11\Omega$			0.5	ms
Turn On Time, T_{on}	$C_L=100\mu F$, $R_L=11\Omega$			3	ms
Turn Off Time, T_{off}	$C_L=100\mu F$, $R_L=11\Omega$			10	ms
FLAG Deglitch Time		4	8	15	ms
ENx Input Leakage			1		μA
Reverse Leakage Current	OUTX=5.5V, IN=GND		0.2		μA

Notes:

 4) Production test at $+25^{\circ}C$. Specifications over the temperature range are guaranteed by design and characterization.

PIN FUNCTIONS

MP6231/MP6232

SOIC8 SOIC8E MSOP8E	Name	Description
1	GND	Ground.
2	IN	Input Voltage. Accepts 2.7V to 5.5V input.
3	$\overline{\text{EN1}}$	Active Low: (MP6232), Active High: (MP6231)
4	$\overline{\text{EN2}}$	Active Low: (MP6232), Active High: (MP6231)
5	$\overline{\text{FLAG2}}$	IN-to-OUT2 Over-current, active-low output flag. Open-Drain.
6	OUT2	IN-to-OUT2 Power-Distribution Switch Output.
7	OUT1	IN-to-OUT1 Power-Distribution Switch Output
8	$\overline{\text{FLAG1}}$	IN-to-OUT1 Over-current, active-low output flag. Open-Drain.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, unless otherwise noted.

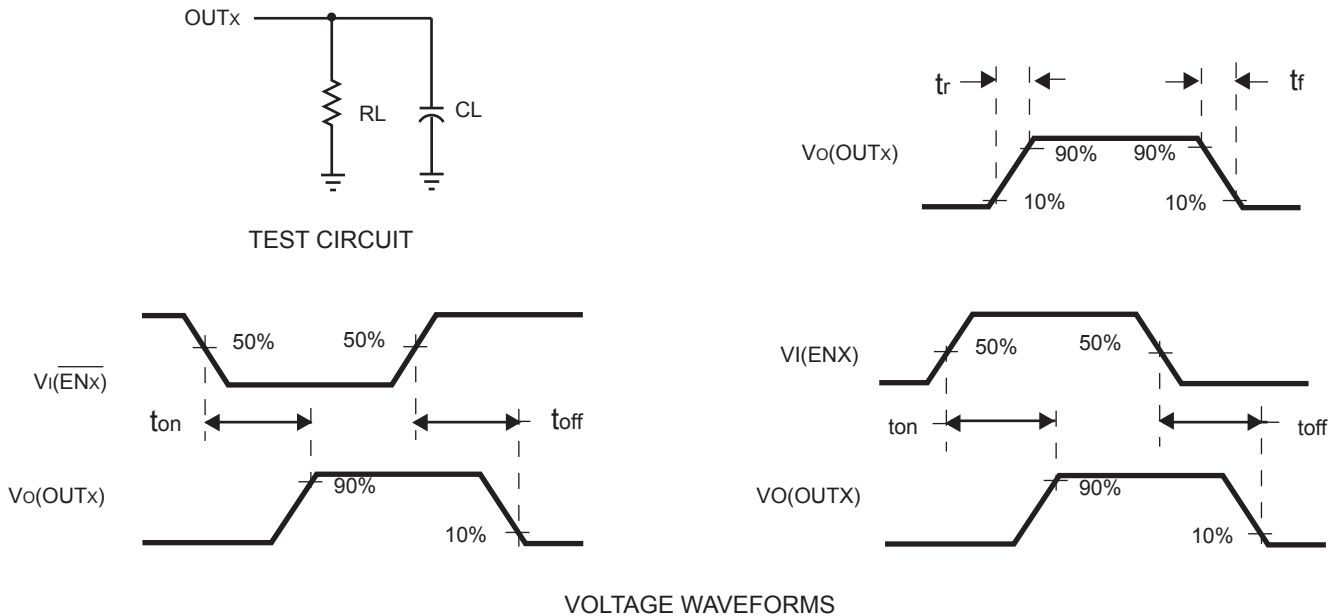


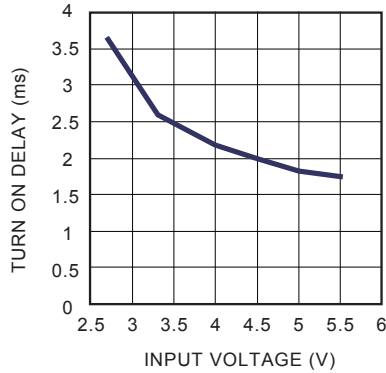
Figure 1—Test Circuit and Voltage Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=5.5V$, $C_L = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

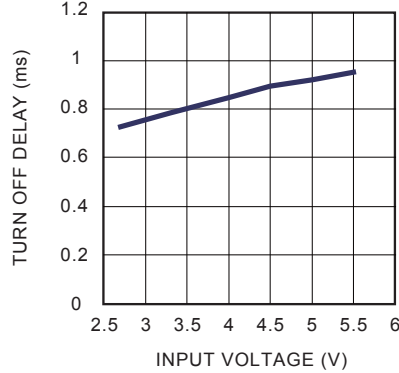
Turn on Delay vs. Input Voltage

$V_{EN}=5V$, $R_L=11\Omega$



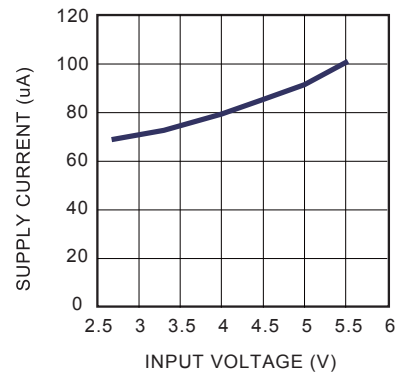
Turn off Delay vs. Input Voltage

$V_{EN}=5V$, $R_L=11\Omega$



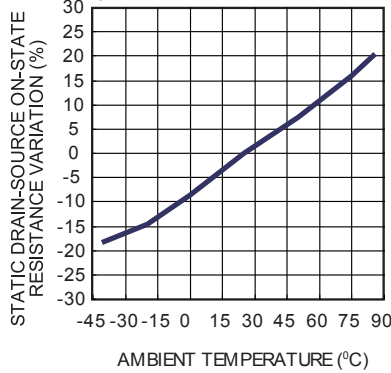
Supply Current, Output Enabled vs. Input Voltage

$V_{EN}=5V$



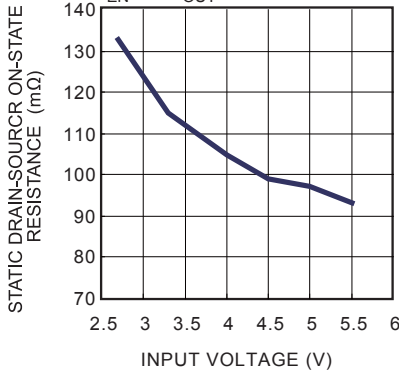
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

$I_O=0.1A$, $V_{IN}=5V$



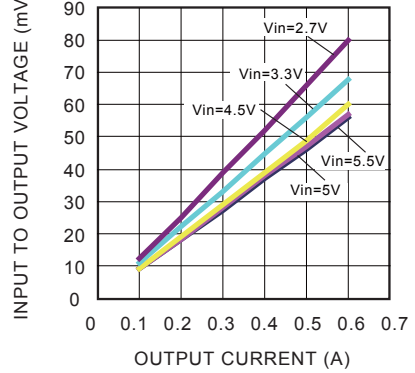
Static Drain-Source On-State Resistance vs. Input Voltage

$V_{EN}=5V$, $I_{OUT}=0.5A$



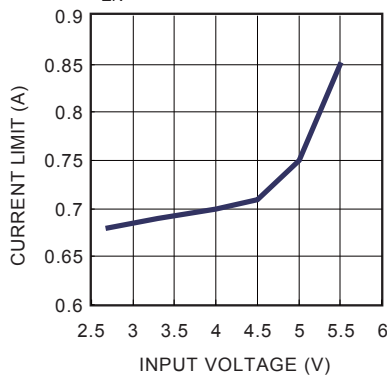
Input to Output Voltage vs. Load Current

$V_{EN}=5V$



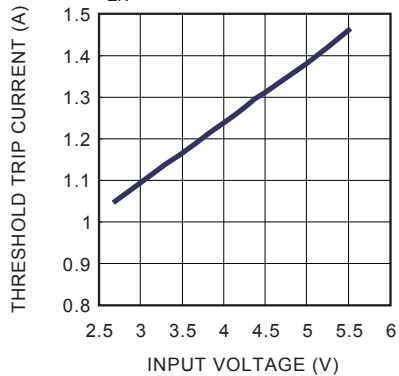
Current Limit vs. Input Voltage

$V_{EN}=5V$



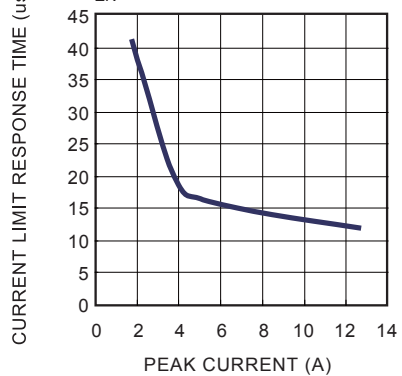
Threshold Trip Current vs. Input Voltage

$V_{EN}=5V$



Current Limit Response Time vs. Peak Current

$V_{EN}=5V$

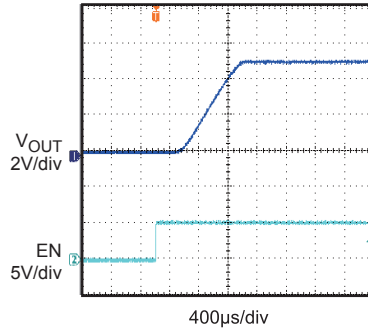


TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=5.5V$, $C_L = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

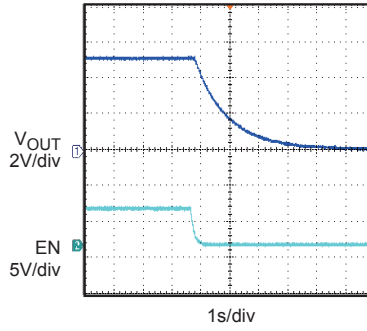
Turn On Delay and Rise Time with 0.1 μF Load

$V_{EN}=5V$, $C_L=0.1\mu F$



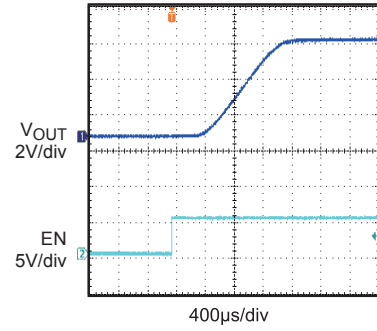
Turn Off Delay and Fall Time with 0.1 μF Load

$V_{EN}=5V$, $C_L=0.1\mu F$



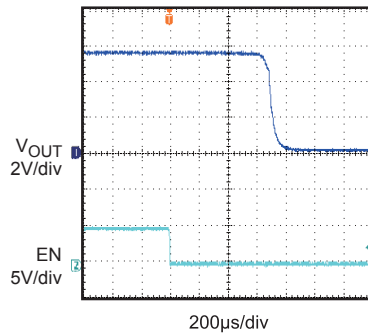
Turn On Delay and Rise Time with 1 μF Load

$V_{EN}=5V$, $R_L=11\Omega$, $C_L=1\mu F$



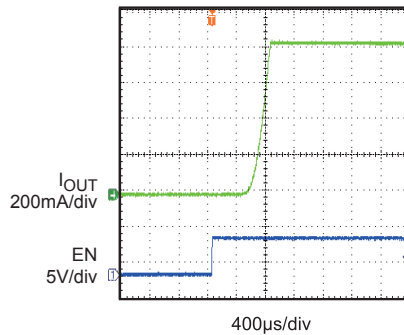
Turn Off Delay and Fall Time with 1 μF Load

$V_{EN}=5V$, $R_L=11\Omega$, $C_L=1\mu F$



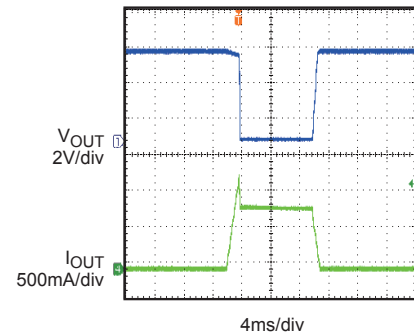
Short Circuit Current Device Enabled into Short

$V_{EN}=5V$, $C_L=1\mu F$



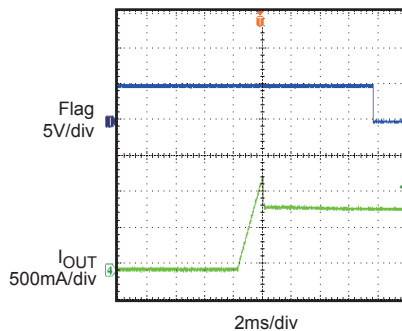
Threshold Trip Current with Ramped Load on Enabled Device

$V_{EN}=5V$, $C_L=1\mu F$



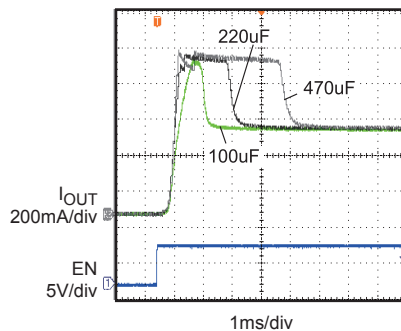
Ramped Load on Enabled Device

$V_{EN}=5V$, $C_L=1\mu F$



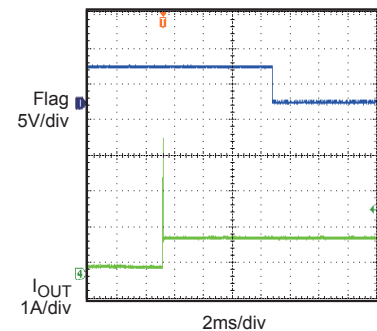
Inrush Current with Different Load Capacitance

$V_{EN}=5V$, $R_L=11\Omega$,
Start up by EN



1 Ω Load Connected to Enabled Device

$V_{EN}=5V$, $C_L=1\mu F$



Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing excessive current to flow and heating the junction. The die temp. is internally monitored until the thermal limit is reached. Once this temp. is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP6231/MP6232 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

APPLICATION INFORMATION

Power-Supply Considerations

Over 10 μ F capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy.

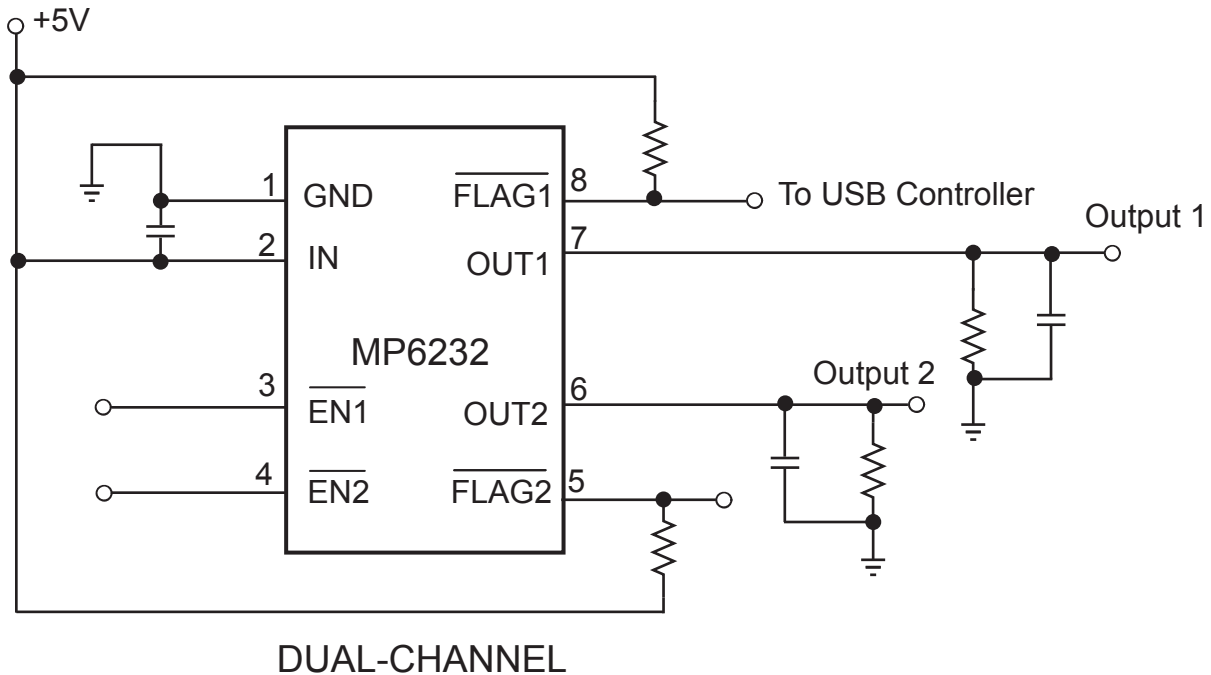
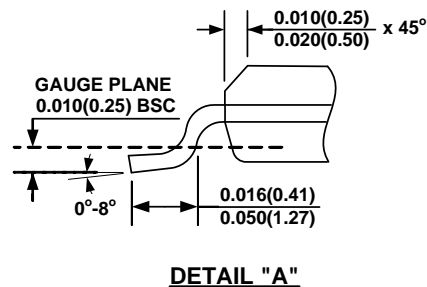
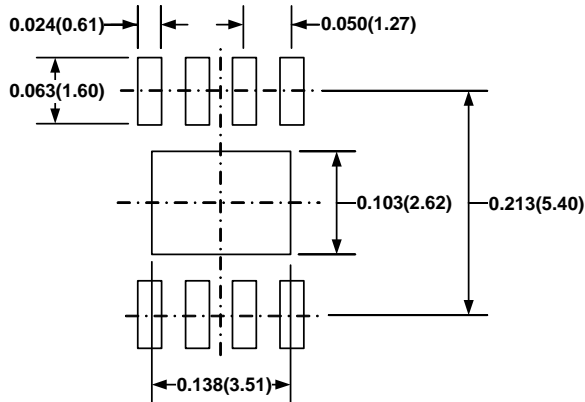
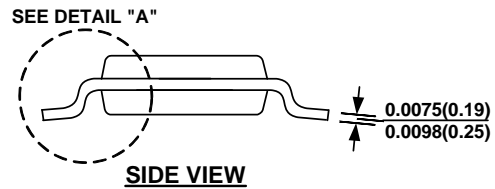
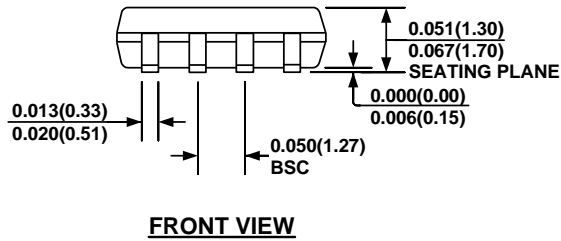
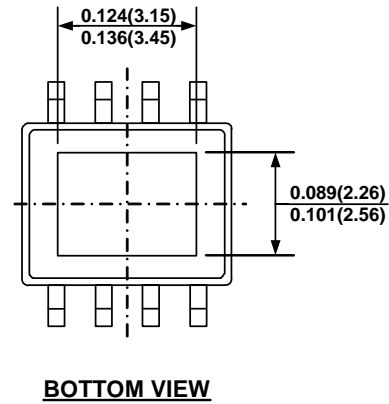
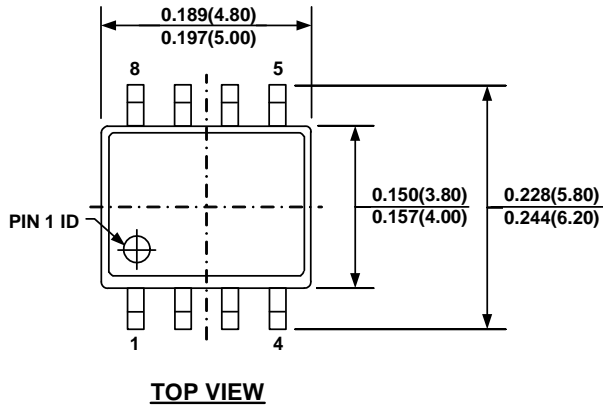


Figure 3—Application Circuit

PACKAGE INFORMATION

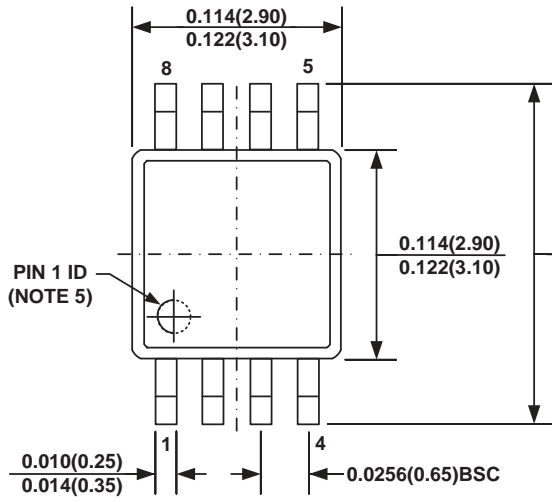
SOIC8E



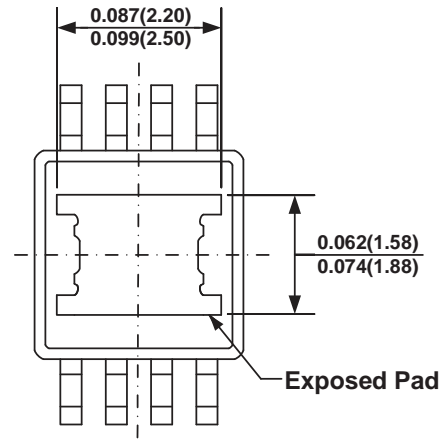
NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

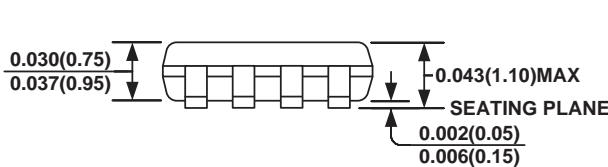
MSOP8E (EXPOSED PAD)



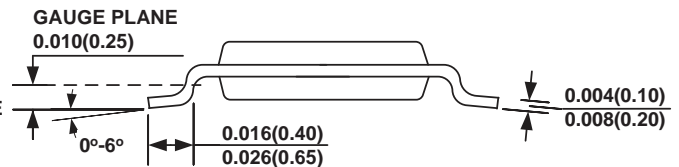
TOP VIEW



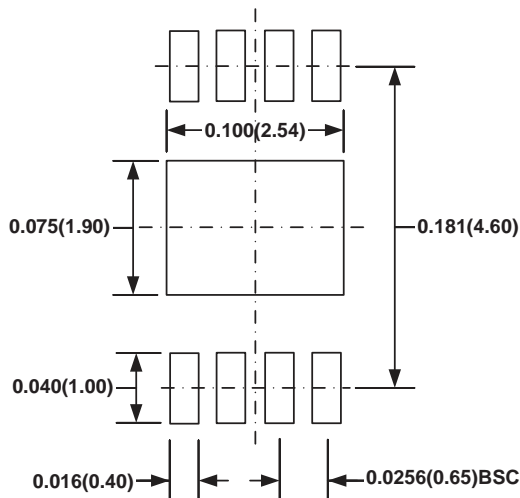
BOTTOM VIEW



FRONT VIEW



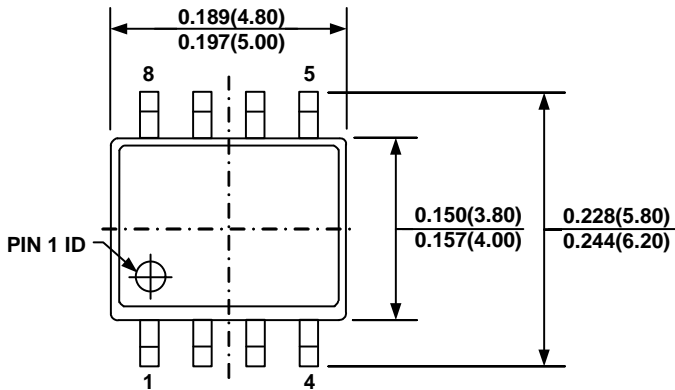
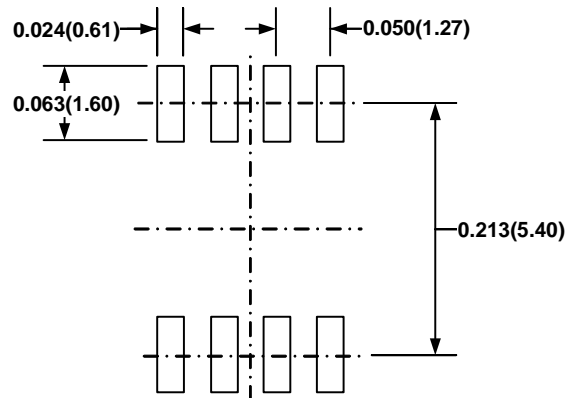
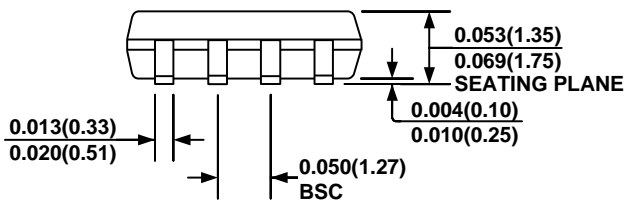
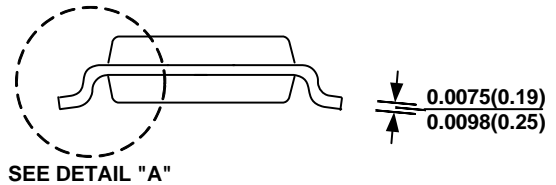
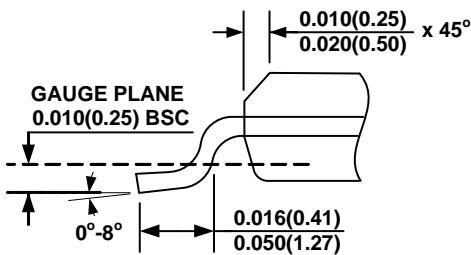
SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
- 6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
- 7) DRAWING IS NOT TO SCALE.

SOIC8

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"
NOTE:

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- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management