# THE DATASHEET OF

# MPC8272ZQMIBA

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**Technical Data**

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# MPC8272 PowerQUICC II Family Hardware Specifications

This document contains detailed information about power considerations, DC/AC electrical characteristics, and AC timing specifications for .13µm (HiP7) members of the PowerQUICC II family of integrated communications processors—the MPC8272, the MPC8248, the MPC8271, and the MPC8247. They include on a single chip a 32-bit Power Architecture® core that incorporates memory management units (MMUs) and instruction and data caches and that implements the Power Architecture instruction set; a modified communications processor module (CPM); and an integrated security engine (SEC) for encryption (the MPC8272 and the MPC8248 only).

All four devices are collectively referred to throughout this hardware specification as “the MPC8272” unless otherwise noted.

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# 1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

**Table 1. MPC8272 PowerQUICC II Family Functionality**

| Functionality | SoCs | | | |
|---|---|---|---|---|
| | MPC8272 | MPC8248 | MPC8271 | MPC8247 |
| Package[1] | 516 PBGA | | | |
| Serial communications controllers (SCCs) | 3 | 3 | 3 | 3 |
| QUICC multi-channel controller (QMC) | Yes | Yes | Yes | Yes |
| Fast communication controllers (FCCs) | 2 | 2 | 2 | 2 |
| I-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| D-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| Ethernet (10/100) | 2 | 2 | 2 | 2 |
| UTOPIA II Ports | 1 | 0 | 1 | 0 |
| Multi-channel controllers (MCCs) | 0 | 0 | 0 | 0 |
| PCI bridge | Yes | Yes | Yes | Yes |
| Transmission convergence (TC) layer | — | — | — | — |
| Inverse multiplexing for ATM (IMA) | — | — | — | — |
| Universal serial bus (USB) 2.0 full/low rate | 1 | 1 | 1 | 1 |
| Security engine (SEC) | Yes | Yes | — | — |

[1] See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, “Ordering Information.”

**Table 2. MPC8272 PowerQUICC II Device Packages**

| Code (Package) | VR (516 PBGA—Lead free) | ZQ (516 PBGA—Lead spheres) |
|---|---|---|
| Device | MPC8272VR | MPC8272ZQ |
| | MPC8248VR | MPC8248ZQ |
| | MPC8271VR | MPC8271ZQ |
| | MPC8247VR | MPC8247ZQ |

This figure shows the block diagram of the SoC.

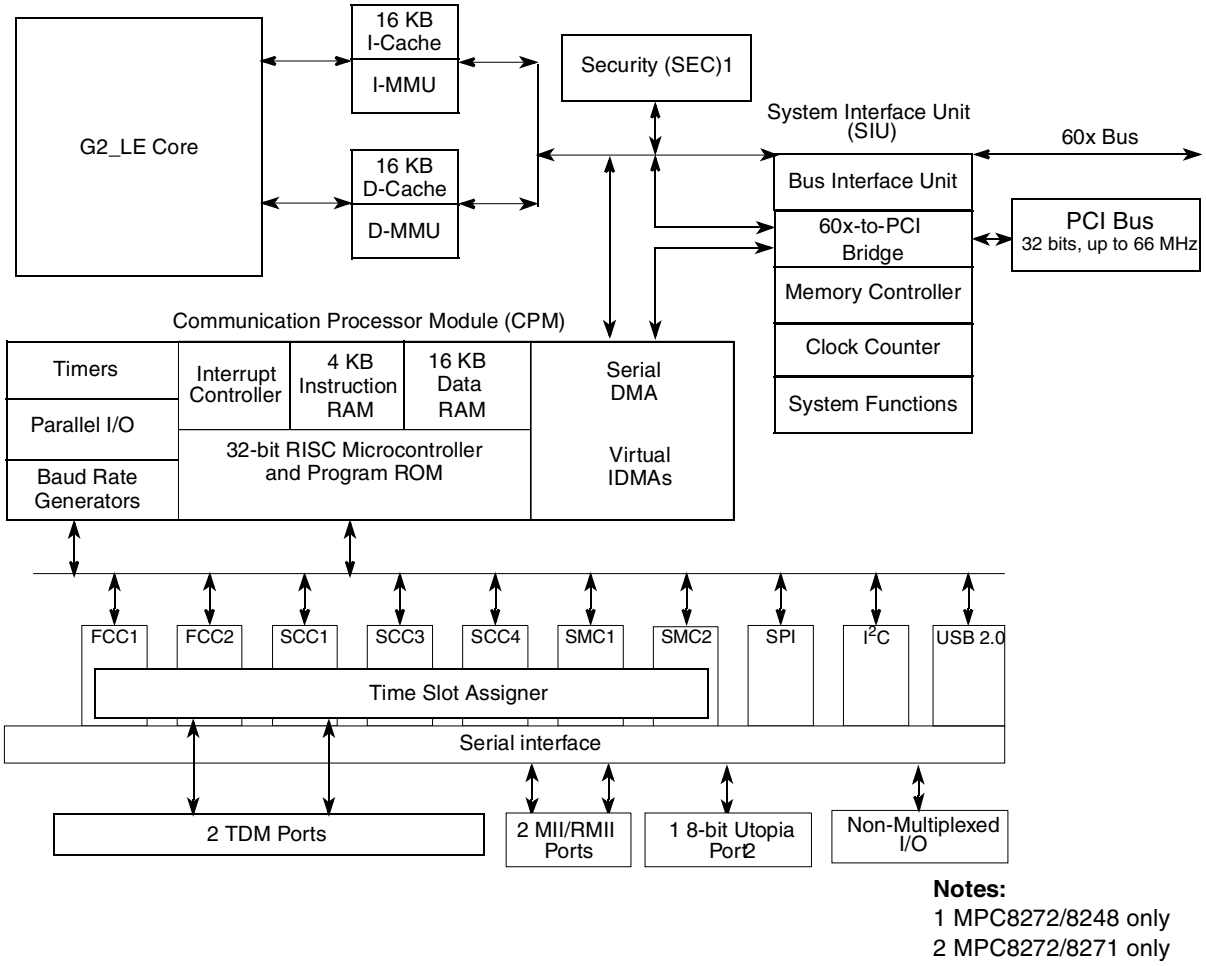



**Figure 1. SoC Block Diagram**

## 1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the MPC603e microprocessor
  - System core microprocessor supporting frequencies of 266–400 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - Supports bus snooping for cache coherency

  - Floating-point unit (FPU) supports floating-point arithmetic
  - Support for cache locking
- Low-power consumption
- Separate power supply for internal logic (1.5 V) and for I/O (3.3 V)
- Separate PLLs for G2_LE core and for the communications processor module (CPM)
  - G2_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 5.5:1, 6:1, 7:1, 8:1
  - Internal CPM/bus clock multiplier that provides ratios 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs—up to two external masters
  - Supports single transfers and burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
    - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- Eight bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash, and other user-definable peripherals
  - Byte write enables
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page mode pipeline SDRAM machine
  - Byte selects for 64-bit bus width (60x)
  - Dedicated interface logic for SDRAM
- Disable CPU mode

- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
  - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
  - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
  - Microcode tracing capabilities
  - Eight CPM trap registers
- Universal serial bus (USB) controller
  - Supports USB 2.0 full/low rate compatible
  - USB host mode
    - Supports control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - Flexible data buffers with multiple buffers per frame
    - Supports local loopback mode for diagnostics (12 Mbps only)
  - Supports USB slave mode
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Two fast communication controllers (FCCs) supporting the following protocols:
    - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—up to T3 rates (clear channel)

  - One of the FCCs supports ATM (MPC8272 and MPC8271 only)—full-duplex SAR at 155 Mbps, 8-bit UTOPIA interface 31 Mphys, AAL5, AAL1, AAL2, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64-K external connections

— Three serial communications controllers (SCCs) identical to those on the MPC860 supporting the digital portions of the following protocols:
  - Ethernet/IEEE 802.3 CDMA/CS
  - HDLC/SDLC and HDLC bus
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Binary synchronous (BiSync) communications
  - Transparent
  - QUICC multichannel controller (QMC) up to 64 channels
    - Independent transmit and receive routing, frame synchronization.
    - Serial-multiplexed (full-duplex) input/output 2048, 1544, and 1536 Kbps PCM highways
    - Compatible with T1/DS1 24-channel and CEPT E1 32-channel PCM highway, ISDN basic rate, ISDN primary rate, and user defined.
    - Subchanneling on each time slot.
    - Independent transmit and receive routing, frame synchronization and clocking
    - Concatenation of any not necessarily consecutive time slots to channels independently for receiver/transmitter
    - Supports H1,H11, and H12 channels
    - Allows dynamic allocation of channels
  - SCC3 in NMSI mode is not usable when USB is enabled.
— Two serial management controllers (SMCs), identical to those of the MPC860
  - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
— One serial peripheral interface identical to the MPC860 SPI
— One $I^2C$ controller (identical to the MPC860 $I^2C$ controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
— Up to two TDM interfaces
  - Supports one groups of two TDM channels
  - 1024 bytes of SI RAM
— Eight independent baud rate generators and 14 input clock pins for supplying clocks to FCC, SCC, SMC, and USB serial channels
— Four independent 16-bit timers that can be interconnected as two 32-bit timers

- PCI bridge
  - PCI Specification revision 2.2-compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI to 60x memory and 60x memory to PCI streaming
  - PCI host bridge or peripheral capabilities
  - Includes four DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes the configuration registers required by the PCI standard (which are automatically loaded from the EPROM to configure the MPC8272) and message and doorbell registers
  - Supports the $I_2O$ standard
  - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66 MHz, 3.3 V specification
  - 60x-PCI bus core logic, which uses a buffer pool to allocate buffers for each port

# 2 Operating Conditions

This table shows the maximum electrical ratings.

**Table 3. Absolute Maximum Ratings[1]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage[2] | VDD | –0.3 – 2.25 | V |
| PLL supply voltage[2] | VCCSYN | –0.3 – 2.25 | V |
| I/O supply voltage[3] | VDDH | –0.3 – 4.0 | V |
| Input voltage[4] | VIN | GND(–0.3) – 3.6 | V |
| Junction temperature | $T_j$ | 120 | °C |
| Storage temperature range | $T_{STG}$ | (–55) – (+150) | °C |

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.

3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

This table lists recommended operational voltage conditions.

**Table 4. Recommended Operating Conditions[1]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage | VDD | 1.425 – 575 | V |
| PLL supply voltage | VCCSYN | 1.425 – 575 | V |
| I/O supply voltage | VDDH | 3.135 – 3.465 | V |
| Input voltage | VIN | GND (–0.3) – 3.465 | V |
| Junction temperature (maximum) | $T_j$ | 105[2] | °C |
| Ambient temperature | $T_A$ | 0–70[2] | °C |

1 **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

2 Note that for extended temperature parts the range is $(-40)_{T_A}$ – $105_{T_j}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or $V_{CC}$).

This figure shows the undershoot and overshoot voltage of the 60x bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

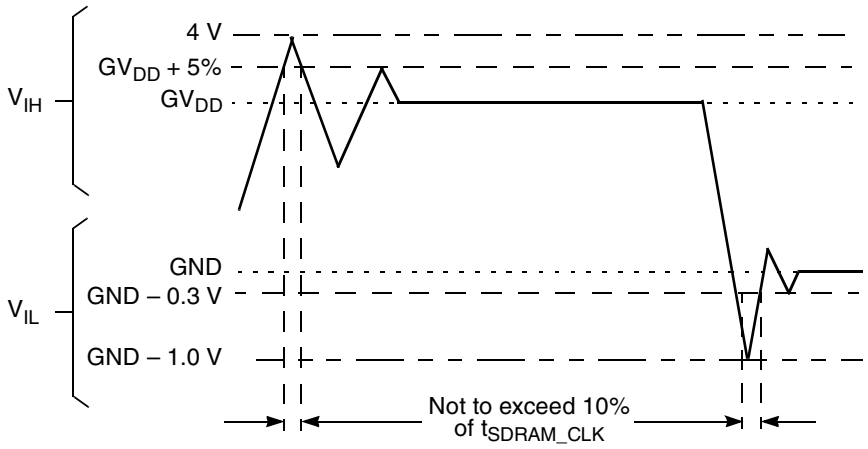



**Figure 2. Overshoot/Undershoot Voltage**

# 3 DC Electrical Characteristics

This table shows DC electrical characteristics.

**Table 5. DC Electrical Characteristics[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage[3] | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[4] | $I_{IN}$ | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | μA |
| Signal low input current, $V_{IL}$ = 0.8 V | $I_L$ | — | 1 | μA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | μA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[5] (UTOPIA pins only): $I_{OH}$ = -8.0mA<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31] | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[5] (UTOPIA pins only): $I_{OL}$ = 8.0mA<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31] | $V_{OL}$ | — | 0.5 | V |

**Table 5. DC Electrical Characteristics[1] (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 6.0mA<br>BR<br>BG/IRQ6<br>ABB/IRQ2<br>TS<br>A[0-31]<br>TT[0-4]<br>TBST<br>TSIZE[0–3]<br>AACK<br>ARTRY<br>DBG/IRQ7<br>DBB/IRQ3<br>D[0–63]<br>IRQ3/CKSTP_OUT/EXT_BR3<br>IRQ4/CORE_SRESET/EXT_BG3<br>IRQ5/TBEN/EXT_DBG3/CINT<br>PSDVAL<br>TA<br>TEA<br>GBL/IRQ1<br>CI/BADDR29/IRQ2<br>WT/BADDR30/IRQ3<br>BADDR31/IRQ5/CINT<br>CPU_BR/INT_OUT<br>IRQ0/NMI_OUT<br>PORESET/PCI_RST<br>HRESET<br>SRESET<br>RSTCONF | $V_{OL}$ | — | 0.4 | V |

**Table 5. DC Electrical Characteristics[1] (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 5.3mA<br>CS[0–5]<br>CS6/BCTL1/SMI<br>CS7/TLBSYNC<br>BADDR27/ IRQ1<br>BADDR28/ IRQ2<br>ALE/ IRQ4<br>BCTL0<br>PWE[0–7]/PSDDQM[0–7]/PBS[0–7]<br>PSDA10/PGPL0<br>PSDWE/PGPL1<br>POE/PSDRAS/PGPL2<br>PSDCAS/PGPL3<br>PGTA/PUPMWAIT/PGPL4<br>PSDAMUX/PGPL5<br>PCI_CFG0 (PCI_HOST_EN)<br>PCI_CFG1 (PCI_ARB_EN)<br>PCI_CFG2 (DLL_ENABLE)<br>MODCK1/RSRV/TC(0)/BNKSEL(0)<br>MODCK2/CSE0/TC(1)/BNKSEL(1)<br>MODCK3CSE1/TC(2)/BNKSEL(2) | $V_{OL}$ | — | 0.4 | V |
| $I_{OL}$ = 3.2mA<br>PCI_PAR<br>PCI_FRAME<br>PCI_TRDY<br>PCI_IRDY<br>PCI_STOP<br>PCI_DEVSEL<br>PCI_IDSEL<br>PCI_PERR<br>PCI_SERR<br>PCI_REQ0<br>PCI_REQ1/ CPI_HS_ES<br>PCI_GNT0<br>PCI_GNT1/ CPI_HS_LES<br>PCI_GNT2/ CPI_HS_ENUM<br>PCI_RST<br>PCI_INTA<br>PCI_REQ2<br>DLLOUT<br>PCI_AD(0-31)<br>PCI_C(0–3)/BE(0-3)<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31]<br>TDO | | | | |

1 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

2 TCK, TRST and PORESET have min VIH = 2.5V.

3 $V_{IL}$ for IIC interface does not match IIC standard, but does meet IIC standard for $V_{OL}$ and should not cause any compatibility issue.

4 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

[5] MPC8272 and MPC8271 only.

**Table 6.**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, TRST and PORESET[1] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[2] | $I_{IN}$ | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | μA |
| Signal low input current, $V_{IL}$ = 0.8 V[3] | $I_L$ | — | 1 | μA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | μA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[4] (UTOPIA pins only): $I_{OH}$ = -8.0mA | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[4] (UTOPIA pins only): $I_{OL}$ = 8.0mA | $V_{OL}$ | — | 0.5 | V |
| $I_{OL}$ = 6.0mA<br>BR<br>BG<br>ABB/IRQ2<br>TS<br>A[0-31]<br>TT[0-4]<br>TBST<br>TSIZE[0–3]<br>AACK<br>ARTRY<br>DBG<br>DBB/IRQ3<br>D[0-63]<br>//EXT_BR3<br>//EXT_BG3<br>/TBEN/EXT_DBG3/CINT<br>PSDVAL<br>TA<br>TEA<br>GBL/IRQ1<br>CI/BADDR29/IRQ2<br>WT/BADDR30/IRQ3<br>BADDR31/IRQ5/CINT<br>CPU_BR<br>IRQ0/NMI_OUT<br>/PCI_RST<br>HRESET<br>SRESET<br>RSTCONF | $V_{OL}$ | — | 0.4 | V |

**Table 6.**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 5.3mA<br>CS[0-9]<br>CS(10)/BCTL1<br>CS(11)/AP(0)<br>BADDR[27–28]<br>ALE<br>BCTL0<br>PWE[0–7]/PSDDQM[0–7]/PBS[0–7]<br>PSDA10/PGPL0<br>PSDWE/PGPL1<br>POE/PSDRAS/PGPL2<br>PSDCAS/PGPL3<br>PGTA/PUPMWAIT/PGPL4/PPBS<br>PSDAMUX/PGPL5<br>LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3]<br>LSDA10/LGPL0/PCI_MODCKH0<br>LSDWE/LGPL1/PCI_MODCKH1<br>LOE/LSDRAS/LGPL2/PCI_MODCKH2<br>LSDCAS/LGPL3/PCI_MODCKH3<br>LGTA/LUPMWAIT/LGPL4/LPBS<br>LSDAMUX/LGPL5/PCI_MODCK<br>LWR<br>MODCK[1–3]/AP[1–3]/TC[0–2]/BNKSEL[0–2] | $V_{OL}$ | — | 0.4 | V |
| $I_{OL}$ = 3.2mA<br>L_A14/PAR<br>L_A15/FRAME/SMI<br>L_A16/TRDY<br>L_A17/IRDY/CKSTP_OUT<br>L_A18/STOP<br>L_A19/DEVSEL<br>L_A20/IDSEL<br>L_A21/PERR<br>L_A22/SERR<br>L_A23/REQ0<br>L_A24/REQ1/HSEJSW<br>L_A25/GNT0<br>L_A26/GNT1/HSLED<br>L_A27/GNT2/HSENUM<br>L_A28/RST/CORE_SRESET<br>L_A29/INTAL_A30/REQ2<br>L_A31<br>LCL_D[0-31)]/AD[0-31]<br>LCL_DP[03]/C/BE[0-3]<br>PA[0–31]<br>PB[4–31]<br>PC[0–31]<br>PD[4–31]<br>TDO<br>QREQ | | | | |

1 TCK, TRST and PORESET have min VIH = 2.5V.

2 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

3 $V_{IL}$ for IIC interface does not match IIC standard, but does meet IIC standard for $V_{OL}$ and should not cause any compatibility issue.

4 MPC8280, MPC8275VR, MPC8275ZQ only.

# 4 Thermal Characteristics

This table describes thermal characteristics. See Table 2 for information on a given SoC's package. Discussions of each characteristic are provided in Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance," through Section 4.7, "References." For the these discussions, $P_D = (V_{DD} \times I_{DD}) +$ PI/O, where PI/O is the power dissipation of the I/O drivers.

**Table 7. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit | Air Flow |
|---|---|---|---|---|
| Junction-to-ambient—single-layer board[1] | $R_{\theta JA}$ | 27 | °C/W | Natural convection |
| | | 21 | | 1 m/s |
| Junction-to-ambient—four-layer board | $R_{\theta JA}$ | 19 | °C/W | Natural convection |
| | | 16 | | 1 m/s |
| Junction-to-board[2] | $R_{\theta JB}$ | 11 | °C/W | — |
| Junction-to-case[3] | $R_{\theta JC}$ | 8 | °C/W | — |
| Junction-to-package top[4] | $R_{\theta JT}$ | 2 | °C/W | — |

1 Assumes no thermal vias
2 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in  C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature (ºC)
$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)
$P_D$ = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

## 4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature (ºC)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

## 4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

## 4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

## 4.7 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see Section 7, “Clock Configuration Modes.”

**Table 8. Estimated Power Dissipation for Various Configurations[1]**

| Bus (MHz) | CPM Multiplication Factor | CPM (MHz) | CPU Multiplication Factor | CPU (MHz) | $P_{INT}$(W)[2,3] | |
|---|---|---|---|---|---|---|
| | | | | | Vddl 1.5 Volts | |
| | | | | | Nominal | Maximum |
| 66.67 | 3 | 200 | 4 | 266 | 1 | 1.2 |
| 100 | 2 | 200 | 3 | 300 | 1.1 | 1.3 |
| 100 | 2 | 200 | 4 | 400 | 1.3 | 1.5 |
| 133 | 2 | 267 | 3 | 400 | 1.5 | 1.8 |

1 Test temperature = 105° C
2 $P_{INT} = I_{DD} \times V_{DD}$ Watts
3 Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:
66.7 MHz = 0.35 W (nominal), 0.4 W (maximum)
83.3 MHz = 0.4 W (nominal), 0.5 W (maximum)
100 MHz = 0.5 W (nominal), 0.6 W (maximum)
133 MHz = 0.7 W (nominal), 0.8 W (maximum)

# 6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100/133 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

**Table 9. Output Buffer Impedances[1]**

| Output Buffers | Typical Impedance (Ω) |
|---|---|
| 60x bus | 45 or 27[2] |
| Memory controller | 45 or 27[2] |
| Parallel I/O | 45 |
| PCI | 27 |

1 These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.
2 Impedance value is selected through SIUMCR[20,21]. See the SoC reference manual.

## 6.1 CPM AC Characteristics

This table lists CPM output characteristics.

**Table 10. AC Characteristics for CPM Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Maximum Delay | | | | Minimum Delay | | | |
| Max | Min | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp36a | sp37a | FCC outputs—internal clock (NMSI) | 6 | 5.5 | 5.5 | 5.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| sp36b | sp37b | FCC outputs—external clock (NMSI) | 8 | 8 | 8 | 8 | 2 | 2 | 2 | 2 |
| sp38a | sp39a | SCC/SMC/SPI/I2C outputs—internal clock (NMSI) | 10 | 10 | 10 | 10 | 0 | 0 | 0 | 0 |
| sp38b | sp39b | SCC/SMC/SPI/I2C outputs—external clock (NMSI) | 8 | 8 | 8 | 8 | 2 | 2 | 2 | 2 |
| sp40 | sp41 | TDM outputs/SI | 11 | 11 | 11 | 11 | 2.5 | 2.5 | 2.5 | 2.5 |
| sp42 | sp43 | TIMER/IDMA outputs | 11 | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 | 0.5 |
| sp42a | sp43a | PIO outputs | 11 | 11 | 11 | 11 | 0.5 | 0.5 | 0.5 | 0.5 |

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This table lists CPM input characteristics.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 11. AC Characteristics for CPM Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Setup | | | | Hold | | | |
| Setup | Hold | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp16a | sp17a | FCC inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp16b | sp17b | FCC inputs—external clock (NMSI) | 2.5 | 2.5 | 2.5 | 2.5 | 2 | 2 | 2 | 2 |
| sp18a | sp19a | SCC/SMC/SPI/I2C inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp18b | sp19b | SCC/SMC/SPI/I2C inputs—external clock (NMSI) | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 2 |
| sp20 | sp21 | TDM inputs/SI | 3 | 3 | 3 | 3 | 2.5 | 2.5 | 2.5 | 2.5 |
| sp22 | sp23 | PIO/TIMER/IDMA inputs | 8 | 8 | 8 | 8 | 0.5 | 0.5 | 0.5 | 0.5 |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

**NOTE**

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

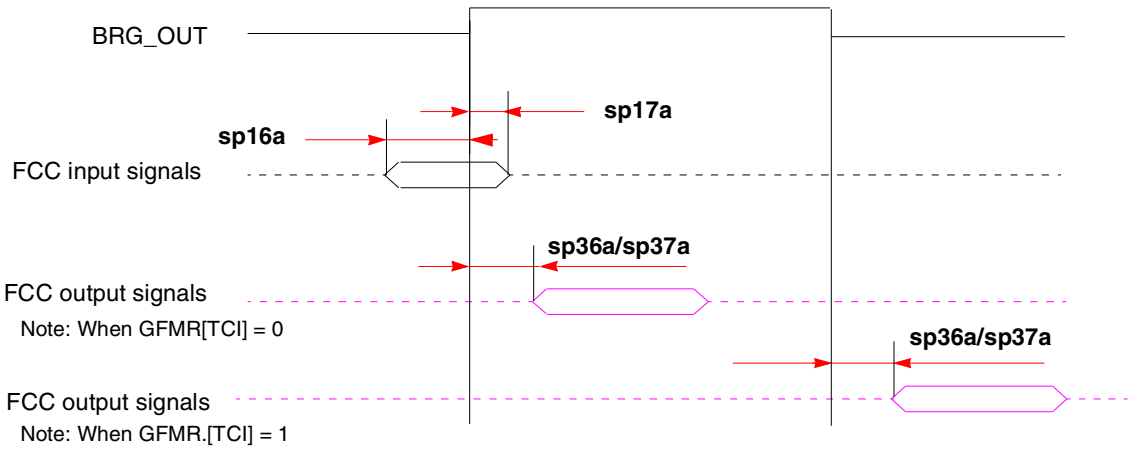



**Figure 3. FCC Internal Clock Diagram**

This figure shows the FCC external clock.

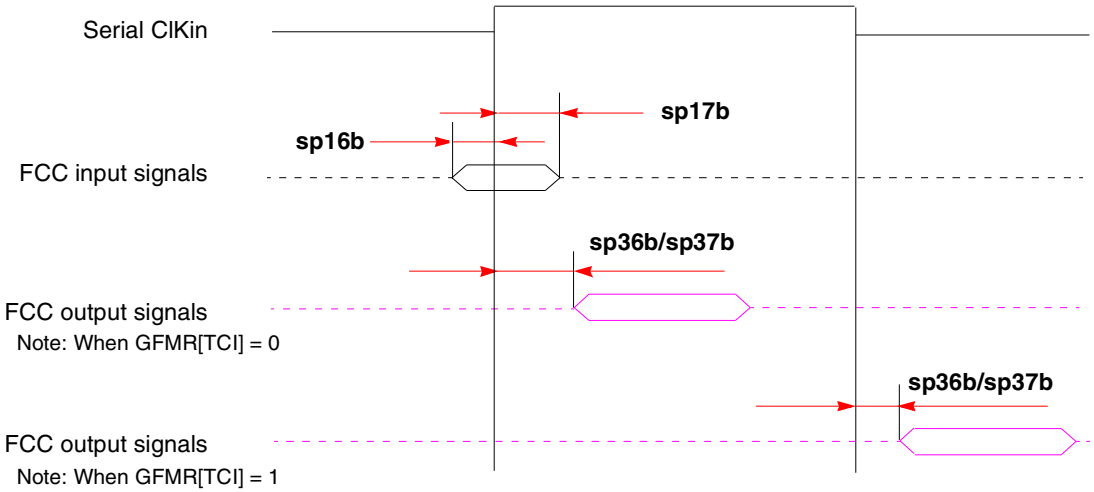
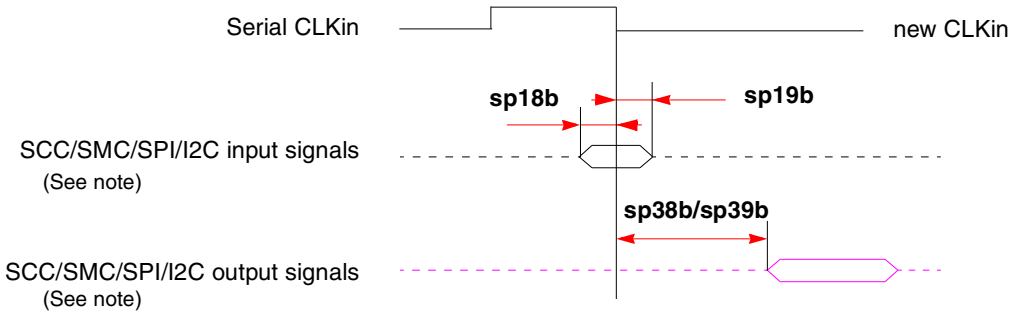



**Figure 4. FCC External Clock Diagram**

This figure shows the SCC/SMC/SPI/$I^2C$ external clock.

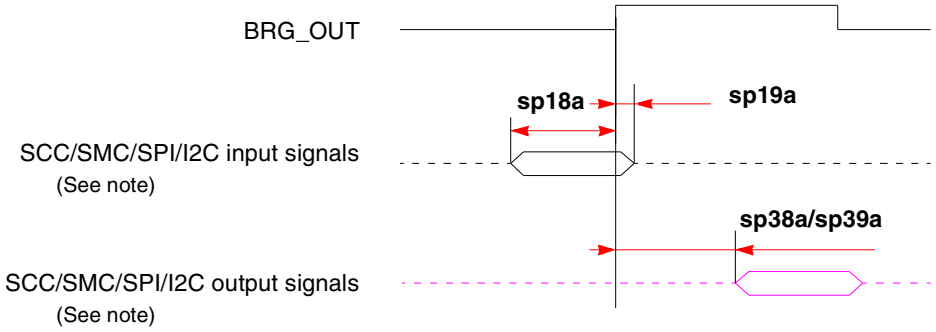



**Note:** There are four possible timing conditions for SPI:
1. Input sampled on the rising edge and output driven on the rising edge.
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge (shown).
4. Input sampled on the falling edge and output driven on the rising edge.

**Note:** There are two possible timing conditions for SCC/SMC/$I^2C$:
1. Input sampled on the falling edge and output driven on the falling edge (shown).
2. Input sampled on the falling edge and output driven on the rising edge.

**Figure 5. SCC/SMC/SPI/$I^2C$ External Clock Diagram**

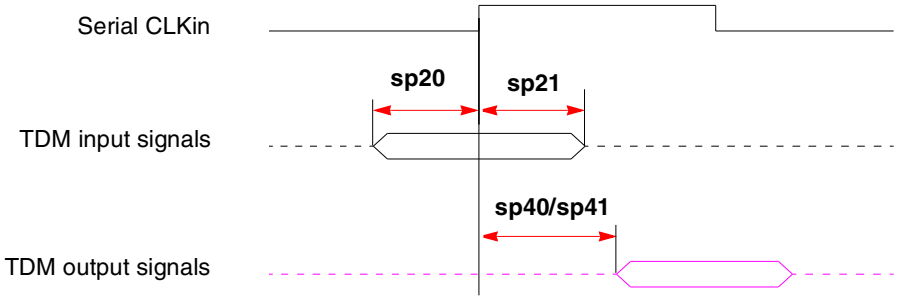
This figure shows the SCC/SMC/SPI/I$^2$C internal clock.




**Note:** There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I$^2$C Internal Clock Diagram**

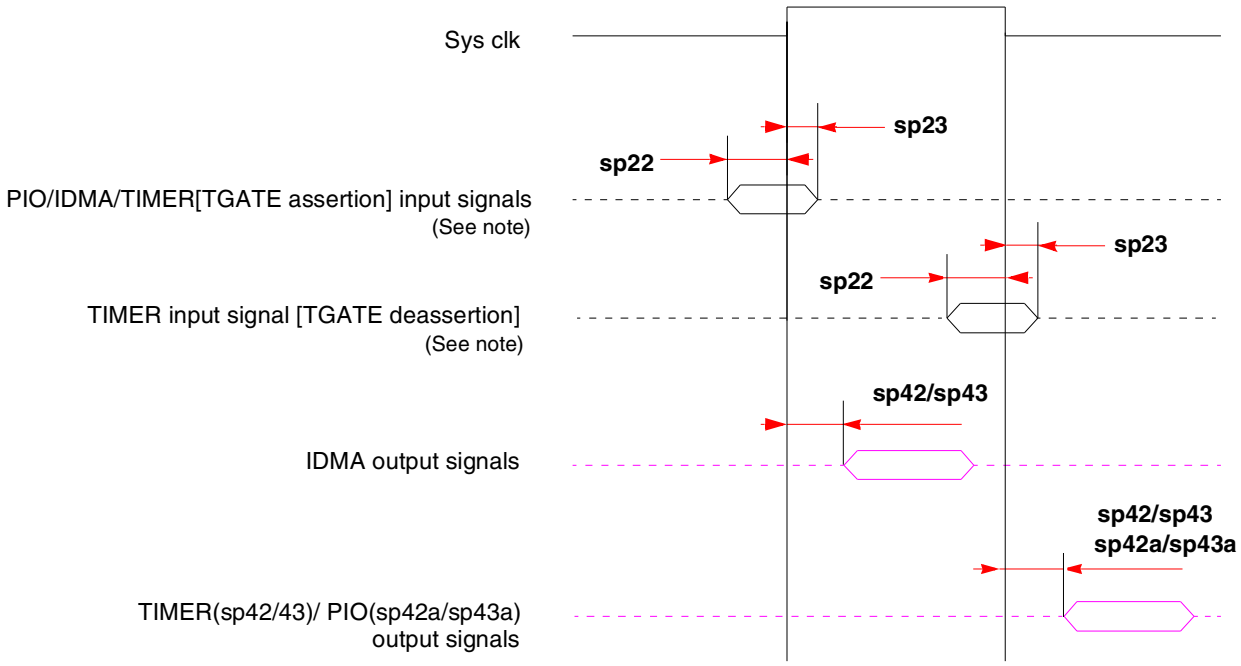
This figure shows TDM input and output signals.




**Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

This figure shows PIO and timer signals.




**Note:** TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

**Figure 8. PIO and Timer Signal Diagram**

## 6.2 SIU AC Characteristics

This table lists SIU input characteristics.

### NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (peak-to-peak) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60.

### NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

### NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

### NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

**Table 12. AC Characteristics for SIU Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Setup | | | | Hold | | | |
| Setup | Hold | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp11 | sp10 | $\overline{\text{AACK}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{ARTRY}}/\overline{\text{TEA}}$ | 6 | 5 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |
| sp12 | sp10 | Data bus in normal mode | 5 | 4 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |
| sp13 | sp10 | Data bus in pipeline mode (without ECC and PARITY) | N/A | 4 | 2.5 | 1.5 | N/A | 0.5 | 0.5 | 0.5 |
| sp15 | sp10 | All other pins | 5 | 4 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

**Table 13. AC Characteristics for SIU Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Maximum Delay | | | | Minimum Delay | | | |
| Max | Min | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp31 | sp30 | $\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ | 7 | 6 | 5.5 | N/A | 1 | 1 | 1 | N/A |
| sp32 | sp30 | ADD/ADD_atr./BADDR/CI/GBL/WT | 8 | 6.5 | 5.5 | 4.5[2] | 1 | 1 | 1 | 1 [2] |
| sp33 | sp30 | Data bus[3] | 6.5 | 6.5 | 5.5 | 4.5 | 0.8 | 0.8 | 0.8 | 1 |
| sp34 | sp30 | Memory controller signals/ALE | 6 | 5.5 | 5.5 | 4.5 | 1 | 1 | 1 | 1 |
| sp35 | sp30 | All other signals | 6 | 5.5 | 5.5 | N/A | 1 | 1 | 1 | N/A |

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2 Value is for ADD only; other sp32/sp30 signals are not applicable.
3 To achieve 1 ns of hold time at 66.67/83.33/100 MHZ, a minimum loading of 20 pF is required.

**NOTE**

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing.

This figure shows the interaction of several bus signals.

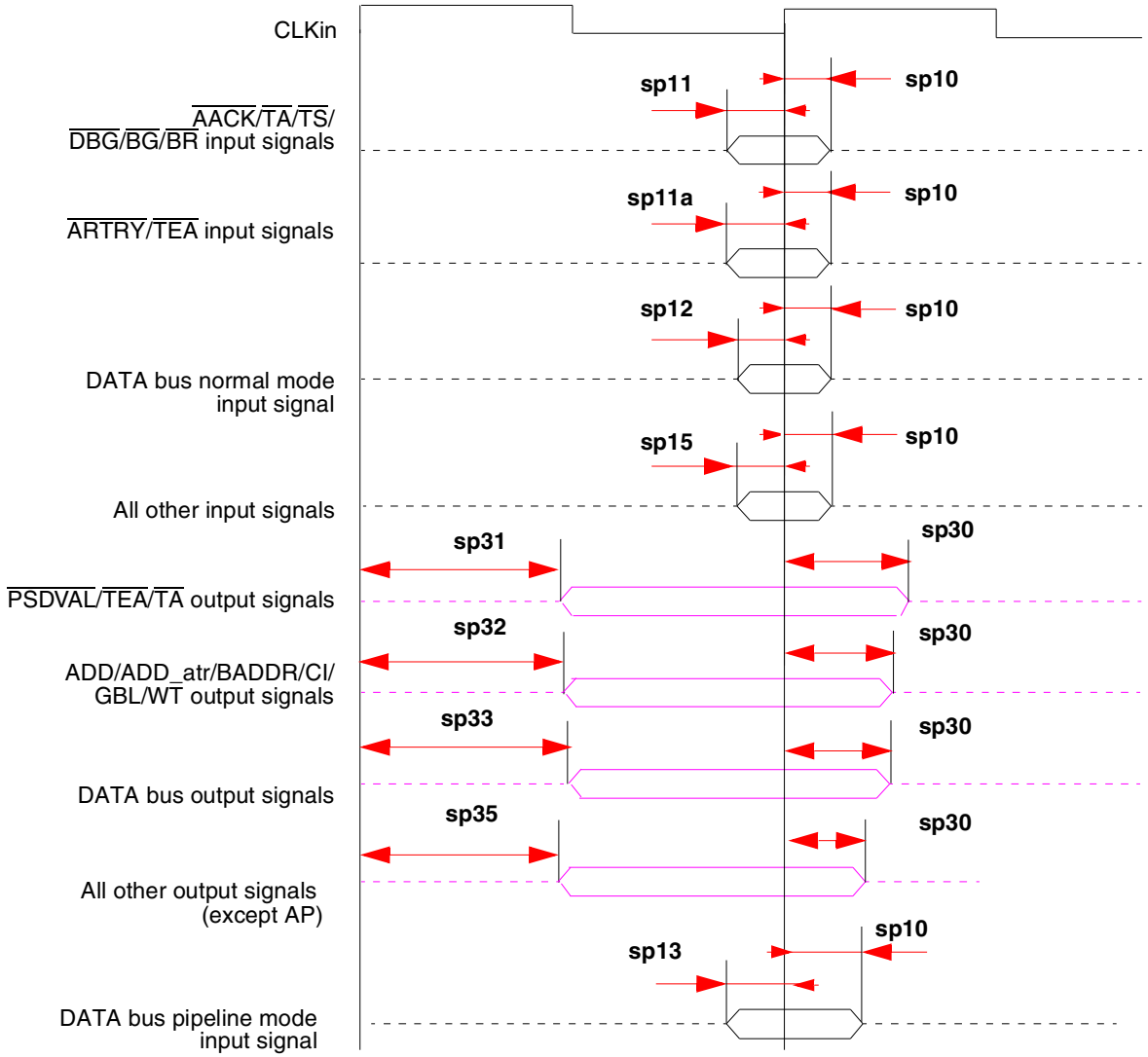



**Figure 9. Bus Signals**

This figure shows signal behavior in MEMC mode.

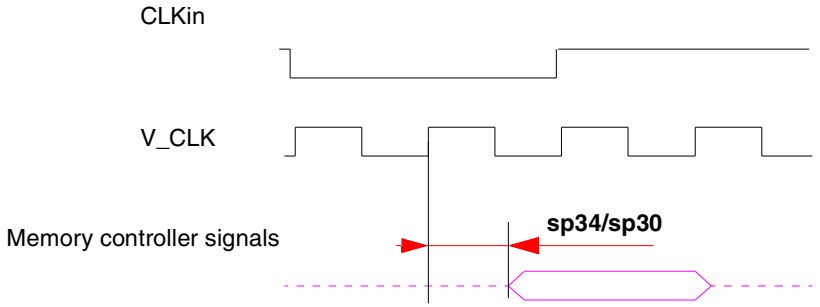



**Figure 10. MEMC Mode Diagram**

**NOTE**

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 14.

**Table 14. Tick Spacing for Memory Controller Signals**

| PLL Clock Ratio | Tick Spacing (T1 Occurs at the Rising Edge of CLKin) | | |
|---|---|---|---|
| | T2 | T3 | T4 |
| 1:2, 1:3, 1:4, 1:5, 1:6 | 1/4 CLKin | 1/2 CLKin | 3/4 CLKin |
| 1:2.5 | 3/10 CLKin | 1/2 CLKin | 8/10 CLKin |
| 1:3.5 | 4/14 CLKin | 1/2 CLKin | 11/14 CLKin |

This table is a representation of the information in Table 14.

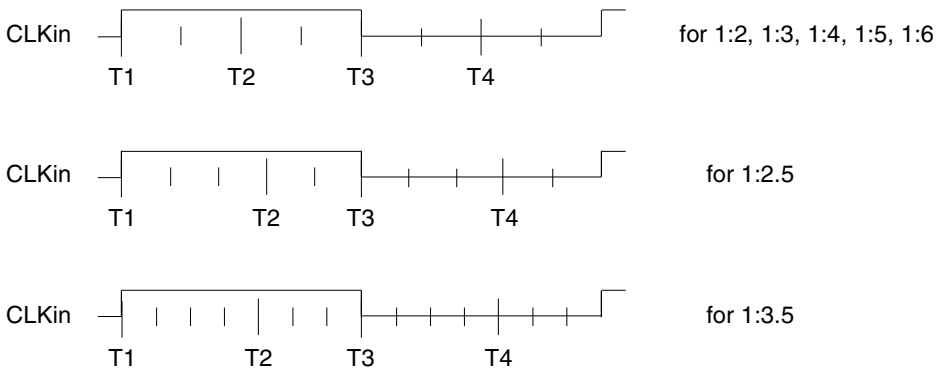



**Figure 11. Internal Tick Spacing for Memory Controller Signals**

**NOTE**

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

## 6.3 JTAG Timings

This table lists the JTAG timings.

**Table 15. JTAG Timings[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ and $t_{JTGF}$ | 0 | 5 | ns | 6 |
| TRST assert time | $t_{TRST}$ | 25 | — | ns | 3, 6 |
| Input setup times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |
| Input hold times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |
| Output valid times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>—<br>— | <br>10<br>10 | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| Output hold times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>1<br>1 | <br>—<br>— | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| JTAG external clock to output high impedance<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>1<br>1 | <br>10<br>10 | <br>ns<br>ns | <br>5, 6<br>5, 6 |

1 All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to $t_{TCLK}$.

5 Non-JTAG signal output timing with respect to $t_{TCLK}$.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

# 7 Clock Configuration Modes

As shown in this table, the clocking mode is set according to two sources:

- PCI_CFG[0]— An input signal. Also defined as "PCI_HOST_EN." See Chapter 6, "External Signals," and Chapter 9, "PCI Bridge," in the SoC reference manual.
- PCI_MODCK—Bit 27 in the Hard Reset Configuration Word. See Chapter 5, "Reset," in the SoC reference manual.

**Table 16. SoC Clocking Modes**

| Pins | | Clocking Mode | PCI Clock Frequency Range (MHz) | Reference |
|---|---|---|---|---|
| PCI_CFG[0][1] | PCI_MODCK[2] | | | |
| 0 | 0 | PCI host | 50–66 | Table 17 |
| 0 | 1 | | 25–50 | Table 18 |
| 1 | 0 | PCI agent | 50–66 | Table 19 |
| 1 | 1 | | 25–50 | Table 20 |

1 PCI_HOST_EN
2 Determines PCI clock frequency range.

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

**NOTE**

Clock configurations change only after PORESET is asserted.

**NOTE: Tval (Output Hold)**

The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

## 7.1 PCI Host Mode

These tables show configurations for PCI host mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI host mode the input clock is the bus clock.

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| Default Modes (MODCK_H=0000) | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 3 | 50.0 | 66.7 |
| 0000_100 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 3 | 50.0 | 66.7 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_110 | 50.0 | 66.7 | 3.5 | 150.0 | 200.0 | 3.5 | 175.0 | 233.3 | 3 | 50.0 | 66.7 |
| 0000_111 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| Full Configuration Modes | | | | | | | | | | | |
| 0001_000 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 5 | 250.0 | 333.3 | 3 | 50.0 | 66.7 |
| 0001_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 6 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| 0001_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 7 | 350.0 | 466.6 | 3 | 50.0 | 66.7 |
| 0001_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 8 | 400.0 | 533.3 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0010_000 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 5 | 250.0 | 333.3 | 4 | 50.0 | 66.7 |
| 0010_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 6 | 300.0 | 400.0 | 4 | 50.0 | 66.7 |
| 0010_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 7 | 350.0 | 466.6 | 4 | 50.0 | 66.7 |
| 0010_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 8 | 400.0 | 533.3 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0010_100 | 75.0 | 100.0 | 4 | 300.0 | 400.0 | 5 | 375.0 | 500.0 | 6 | 50.0 | 66.7 |
| 0010_101 | 75.0 | 100.0 | 4 | 300.0 | 400.0 | 5.5 | 412.5 | 549.9 | 6 | 50.0 | 66.7 |
| 0010_110 | 75.0 | 100.0 | 4 | 300.0 | 400.0 | 6 | 450.0 | 599.9 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0011_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 250.0 | 333.3 | 5 | 50.0 | 66.7 |
| 0011_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 6 | 300.0 | 400.0 | 5 | 50.0 | 66.7 |
| 0011_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 7 | 350.0 | 466.6 | 5 | 50.0 | 66.7 |
| 0011_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 8 | 400.0 | 533.3 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 6 | 300.0 | 400.0 | 6 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 7 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 8 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0101_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0101_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3.5 | 175.0 | 233.3 | 2 | 50.0 | 66.7 |
| 0101_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4 | 200.0 | 266.6 | 2 | 50.0 | 66.7 |
| 0101_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4.5 | 225.0 | 300.0 | 2 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_101 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 3.5 | 291.7 | 388.9 | 5 | 50.0 | 66.7 |
| 0101_110 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 5 | 50.0 | 66.7 |
| 0101_111 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 2.5 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0110_001 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 3 | 50.0 | 66.7 |
| 0110_010 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 3 | 50.0 | 66.7 |
| 0110_011 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 3 | 50.0 | 66.7 |
| 0110_100 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 3 | 50.0 | 66.7 |
| 0110_101 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 5 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| 0110_110 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 6 | 360.0 | 480.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 233.3 | 3 | 50.0 | 66.7 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0111_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 4 | 50.0 | 66.7 |
| 1000_011 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 4 | 50.0 | 66.7 |
| 1000_100 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 4 | 50.0 | 66.7 |
| 1000_101 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 6 | 400.0 | 533.3 | 4 | 50.0 | 66.7 |
| 1000_110 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 6.5 | 433.3 | 577.7 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 3.5 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_011 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 4 | 228.6 | 304.7 | 4 | 50.0 | 66.7 |
| 1001_100 | 57.1 | 76.2 | 3.5 | 200.0 | 266.6 | 4.5 | 257.1 | 342.8 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1001_101 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 5 | 428.6 | 571.4 | 6 | 50.0 | 66.7 |
| 1001_110 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 5.5 | 471.4 | 628.5 | 6 | 50.0 | 66.7 |
| 1001_111 | 85.7 | 114.3 | 3.5 | 300.0 | 400.0 | 6 | 514.3 | 685.6 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 2 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 1010_001 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 2.5 | 187.5 | 250.0 | 3 | 50.0 | 66.7 |
| 1010_010 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 3 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| 1010_011 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 3.5 | 262.5 | 350.0 | 3 | 50.0 | 66.7 |
| 1010_100 | 75.0 | 100.0 | 2 | 150.0 | 200.0 | 4 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 133.3 | 2 | 200.0 | 266.6 | 2.5 | 250.0 | 333.3 | 4 | 50.0 | 66.7 |
| 1010_110 | 100.0 | 133.3 | 2 | 200.0 | 266.6 | 3 | 300.0 | 400.0 | 4 | 50.0 | 66.7 |
| 1010_111 | 100.0 | 133.3 | 2 | 200.0 | 266.6 | 3.5 | 350.0 | 466.6 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1011_010 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 4 | 50.0 | 66.7 |
| 1011_011 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 4 | 50.0 | 66.7 |

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1011_100 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 4 | 50.0 | 66.7 |
| 1011_101 | 80.0 | 106.7 | 2.5 | 200.0 | 266.6 | 4.5 | 360.0 | 480.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1101_000 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 3 | 300.0 | 400.0 | 5 | 50.0 | 66.7 |
| 1101_001 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 3.5 | 350.0 | 466.6 | 5 | 50.0 | 66.7 |
| 1101_010 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 4 | 400.0 | 533.3 | 5 | 50.0 | 66.7 |
| 1101_011 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 4.5 | 450.0 | 599.9 | 5 | 50.0 | 66.7 |
| 1101_100 | 100.0 | 133.3 | 2.5 | 250.0 | 333.3 | 5 | 500.0 | 666.6 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1101_101 | 125.0 | 166.7 | 2 | 250.0 | 333.3 | 3 | 375.0 | 500.0 | 5 | 50.0 | 66.7 |
| 1101_110 | 125.0 | 166.7 | 2 | 250.0 | 333.3 | 4 | 500.0 | 666.6 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1110_000 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 3.5 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 1110_001 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 4 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| 1110_010 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 4.5 | 450.0 | 599.9 | 6 | 50.0 | 66.7 |
| 1110_011 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 5 | 500.0 | 666.6 | 6 | 50.0 | 66.7 |
| 1110_100 | 100.0 | 133.3 | 3 | 300.0 | 400.0 | 5.5 | 550.0 | 733.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. SeeTable 18 for lower range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 0, the ratio of CPM_CLK/PCI_CLK should be calculated from SCCR[PCIDF] as follows:
CPM_CLK/PCI_CLK = (PCIDF + 1) / 2.

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2]**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| Default Modes (MODCK_H=0000) | | | | | | | | | | | |
| 0000_000 | 60.0 | 100.0 | 2 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0000_001 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0000_010 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 6 | 25.0 | 50.0 |
| 0000_011 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 6 | 25.0 | 50.0 |
| 0000_100 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 6 | 25.0 | 50.0 |
| 0000_101 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0000_110 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0000_111 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| Full Configuration Modes | | | | | | | | | | | |
| 0001_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 0001_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 6 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| 0001_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 7 | 350.0 | 700.0 | 6 | 25.0 | 50.0 |
| 0001_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 8 | 400.0 | 800.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_000 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 0010_001 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 6 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 0010_010 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 7 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| 0010_011 | 50.0 | 100.0 | 4 | 200.0 | 400.0 | 8 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_100 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 0010_101 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 5.5 | 206.3 | 412.5 | 6 | 25.0 | 50.0 |
| 0010_110 | 37.5 | 75.0 | 4 | 150.0 | 300.0 | 6 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0011_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 5 | 150.0 | 250.0 | 5 | 30.0 | 50.0 |
| 0011_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 6 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |
| 0011_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 7 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 0011_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 8 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 6 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0100_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 7 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0100_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 8 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 100.0 | 2 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0101_001 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0101_010 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3.5 | 175.0 | 350.0 | 4 | 25.0 | 50.0 |
| 0101_011 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 4 | 200.0 | 400.0 | 4 | 25.0 | 50.0 |
| 0101_100 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 4.5 | 225.0 | 450.0 | 4 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0101_101 | 42.9 | 83.3 | 3 | 128.6 | 250.0 | 3.5 | 150.0 | 291.7 | 5 | 25.7 | 50.0 |
| 0101_110 | 41.7 | 83.3 | 3 | 125.0 | 250.0 | 4 | 166.7 | 333.3 | 5 | 25.0 | 50.0 |
| 0101_111 | 41.7 | 83.3 | 3 | 125.0 | 250.0 | 4.5 | 187.5 | 375.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0110_001 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 6 | 25.0 | 50.0 |
| 0110_010 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 6 | 25.0 | 50.0 |
| 0110_011 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 6 | 25.0 | 50.0 |
| 0110_100 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 6 | 25.0 | 50.0 |
| 0110_101 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 5 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| 0110_110 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 6 | 360.0 | 720.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0111_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0111_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| 0111_100 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 1010_110 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1010_111 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1011_101 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4.5 | 360.0 | 720.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_000 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |
| 1101_001 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 1101_010 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| 1101_011 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 5 | 25.0 | 50.0 |
| 1101_100 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_101 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 3 | 187.5 | 375.0 | 5 | 25.0 | 50.0 |
| 1101_110 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 4 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 1110_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| 1110_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1110_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 1110_100 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5.5 | 275.0 | 550.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 17 for higher range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

## 7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0000_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0000_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_001 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 5 | 150.0 | 166.7 | 4 | 30.0 | 33.3 |
| 0001_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 6 | 150.0 | 200.0 | 4 | 25.0 | 33.3 |
| 0001_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 7 | 175.0 | 233.3 | 4 | 25.0 | 33.3 |
| 0001_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 8 | 200.0 | 266.6 | 4 | 25.0 | 33.3 |
| | | | | | | | | | | | |
| 0010_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0010_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0010_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 0010_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0011_000 | Reserved | | | | | | | | | | |
| 0011_001 | Reserved | | | | | | | | | | |
| 0011_010 | Reserved | | | | | | | | | | |
| 0011_011 | Reserved | | | | | | | | | | |
| 0011_100 | Reserved | | | | | | | | | | |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0100_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 250.0 | 333.3 | 2.5 | 100.0 | 133.3 |
| 0101_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 300.0 | 400.0 | 2.5 | 100.0 | 133.3 |
| 0101_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 350.0 | 466.6 | 2.5 | 100.0 | 133.3 |
| 0101_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 400.0 | 533.3 | 2.5 | 100.0 | 133.3 |
| 0101_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 450.0 | 599.9 | 2.5 | 100.0 | 133.3 |
| 0101_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 500.0 | 666.6 | 2.5 | 100.0 | 133.3 |
| 0101_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 550.0 | 733.3 | 2.5 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 0110_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0110_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 0110_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 0111_000 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2 | 150.0 | 200.0 | 2 | 75.0 | 100.0 |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 187.5 | 250.0 | 2 | 75.0 | 100.0 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 225.0 | 300.0 | 2 | 75.0 | 100.0 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 262.5 | 350.0 | 2 | 75.0 | 100.0 |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 150.0 | 166.7 | 2.5 | 60.0 | 80.0 |
| 1000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 1000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 1000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 1000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 225.0 | 300.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 1010_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 1010_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 1010_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 2.5 | 80.0 | 106.7 |
| 1011_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| 1011_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 2.5 | 80.0 | 106.7 |
| 1011_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 2.5 | 80.0 | 106.7 |
| | | | | | | | | | | | |
| 1011_101 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 250.0 | 333.3 | 2 | 100.0 | 133.3 |
| 1011_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 300.0 | 400.0 | 2 | 100.0 | 133.3 |
| 1011_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 350.0 | 466.6 | 2 | 100.0 | 133.3 |
| | | | | | | | | | | | |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1100_101 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 400.0 | 533.3 | 3 | 100.0 | 133.3 |
| 1100_110 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 450.0 | 599.9 | 3 | 100.0 | 133.3 |
| 1100_111 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 500.0 | 666.6 | 3 | 100.0 | 133.3 |
| 1101_000 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5.5 | 550.0 | 733.3 | 3 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 1101_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 3.5 | 420.0 | 559.9 | 2.5 | 120.0 | 160.0 |
| 1101_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 480.0 | 639.9 | 2.5 | 120.0 | 160.0 |
| 1101_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 540.0 | 719.9 | 2.5 | 120.0 | 160.0 |
| 1101_100 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 600.0 | 799.9 | 2.5 | 120.0 | 160.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 312.5 | 416.6 | 2 | 125.0 | 166.7 |
| 1110_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 375.0 | 500.0 | 2 | 125.0 | 166.7 |
| 1110_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 437.5 | 583.3 | 2 | 125.0 | 166.7 |
| 1110_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 500.0 | 666.6 | 2 | 125.0 | 166.7 |
| | | | | | | | | | | | |
| 1110_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 3 | 83.3 | 111.1 |
| 1110_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 3 | 83.3 | 111.1 |
| 1110_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 416.7 | 555.5 | 3 | 83.3 | 111.1 |
| 1110_111 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 458.3 | 611.1 | 3 | 83.3 | 111.1 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| Default Modes (MODCK_H=0000) | | | | | | | | | | | |
| 0000_000 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 2 | 60.0 | 100.0 |
| 0000_001 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 2 | 50.0 | 100.0 |
| 0000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 0000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0000_110 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0000_111 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 2.5 | 80.0 | 160.0 |
| Full Configuration Modes | | | | | | | | | | | |
| 0001_001 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0001_010 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 6 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0001_011 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 7 | 175.0 | 350.0 | 4 | 25.0 | 50.0 |
| 0001_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 8 | 200.0 | 400.0 | 4 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0010_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0010_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 0010_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 0011_000 | Reserved | | | | | | | | | | |
| 0011_001 | 37.5 | 50.0 | 4 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0011_010 | 32.1 | 50.0 | 4 | 128.6 | 200.0 | 3.5 | 150.0 | 233.3 | 3 | 42.9 | 66.7 |
| 0011_011 | 28.1 | 50.0 | 4 | 112.5 | 200.0 | 4 | 150.0 | 266.7 | 3 | 37.5 | 66.7 |
| 0011_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 4.5 | 150.0 | 300.0 | 3 | 33.3 | 66.7 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0100_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 3 | 50.0 | 100.0 |
| 0100_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0101_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 2.5 | 150.0 | 250.0 | 2.5 | 60.0 | 100.0 |
| 0101_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 2.5 | 50.0 | 100.0 |
| 0101_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 2.5 | 50.0 | 100.0 |
| 0101_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 2.5 | 50.0 | 100.0 |
| 0101_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 2.5 | 50.0 | 100.0 |
| 0101_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 2.5 | 50.0 | 100.0 |
| 0101_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 275.0 | 550.0 | 2.5 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 0110_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0110_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 0110_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 0111_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 2 | 75.0 | 150.0 |
| 0111_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 2 | 75.0 | 150.0 |
| 0111_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 2 | 75.0 | 150.0 |
| 0111_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 2 | 75.0 | 150.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 2.5 | 60.0 | 120.0 |
| 1000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 1000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 200.0 | 400.0 | 4 | 50.0 | 100.0 |
| 1001_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 225.0 | 450.0 | 4 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 1010_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 1010_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 1010_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 2.5 | 80.0 | 160.0 |
| 1011_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 2.5 | 80.0 | 160.0 |
| 1011_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 2.5 | 80.0 | 160.0 |
| 1011_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 2.5 | 80.0 | 160.0 |
| | | | | | | | | | | | |
| 1011_101 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 2 | 100.0 | 200.0 |
| 1011_110 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 2 | 100.0 | 200.0 |
| 1011_111 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 2 | 100.0 | 200.0 |
| | | | | | | | | | | | |
| 1100_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 1100_110 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| 1100_111 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 3 | 50.0 | 100.0 |
| 1101_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5.5 | 275.0 | 550.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 1101_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1101_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1101_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| 1101_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5 | 300.0 | 600.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1110_000 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 2.5 | 156.3 | 312.5 | 2 | 62.5 | 125.0 |
| 1110_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 187.5 | 375.0 | 2 | 62.5 | 125.0 |
| 1110_010 | 28.6 | 50.0 | 5 | 142.9 | 250.0 | 3.5 | 250.0 | 437.5 | 2 | 71.4 | 125.0 |
| 1110_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 250.0 | 500.0 | 2 | 62.5 | 125.0 |
| | | | | | | | | | | | |
| 1110_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 166.7 | 333.3 | 3 | 41.7 | 83.3 |
| 1110_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 187.5 | 375.0 | 3 | 41.7 | 83.3 |
| 1110_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 208.3 | 416.7 | 3 | 41.7 | 83.3 |
| 1110_111 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 229.2 | 458.3 | 3 | 41.7 | 83.3 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 19 for higher range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

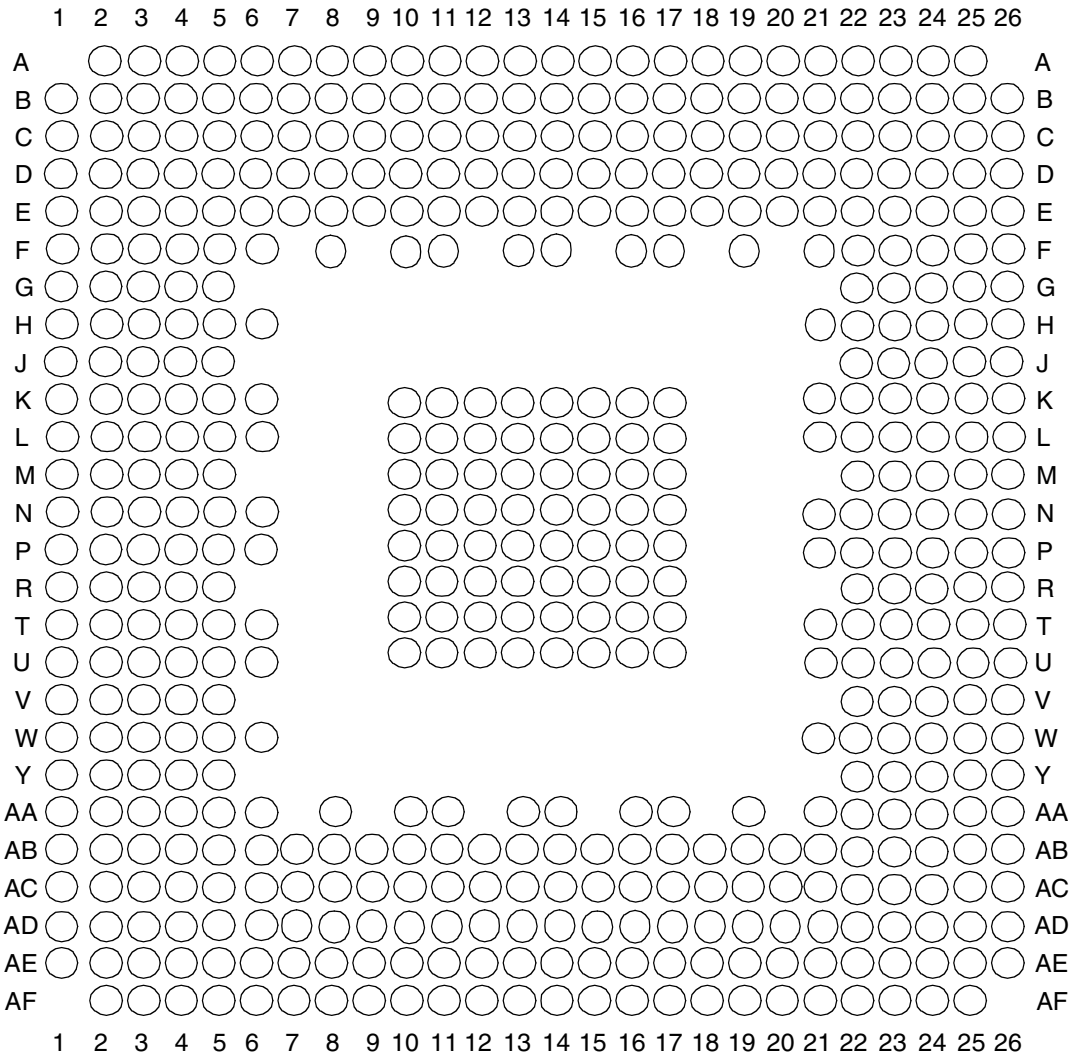
4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

# 8 Pinout

This figure and table show the pin assignments and pinout for the 516 PBGA package.

This figure shows the pinout of the 516 PBGA package as viewed from the top surface.




Not to Scale

**Figure 12. Pinout of the 516 PBGA Package (View from Top)**

This table lists the pins of the MPC8272. Note that the pins in the “MPC8272/8271 Only” column relate to Utopia functionality.

**Table 21. Pinout**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{BR}$ | | A19 |
| $\overline{BG}$/$\overline{IRQ6}$ | | D2 |
| $\overline{ABB}$/$\overline{IRQ2}$ | | C1 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{TS}$ | | D1 |
| A0 | | A3 |
| A1 | | B5 |
| A2 | | D8 |
| A3 | | C6 |
| A4 | | A4 |
| A5 | | A6 |
| A6 | | B6 |
| A7 | | C7 |
| A8 | | B7 |
| A9 | | A7 |
| A10 | | D9 |
| A11 | | E11 |
| A12 | | C9 |
| A13 | | B9 |
| A14 | | D11 |
| A15 | | A9 |
| A16 | | B10 |
| A17 | | A10 |
| A18 | | B11 |
| A19 | | A11 |
| A20 | | D12 |
| A21 | | A12 |
| A22 | | D13 |
| A23 | | B13 |
| A24 | | C13 |
| A25 | | C14 |
| A26 | | B14 |
| A27 | | D14 |
| A28 | | E14 |
| A29 | | A14 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| A30 | | B15 |
| A31 | | A15 |
| TT0 | | B3 |
| TT1 | | E8 |
| TT2 | | D7 |
| TT3 | | C4 |
| TT4 | | E7 |
| $\overline{\text{TBST}}$ | | E3 |
| TSIZ0 | | E4 |
| TSIZ1 | | E5 |
| TSIZ2 | | C3 |
| TSIZ3 | | D5 |
| $\overline{\text{AACK}}$ | | D3 |
| $\overline{\text{ARTRY}}$ | | C2 |
| $\overline{\text{DBG}}$/$\overline{\text{IRQ7}}$ | | F16 |
| $\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$ | | D18 |
| D0 | | AC1 |
| D1 | | AA1 |
| D2 | | V3 |
| D3 | | R5 |
| D4 | | P4 |
| D5 | | M4 |
| D6 | | J4 |
| D7 | | G1 |
| D8 | | W6 |
| D9 | | Y3 |
| D10 | | V1 |
| D11 | | N6 |
| D12 | | P3 |
| D13 | | M2 |
| D14 | | J5 |

Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| D15 | | G3 |
| D16 | | AB3 |
| D17 | | Y1 |
| D18 | | T4 |
| D19 | | T3 |
| D20 | | P2 |
| D21 | | M1 |
| D22 | | J1 |
| D23 | | G4 |
| D24 | | AB2 |
| D25 | | W4 |
| D26 | | V2 |
| D27 | | T1 |
| D28 | | N5 |
| D29 | | L1 |
| D30 | | H1 |
| D31 | | G5 |
| D32 | | W5 |
| D33 | | W2 |
| D34 | | T5 |
| D35 | | T2 |
| D36 | | N1 |
| D37 | | K3 |
| D38 | | H2 |
| D39 | | F1 |
| D40 | | AA2 |
| D41 | | W1 |
| D42 | | U3 |
| D43 | | R2 |
| D44 | | N2 |
| D45 | | L2 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| D46 | | H4 |
| D47 | | F2 |
| D48 | | AB1 |
| D49 | | U4 |
| D50 | | U1 |
| D51 | | R3 |
| D52 | | N3 |
| D53 | | K2 |
| D54 | | H5 |
| D55 | | F4 |
| D56 | | AA3 |
| D57 | | U5 |
| D58 | | U2 |
| D59 | | P5 |
| D60 | | M3 |
| D61 | | K4 |
| D62 | | H3 |
| D63 | | E1 |
| $\overline{\text{IRQ3}}$/CKSTP_OUT/EXT_BR3 | | B16 |
| $\overline{\text{IRQ4}}$/CORE_SRESET/EXT_BG3 | | C15 |
| $\overline{\text{IRQ5}}$/TBEN/EXT_DBG3/$\overline{\text{CINT}}$ | | Y4 |
| $\overline{\text{PSDVAL}}$ | | C19 |
| $\overline{\text{TA}}$ | | AA4 |
| $\overline{\text{TEA}}$ | | AB6 |
| $\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$ | | D15 |
| $\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$ | | D16 |
| $\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$ | | C16 |
| BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$ | | E17 |
| $\overline{\text{CPU_BR}}$/$\overline{\text{INT_OUT}}$ | | B20 |
| $\overline{\text{CS0}}$ | | AE6 |
| $\overline{\text{CS1}}$ | | AD7 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{\text{CS2}}$ | | AF5 |
| $\overline{\text{CS3}}$ | | AC8 |
| $\overline{\text{CS4}}$ | | AF6 |
| $\overline{\text{CS5}}$ | | AD8 |
| $\overline{\text{CS6}}$/$\overline{\text{BCTL1}}$/$\overline{\text{SMI}}$ | | AC9 |
| $\overline{\text{CS7}}$/TLBISYNC | | AB9 |
| BADDR27/$\overline{\text{IRQ1}}$ | | AB8 |
| BADDR28/$\overline{\text{IRQ2}}$ | | AC7 |
| ALE/$\overline{\text{IRQ4}}$ | | AF4 |
| $\overline{\text{BCTL0}}$ | | AF3 |
| $\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$ | | AD6 |
| $\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$ | | AE5 |
| $\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$ | | AE3 |
| $\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$ | | AF2 |
| $\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$ | | AC6 |
| $\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$ | | AC5 |
| $\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$ | | AD4 |
| $\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$ | | AB5 |
| PSDA10/PGPL0 | | AE2 |
| $\overline{\text{PSDWE}}$/PGPL1 | | AD3 |
| $\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2 | | AB4 |
| $\overline{\text{PSDCAS}}$/PGPL3 | | AC3 |
| $\overline{\text{PGTA}}$/PUPMWAIT/PGPL4 | | AD2 |
| PSDAMUX/PGPL5 | | AC2 |
| $\overline{\text{PCI_MODE}}$[1] | | AD22 |
| PCI_CFG0 ($\overline{\text{PCI_HOST_EN}}$) | | AC21 |
| PCI_CFG1 ($\overline{\text{PCI_ARB_EN}}$) | | AE22 |
| PCI_CFG2 (DLL_ENABLE) | | AE23 |
| PCI_ PAR | | AF12 |
| $\overline{\text{PCI_FRAME}}$ | | AD15 |
| $\overline{\text{PCI_TRDY}}$ | | AF16 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{\text{PCI_IRDY}}$ | | AF15 |
| $\overline{\text{PCI_STOP}}$ | | AE15 |
| $\overline{\text{PCI_DEVSEL}}$ | | AE14 |
| PCI_IDSEL | | AC17 |
| $\overline{\text{PCI_PERR}}$ | | AD14 |
| $\overline{\text{PCI_SERR}}$ | | AD13 |
| $\overline{\text{PCI_REQ0}}$ | | AE20 |
| $\overline{\text{PCI_REQ1}}$/CPCI_HS_ES | | AF14 |
| $\overline{\text{PCI_GNT0}}$ | | AD20 |
| $\overline{\text{PCI_GNT1}}$/CPCI_HS_LED | | AE13 |
| $\overline{\text{PCI_GNT2}}$/$\overline{\text{CPCI_HS_ENUM}}$ | | AF21 |
| $\overline{\text{PCI_RST}}$ | | AF22 |
| $\overline{\text{PCI_INTA}}$ | | AE21 |
| $\overline{\text{PCI_REQ2}}$ | | AB14 |
| DLLOUT | | AC22 |
| PCI_AD0 | | AF7 |
| PCI_AD1 | | AE10 |
| PCI_AD2 | | AB10 |
| PCI_AD3 | | AD10 |
| PCI_AD4 | | AE9 |
| PCI_AD5 | | AF8 |
| PCI_AD6 | | AC10 |
| PCI_AD7 | | AE11 |
| PCI_AD8 | | AB11 |
| PCI_AD9 | | AF10 |
| PCI_AD10 | | AF9 |
| PCI_AD11 | | AB12 |
| PCI_AD12 | | AC12 |
| PCI_AD13 | | AD12 |
| PCI_AD14 | | AF11 |
| PCI_AD15 | | AB13 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| PCI_AD16 | | AE16 |
| PCI_AD17 | | AF17 |
| PCI_AD18 | | AD16 |
| PCI_AD19 | | AC16 |
| PCI_AD20 | | AF18 |
| PCI_AD21 | | AB16 |
| PCI_AD22 | | AD17 |
| PCI_AD23 | | AF19 |
| PCI_AD24 | | AB17 |
| PCI_AD25 | | AF20 |
| PCI_AD26 | | AE19 |
| PCI_AD27 | | AC18 |
| PCI_AD28 | | AB18 |
| PCI_AD29 | | AD19 |
| PCI_AD30 | | AD21 |
| PCI_AD31 | | AC20 |
| $\overline{\text{PCI_C0}}/\overline{\text{BE0}}$ | | AE12 |
| $\overline{\text{PCI_C1}}/\overline{\text{BE1}}$ | | AF13 |
| $\overline{\text{PCI_C2}}/\overline{\text{BE2}}$ | | AC15 |
| $\overline{\text{PCI_C3}}/\overline{\text{BE3}}$ | | AE18 |
| $\overline{\text{IRQ0}}/\overline{\text{NMI_OUT}}$ | | A17 |
| $\overline{\text{TRST}}$[2] | | E21 |
| TCK | | B22 |
| TMS | | C23 |
| TDI | | B24 |
| TDO | | A22 |
| $\overline{\text{TRIS}}$ | | B23 |
| $\overline{\text{PORESET}}$[2]/$\overline{\text{PCI_RST}}$ | | C24 |
| $\overline{\text{HRESET}}$ | | D22 |
| $\overline{\text{SRESET}}$ | | F22 |
| $\overline{\text{RSTCONF}}$ | | A24 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| MODCK1/$\overline{\text{RSRV}}$/TC0/BNKSEL0 | | A20 |
| MODCK2/CSE0/TC1/BNKSEL1 | | C20 |
| MODCK3/CSE1/TC2/BNKSEL2 | | A21 |
| CLKIN1 | | D21 |
| PA8/SMRXD2 | | AF25[3] |
| PA9/SMTXD2 | | AA22[3] |
| PA10/MSNUM5 | FCC1_UT_RXD0 | AB23[3] |
| PA11/MSNUM4 | FCC1_UT_RXD1 | AD26[3] |
| PA12/MSNUM3 | FCC1_UT_RXD2 | AD25[3] |
| PA13/MSNUM2 | FCC1_UT_RXD3 | AA24[3] |
| PA14/FCC1_MII_HDLC_RXD3 | FCC1_UT_RXD4 | W22[3] |
| PA15/FCC1_MII_HDLC_RXD2 | FCC1_UT_RXD5 | Y24[3] |
| PA16/FCC1_MII_HDLC_RXD1 | FCC1_UT_RXD6 | T22[3] |
| PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/FCC1_RMII_RXD0 | FCC1_UT_RXD7 | W26[3] |
| PA18/FCC1_MII_HDLC_TXD0/FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0 | FCC1_UT_TXD7 | V26[3] |
| PA19/FCC1_MII_HDLC_TXD1/FCC1_RMII_TXD1 | FCC1_UT_TXD6 | R23[3] |
| PA20/FCC1_MII_HDLC_TXD2 | FCC1_UT_TXD5 | P25[3] |
| PA21/FCC1_MII_HDLC_TXD3 | FCC1_UT_TXD4 | N22[3] |
| PA22 | FCC1_UT_TXD3 | N26[3] |
| PA23 | FCC1_UT_TXD2 | N23[3] |
| PA24/MSNUM1 | FCC1_UT_TXD1 | H26[3] |
| PA25/MSNUM0 | FCC1_UT_TXD0 | G25[3] |
| PA26/FCC1_MII_RMIIRX_ER | FCC1_UT_RXCLAV | L22[3] |
| PA27/FCC1_MII_RX_DV/FCC1_RMII_CRS_DV | FCC1_UT_RXSOC | G24[3] |
| PA28/FCC1_MII_RMII_TX_EN | FCC1_UT_RXENB | G23[3] |
| PA29/FCC1_MII_TX_ER | $\overline{\text{FCC1_UT_TXSOC}}$ | B26[3] |
| PA30/FCC1_MII_CRS/$\overline{\text{FCC1_RTS}}$ | FCC1_UT_TXCLAV | A25[3] |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| PA31/FCC1_MII_COL | $\overline{\text{FCC1_UT_TXENB}}$ | G22[3] |
| PB18/FCC2_MII_HDLC_RXD3 | | T25[3] |
| PB19/FCC2_MII_HDLC_RXD2 | | P22[3] |
| PB20/FCC2_MII_HDLC_RMII_RXD1 | | L25[3] |
| PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD | | J26[3] |
| PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0 | | U23[3] |
| PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1 | | U26[3] |
| PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2 | | M24[3] |
| PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2 | | M23[3] |
| PB26/FCC2_MII_CRS/L1RXDB2 | | H24[3] |
| PB27/FCC2_MII_COL/L1TXDB2 | | E25[3] |
| PB28/FCC2_MII_RMII_RX_ER/$\overline{\text{FCC2_RTS}}$/TXD1 | | D26[3] |
| PB29/FCC2_MII_RMII_TX_EN | | K21[3] |
| PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV | | D24[3] |
| PB31/FCC2_MII_TX_ER | | E23[3] |
| PC0/$\overline{\text{DREQ3}}$/BRGO7/$\overline{\text{SMSYN1}}$/L1CLKOA2 | | AF23[3] |
| PC1/BRGO6/$\overline{\text{L1RQA2}}$ | | AD23[3] |
| PC4/SMRXD1/SI2_L1ST4/$\overline{\text{FCC2_CD}}$ | | AB22[3] |
| PC5/SMTXD1/SI2_L1ST3/$\overline{\text{FCC2_CTS}}$ | | AE24[3] |
| PC6/$\overline{\text{FCC1_CD}}$/SI2_L1ST2 | FCC1_UT_RXADDR2 | AF24[3] |
| PC7/$\overline{\text{FCC1_CTS}}$ | FCC1_UT_TXADDR2 | AE26[3] |
| PC8/$\overline{\text{CD4}}$/RTS1/SI2_L1ST2/$\overline{\text{CTS3}}$ | | AC24[3] |
| PC9/$\overline{\text{CTS4}}$/L1TSYNCA2 | | AA23[3] |
| PC10/$\overline{\text{CD3}}$/USB_RN | | AB25[3] |
| PC11/$\overline{\text{CTS3}}$/USB_RP/L1TXD3A2 | | V22[3] |
| PC12 | FCC1_UT_RXADDR1 | AA26[3] |
| PC13/BRGO5 | FCC1_UT_TXADDR1 | V23[3] |
| PC14/$\overline{\text{CD1}}$ | FCC1_UT_RXADDR0 | W24[3] |
| PC15/$\overline{\text{CTS1}}$ | FCC1_UT_TXADDR0 | U24[3] |
| PC16/CLK16 | | T23[3] |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| PC17/CLK15/BRGO8/$\overline{\text{DONE2}}$ | | T26[3] |
| PC18/CLK14/$\overline{\text{TGATE2}}$ | | R26[3] |
| PC19/CLK13/BRGO7/$\overline{\text{TGATE1}}$ | | P24[3] |
| PC20/CLK12/$\overline{\text{USBOE}}$ | | L26[3] |
| PC21/CLK11/BRGO6/CP_INT | | L24[3] |
| PC22/CLK10/$\overline{\text{DONE3}}$ | FCC1_UT_TXPRTY | L23[3] |
| PC23/CLK9/BRGO5/$\overline{\text{DACK3}}$/$\overline{\text{CD1}}$ | | K24[3] |
| PC24/CLK8/TIN3/$\overline{\text{TOUT4}}$/DREQ2/BRGO1 | | K23[3] |
| PC25/CLK7/BRGO4/$\overline{\text{DACK2}}$/SPISEL | | F26[3] |
| PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK | | H23[3] |
| PC27/CLK5/BRGO3/$\overline{\text{TOUT1}}$ | FCC1_UT_RXPRTY | K22[3] |
| PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/SPICLK | | D25[3] |
| PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$ | | F24[3] |
| PD7/SMSYN2 | FCC1_UT_TXADDR3 | AB21[3] |
| PD14/I2CSCL | | AC26[3] |
| PD15/I2CSDA | | Y23[3] |
| PD16/SPIMISO | FCC1_UT_TXPRTY | AA25[3] |
| PD17/BRGO2/SPIMOSI | FCC1_UT_RXPRTY | Y26[3] |
| PD18/SPICLK | FCC1_UT_RXADDR4 | W25[3] |
| PD19/SPISEL/BRGO1 | FCC1_UT_TXADDR4 | V25[3] |
| PD20/$\overline{\text{RTS4}}$/L1RSYNCA2 | | R24[3] |
| PD21/TXD4/L1RXD0A2 | | P23[3] |
| PD22/RXD4/L1TXD0A2 | | N25[3] |
| PD23/$\overline{\text{RTS3}}$/USB_TP | | K26[3] |
| PD24/TXD3/USB_TN | | K25[3] |
| PD25/RXD3/USB_RXD | | J25[3] |
| PD29/$\overline{\text{RTS1}}$ | FCC1_UT_RXADDR3 | C26[3] |
| PD30/TXD1 | | E24[3] |
| PD31/RXD1 | | B25[3] |
| VCCSYN | | C18 |
| VCCSYN1 | | K6 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| CLKIN2 | | C21 |
| No connect[4] | | D19[4], J3[4], AD24[5] |
| I/O power | | B4, F3, J2, N4, AD1, AD5, AE8, AC13, AD18, AB24, AB26, W23, R25, M25, F25, C25, C22, B17, B12, B8, E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9 |
| Core Power | | F5, K5, M5, AA5, AB7, AA13, AA19, AA21, Y22, AC25, U22, R22, L21, H22, E22, E20, E15, F13, F11, F8, L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10 |
| Ground | | E19, E2, K1, Y2, AE1, AE4, AD9, AC14, AE17, AC19, AE25, V24, P26, M26, G26, E26, B21, C12, C11, C8, A8, B18, A18, A2, B1, B2, A5, C5, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17 |

1 Must be tied to ground.

2 Should be tied to VDDH via a 2K Ω external pull-up resistor.

3 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

4 This pin is not connected. It should be left floating.

5 Must be pulled down or left floating

# 9 Package Description

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

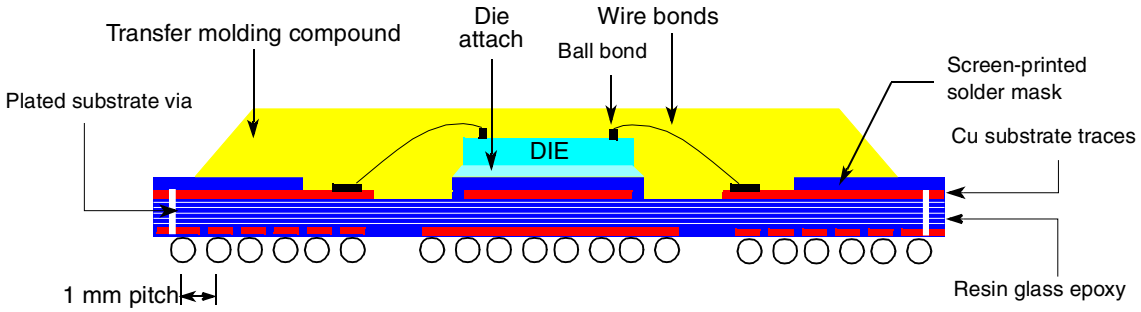



**Figure 13. Side View of the PBGA Package Remove**

## 9.1 Package Parameters

This table provides package parameters.

**Table 22. Package Parameters**

| Code | Type | Outline (mm) | Interconnects | Pitch (mm) | Nominal Unmounted Height (mm) |
|---|---|---|---|---|---|
| VR, ZQ | PBGA | 27 x 27 | 516 | 1 | 2.25 |

**NOTE: Temperature Reflow for the VR Package**

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

## 9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

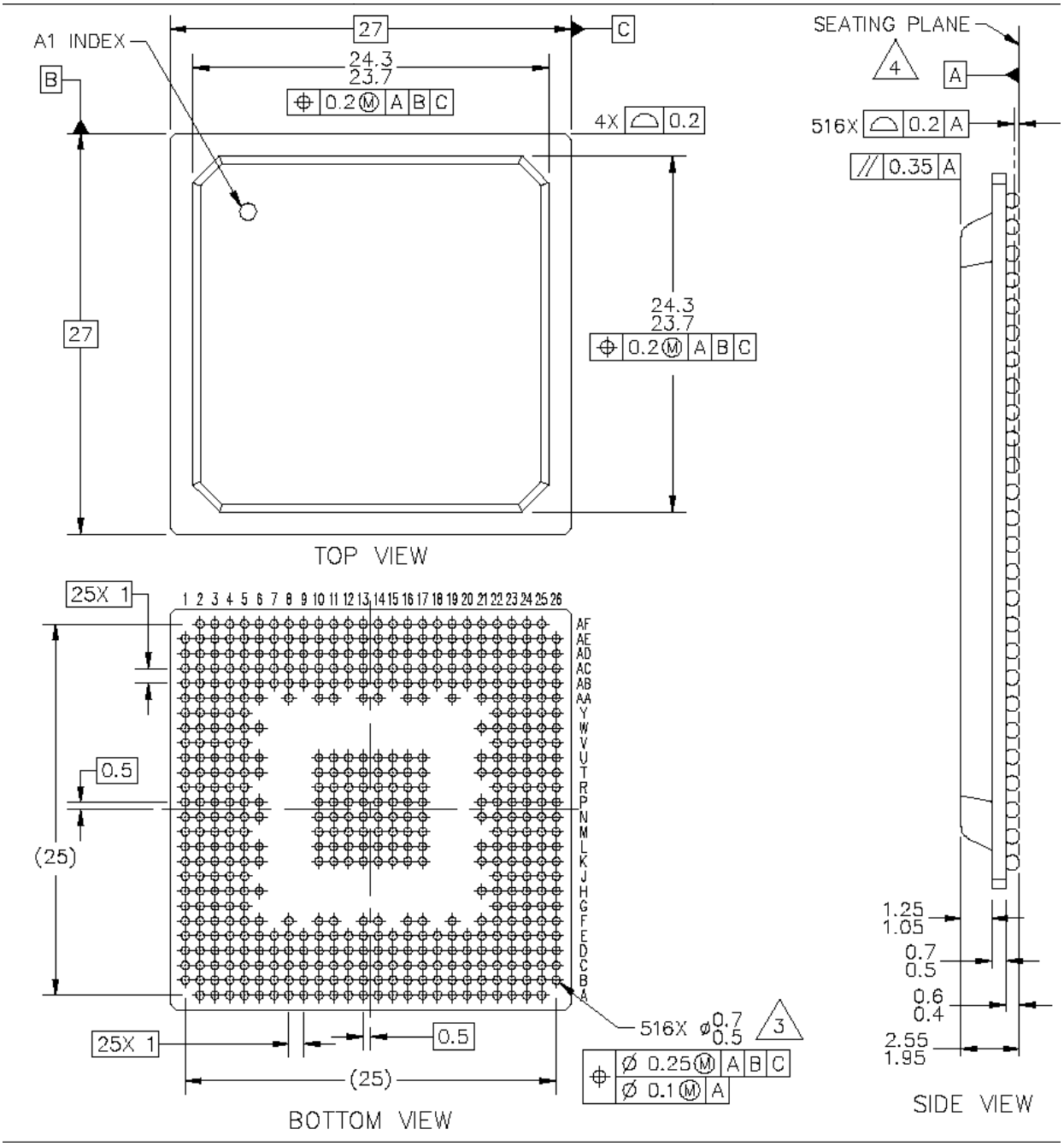



**Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA**

# 10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

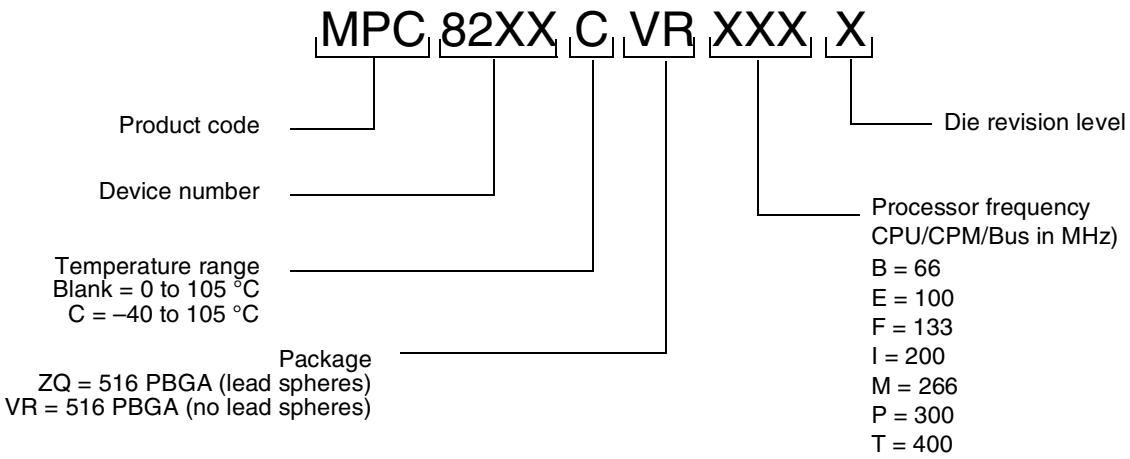



**Figure 15. Freescale Part Number Key**

# 11 Document Revision History

This table summarizes changes to this document.

**Table 23. Document Revision History**

| Revision | Date | Substantive Changes |
|---|---|---|
| 3 | 09/2011 | In Figure 15, “Freescale Part Number Key,” added speed decoding information below processor frequency information. |
| 2 | 12/2008 | • Modified Figure 5, “SCC/SMC/SPI/I2C External Clock Diagram,” and added second section of figure notes.<br>• In Table 12, modified “Data bus in pipeline mode” row and showed 66 MHz as “N/A.”<br>• In Section 10, “Ordering Information,” added “F = 133” to CPU/CPM/Bus Frequency.<br>• Added footnote concerning CPM_CLK/PCI_CLK ratio to column “PCI Division Factor” in Table 17, “Clock Configurations for PCI Host Mode (PCI_MODCK=0),” and Table 18, “Clock Configurations for PCI Host Mode (PCI_MODCK=1),.”<br>• Removed overbar from DLL_ENABLE in Table 21, “Pinout.” |
| 1.5 | 12/2006 | • Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions. |
| 1.4 | 05/2006 | • Added row for 133 MHz configurations to Table 8. |
| 1.3 | 02/2006 | • Inserted Section 6.3, “JTAG Timings.” |

**Table 23. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.2 | 09/2005 | • Added 133-MHz to the list of frequencies in the opening sentence of Section 6, "AC Electrical Characteristics".<br>• Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13.<br>• Added footnote 2 to Table 13.<br>• Added the conditions note directly above Table 12. |
| 1.1 | 01/2005 | • Modification for correct display of assertion level ("overbar") for some signals |
| 1.0 | 12/2004 | • Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values<br>• Section 2: removed voltage tracking note<br>• Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset<br>• Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V<br>• Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed.<br>• Section 4.6: Updated description of layout practices<br>• Table 8: Note 3 added regarding IIC compatibility<br>• Table 8: Updated nominal and maximum power dissipation values<br>• Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance<br>• Section 6: Added sentence providing derating factor<br>• Section 6.1: added Note: Rise/Fall Time on CPM Input Pins<br>• Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a<br>• Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22<br>• Section 6.2: added spread spectrum clocking note<br>• Section 6.2: added CLKIN jitter note<br>• Table 12: combined specs sp11 and sp11a<br>• Table 13: sp30 Data Bus minimum delay values changed to 0.8<br>• Section 7: unit of ns added to Tval notes<br>• Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Table 21: correct superscript of footnote number after pin AD22<br>• Table 21: remove DONE3 from PC12<br>• Table 21: signals referring to TDMs C2 and D2 removed |

**Table 23. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 0.2 | 12/2003 | • Table 1: New<br>• Table 2: New<br>• Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V<br>• Table 8: Addition of note 2 regarding TRST and PORESET (see $V_{IH}$ row of Table 8)<br>• Table 8 and Table 21: Addition of muxed signals<br>CPCI_HS_ES to PCI_REQ1 (AF14)<br>CPCI_HS_LED to PCI_GNT1 (AE13)<br>CPCI_HS_ENUM to PCI_GNT2 (AF21)<br>• Table 8 and Table 21: Modification of PCI signal names for consistency with PCI signal names on other PowerQUICC II devices:<br>PCI_CFG0 (PCI_HOST_EN) (AC21)<br>PCI_CFG1 (PCI_ARB_EN) (AE22)<br>PCI_CFG2 (DLL_ENABLE) (AE23)<br>PCI_PAR (AF12)<br>PCI_FRAME (AD15)<br>PCI_TRDY(AF16)<br>PCI_IRDY (AF15)<br>PCI_STOP (AE15)<br>DEVSEL (AE14)<br>PCI_IDSEL (AC17)<br>PCI_PERR (AD14)<br>PCI_SERR (AD13)<br>PCI_REQ0–2 (AAE20, AF14, AB14)<br>PCI_GNT0–2 (AD20, AE13, AF21)<br>PCI_RST (AF22)<br>PCI_INTA (AE21)<br>PCI_C0-3 (AE12, AF13, AC15, AE18)<br>PCI_AD0-31<br>• Table 8 and Table 21: Corrected assertion level (added "‾") PCI_HOST_EN (AC21) and PCI_ARB_EN (AE22)<br>• Table 7: Addition of $R_{\theta JT}$ and note 4<br>• Sections 4.1–4.5 and 4.7 on thermal characteristics: New<br>• Section 7, "Clock Configuration Modes": Modification to first paragraph. Note that PCI_MODCK is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPC8280 Family and MPC8260 Family.<br>• Addition of "Note: Temperature Reflow for the VR Package" on page 56<br>• Table 21: Addition of note 2 to TRST (E21) and PORESET (C24)<br>• Table 21: Removal of Thermal0 (D19) and Thermal1(J3). These pins are now "No connects." Note 4 unchanged.<br>• Table 21: Removal of Spare0 (AD24). This pin is now a "No connect." Note 5 unchanged.<br>• Table 21: Addition of PCI_MODE (AD22). This pin was previously listed as "Ground." Addition of note 1. |
| 0.1 | 9/2003 | • Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine)<br>• Table 8: Addition of note 2 to $V_{IH}$<br>• Table 8: Changed $I_{OL}$ for 60x signals to 6.0 mA<br>• Modification of note 1 for Table 17, Table 18, Table 19, and Table 20<br>• Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both CS5 and GND. AD8 is only assigned to CS5.<br>• Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1(J3)<br>• Addition of ZQ package code to Figure 15 |
| 0 | 5/2003 | NDA release |

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