THE DATASHEET OF

MSC1202Y2RHHT

SBAS317E − APRIL 2004 − REVISED MAY 2006

Precision Analog-to-Digital Converter (ADC) and Current-Output Digital-to-Analog Converter (DAC) with 8051 Microcontroller and Flash Memory

FEATURES

ANALOG FEATURES

- MSC1200 and MSC1201:
  - 24 Bits No Missing Codes
  - 22 Bits Effective Resolution At 10Hz
  - Low Noise: 75nV
- MSC1202:
  - 16 Bits No Missing Codes
  - 16 Bits Effective Resolution At 200Hz
  - Noise: 600nV
- PGA From 1 to 128
- Precision On-Chip Voltage Reference
- 8 Diff/Single-Ended Channels (MSC1200)
- 6 Diff/Single-Ended Channels (MSC1201/02)
- On-Chip Offset/Gain Calibration
- Offset Drift: 0.1ppm/°C
- Gain Drift: 0.5ppm/°C
- On-Chip Temperature Sensor
- Selectable Buffer Input
- Signal-Source Open-Circuit Detect
- 8-Bit Current DAC

DIGITAL FEATURES

Microcontroller Core

- 8051-Compatible
- High-Speed Core:
  - 4 Clocks per Instruction Cycle
- DC to 33MHz
- On-Chip Oscillator
- PLL with 32kHz Capability
- Single Instruction 121ns
- Dual Data Pointer

Memory

- 4kB or 8kB of Flash Memory
- Flash Memory Partitioning
- Endurance 1M Erase/Write Cycles, 100-Year Data Retention
- 256 Bytes Data SRAM
- In-System Serially Programmable
- Flash Memory Security
- 1kB Boot ROM

Peripheral Features

- 16 Digital I/O Pins
- Additional 32-Bit Accumulator
- Two 16-Bit Timer/Counters
- System Timers
- Programmable Watchdog Timer
- Full-Duplex USART
- Basic SPI™
- Basic I^2C™
- Power Management Control
- Internal Clock Divider
- Idle Mode Current < 200μA
- Stop Mode Current < 100nA
- Digital Brownout Reset
- Analog Low-Voltage Detect
- 20 Interrupt Sources

GENERAL FEATURES

- Each Device Has Unique Serial Number
- Packages:
  - TQFP-48 (MSC1200)
  - QFN-36 (MSC1201/02)
- Low Power: 3mW at 3.0V, 1MHz
- Industrial Temperature Range: −40°C to +125°C
- Power Supply: 2.7V to 5.25V

APPLICATIONS

- Industrial Process Control
- Instrumentation
- Liquid/Gas Chromatography
- Blood Analysis
- Smart Transmitters
- Portable Instruments
- Weigh Scales
- Pressure Transducers
- Intelligent Sensors
- Portable Applications
- DAS Systems

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	FLASH MEMORY (BYTES)	ADC RESOLUTION (BITS)	PACKAGE MARKING
MSC1200Y2	4k	24	MSC1200Y2
MSC1200Y3	8k	24	MSC1200Y3
MSC1201Y2	4k	24	MSC1201Y2
MSC1201Y3	8k	24	MSC1201Y3
MSC1202Y2	4k	16	MSC1202Y2
MSC1202Y3	8k	16	MSC1202Y3

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet, or refer to our web site at www.ti.com.

MSC120x FAMILY FEATURES

FEATURES(1)	MSC120xY2(2)	MSC120xY3(2)
Flash Program Memory (Bytes)	Up to 4k	Up to 8k
Flash Data Memory (Bytes)	Up to 2k	Up to 4k
Internal Scratchpad RAM (Bytes)	256	256

(1) All peripheral features are the same on all devices; the flash memory size is the only difference.
(2) The last digit of the part number (*N*) represents the onboard flash size = (2^N)kBytes.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

			MSC120x	UNITS
Analog Inputs				
Input current	Momentary		100	mA
	Continuous		10	mA
Input voltage			AGND − 0.3 to AV_{DD} + 0.3	V
Power Supply				
DV_{DD} to DGND			−0.3 to +6	V
AV_{DD} to AGND			−0.3 to +6	V
AGND to DGND			−0.3 to +0.3	V
VREF to AGND			−0.3 to AV_{DD} + 0.3	V
Digital input voltage to DGND			−0.3 to DV_{DD} + 0.3	V
Digital output voltage to DGND			−0.3 to DV_{DD} + 0.3	V
Maximum junction temperature (T_J Max)			+150	°C
Operating temperature range			−40 to +125	°C
Storage temperature range			−65 to +150	°C
Package power dissipation			(T_J Max − $T_{AMBIENT}$)/θ_{JA}	W
Output current, all pins			200	mA
Output pin short-circuit			10	s
Thermal resistance	Junction to ambient (θ_{JA})	High K (2s 2p)	21.9	°C/W
		Low K (1s)	103.7	°C/W
	Junction to case (θ_{JC})		21.9	°C/W
Digital Outputs				
Output current	Continuous		100	mA
I/O source/sink current			100	mA
Power pin maximum			300	mA

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, ADC Bipolar Mode, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise noted.

PARAMETER		CONDITION	MSC120x MIN	MSC120x TYP	MSC120x MAX	UNITS
Analog Input (AIN0-AIN5, AINCOM)						
Analog Input Range		Buffer OFF	AGND − 0.1		AV_{DD} + 0.1	V
		Buffer ON	AGND + 50mV		AV_{DD} − 1.5	V
Full-Scale Input Voltage Range		(In+) − (In−), Bipolar Mode			$\pm V_{REF}$/PGA	V
Differential Input Impedance		Buffer OFF		7/PGA(1)		MΩ
Input Current		Buffer ON		0.5		nA
Bandwidth	Fast Settling Filter	−3dB		0.469 • f_{DATA}		
	$Sinc^2$ Filter	−3dB		0.318 • f_{DATA}		
	$Sinc^3$ Filter	−3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier		User-Selectable Gain Range	1		128	
Input Capacitance		Buffer ON		7		pF
Input Leakage Current		Multiplexer Channel OFF, T = +25°C		0.5		pA
Burnout Current Sources		Buffer ON		±2		µA
ADC Offset DAC						
Offset DAC Range				$\pm V_{REF}/(2 \bullet PGA)$		V
Offset DAC Resolution			8			Bits
Offset DAC Full-Scale Gain Error				±1.0		% of Range
Offset DAC Full-Scale Gain Error Drift				0.6		ppm/°C
System Performance						
Resolution		MSC1200, MSC1201	24			Bits
		MSC1202	16			Bits
ENOB		MSC1200, MSC1201		22		Bits
		MSC1202		16		Bits
Output Noise			See Typical Characteristics			
No Missing Codes		MSC1201, $Sinc^3$ Filter, Decimation > 360	24			Bits
		MSC1202, $Sinc^3$ Filter	16			Bits
Integral Nonlinearity		End Point Fit, Differential Input		±0.0004	±0.0015	% of FSR
Offset Error		After Calibration		1.5		ppm of FS
Offset Drift(2)		Before Calibration		0.1		ppm of FS/°C
Gain Error(3)		After Calibration		0.005		%
Gain Error Drift(2)		Before Calibration		0.5		ppm/°C
System Gain Calibration Range			80		120	% of FS
System Offset Calibration Range			−50		50	% of FS
Common-Mode Rejection		At DC, V_{IN} = 0V		120		dB
		f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
		f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
		f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal-Mode Rejection		f_{CM} = 50Hz, f_{DATA} = 50Hz		100		dB
		f_{CM} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection		At DC, dB = $-20\log(\Delta V_{OUT}/\Delta V_{DD})$(4), V_{IN} = 0V		100		dB

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The gain self-calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (continued)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, ADC Bipolar Mode, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise noted.

PARAMETER		CONDITION	MSC120x MIN	MSC120x TYP	MSC120x MAX	UNITS
Voltage Reference Input						
Reference Input Range		REF IN+, REF IN−	AGND		AV_{DD}(3)	V
ADC V_{REF}		$V_{REF} \equiv$ (REFIN+) − (REFIN−)	0.1	2.5	AV_{DD}	V
V_{REF} Common-Mode Rejection		At DC		115		dB
Input Current		V_{REF} = 2.5V, PGA = 1		1		µA
On-Chip Voltage Reference						
Output Voltage		VREFH = 1, T = +25°C	2.49	2.5	2.51	V
		VREFH = 0	1.23	1.25	1.27	V
Short-Circuit Current Source				8		mA
Short-Circuit Current Sink				65		µA
Short-Circuit Duration		Sink or Source		Indefinite		
Startup Time from Power ON		C_{REFOUT} = 0.1µF		0.4		ms
Temperature Sensor						
Temperature Sensor Voltage		T = +25°C		115		mV
Temperature Sensor Coefficient		MSC1200		375		µV/°C
		MSC1201, MSC1202		345		µV/°C
IDAC Output Characteristics						
IDAC Resolution				8		Bits
Full-Scale Output Current		IDAC = 0FFh		1		mA
Maximum Short-Circuit Current Duration				Indefinite		
Compliance Voltage		IDAC = 00h		AV_{DD} − 1.5		V
IDAC Zero Code Current				0		µA
IDAC INL				1.3		LSB
Analog Power-Supply Requirements						
Analog Power-Supply Voltage		AV_{DD}	4.75	5.0	5.25	V
Analog Power-Supply Current	Analog Current	BOR OFF, External Clock Mode, Analog OFF, ALVD OFF, PDADC = PDIDAC = 1		< 1		nA
	ADC Current (I_{ADC})	PGA = 1, Buffer OFF		170		µA
		PGA = 128, Buffer OFF		430		µA
		PGA = 1, Buffer ON		230		µA
		PGA = 128, Buffer ON		770		µA
	V_{REF} Supply Current (I_{VREF})	ADC ON		360		µA
	I_{DAC} Supply Current (I_{IDAC})	IDAC = 00h		230		µA

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The gain self-calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, ADC Bipolar Mode, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +1.25V, unless otherwise noted.

PARAMETER		CONDITIONS	MSC120x MIN	MSC120x TYP	MSC120x MAX	UNITS
Analog Input (AIN0-AIN5, AINCOM)						
Analog Input Range		Buffer OFF	AGND − 0.1		AV_{DD} + 0.1	V
		Buffer ON	AGND + 50mV		AV_{DD} − 1.5	V
Full-Scale Input Voltage Range		(In+) − (In−), Bipolar Mode			$\pm V_{REF}$/PGA	V
Differential Input Impedance		Buffer OFF		7/PGA(1)		MΩ
Input Current		Buffer ON		0.5		nA
Bandwidth	Fast Settling Filter	−3dB		0.469 • f_{DATA}		
	$Sinc^2$ Filter	−3dB		0.318 • f_{DATA}		
	$Sinc^3$ Filter	−3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier		User-Selectable Gain Range	1		128	
Input Capacitance		Buffer ON		7		pF
Input Leakage Current		Multiplexer Channel Off, T = +25°C		0.5		pA
Burnout Current Sources		Buffer ON		±2		µA
ADC Offset DAC						
Offset DAC Range				$\pm V_{REF}$/(2•PGA)		V
Offset DAC Resolution			8			Bits
Offset DAC Full-Scale Gain Error				±1.5		% of Range
Offset DAC Full-Scale Gain Error Drift				0.6		ppm/°C
System Performance						
Resolution		MSC1200, MSC1201	24			Bits
		MSC1202	16			Bits
ENOB		MSC1200, MSC1201		22		Bits
		MSC1202		16		Bits
Output Noise			See Typical Characteristics			
No Missing Codes		MSC1200, MSC1201, $Sinc^3$ Filter, Decimation > 360	24			Bits
		MSC1202, $Sinc^3$ Filter	16			Bits
Integral Nonlinearity		End Point Fit, Differential Input		±0.0004	±0.0015	% of FSR
Offset Error		After Calibration		1.3		ppm of FS
Offset Drift(2)		Before Calibration		0.1		ppm of FS/°C
Gain Error(3)		After Calibration		0.005		%
Gain Error Drift(2)		Before Calibration		0.5		ppm/°C
System Gain Calibration Range			80		120	% of FS
System Offset Calibration Range			−50		50	% of FS
Common-Mode Rejection		At DC, V_{IN} = 0V		130		dB
		f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
		f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
		f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal-Mode Rejection		f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
		f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection		At DC, dB = $-20\log(\Delta V_{OUT}/\Delta V_{DD})$(4), V_{IN} = 0V		88		dB

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The gain self-calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V (continued)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to +5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, ADC Bipolar Mode, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +1.25V, unless otherwise noted.

PARAMETER		CONDITIONS	MSC120x MIN	MSC120x TYP	MSC120x MAX	UNITS
Voltage Reference Input						
Reference Input Range		REF IN+, REF IN−	AGND		AV_{DD}(3)	V
ADC V_{REF}		$V_{REF} \equiv$ (REFIN+) − (REFIN−)	0.1	1.25	AV_{DD}	V
V_{REF} Common-Mode Rejection		At DC		110		dB
Input Current		V_{REF} = 1.25V, PGA = 1		0.5		µA
On-Chip Voltage Reference						
Output Voltage		VREFH = 0, T = +25°C	1.23	1.25	1.27	V
Short-Circuit Current Source				2.9		mA
Short-Circuit Current Sink				60		µA
Short-Circuit Duration		Sink or Source		Indefinite		
Startup Time from Power ON		C_{REFOUT} = 0.1µF		0.2		ms
Temperature Sensor						
Temperature Sensor Voltage		T = +25°C		115		mV
Temperature Sensor Coefficient		MSC1200		375		µV/°C
		MSC1201, MSC1202		345		µV/°C
IDAC Output Characteristics						
IDAC Resolution				8		Bits
Full-Scale Output Source Current				1		mA
Maximum Short-Circuit Current Duration				Indefinite		
Compliance Voltage				AV_{DD} − 1.5		V
IDAC Zero Code Current				0		µA
IDAC INL				1.5		LSB
Analog Power-Supply Requirements						
Analog Power-Supply Voltage		AV_{DD}	2.7	3.3	3.6	V
Analog Power-Supply Current	Analog Current	BOR OFF, External Clock Mode, Analog OFF, ALVD OFF, PDADC = PDIDAC = 1		< 1		nA
	ADC Current (I_{ADC})	PGA = 1, Buffer OFF		150		µA
		PGA = 128, Buffer OFF		380		µA
		PGA = 1, Buffer ON		200		µA
		PGA = 128, Buffer ON		610		µA
	V_{REF} Supply Current (I_{VREF})	ADC ON		330		µA
	I_{DAC} Supply Current (I_{IDAC})	IDAC = 00h		220		µA

(1) The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).
(2) Calibration can minimize these errors.
(3) The gain self-calibration cannot have a REF IN+ of more than AV_{DD} −1.5V with Buffer ON. To calibrate gain, turn Buffer OFF.
(4) ΔV_{OUT} is change in digital result.

DIGITAL CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

All specifications from T_{MIN} to T_{MAX}, FMCON = 10h, all digital outputs high, and PDCON = 00h (all peripherals ON) or PDCON = FFh (all peripherals OFF), unless otherwise specified.

PARAMETER		CONDITIONS	MSC120x MIN	MSC120x TYP	MSC120x MAX	UNITS
Digital Power-Supply Requirements						
DV_{DD}			2.7	3.3	3.6	V
Digital Power-Supply Current		Normal Mode, f_{OSC} = 1MHz, All Peripherals ON		0.7		mA
		Normal Mode, f_{OSC} = 1MHz, All Peripherals OFF		0.6		mA
		Normal Mode, f_{OSC} = 8MHz, All Peripherals ON		4.7		mA
		Normal Mode, f_{OSC} = 8MHz, All Peripherals OFF		4.3		mA
		Internal Oscillator LF Mode (14.8MHz nominal), All Peripherals ON		8.6		mA
		Internal Oscillator LF Mode (14.8MHz nominal), All Peripherals OFF		7.9		mA
		Stop Mode, External Clock OFF		100		nA
DV_{DD}			4.75	5.0	5.25	V
Digital Power-Supply Current		Normal Mode, f_{OSC} = 1MHz, All Peripherals ON		1.4		mA
		Normal Mode, f_{OSC} = 1MHz, All Peripherals OFF		1.3		mA
		Normal Mode, f_{OSC} = 8MHz, All Peripherals ON		9.3		mA
		Normal Mode, f_{OSC} = 8MHz, All Peripherals OFF		8.6		mA
		Internal Oscillator LF Mode (14.8MHz nom), All Peripherals ON		18		mA
		Internal Oscillator LF Mode (14.8MHz nom), All Peripherals OFF		16		mA
		Internal Oscillator HF Mode (29.5MHz nom), All Peripherals ON		33		mA
		Internal Oscillator HF Mode (29.5MHz nom), All Peripherals OFF		31		mA
		Stop Mode, External Clock OFF		100		nA
Digital Input/Output (CMOS)						
Logic Level	V_{IH} (except XIN pin)		0.6 • DV_{DD}		DV_{DD}	V
	V_{IL} (except XIN pin)		DGND		0.2 • DV_{DD}	V
Ports 1 and 3, Input Leakage Current, Input Mode		V_{IH} = DV_{DD} or V_{IH} = 0V		0		µA
I/O Pin Hysteresis				700		mV
V_{OL}, Ports 1 and 3, All Output Modes		I_{OL} = 1mA	DGND		0.4	V
		I_{OL} = 30mA, 3V (20mA)		1.5		V
V_{OH}, Ports 1 and 3, Strong Drive Output		I_{OH} = 1mA	DV_{DD} − 0.4	DV_{DD} − 0.1	DV_{DD}	V
		I_{OH} = 30mA, 3V (20mA)		DV_{DD} − 1.5		V
Ports 1 and 3, Pull-Up Resistors		Tolerance = ±25%		13		kΩ

FLASH MEMORY CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

PARAMETER	CONDITIONS	MSC120x MIN	MSC120x TYP	MSC120x MAX	UNITS
Flash Memory Endurance		100,000	1,000,000		cycles
Flash Memory Data Retention		100			Years
Mass and Page Erase Time	Set with FER Value in FTCON, from T_{MIN} to T_{MAX}	10			ms
Flash Memory Write Time	Set with FWR Value in FTCON	30		40	µs

AC ELECTRICAL CHARACTERISTICS(1): DV_{DD} = 2.7V to 5.25V

PARAMETER	CONDITION	MSC120x MIN	MSC120x TYP	MSC120x MAX	UNITS
PHASE LOCK LOOP (PLL)					
Input Frequency Range	External Crystal/Clock Frequency (f_{OSC})		32.768		kHz
PLL LF Mode	PLLDIV = 449 (default)		14.8		MHz
PLL HF Mode	PLLDIV = 899 (must be set by user), DV_{DD} = 5V		29.5		MHz
PLL Lock Time	Within 1%			2	ms
INTERNAL OSCILLATOR (IO)	See Typical Characteristics				
IO LF Mode	DV_{DD} = 5V		14.8		MHz
IO HF Mode	DV_{DD} = 5V		29.5		MHz
IO Settling Time	Within 1%			1	ms

(1) Parameters are valid over operating temperature range, unless otherwise specified.

EXTERNAL CLOCK DRIVE CLK TIMING: SEE FIGURE 1

SYMBOL	PARAMETER	2.7V to 3.6V MIN	2.7V to 3.6V MAX	4.75V to 5.25V MIN	4.75V to 5.25V MAX	UNITS
External Clock Mode						
f_{OSC}(1)	External Crystal Frequency (f_{OSC})	1	20	1	33	MHz
$1/t_{OSC}$(1)	External Clock Frequency (f_{OSC})	0	20	0	33	MHz
f_{OSC}(1)	External Ceramic Resonator Frequency (f_{OSC})	1	12	1	12	MHz
t_{HIGH}	High Time(2)	15		10		ns
t_{LOW}	Low Time(2)	15		10		ns
t_R	Rise Time(2)		5		5	ns
t_F	Fall Time(2)		5		5	ns

(1) $t_{CLK} = 1/f_{OSC}$ = one oscillator clock period for clock divider = 1.
(2) These values are characterized but not 100% production tested.

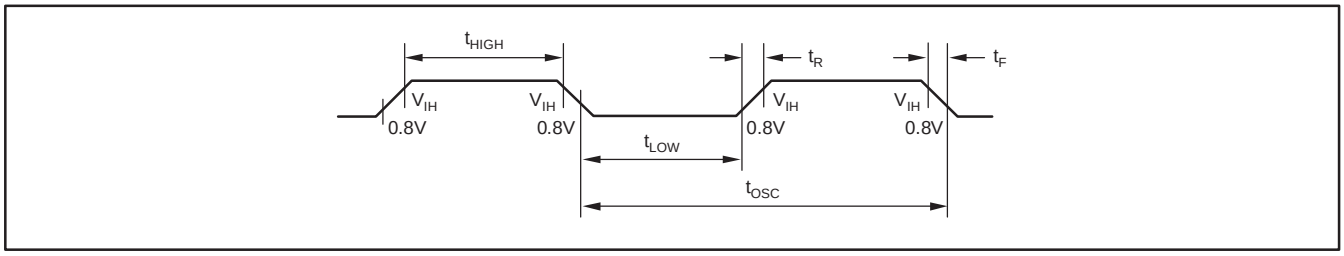
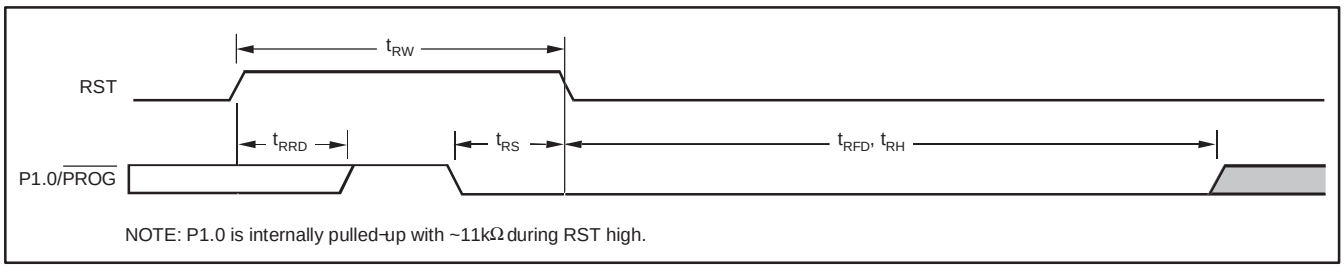


Figure 1. External Clock Drive CLK

SERIAL FLASH PROGRAMMING TIMING: SEE FIGURE 2

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{RW}	RST width	2 t_{OSC}	—	ns
t_{RRD}	RST rise to P1.0 internal pull high	—	5	µs
t_{RFD}	RST falling to CPU start	—	18	ms
t_{RS}	Input signal to RST falling setup time	t_{OSC}	—	ns
t_{RH}	RST falling to P1.0 hold time	18	—	ms

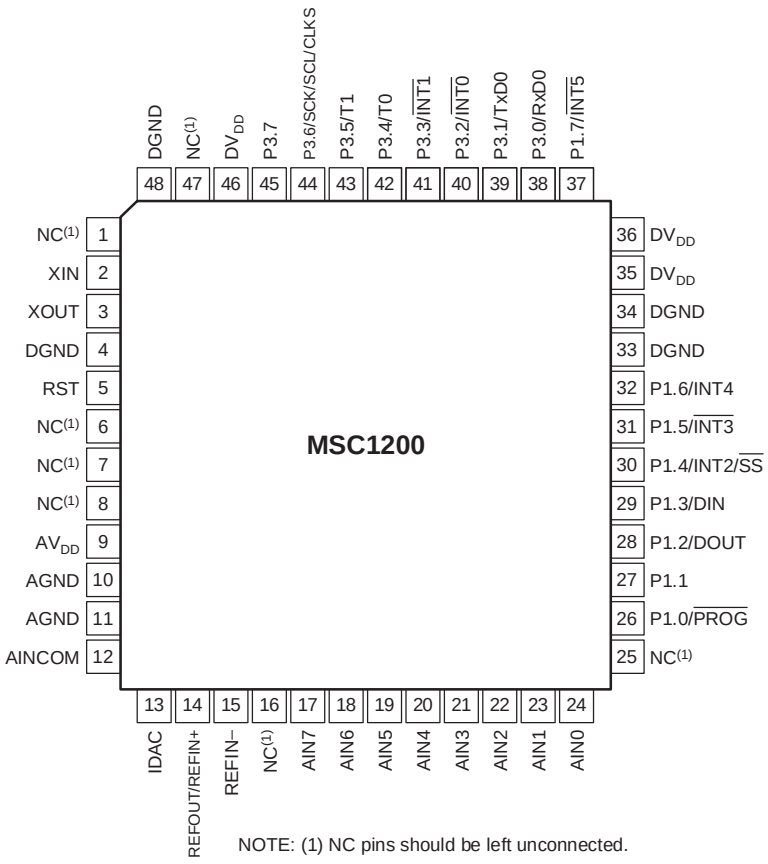


NOTE: P1.0 is internally pulled-up with ~11kΩ during RST high.

Figure 2. Serial Flash Programming Timing

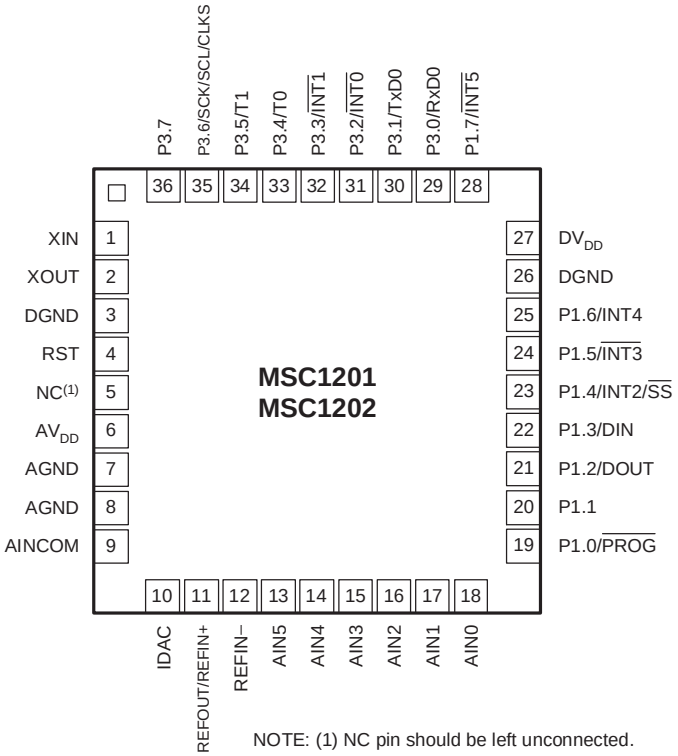
PIN CONFIGURATIONS

Top View **TQFP**



NOTE: (1) NC pins should be left unconnected.

Top View **QFN**



NOTE: (1) NC pin should be left unconnected.

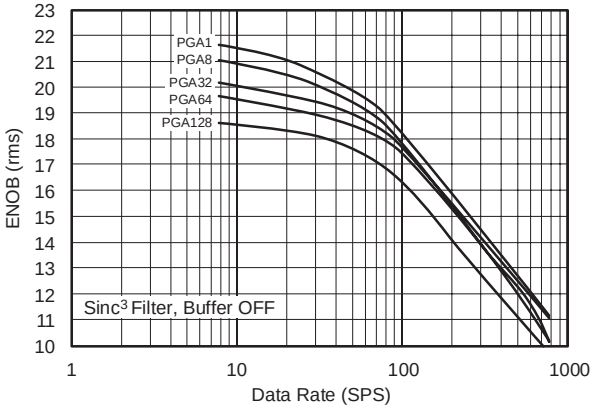
PIN ASSIGNMENTS

NAME	MSC1200 PIN #	MSC1201/1202 PIN #	DESCRIPTION
NC	1, 6, 7, 8, 16, 25, 47	5	No Connection. Leave unconnected.
XIN	2	1	The crystal oscillator pin XIN supports parallel resonant AT-cut fundamental frequency crystals and ceramic resonators. XIN can also be an input if there is an external clock source instead of a crystal. XIN must not be left floating.
XOUT	3	2	The crystal oscillator pin XOUT supports parallel resonant AT-cut fundamental frequency crystals and ceramic resonators. XOUT serves as the output of the crystal amplifier.
DGND	4, 33, 34, 48	3, 26	Digital Ground
RST	5	4	Holding the reset input high for two t_{OSC} periods will reset the device.
AV_{DD}	9	6	Analog Power Supply
AGND	10, 11	7, 8	Analog Ground
AINCOM	12	9	Analog Input (can be analog common for single-ended inputs or analog input for differential inputs)
IDAC	13	10	IDAC Output
REFOUT/REF IN+	14	11	Internal Voltage Reference Output/Voltage Reference Positive Input (required C_{REF} = 0.1µF)
REF IN−	15	12	Voltage Reference Negative Input (tie to AGND for internal voltage reference)
AIN7	17	—	Analog Input Channel 7
AIN6	18	—	Analog Input Channel 6
AIN5	19	13	Analog Input Channel 5
AIN4	20	14	Analog Input Channel 4
AIN3	21	15	Analog Input Channel 3
AIN2	22	16	Analog Input Channel 2
AIN1	23	17	Analog Input Channel 1
AIN0	24	18	Analog Input Channel 0
P1.0−P1.7	26−32, 37	19−25, 28	Port 1 is a bidirectional I/O port (refer to P1DDRL, SFR AEh, and P1DDRH, SFR AFh, for port pin configuration control). The alternate functions for Port 1 are listed below.
			Port / **Alternate Name(s)** / **Alternate Use**
			P1.0 / $\overline{\text{PROG}}$ / Serial programming mode (must be DGND on reset)
			P1.1 / N/A /
			P1.2 / DOUT / Serial data out
			P1.3 / DIN / Serial data in
			P1.4 / INT2/$\overline{\text{SS}}$ / External interrupt 2 / Slave Select
			P1.5 / $\overline{\text{INT3}}$ / External interrupt 3
			P1.6 / INT4 / External interrupt 4
			P1.7 / $\overline{\text{INT5}}$ / External interrupt 5
DV_{DD}	35, 36, 46	27	Digital Power Supply
P3.0−P3.7	38−45	29−36	Port 3 is a bidirectional I/O port (refer to P3DDRL, SFR B3h, and P3DDRH, SFR B4h, for port pin configuration control). The alternate functions for Port 3 are listed below.
			Port / **Alternate Name(s)** / **Alternate Use**
			P3.0 / RxD0 / Serial port 0 input
			P3.1 / TxD0 / Serial port 0 output
			P3.2 / $\overline{\text{INT0}}$ / External interrupt 0
			P3.3 / $\overline{\text{INT1}}$ / External interrupt 1
			P3.4 / T0 / Timer 0 external input
			P3.5 / T1 / Timer 1 external input
			P3.6 / SCK/SCL/CLKS / SCK / SCL / various clocks (refer to PASEL, SFR F2h)
			P3.7 / N/A /

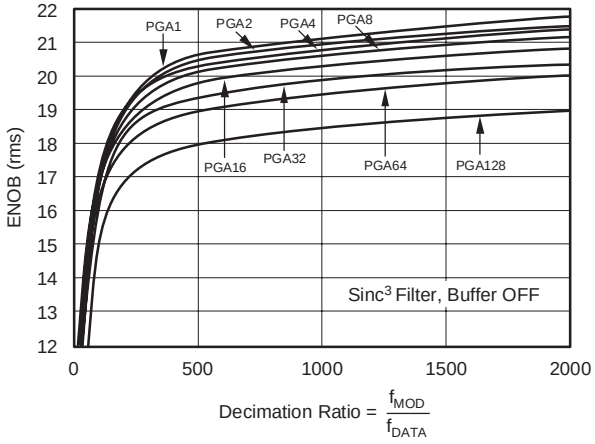
TYPICAL CHARACTERISTICS: MSC1200 AND MSC1201 ONLY

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

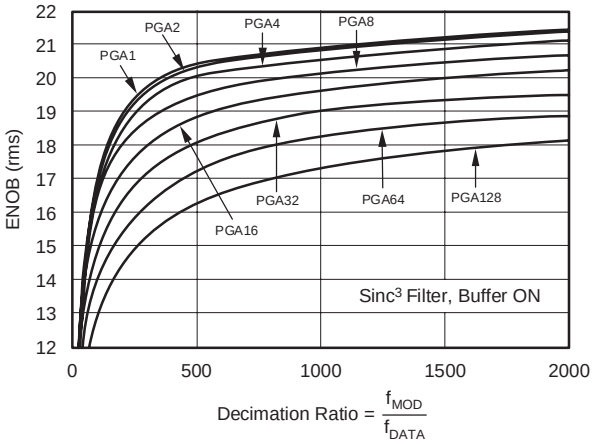
EFFECTIVE NUMBER OF BITS vs DATA RATE



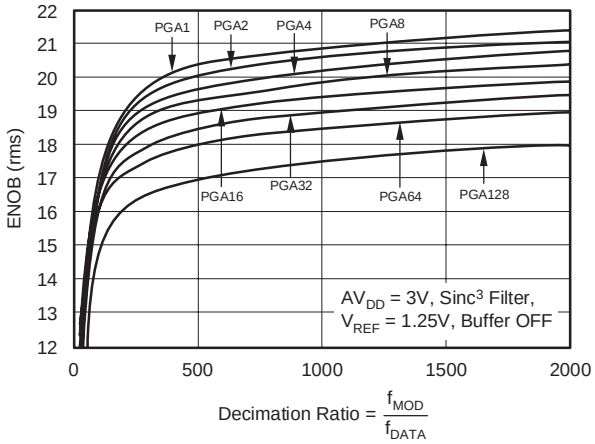
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



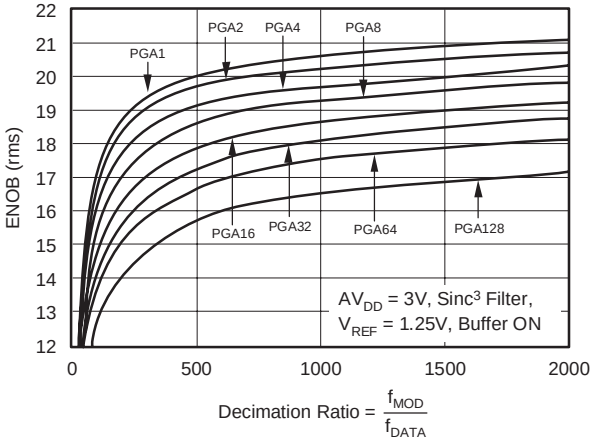
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



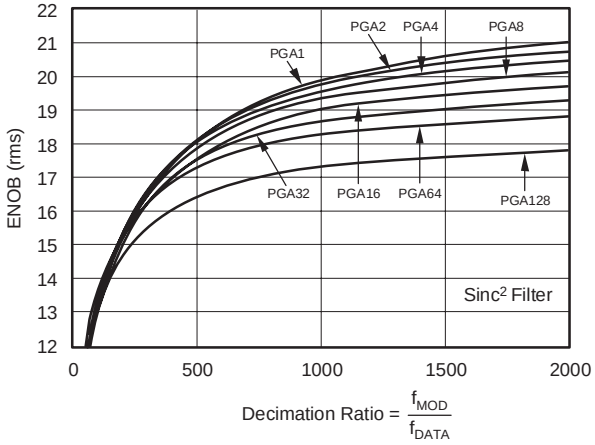
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



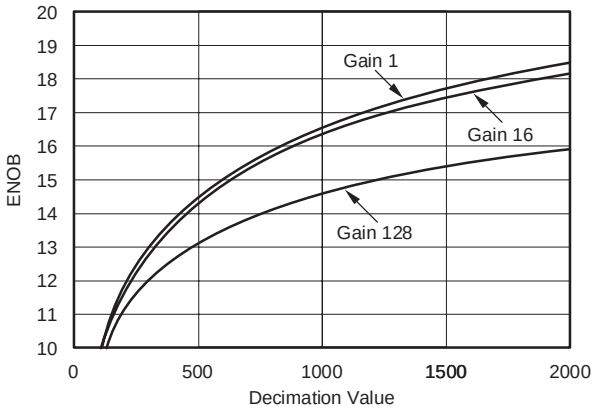
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



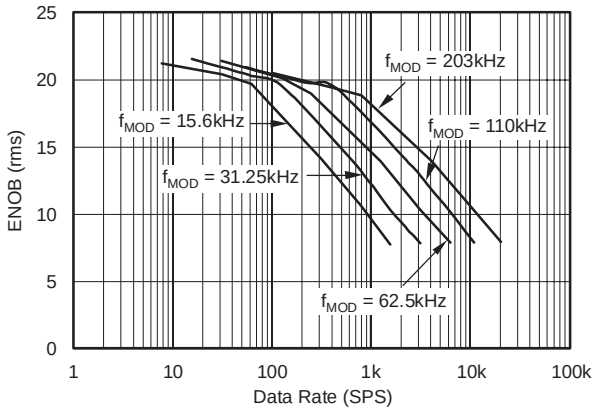
TYPICAL CHARACTERISTICS: MSC1200 AND MSC1201 ONLY (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

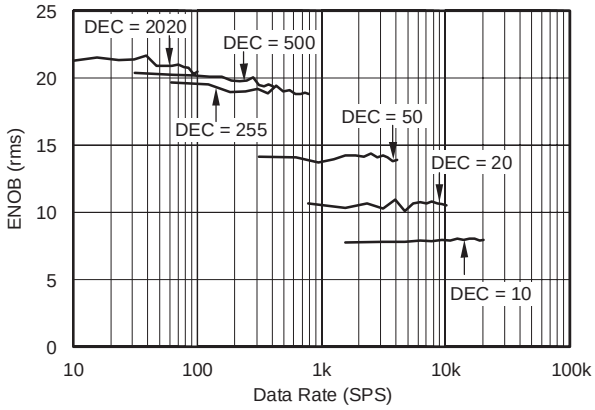
FAST SETTLING FILTER
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



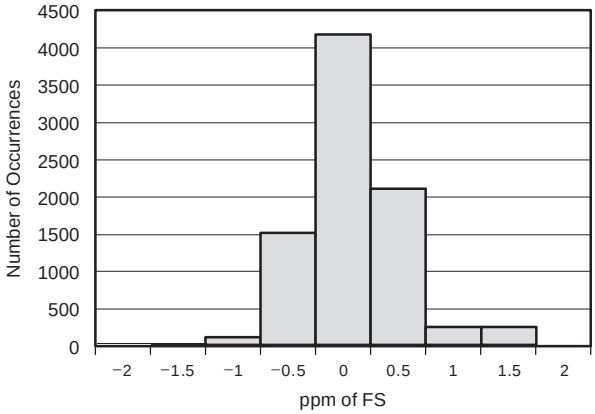
EFFECTIVE NUMBER OF BITS vs f_{MOD}
(set with ACLK)



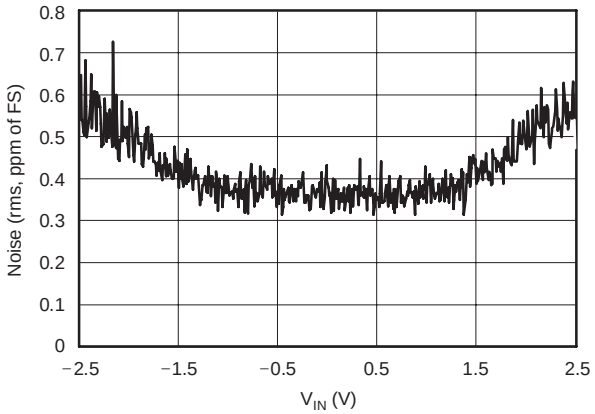
EFFECTIVE NUMBER OF BITS vs f_{MOD} (set with ACLK)
WITH FIXED DECIMATION



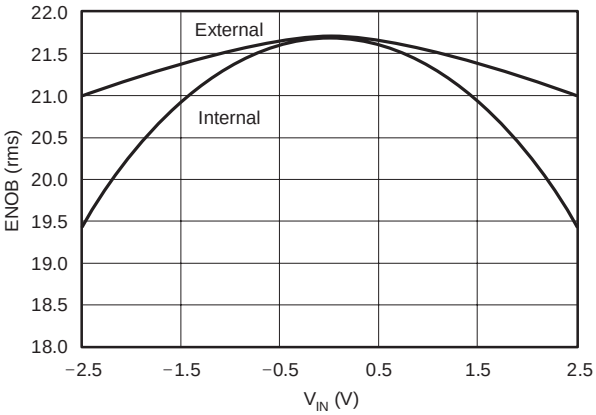
HISTOGRAM OF ADC OUTPUT DATA



NOISE vs INPUT SIGNAL



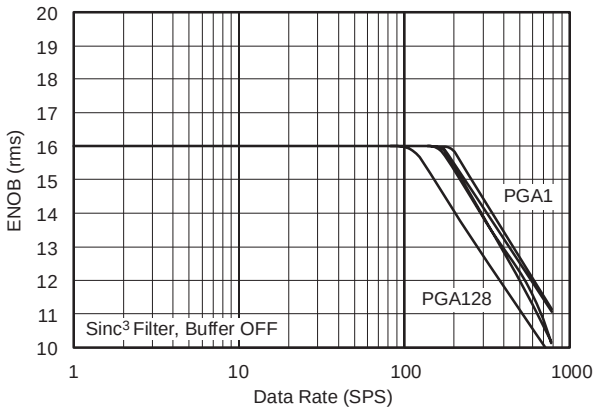
EFFECTIVE NUMBER OF BITS vs INPUT SIGNAL
(Internal and External V_{REF})



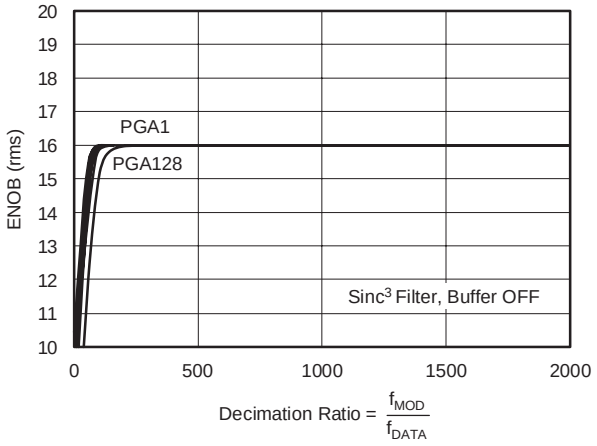
TYPICAL CHARACTERISTICS: MSC1202 ONLY

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

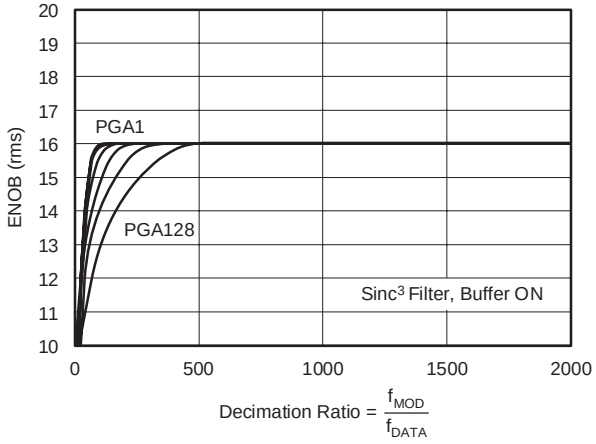
EFFECTIVE NUMBER OF BITS
vs DATA RATE



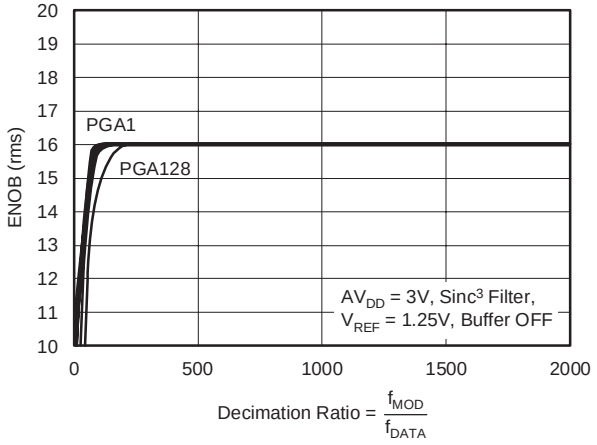
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



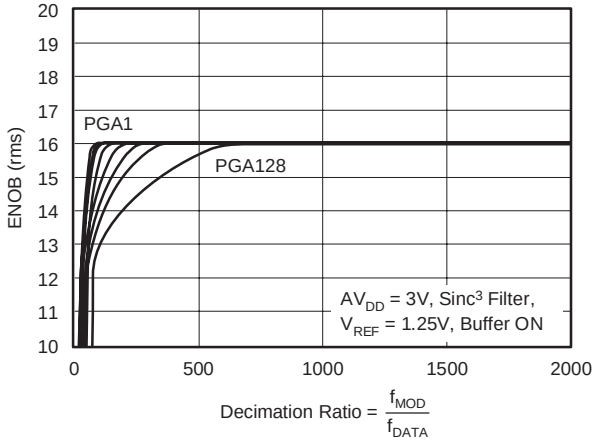
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



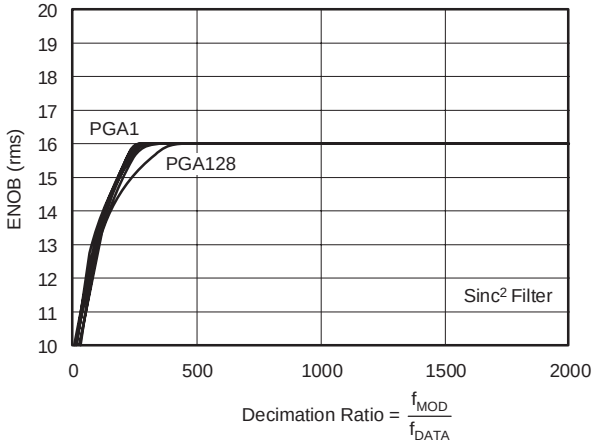
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



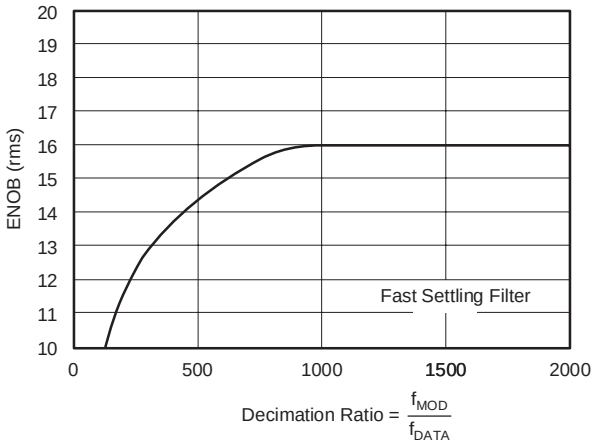
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



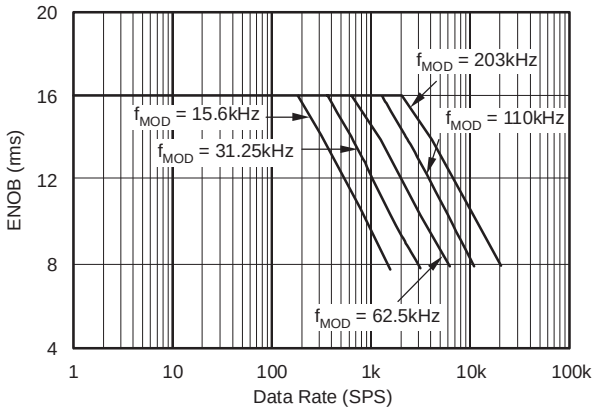
TYPICAL CHARACTERISTICS: MSC1202 ONLY (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

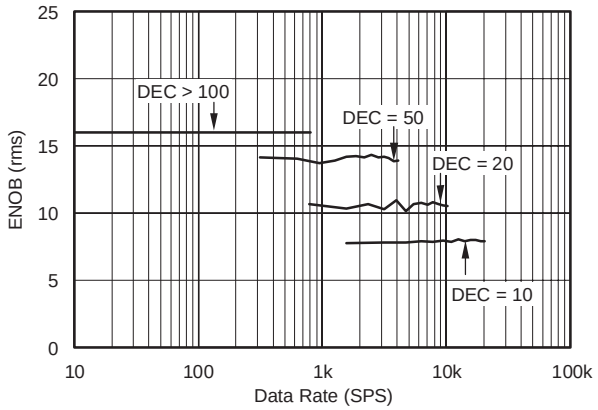
FAST SETTLING FILTER
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



EFFECTIVE NUMBER OF BITS vs f_{MOD}
(set with ACLK)



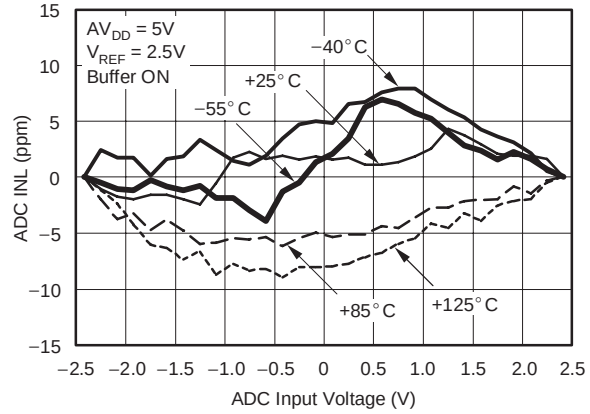
EFFECTIVE NUMBER OF BITS vs f_{MOD} (set with ACLK)
WITH FIXED DECIMATION



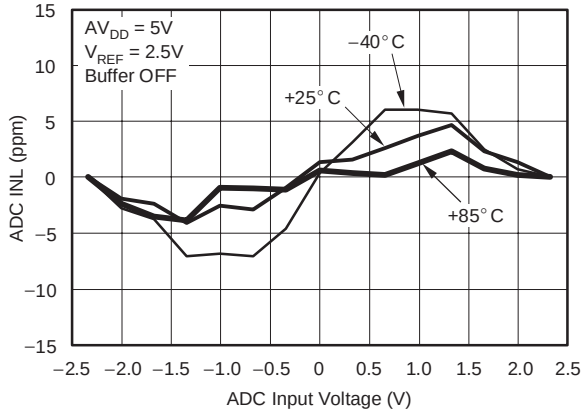
TYPICAL CHARACTERISTICS: ALL DEVICES

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

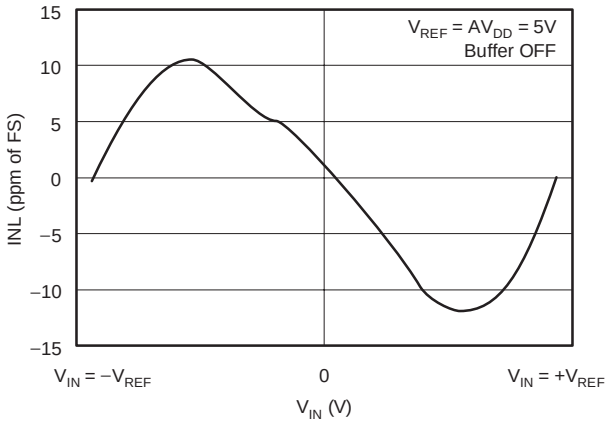
ADC INTEGRAL NONLINEARITY
vs INPUT VOLTAGE



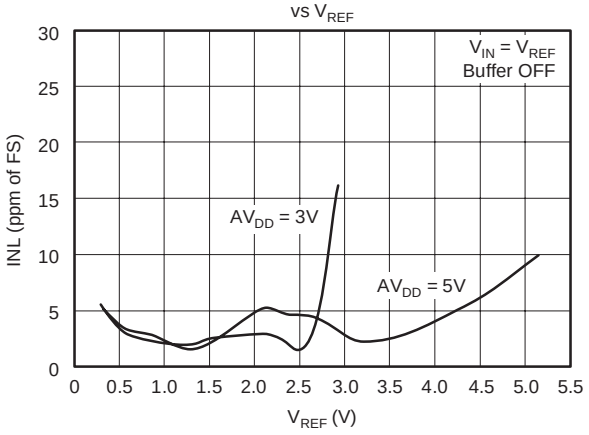
ADC INTEGRAL NONLINEARITY
vs INPUT VOLTAGE



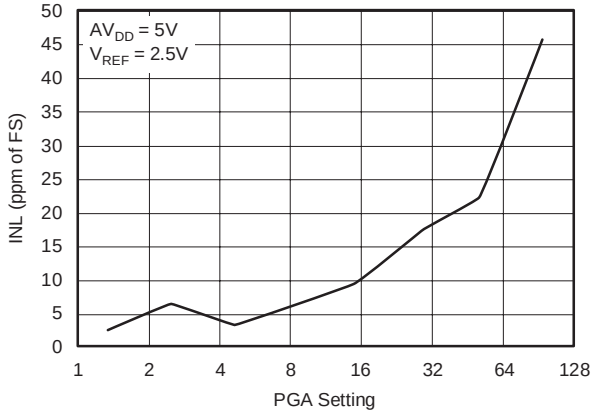
ADC INTEGRAL NONLINEARITY
vs INPUT SIGNAL



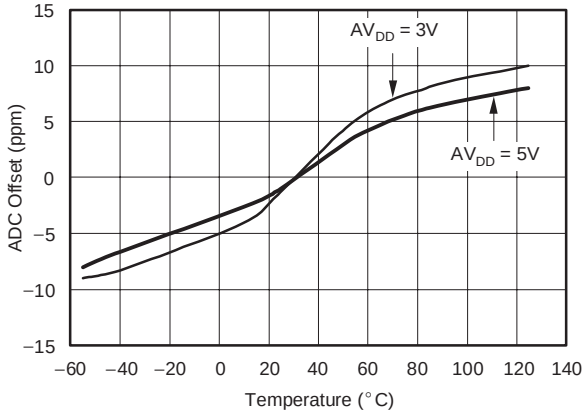
ADC INTEGRAL NONLINEARITY
vs V_{REF}



ADC INTEGRAL NONLINEARITY ERROR
vs PGA



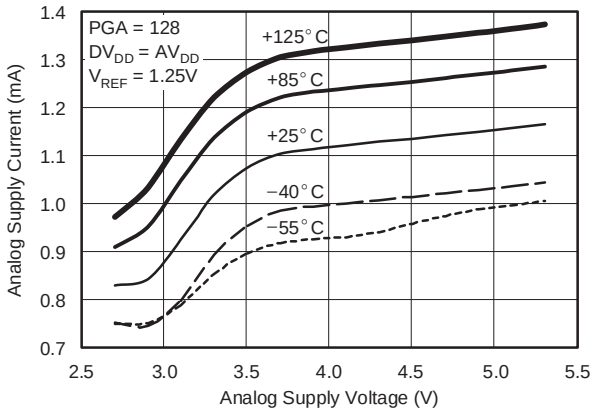
ADC OFFSET vs TEMPERATURE
(Offset Calibration at 25°C Only)



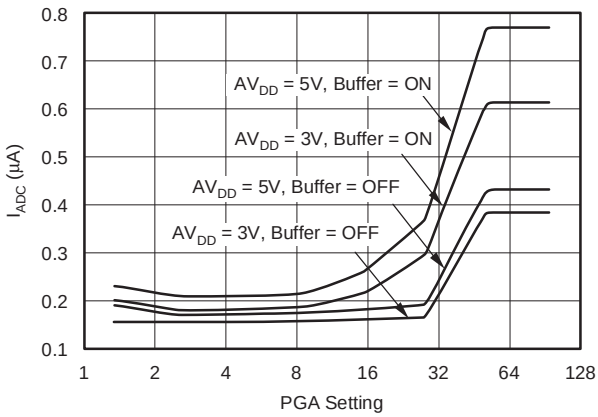
TYPICAL CHARACTERISTICS: ALL DEVICES (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

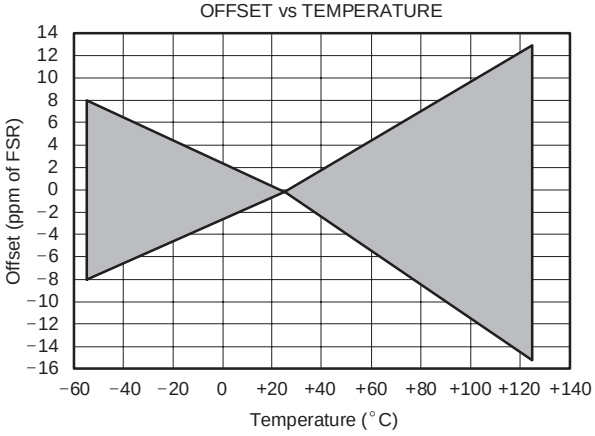
ANALOG SUPPLY CURRENT
vs ANALOG SUPPLY VOLTAGE



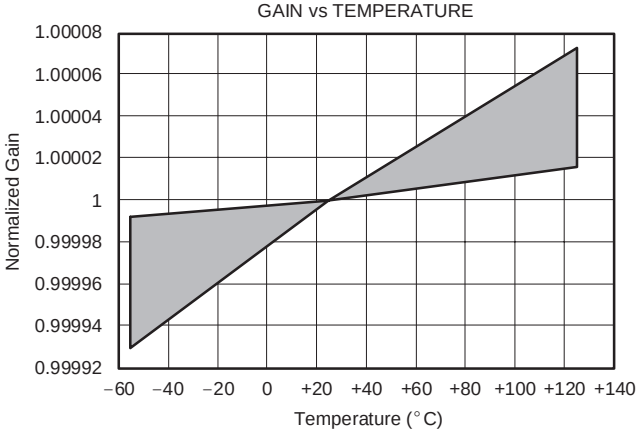
ADC POWER−SUPPLY CURRENT
vs PGA



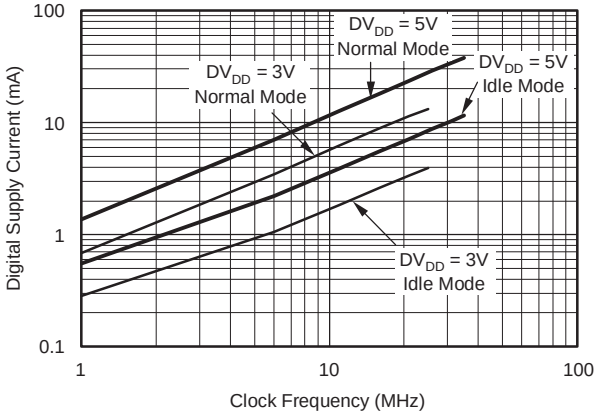
ADC OFFSET DAC:
OFFSET vs TEMPERATURE



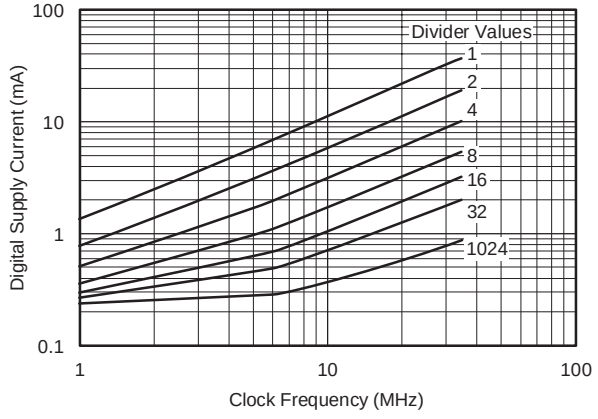
ADC OFFSET DAC:
GAIN vs TEMPERATURE



DIGITAL SUPPLY CURRENT
vs EXTERNAL CLOCK FREQUENCY



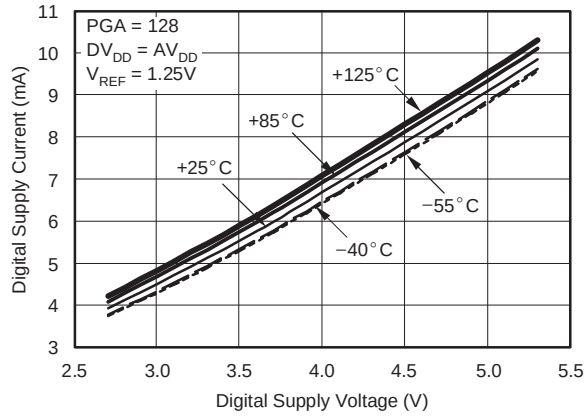
DIGITAL SUPPLY CURRENT vs CLOCK DIVIDER



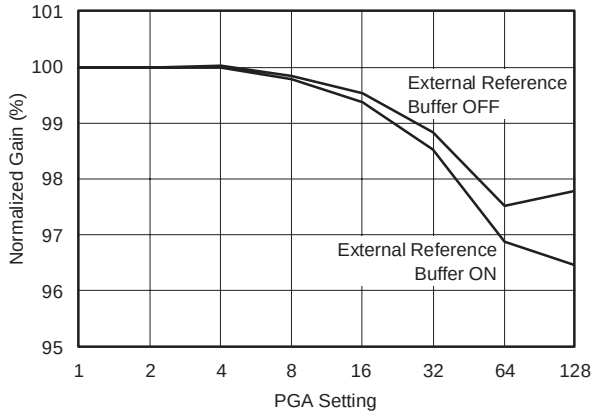
TYPICAL CHARACTERISTICS: ALL DEVICES (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and $V_{REF} \equiv$ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

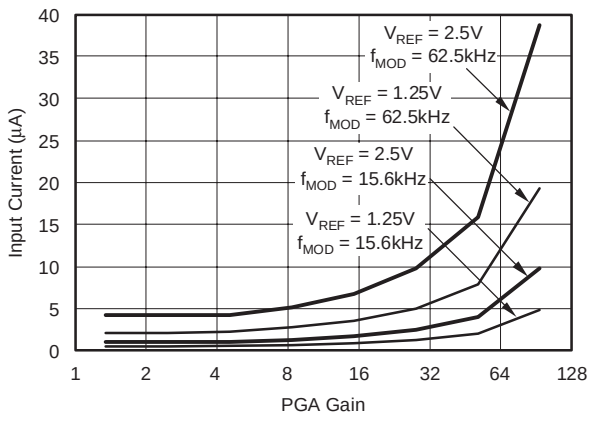
DIGITAL SUPPLY CURRENT
vs DIGITAL SUPPLY VOLTAGE



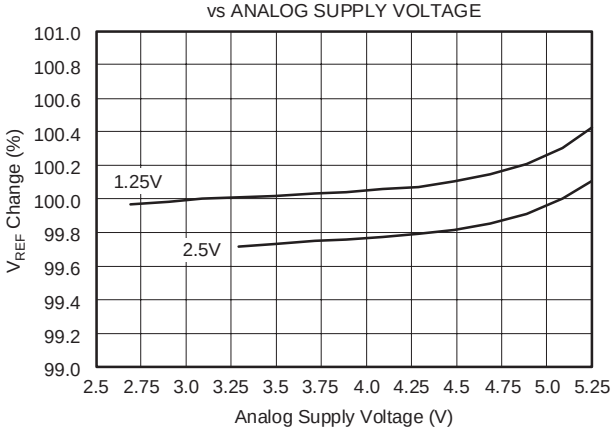
ADC NORMALIZED GAIN
vs PGA



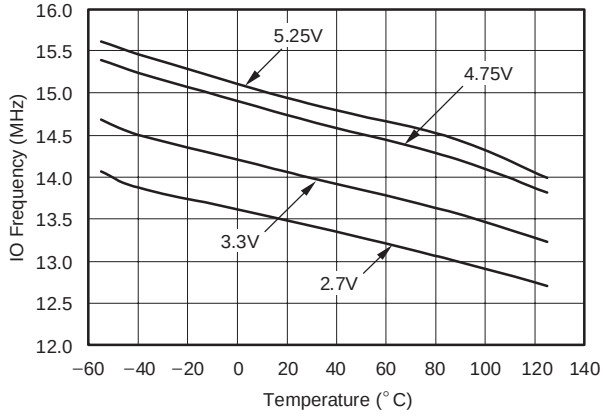
VOLTAGE REFERENCE INPUT CURRENT
vs PGA SETTING



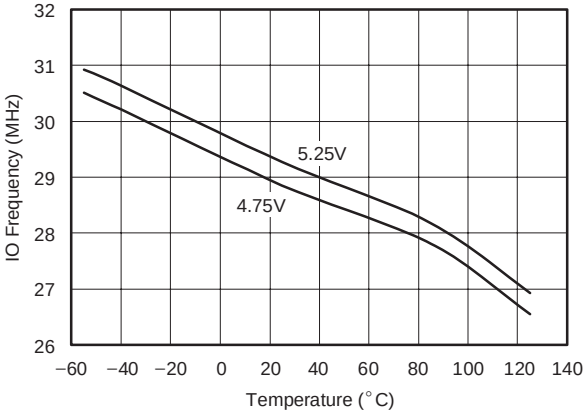
VOLTAGE REFERENCE CHANGE
vs ANALOG SUPPLY VOLTAGE



INTERNAL OSCILLATOR LOW−FREQUENCY MODE
vs TEMPERATURE



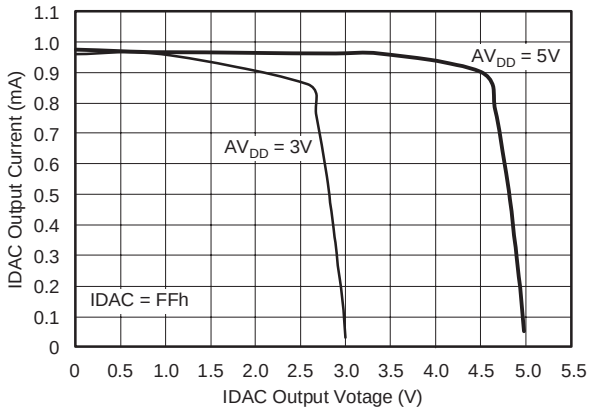
INTERNAL OSCILLATOR HIGH−FREQUENCY MODE
vs TEMPERATURE



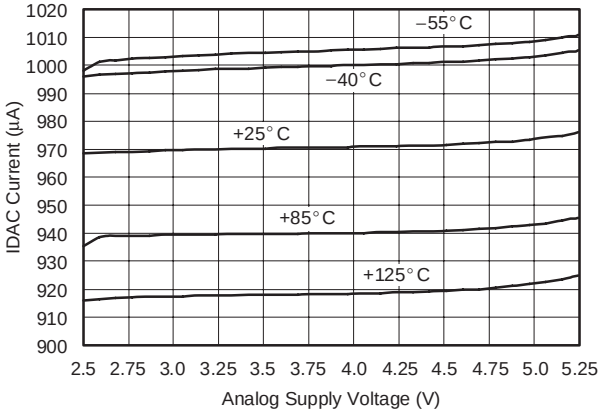
TYPICAL CHARACTERISTICS: ALL DEVICES (Continued)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, ADC Bipolar Mode, Buffer ON, and V_{REF} ≡ (REF IN+) − (REF IN−) = +2.5V, unless otherwise specified.

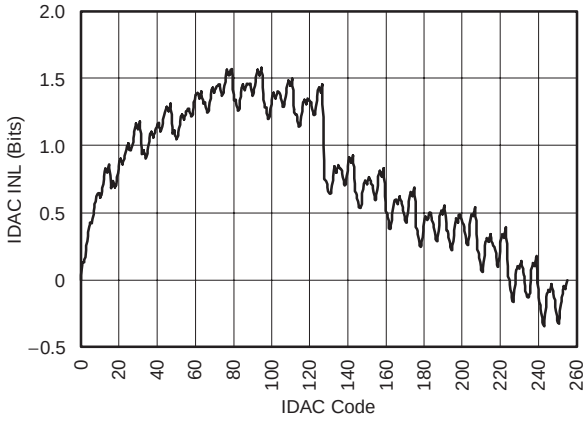
IDAC OUTPUT CURRENT
vs IDAC OUTPUT VOLTAGE



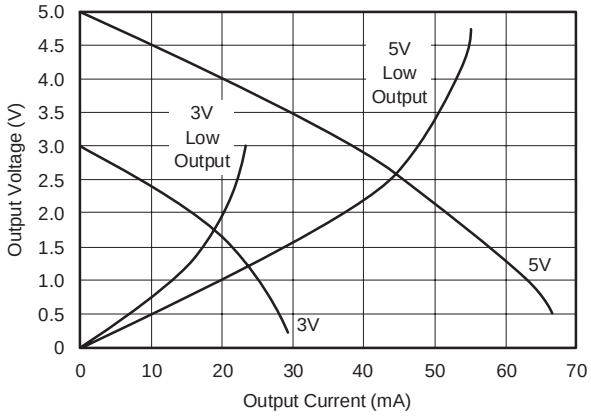
IDAC OUTPUT CURRENT AT TEMPERATURE
vs ANALOG SUPPLY VOLTAGE



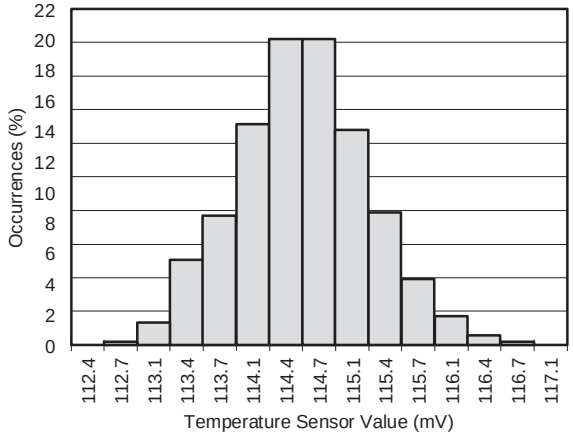
IDAC INTEGRAL NONLINEARITY
vs IDAC CODE



DIGITAL OUTPUT PIN VOLTAGE



HISTOGRAM OF
TEMPERATURE SENSOR VALUES



DESCRIPTION

The MSC1200Yx, MSC1201Yx, and MSC1202Yx are completely integrated families of mixed-signal devices incorporating a high-resolution, delta-sigma ADC, 8-bit cuurent output DAC, input multiplexer, burnout detect current sources, selectable buffered input, offset DAC, programmable gain amplifier (PGA), temperature sensor, voltage reference, 8-bit 8051 microcontroller, Flash Program Memory, Flash Data Memory, and Data SRAM, as shown in Figure 3. The MSC1200, MSC1201, and MSC1202 will be referred to as the MSC120x in this document, unless otherwise noted.

On-chip peripherals include an additional 32-bit summation register, basic SPI, basic I^2C, USART, two 8-bit digital input/output ports, a watchdog timer, low-voltage detect, on-chip power-on reset, brownout reset, timer/counters, system clock divider, PLL, on-chip oscillator, and external or internal interrupts.

The devices accept differential or single-ended signals directly from a transducer. The ADC provides 24 bits (MSC1200/01) or 16 bits (MSC1202) of resolution and 24 bits (MSC1200/01) or 16 bits (MSC1202) of no-missing-code performance using a $Sinc^3$ filter with a programmable sample rate. The ADC also has a selectable filter that allows for high-resolution, single-cycle conversions.

The microcontroller core is 8051 instruction set compatible. The microcontroller core is an optimized 8051 core that executes up to three times faster than the standard 8051 core, given the same clock source. This design makes it possible to run the device at a lower external clock frequency and achieve the same performance at lower power than the standard 8051 core.

The MSC120x allow users to uniquely configure the Flash Memory map to meet the needs of their applications. The Flash is programmable down to +2.7V using serial programming. Flash endurance is typically 1M Erase/Write cycles.

The parts have separate analog and digital supplies, which can be independently powered from +2.7V to +5.25V. At +3V operation, the power dissipation for the part is typically less than 3mW. The MSC1200 is available in a TQFP-48 package. The MSC1201 and MSC1202 are both available in a QFN-36 package.

The MSC120x are designed for high-resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation.

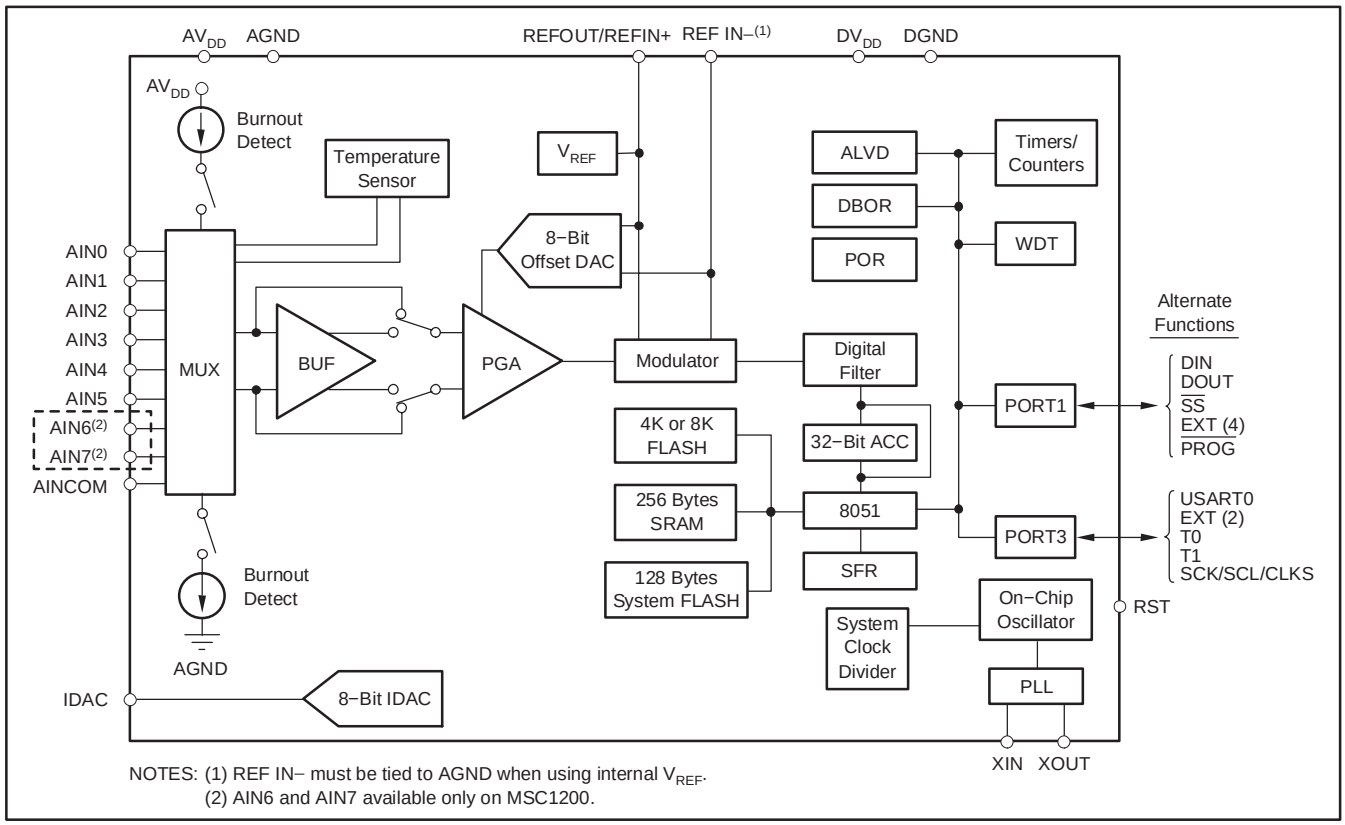


Figure 3. Block Diagram

ENHANCED 8051 CORE

All instructions in the MSC120x families perform exactly the same functions as they would in a standard 8051. The effects on bits, flags, and registers are the same; however, the timing is different. The MSC120x families use an efficient 8051 core that results in an improved instruction execution speed of between 1.5 and 3 times faster than the original core for the same external clock speed (4 clock cycles per instruction versus 12 clock cycles per instruction, as shown in Figure 4). This efficiency translates into an effective throughput improvement of more than 2.5 times, using the same code and same external clock speed. Therefore, a device frequency of 33MHz for the MSC120x actually performs at an equivalent execution speed of 82.5MHz compared to the standard 8051 core. This increased performance allows the device to be tun at slower clock speeds, which reduces system noise and power consumption, but provides greater throughput. This performance difference can be seen in Figure 5. The timing of software loops will be faster with the MSC120x. However, the timer/counter operation of the MSC120x may be maintained at 12 clocks per increment or optionally run at 4 clocks per increment.

The MSC120x also provide dual data pointers (DPTRs).

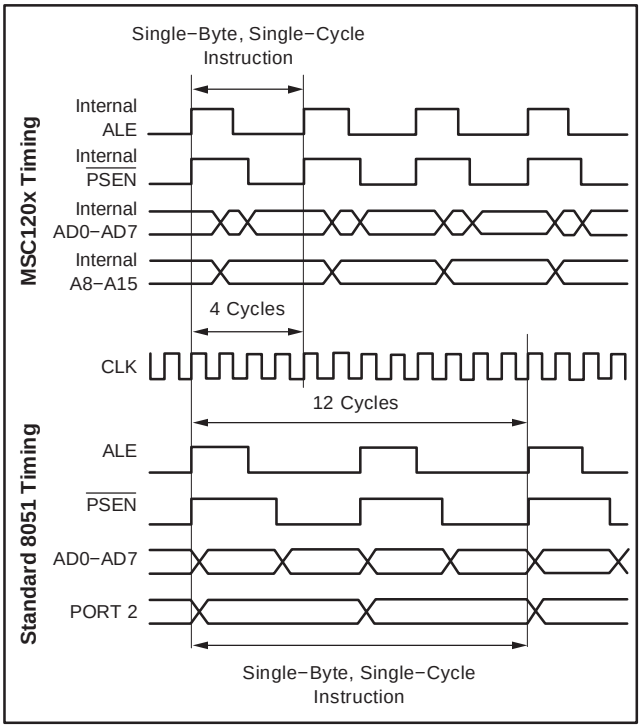


Figure 5. Comparison of MSC120x Timing to Standard 8051 Timing

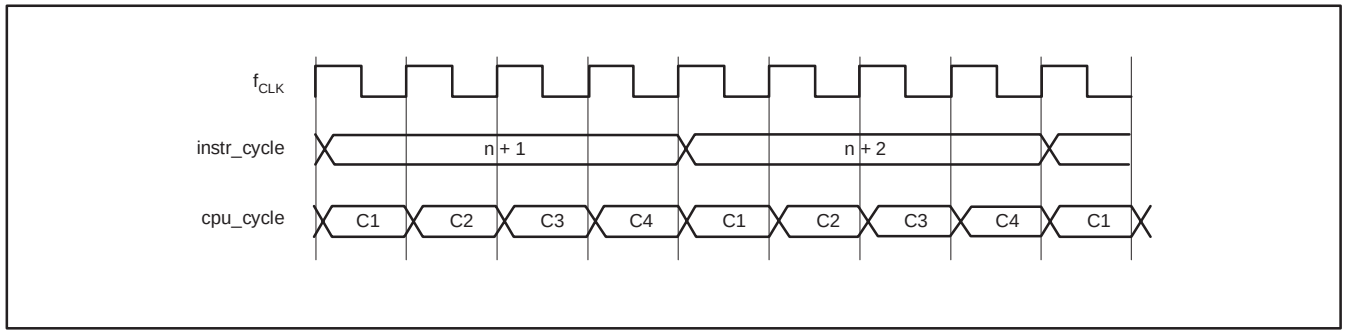


Figure 4. Instruction Timing Cycle

Furthermore, improvements were made to peripheral features that off-load processing from the core, and the user, to further improve efficiency. These iprovements allow for 32-bit addition, subtraction and shifting to be accomplished in a few instruction cycles, compared to hundreds of instruction cycles executed through software implementation. For instance, 32-bit accumulation can be done through the summation register to significantly reduce the processing overhead for multiple-byte data from the ADC or other sources.

Family Device Compatibility

The hardware functionality and pin configuration across the MSC120x families are fully compatible. To the user, the only difference between family members is the memory configuration. This design makes migration between family members simple. Code written for the MSC1200Y2, MSC1201Y2, or MSC1202Y2 can be executed directly on an MSC1200Y3, MSC1201Y3, or MSC1202Y3, respectively. (However, the ADC registers for the MSC1202 are mapped differently than the MSC1200 or MSC1201.) This gives the user the ability to add or subtract software functions and to migrate between family members. Thus, the MSC120x can become a standard device used across several application platforms.

Family Development Tools

The MSC120x are fully compatible with the standard 8051 instruction set. This compatibility means that users can develop software for the MSC120x with their existing 8051 development tools. Additionally, a complete, integrated development environment is provided with each demo board, and third-party developers also provide support.

Power-Down Modes

The MSC120x can power several of the on-chip peripherals and put the CPU into Idle mode. This is accomplished by shutting off the clocks to those sections, as shown in Figure 6.

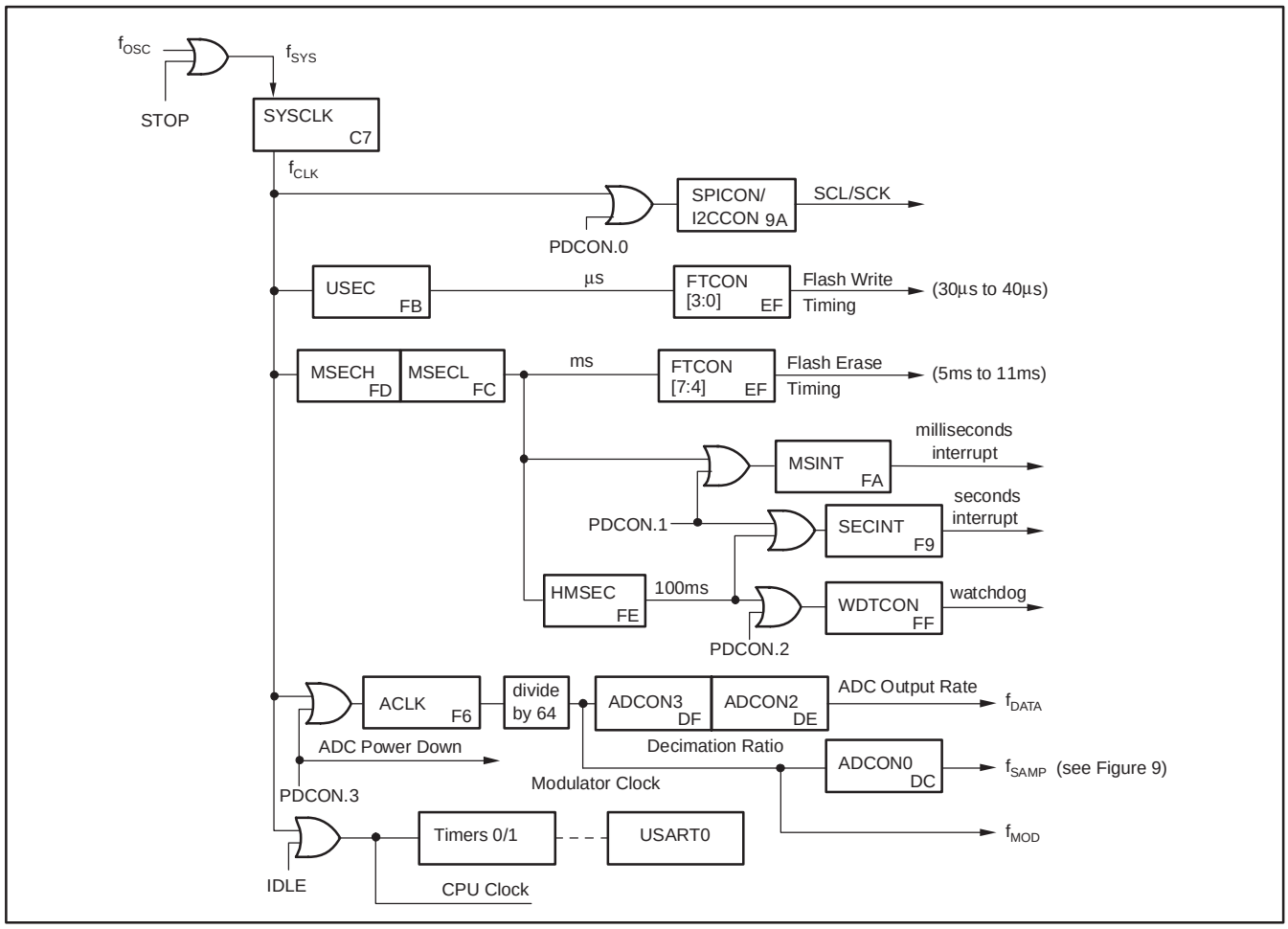
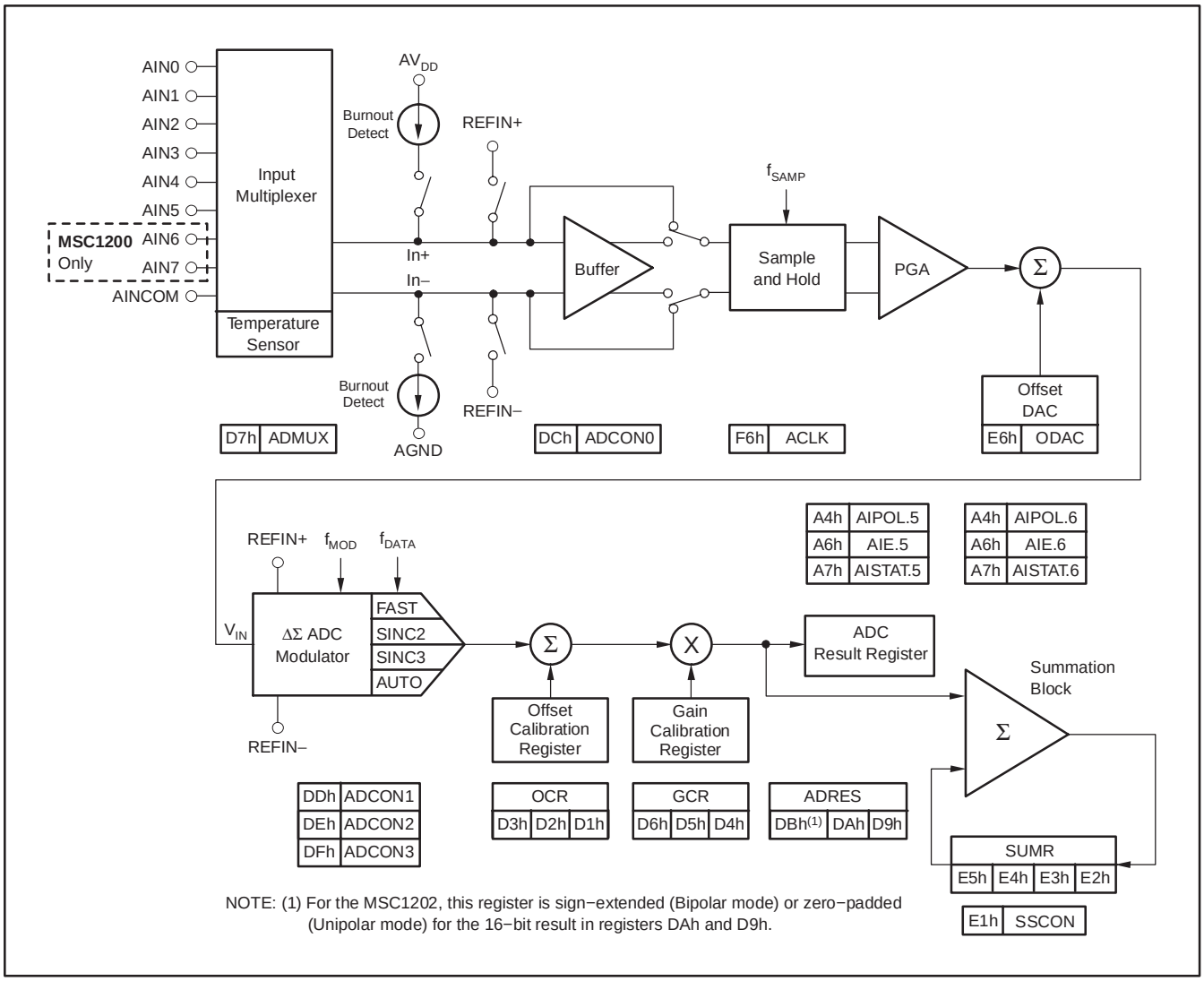


Figure 6. MSC120x Timing Chain and Clock Control

OVERVIEW

The MSC120x ADC structure is shown in Figure 7. The figure lists the components that make up the ADC, along with the corresponding special function register (SFR) associated with each component.

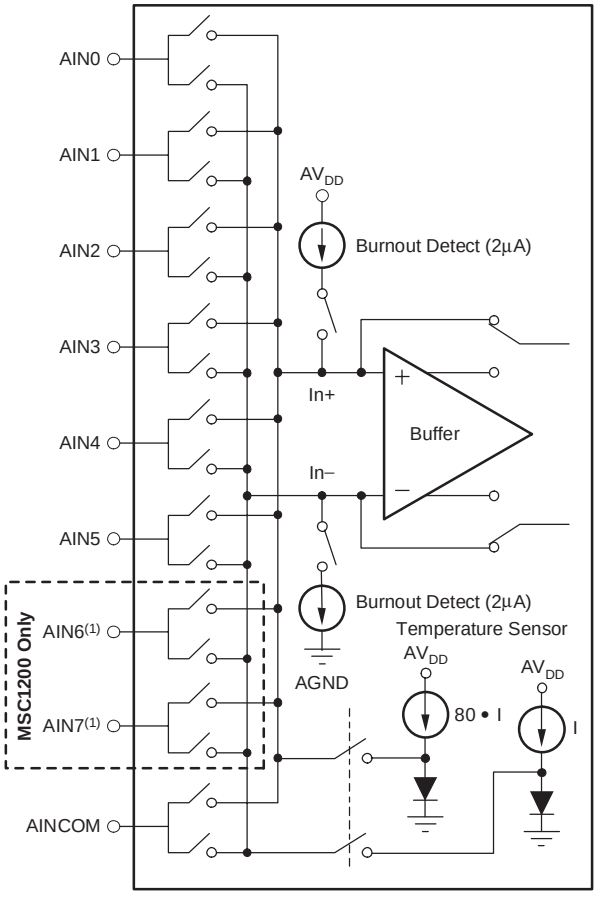


NOTE: (1) For the MSC1202, this register is sign−extended (Bipolar mode) or zero−padded (Unipolar mode) for the 16−bit result in registers DAh and D9h.

Figure 7. MSC120x ADC Structure

ADC INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected as the input channel, as shown in Figure 8. For example, if AIN0 is selected as the positive differential input channel, then any other channel can be selected as the negative differential input channel. With this method, it is possible to have up to six fully differential input channels. It is also possible to switch the polarity of the differential input pair to negate any offset voltages. In addition, current sources are supplied that will source or sink current to detect open or short circuits on the pins.



NOTE: (1) For MSC1201/MSC1202, AIN6 and AIN7 are tied to REFIN−.

Figure 8. Input Multiplexer Configuration

TEMPERATURE SENSOR

On-chip diodes provide temperature sensing capability. When the configuration register for the input mux is set to all 1s, the diodes are connected to the inputs of the ADC. All other channels are open. The internal device power dissipation affects the temperature sensor reading. It is recommended that the internal buffer be enabled for temperature sensor measurements.

BURNOUT DETECT

When the Burnout Detect (BOD) bit is set in the ADC control configuration register (ADCON0, SFR DCh), two current sources are enabled. The current source on the positive input channel sources approximately 2µA of current. The current source on the negative input channel sinks approximately 2µA. These current sources allow for the detection of an open circuit (full-scale reading) or short circuit (small differential reading) on the selected input differential pair. The buffer should be on for sensor burnout detection.

ADC INPUT BUFFER

The analog input impedance is always high, regardless of PGA setting (when the buffer is enabled). With the buffer enabled, the input voltage range is reduced and the analog power-supply current is higher. If the limitation of input voltage range is acceptable, then the buffer is always preferred.

The input impedance of the MSC120x without the buffer is 7MΩ/PGA. The buffer is controlled by the state of the BUF bit in the ADC control register (ADCON0, SFR DCh).

ADC ANALOG INPUT

When the buffer is not selected, the input impedance of the analog input changes with ACLK clock frequency (ACLK, SFR F6h) and gain (PGA). The relationship is:

$$\text{Impedance } (\Omega) = \frac{1}{f_{SAMP} \cdot C_S}$$

$$A_{IN} \text{ Impedance } (\Omega) = \left(\frac{1\text{MHz}}{\text{ACLK Frequency}}\right) \cdot \left(\frac{7\text{M}\Omega}{\text{PGA}}\right)$$

where ACLK frequency $(f_{ACLK}) = \frac{f_{CLK}}{\text{ACLK} + 1}$

and $f_{MOD} = \frac{f_{ACLK}}{64}$.

NOTE: The input impedance for PGA = 128 is the same as that for PGA = 64 (that is, 7MΩ/64).

Figure 9 shows the basic input structure of the MSC120x.

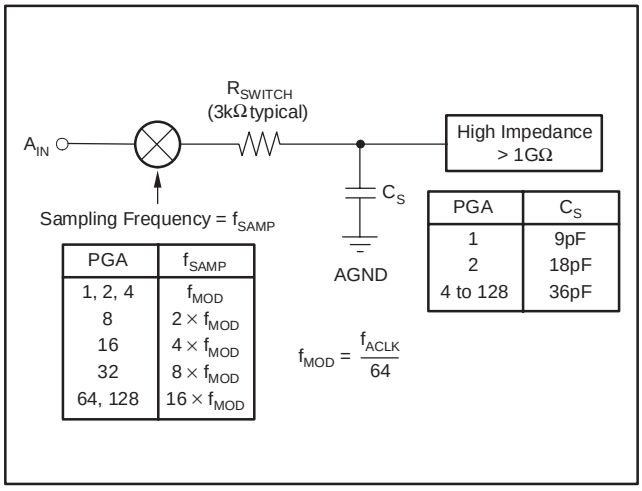


Figure 9. Analog Input Structure (without Buffer)

ADC PGA

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can actually improve the effective resolution of the ADC. For instance, with a PGA of 1 on a ±2.5V full-scale range (FSR), the ADC can resolve to 1.5µV. With a PGA of 128 on a ±19mV FSR, the ADC can resolve to 75nV. With a PGA of 1 on a ±2.5V FSR, it would require a 26-bit ADC to resolve 75nV, as shown in Table 1.

Table 1. ENOB versus PGA (Bipolar Mode)

PGA SETTING	FULL-SCALE RANGE (V)	MSC1200 MSC1201 ENOB(1) AT 10HZ (BITS)	MSC1202 ENOB(1) UP TO 200HZ (BITS)	RMS INPUT-REFERRED NOISE	
				MSC1200 MSC1201 (nV)	MSC1202 (µV)
1	±2.5	21.7	16	1468	76.3
2	±1.25	21.5	15.6	843	38.1
4	±0.625	21.4	15.5	452	19.1
8	±0.313	21.2	15.4	259	9.5
16	±0.156	20.8	15.4	171	4.8
32	±0.078	20.4	15.3	113	2.4
64	±0.039	20	15.2	74.5	12
128	±0.019	19	14.2	74.5	0.6

(1) ENOB = $\text{Log}_2(\text{FSR/RMS Noise}) = \text{Log}_2(2^{24}) - \text{Log}_2(\sigma_{CODES}) = 24 - \text{Log}_2(\sigma_{CODES})$

ADC OFFSET DAC

The analog output from the PGA can be offset by up to half the full-scale range of the ADC by using the ODAC register (SFR E6h). The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset.

ADC MODULATOR

The modulator is a single-loop, 2nd-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from CLK using the value in the Analog Clock register (ACLK, SFR F6h). The data output rate is:

$$\text{Data Rate} = f_{DATA} = \frac{f_{MOD}}{\text{Decimation Ratio}}$$

where $f_{MOD} = \frac{f_{CLK}}{(\text{ACLK} + 1) \cdot 64} = \frac{f_{ACLK}}{64}$.

and Decimation Ratio is set in [ADCON3:ADCON2]

ADC CALIBRATION

The offset and gain errors in the MSC120x, or the complete system, can be reduced with calibration. Calibration is controlled through the ADCON1 register (SFR DDh), bits CAL2:CAL0. Each calibration process takes seven t_{DATA} periods (data conversion time) to complete. Therefore, it takes 14 t_{DATA} periods to complete both an offset and gain calibration.

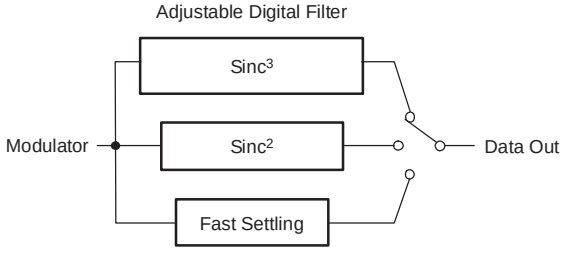
For system calibration, the appropriate signal must be applied to the inputs. It then computes an offset that will nullify offset in the system. The system gain calibration requires a positive full-scale differential input signal. It then computes a gain value to nullify gain errors in the system. Each of these calibrations will take seven t_{DATA} periods to complete.

Calibration should be performed after power on. It should also be done after a change in temperature, decimation ratio, buffer, power supply, voltage reference, or PGA. The offset DAC will affect offset calibration; therefore, the value of the offset should be zero before performing a calibration.

At the completion of calibration, the ADC Interrupt bit goes high, which indicates the calibration is finished and valid data is available.

ADC DIGITAL FILTER

The Digital Filter can use either the Fast Settling, $Sinc^2$, or $Sinc^3$ filter, as shown in Figure 10. In addition, the Auto mode changes the Sinc filter after the input channel or PGA is changed. When switching to a new channel, it will use the Fast Settling filter for the next two conversions, the first of which should be discarded. It will then use the $Sinc^2$ followed by the $Sinc^3$ filter to improve noise performance. This combines the low-noise advantage of the $Sinc^3$ filter with the quick response of the Fast Settling Time filter. The frequency response of each filter is shown in Figure 11.



FILTER SETTLING TIME

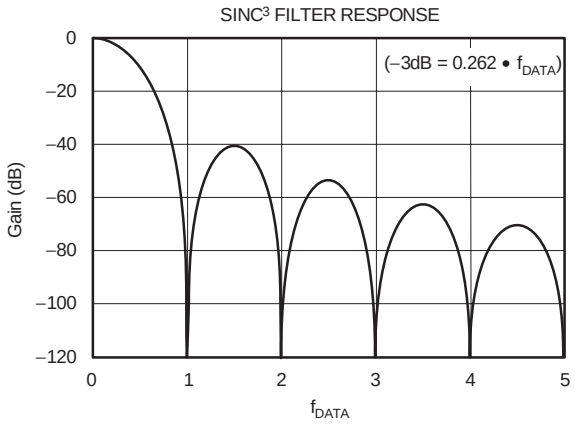
FILTER	SETTLING TIME (Conversion Cycles)(1)
$Sinc^3$	3
$Sinc^2$	2
Fast	1

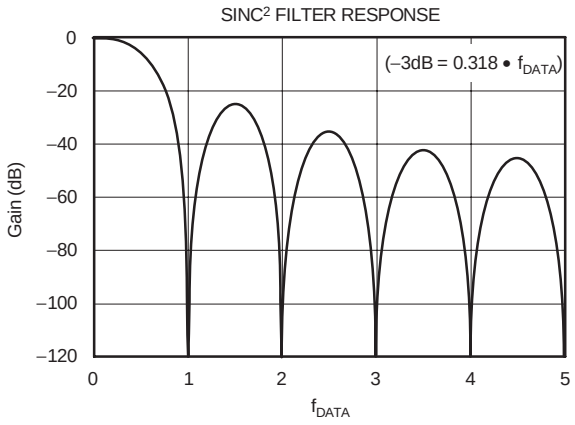
(1) With synchronized channel changes.

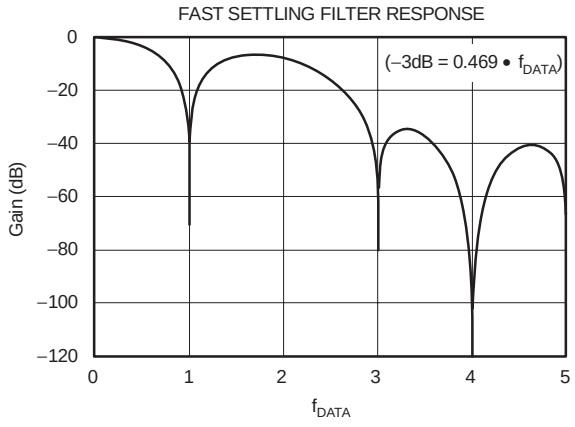
AUTO MODE FILTER SELECTION

CONVERSION CYCLE			
1	2	3	4+
Fast	Fast	$Sinc^2$	$Sinc^3$

Figure 10. Filter Step Responses







NOTE: f_{DATA} = Data Output Rate = $1/t_{DATA}$

Figure 11. Filter Frequency Responses

VOLTAGE REFERENCE

The MSC120x can use either an internal or external voltage reference. The voltage reference selection is controlled via ADC Control Register 0 (ADCON0, SFR DCh). The default power-up configuration for the voltage reference is 2.5V internal.

The internal voltage reference can be selected as either 1.25V or 2.5V. The analog power supply (AV_{DD}) must be within the specified range for the selected internal voltage reference. The valid ranges are: V_{REF} = 2.5 internal (AV_{DD} = 3.3V to 5.25V) and V_{REF} = 1.25 internal (AV_{DD} = 2.7V to 5.25V). If the internal V_{REF} is selected, then AGND must be connected to REFIN−. The REFOUT/REFIN+ pin should also have a 0.1µF capacitor connected to AGND as close as possible to the pin. If the internal V_{REF} is not used, then V_{REF} should be disabled in ADCON0.

If the external voltage reference is selected, it can be used as either a single-ended input or differential input, for ratiometric measures. When using an external reference, it is important to note that the input current will increase for V_{REF} with higher PGA settings and with a higher modulator frequency. The external voltage reference can be used over the input range specified in the *Electrical Characteristics* section.

IDAC

The 8-bit IDAC in the MSC120x provides a current source that can be used for ratiometric measurements. The IDAC operates from its own voltage reference and is not dependent on the ADC voltage reference. The full-scale output current of the IDAC is approximately 1mA (within the compliance voltage range). The equation for the IDAC output current is:

$$IDAC_{OUT}\ \mu A \approx IDAC \cdot 3.9\mu A \text{ (at } 25^{\circ}C)$$

The IDAC output voltage cannot exceed the compliance voltage of AV_{DD} − 1.5V.

RESET

The MSC120x can be reset from the following sources:

- Power-on reset
- External reset
- Software reset
- Watchdog timer reset
- Brownout reset

An external reset is accomplished by taking the RST pin high for two t_{OSC} periods, followed by taking the RST pin low. A software reset is accomplished through the System Reset register (SRTST, 0F7h). A watchdog timer reset is enabled and controlled through Hardware Configuration Register 0 (HCR0) and the Watchdog Timer register (WDTCON, 0FFh). A brownout reset is enabled through Hardware Configuration Register 1 (HCR1). Power-on reset and external reset complete after 2^{17} clock cycles, using the internal oscillator in low-frequency mode. Brownout reset, watchdog timer reset, and software reset complete after 2^{15} clock cycles, using the active clock source.

All sources of reset cause the digital pins to be pulled high from the initiation of the reset procedure. For an external reset, taking the RST pin high stops device operation (crystal oscillation, internal oscillator, or PLL circuit operation) and causes all digital pins to be pulled high from that point. Taking the RST pin low initiates the reset procedure.

A recommended external reset circuit is shown in Figure 12. The serial 10kΩ resistor is recommended for any external reset circuit configuration. For proper execution of the reset procedure, it is necessary to keep the AV_{DD} supply above 2.0V during the reset procedure.

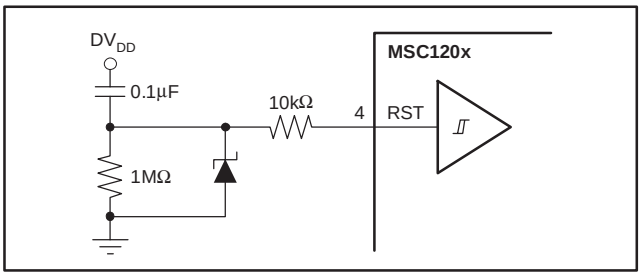


Figure 12. Typical Reset Circuit

Note that pin P1.0/$\overline{PROG}$ defines operation of the device after reset. If P1.0/$\overline{PROG}$ is not connected or pulled high during reset, the device will enter User Application mode (UAM). If P1.0/$\overline{PROG}$ is pulled low during reset, the device will enter Serial Flash Programming mode (SFPM). Refer to the *Electrical Characteristics* section for timing information.

POWER ON RESET

The on-chip Power On Reset (POR) circuitry releases the device from reset when $DV_{DD} \approx 2.0V$. The power supply ramp rate does not affect the POR. If the power supply falls below 1.0V for longer than 200ms, the POR will execute. If the power supply falls below 1.0V for less than 200ms, unexpected operation may occur. If these conditions are not met, the POR will not execute. For example, a negative spike on the DV_{DD} supply that does not remain below 1.0V for at least 200ms, will not initiate a POR.

If the Digital Brownout Reset circuit is on, the POR circuit has no effect.

DIGITAL BROWNOUT RESET

The Digital Brownout Reset (DBOR) is enabled through HCR1. If the conditions for proper POR are not met, the DBOR can be used to ensure proper device operation. The DBOR will hold the state of the device when the power supply drops below the threshold level programmed in HCR1, and then generate a reset when the supply rises above the threshold level. Note that as the device is released from reset and program execution begins, the device current consumption may increase, which can result in a power supply voltage drop, which may initiate another brownout condition. Also, the DBOR comparison is done against an analog reference; therefore, AV_{DD} must be within its valid operating range for DBOR to function.

The DBOR level should be chosen to match closely with the application. That is, with a high external clock frequency, the DBOR level should match the minimum operating voltage range for the device or improper operation may still occur.

ANALOG LOW-VOLTAGE DETECT

The MSC120x contain an analog low-voltage detect circuit. When the analog supply drops below the value programmed in LVDCON (SFR E7h), an interrupt is generated, and/or the flag is set.

IDLE MODE

Idle mode is entered by setting the IDLE bit in the Power Control register (PCON, 087h). In Idle mode, the CPU, Timer0, Timer1, and USART are stopped, but all other peripherals and digital pins remain active. The device can be returned to active mode via an active internal or external interrupt. This mode is typically used for reducing power consumption between ADC samples.

By configuring the device prior to entering Idle mode, further power reductions can be achieved (while in Idle mode). These power reductions include powering down peripherals not in use in the PDCON register (0F1h), and reducing the system clock frequency by using the System Clock Divider register (SYSCLK, 0C7h).

STOP MODE

Stop mode is entered by setting the STOP bit in the Power Control register (PCON, 087h). In Stop mode, all internal clocks are halted. This mode has the lowest power consumption. The device can be returned to active mode only via an external reset or power-on reset (not a brownout reset).

By configuring the device prior to entering Stop mode, further power reductions can be achieved (while in Stop mode). These power reductions include halting the external clock into the device, configuring all digital I/O pins as open drain with low output drive, disabling the ADC buffer, disabling the internal V_{REF}, and setting PDCON to 0FFh to power down all peripherals.

In Stop mode, all digital pins retain their values.

POWER CONSUMPTION CONSIDERATIONS

The following suggestions will reduce current consumption in the MSC120x devices:

1. Use the lowest supply voltage that will work in the application for both AV_{DD} and DV_{DD}.
2. Use the lowest clock frequency that will work in the application.
3. Use Idle mode and the system clock divider whenever possible. Note that the system clock divider also affects the ADC clock.
4. Avoid using 8051-compatible I/O mode on the I/O ports. The internal pull-up resistors will draw current when the outputs are low.
5. Use the delay line for Flash Memory control by setting the FRCM bit in the FMCON register (SFR EEh).
6. Power down the internal oscillator in External Clock mode by setting the PDICLK bit in the PDCON register (SFR F1h).
7. Power down peripherals when they are not needed. Refer to SFR PDCON, LVDCON, ADCON0, and IDAC.

CLOCKS

The MSC120x can operate in three separate clock modes: Internal Oscillator mode (IOM), External Clock mode (ECM), and Phase Lock Loop (PLL) mode. A block diagram is shown in Figure 13. The clock mode for the MSC120x is selected via the CLKSEL bits in HCR2. IO low-frequency (LF) mode is the default mode for the device.

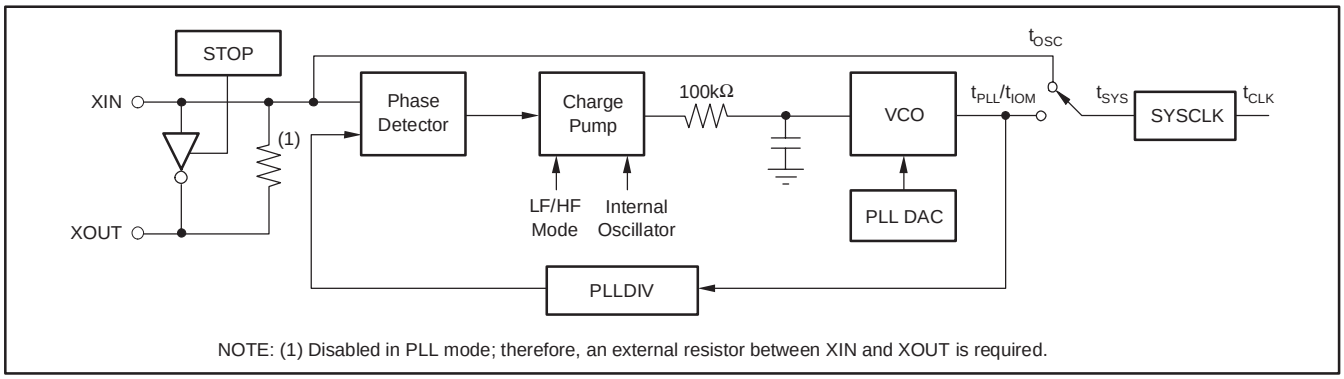
Serial Flash Programming mode (SFPM) uses IO LF mode (the HCR2 and CLKSEL bits have no effect). Table 2 shows the active clock mode for the various startup conditions during User Application mode.

Internal Oscillator

In IOM, the CPU executes either in LF mode (if HCR2, CLKSEL = 111) or high-frequency (HF) mode (if HCR2, CLKSEL = 110 and DV_{DD} = 5.0V). In this mode, XIN must be grounded or tied to supply.

External Clock

In ECM (HCR2, CLKSEL = 011), the CPU can execute from an external crystal, external ceramic resonator, external clock, or external oscillator. If an external clock is detected at startup, then the CPU will begin execution in ECM after startup. If an external clock is not detected at startup, then the device will revert to the mode shown in Table 2.



NOTE: (1) Disabled in PLL mode; therefore, an external resistor between XIN and XOUT is required.

Figure 13. Clock Block Diagram

Table 2. Active Clock Modes

SELECTED CLOCK MODE		HCR2, CLKSEL2:0	STARTUP CONDITION(1)	ACTIVE CLOCK MODE (f_{SYS})
External Clock Mode (ECM)		010	Active clock present at XIN	External Clock Mode
			No clock present at XIN	IO LF Mode
Internal Oscillator Mode (IOM)(2)	IO LF Mode	111	N/A	IO LF Mode
	IO HF Mode	110	N/A	IO HF Mode
PLL(3)	PLL LF Mode	101	Active 32.768kHz clock at XIN	PLL LF Mode
			No clock present at XIN	Nominal 50% of IO LF Mode
	PLL HF Mode	100	Active 32.768kHz clock at XIN	PLL HF Mode
			No clock present at XIN	Nominal 50% of IO HF Mode

(1) Clock detection is only done at startup; refer to *Serial Flash Programming Timing* parameter t_{RFD} in Figure 2.
(2) XIN must not be left floating; it must be tied high or low or parasitic oscillation may occur.
(3) PLL operation requires that both AV_{DD} and DV_{DD} are within their specified ranges.

PLL

In PLL mode (HCR2, CLKSEL = 101 or HCR2, CLKSEL = 100), the CPU can execute from an external 32.768kHz crystal. This mode enables the use of a PLL circuit that synthesizes the selected clock frequencies (PLL LF mode or PLL HF mode). If an external clock is detected at startup, then the CPU begins execution in PLL mode after startup. If an external clock is not detected at startup, then the device reverts to the mode shown in Table 2. The status of the PLL can be determined by first writing the PLLLOCK bit (enable) and then reading the PLLLOCK status bit in the PLLH SFR.

The frequency of the PLL is preloaded with default trimmed values. However, the PLL frequency can be fine-tuned by writing to the PLLH and PLLL SFRs. The equation for the PLL frequency is:

$$\text{PLL Frequency} = ([\text{PLLH:PLLL}] + 1) \bullet f_{OSC}$$

where f_{OSC} = 32.768kHz.

The default value for PLL LF mode is automatically loaded into the PLLH and PLLL SFRs.

For different connections to external clocks, see Figure 14, Figure 15, and Figure 16.

For PLL HF mode, the value of PLL[9:0] is automatically doubled in hardware; however, since PLL[9:0] is writable, it can also be modified by writing to the respective SFRs.

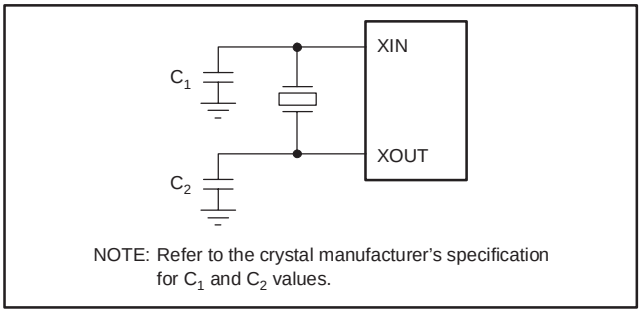


Figure 14. External Crystal Connection

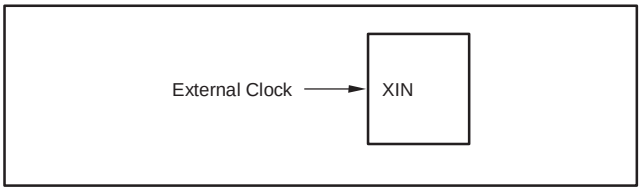


Figure 15. External Clock Connection

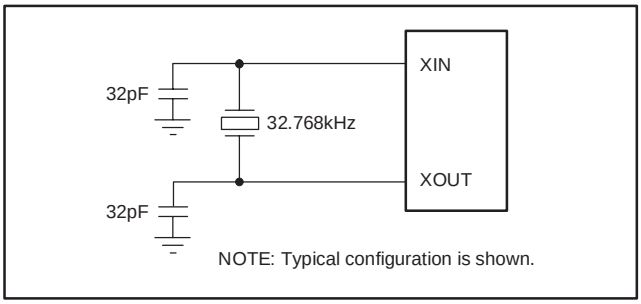


Figure 16. PLL Connection

SPI

The MSC120x implement a basic SPI interface that includes the hardware for simple serial data transfers. Figure 17 shows a block diagram of the SPI. The peripheral supports master and slave modes, full duplex data transfers, both clock polarities, both clock phases, bit order, and slave select.

The timing diagram for supported SPI data transfers is shown in Figure 18.

The I/O pins needed for data transfer are Data In (DIN), Data Out (DOUT) and serial clock (SCK). The slave select ($\overline{SS}$) pin can also be used to control the output of data on DOUT.

The DIN pin is used for shifting data in for both master and slave modes.

The DOUT pin is used for shifting data out for both master and slave modes.

The SCK pin is used to synchronize the transfer of data for both master and slave modes. SCK is always generated by the master. The generation of SCK in master mode can be done either in software (by simply toggling the port pin), or by configuring the output on the SCK pin via PASEL (SFR F2h). A list of the most common methods of generating SCK follows, but the complete list of clock sources can be found by referring to the PASEL SFR.

- Toggle SCK by setting and clearing the port pin.
- Memory Write Pulse ($\overline{WR}$) that is idle high. Whenever an external memory write command (MOVX) is executed, a pulse is seen on P3.6. This method can be used only if CPOL is set to ‘1’.
- Memory Write Pulse toggle version. In this mode, SCK toggles whenever an external write command (MOVX) is executed.
- T0_Out signal can be used as a clock. A pulse is generated on SCK whenever Timer 0 expires. The idle state of the signal is low, so this can be used only if CPOL is cleared to ‘0’.
- T0_Out toggle. SCK toggles whenever Timer 0 expires.
- T1_Out signal can be used as a clock. A pulse is generated whenever Timer 1 expires. The idle state of the signal is low, so this can be used only if CPOL is cleared to ‘0’.
- T1_Out toggle. SCK toggles whenever Timer 1 expires.

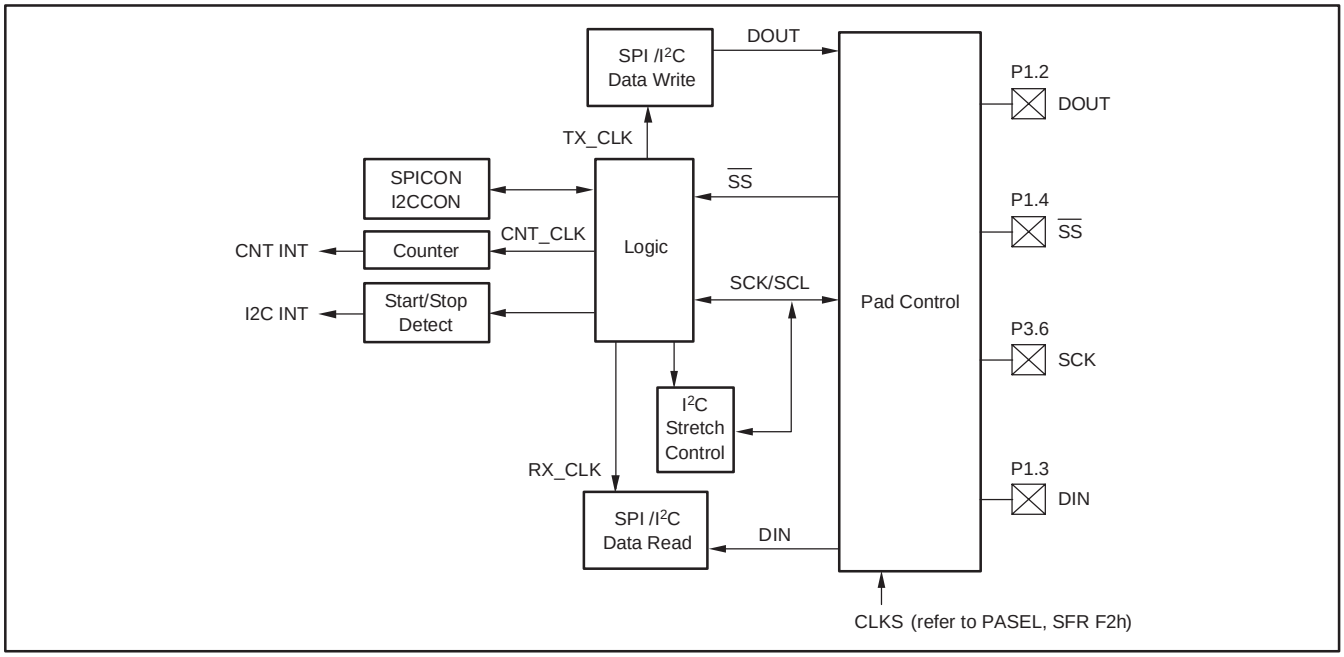


Figure 17. SPI/I2C Block Diagram

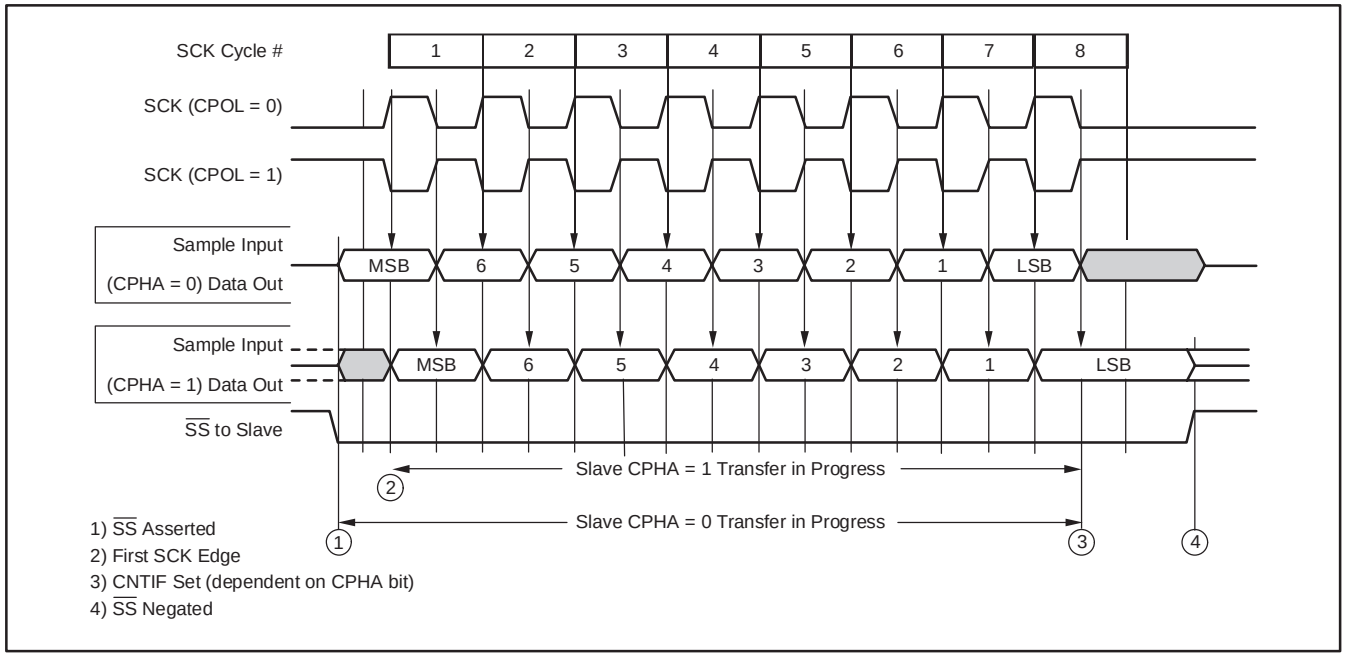


Figure 18. SPI Timing Diagram

The $\overline{SS}$ pin can be used to control the output of data on DOUT when the MSC120x is in slave mode. The $\overline{SS}$ function is enabled or disabled by the ESS bit of the SPICON SFR. When enabled, the $\overline{SS}$ input of a slave device must be externally asserted before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. When $\overline{SS}$ is high, data will not be shifted into the shift register, nor will the counter increment. When SPI is enabled, $\overline{SS}$ also controls the drive of the line DOUT (P1.2). When $\overline{SS}$ is low in slave mode, the DOUT pin will be driven and when $\overline{SS}$ is high, DOUT will be high impedance.

The SPI generates interrupt ECNT (AIE.2) to indicate that the transfer/reception of the byte is complete. The interrupt goes high whenever the counter value is equal to 8 (indicating that eight SCKs have occurred). The interrupt is cleared on reading or writing to the SPIDATA register. During the data transfer, the actual counter value can be read from the SPICON SFR.

Power Down

The SPI is powered down by the PDSPI bit in the power control register (PDCON). This bit needs to be cleared to enable the SPI function. When the SPI is powered down, pins P1.2, P1.3, P1.4, and P3.6 revert to general-purpose I/O pins.

Application Flow

This section explains the typical application usage flow of SPI in master and slave modes.

Master Mode Application Flow

1. Configure the port pins.
2. Configure the SPI.
3. Assert $\overline{SS}$ to enable slave communication (if applicable).
4. Write data to SPIDATA.
5. Generate eight SCKs.
6. Read the received data from SPIDATA.

Slave Mode Application Flow

1. Configure the ports pins.
2. Enable $\overline{SS}$ (if applicable).
3. Configure the SPI.
4. Write data to SPIDATA.
5. Wait for the Count Interrupt (eight SCKs).
6. Read the data from SPIDATA.

CAUTION:
If SPIDATA is not read before the next SPI transaction, the ECNT interrupt will be removed and the previous data will be lost.

I²C

The I/O pins needed for I²C transfer are serial clock (SCL) and serial data (SDA—implemented by connecting DIN and DOUT externally). The I²C transfer timing is shown in Figure 19.

The MSC120x I²C supports:

1. Master or slave I²C operation (control in software)
2. Standard or fast modes of transfer
3. Clock stretching
4. General call

When used in I²C mode, pins DIN (P1.3) and DOUT (P1.2) should be tied together externally. The DIN pin should be configured as an input pin and the DOUT pin should be configured as open drain or standard 8051 by setting the P1DDR (DOUT should be set high so that the bus is not pulled low).

The MSC120x I²C can generate two interrupts:

1. I²C interrupt for START/STOP interrupt (AIE.3)
2. CNT interrupt for bit counter interrupt (AIE.2)

The START/STOP interrupt is generated when a START condition or STOP condition is detected on the bus. The bit counter generates an interrupt on a complete (8-bit) data transfer and also after the transfer of the ACK/NACK.

The bit counter for serial transfer is always incremented on the falling edge of SCL and can be reset by reading or writing to I2CDATA (SFR 9Bh) or when a START/STOP condition is detected. The bit counter can be polled or used as an interrupt. The bit counter interrupt occurs when the bit counter value is equal to 8, indicating that eight bits of data have been transferred. I²C mode also allows for interrupt generation on one bit of data transfer (I2CCON.CNTSEL). This can be used for ACK/NACK interrupt generation. For instance, the I²C interrupt can be configured for 8-bit interrupt detection; on the eighth bit, the interrupt is generated. During this interrupt, the clock is stretched (SCL held low) if the DCS bit is set. The interrupt can then be configured for 1-bit detection (which terminates clock stretching). The ACK/NACK can be written by the software, which will terminate clock stretching. The next interrupt will be generated after the ACK/NACK has been latched by the receiving device. The interrupt is cleared on reading or writing to the I2CDATA register. If I2CDATA is not read before the next data transfer, the interrupt will be removed and the previous data will be lost.

Master Operation

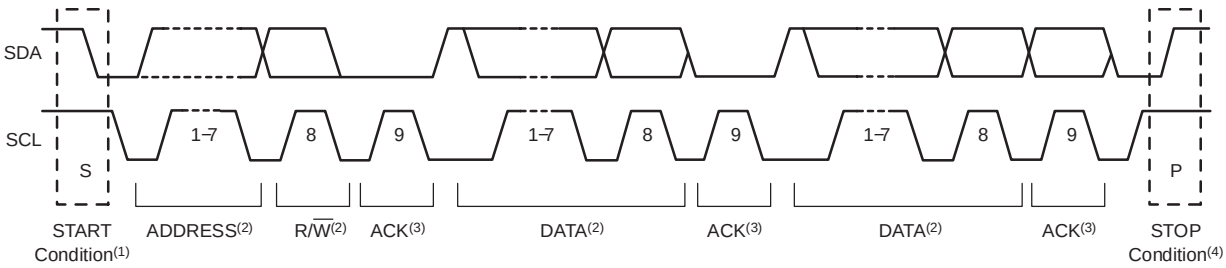
The source for the SCL is controlled in the PASEL register or can be generated in software.

Transmit

The serial data must be stable on the bus while SCL is high. Therefore, the writing of serial data to I2CDATA must be coordinated with the generation of the SCL, since SDA transitions on the bus may be interpreted as a START or STOP while SCL is high. The START and STOP conditions on the bus must be generated in software. After the serial data has been transmitted, the generation of the ACK/NACK clock must be enabled by writing 0xFFh to I2CDATA. This allows the master to read the state of ACK/NACK.

Receive

The serial data is latched into the receive buffer on the rising edge of SCL. After the serial data has been received, ACK/NACK is generated by writing 0x7Fh (for ACK) or 0xFFh (for NACK) to I2CDATA.



NOTES: (1) Generate in software; write 0x7F to I2CDATA.
(2) I2CDATA register.
(3) Generate in software. Can enable bit count = 1 interrupt prior to ACK/NACK for interrupt use. Generate ACK by writing 0x7F to I2CDATA; generate NACK by writing 0xFF to I2CDATA.
(4) Generate in software; write 0xFF to I2CDATA.

Figure 19. Timing Diagram for I²C Transmission and Reception

Slave Operation

Slave operation is supported, but address recognition, R/$\overline{W}$ determination, and ACK/NACK must be done under software control. The Disable Clock Stretch (DCS) bit can be set to disable clock stretching. When the DCS bit is set, the device will no longer stretch the clock and will not generate interrupts. This bit can be used to disable clock stretch interrupts when there is no address match. This bit is automatically cleared when a start or repeated start condition occurs.

Transmit

Once address recognition, R/$\overline{W}$ determination, and ACK/NACK are complete, the serial data to be transferred can be written to I2CDATA. The data is automatically shifted out based on the master SCL. After data transmission, CNTIF is generated and SCL is stretched by the MSC120x until the I2CDATA register is written with a 0xFFh. The ACK/NACK from the master can then be read.

Receive

Once address recognition, R/$\overline{W}$ determination, and ACK/NACK are complete, I2CDATA must be written with 0xFFh to enable data reception. Upon completion of the data shift, the MSC120x generates the CNT interrupt and stretches SCL. Received data can then be read from I2CDATA. After the serial data has been received, ACK/NACK is generated by writing 0x7Fh (for ACK) or 0xFFh (for NACK) to I2CDATA. The write to I2CDATA clears the CNT interrupt and clock stretch.

MEMORY MAP

The MSC120x contain on-chip SFR, Flash Memory, Configuration Memory, Scratchpad SRAM Memory, and Boot ROM. The SFR registers are primarily used for control and status. The standard 8051 features and additional peripheral features of the MSC120x are controlled through the SFR. Reading from an undefined SFR returns zero. Writing to undefined SFR registers is not recommended and will have indeterminate effects.

Flash Memory is used for both Program Memory and Data Memory; however, program execution can only occur from Program Memory. Program/Data Memory partition size is selectable. The partition size is set through HCR0 (in the Configuration Memory), which is programmed serially. Both Program and Data Flash Memory are erasable and writable (programmable) in UAM. Erase and write timing of Flash Memory is controlled in the Flash Memory Timing Control register (FTCON, SFR 0EFh). As an added precaution, a lock feature can be activated through HCR0, which disables erase/write operation to 4kB of Program Flash Memory or the entire Program Flash Memory in UAM.

FLASH MEMORY

The page size for Flash memory is 64 bytes. The respective page must be erased before it can be written to, regardless of whether it is mapped to Program memory or Data memory space. The MSC120x use a memory addressing scheme that separates Program Memory (FLASH/ROM) from Data Memory (FLASH/RAM). Addressing of program and data segments can overlap since they are accessed by different instructions.

The MSC120x have three hardware configuration registers (HCR0, HCR1, and HCR2) that are programmable only during Flash Memory Programming mode.

The MSC120x allow the user to partition the Flash Memory between Program Memory and Data Memory. For instance, the MSC120xY3 contain 8kB of Flash Memory on-chip. Through the hardware configuration registers, the user can define the partition between Program Memory (PM) and Data Memory (DM), as shown in Table 3, Table 4, and Figure 20. The MSC120x families offer two memory configurations.

Table 3. Flash Memory Partitioning

HCR0	MSC120xY2		MSC120xY3	
DFSEL	PM	DM	PM	DM
00	2kB	2kB	4kB	4kB
01	2kB	2kB	6kB	2kB
10	3kB	1kB	7kB	1kB
11 (default)	4kB	0kB	8kB	0kB

Table 4. Flash Memory Partitioning Addresses

HCR0	MSC120xY2		MSC120xY3	
DFSEL	PM	DM	PM	DM
00	0000−07FF	0400−0BFF	0000−0FFF	0400−13FF
01	0000−07FF	0400−0BFF	0000−17FF	0400−0BFF
10	0000−0BFF	0400−07FF	0000−1BFF	0400−07FF
11 (default)	0000−0FFF	0000	0000−1FFF	0000

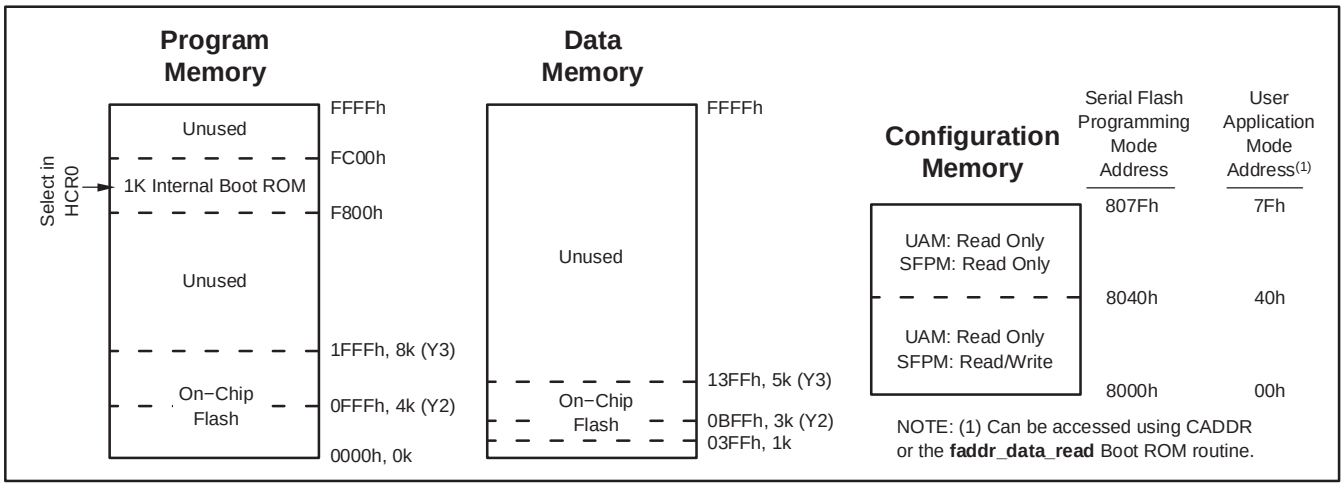


Figure 20. Memory Map

It is important to note that the Flash Memory is readable and writable (depending on the MXWS bit in the MWS SFR) through the MOVX instruction when configured as either Program or Data Memory. This flexibility means that the device can be partitioned for maximum Flash Program Memory size (no Flash Data Memory) and Flash Program Memory can be used as Flash Data Memory. However, this usage may lead to undesirable behavior if the PC points to an area of Flash Program Memory that is being used for data storage. Therefore, it is recommended to use Flash partitioning when Flash Memory is used for data storage. Flash partitioning prohibits execution of code from Data Flash Memory. Additionally, the Program Memory erase/write can be disabled through hardware configuration bits (HCR0), while still providing access (read/write/erase) to Data Flash Memory.

The effect of memory mapping on Program and Data Memory is straightforward. The Program Memory is decreased in size from the top of Flash Memory. To maintain compatibility with the MSC121x, the Flash Data Memory maps to addresses 0400h. Therefore, access to Data Memory (through MOVX) will access Flash Memory for the addresses shown in Table 4.

Data Memory

The MSC120x has on-chip Flash Data Memory, which is readable and writable (depending on the Memory Write Select register) during normal operation (full V_{DD} range). This memory is mapped into the external Data Memory space, which requires the use of the MOVX instruction to program.

CONFIGURATION MEMORY

The MSC120x Configuration Memory consists of 128 bytes of memory. In UAM, all Configuration Memory is readable using the **faddr_data_read** Boot ROM routine or CADDR register, but none of the Configuration Memory is writable. In SFPM, all Configuration Memory is readable, but only the lower 64 bytes (8000h−803Fh) are writable; the upper 64 bytes (8040h−807Fh) are not writable.

Note that reading/writing configuration memory in SFPM requires 16-bit addressing; whereas, reading configuration memory in UAM requires only 8-bit addressing.

Lower 64 Bytes

Note that the three hardware configuration registers (HCR0, HCR1, and HCR2) reside in the lower 64 bytes of Configuration Memory and are located in SFPM at addresses 0803Fh, 0803Eh, and 0803Dh, respectively. Therefore, care should be taken when writing to Configuration Memory so that user parameters are not written into these locations.

Also note that if the Enable Program Memory Access bit (HCR0.7) is cleared, Configuration Memory cannot be changed unless all memory has been cleared with the Mass Erase command.

Upper 64 Bytes

Information such as device trim values and device serial number are located in the upper 64 bytes of Configuration Memory. The locations 08050h through 08053h contain a unique 4-byte serial number. The location 8054h contains the temperature sensor correction value (refer to application note SBAA126, available for download from www.ti.com). None of these memory locations can be altered.

REGISTER MAP

Figure 21 illustrates the Register Map. It is entirely separate from the Program and Data Memory areas discussed previously. A separate class of instructions is used to access the registers. There are 256 potential register locations. In practice, the MSC120x have 256 bytes of Scratchpad RAM and up to 128 SFRs. This is possible since the upper 128 Scratchpad RAM locations can only be accessed indirectly. Thus, a direct reference to one of the upper 128 locations must be an SFR access. Direct RAM is reached at locations 0 to 7Fh (0 to 127).

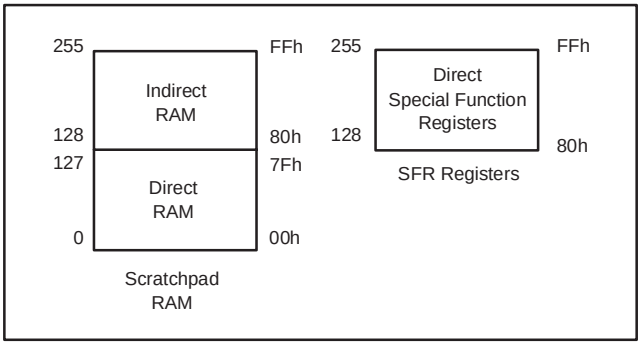


Figure 21. Register Map

SFRs are accessed directly between 80h and FFh (128 to 255). The RAM locations between 128 and 255 can be reached through an indirect reference to those locations. Scratchpad RAM is available for general-purpose data storage. Within the 128 bytes of RAM, there are several special-purpose areas.

Bit Addressable Locations

In addition to direct register access, some individual bits are also accessible. These are individually addressable bits in both the RAM and SFR area. In the Scratchpad RAM area, registers 20h to 2Fh are bit-addressable. This provides 128 (16×8) individual bits available to software. A bit access is distinguished from a full-register access by the type of instruction. In the SFR area, any register location ending in a 0h or 8h is bit-addressable. Figure 22 shows details of the on-chip RAM addressing including the locations of individual RAM bits.

Working Registers

As part of the lower 128 bytes of RAM, there are four banks of Working Registers, as shown in Figure 20. The Working Registers are general-purpose RAM locations that can be addressed in a special way. They are designated R0 through R7. Since there are four banks, the currently selected bank will be used by any instruction using R0−R7. This design allows software to change context by simply switching banks. Bank access is controlled via the Program Status Word register (PSW; 0D0h) in the SFR area described below. The 16 bytes immediately above the R0−R7 registers are bit-addressable, so any of the 128 bits in this area can be directly accessed using bit-addressable instructions.

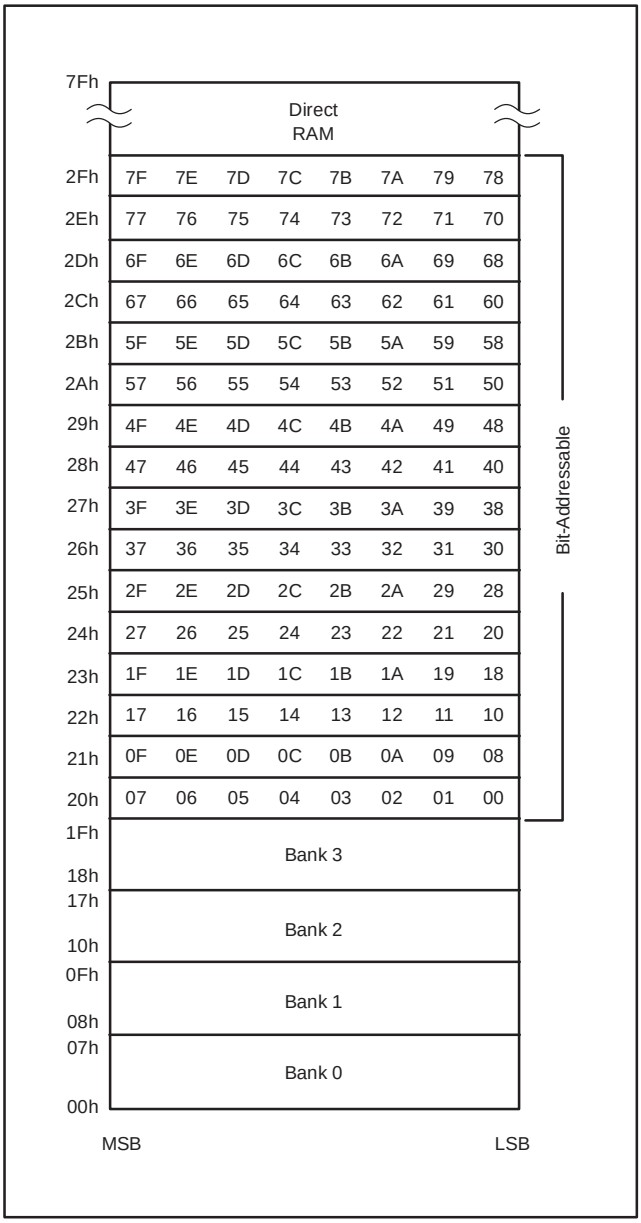


Figure 22. Scratchpad Register Addressing

Thus, an instruction can designate the value stored in R0 (for example) to address the upper RAM. The 16 bytes immediately above the these registers are bit-addressable, so any of the 128 bits in this area can be directly accessed using bit-addressable instructions.

Stack

Another use of the Scratchpad area is for the programmer's stack. This area is selected using the Stack Pointer (SP, SFR 81h). Whenever a call or interrupt is invoked, the return address is placed on the Stack. It also is available to the programmer for variables, etc., since the Stack can be moved and there is no fixed location within the RAM designated as Stack. The Stack Pointer defaults to 07h on reset and the user can then move it as needed. The SP will point to the last used value. Therefore, the next value placed on the Stack is put at SP + 1. Each PUSH or CALL increments the SP by the appropriate value and each POP or RET decrements it.

Program Memory

After reset, the CPU begins execution from Program Memory location 0000h. If enabled, the Boot ROM will appear from address F800h to FFFFh.

Boot ROM

There is a 1kB Boot ROM that controls operation during serial programming. Additionally, the Boot ROM routines shown in Table 5 can be accessed during the user mode, if it is enabled. When enabled, the Boot ROM routines will be located at memory addresses F800h−FBFFh during user mode.

Table 5. MSC120x Boot ROM Routines

HEX ADDRESS	ROUTINE	C DECLARATIONS	DESCRIPTION
F802	sfr_rd	char sfr_rd(void);	Return SFR value pointed to by CADDR(1)
F805	sfr_wr	void sfr_wr(char d);	Write to SFR pointed to by CADDR(1)
FBD8	monitor_isr	void monitor_isr() interrupt 6;	Push registers and call cmd_parser
FBDA	cmd_parser	void cmd_parser(void);	See application note SBAA076, *Programming the MSC1210*, available at www.ti.com.
FBDC	put_string	void put_string(char code *string);	Output string
FBDE	page_erase	char page_erase(int faddr, char fdata, char fdm);	Erase flash page
FBE0	write_flash	Assembly only; DPTR = address, ACC = data	Flash write(2)
FBE2	write_flash_chk	char write_flash_chk(int faddr, char fdata, char fdm);	Write flash byte, verify
FBE4	write_flash_byte	void write_flash_byte(int faddr, char fdata);	Write flash byte(2)
FBE6	faddr_data_read	char faddr_data_read(char faddr);	Read byte from Configuration Memory
FBE8	data_x_c_read	char data_x_c_read(int faddr, char fdm);	Read xdata or code byte
FBEA	tx_byte	void tx_byte(char);	Send byte to USART0
FBEC	tx_hex	void tx_hex(char);	send hex value to USART0
FBEE	putx	void putx(void);	send "x" to USART0 on R7 = 1
FBF0	rx_byte	char rx_byte(void);	Read byte from USART0
FBF2	rx_byte_echo	char rx_byte_echo(void);	Read and echo byte on USART0
FBF4	rx_hex_echo	char rx_hex_echo(void);	Read and echo hex on USART0
FBF6	rx_hex_dbl_echo	int_rx_hex_dbl_echo(void);	Read int as hex and echo: USART0
FBF8	rx_hex_word_echo	int_rx_hex_word_echo(void);	Read int reversed as hex and echo: USART0
FBFA	autobaud	void autobaud(void);	Set USART0 baud rate after CR(3) received
FBFC	putspace1	void putspace1(void);	Output 1 space to USART0
FBFE	putcr	void putcr(void);	Output CR, LF to USART0

(1) CADDR must be set prior to using these routines.
(2) MWS register (SFR 8Fh) defines Data Memory or Program Memory write.
(3) SFR registers CKCON and TCON must be initialized: CKCON = 0x10 and TCON = 0x00.

Serial Flash Programming Mode

Serial Flash Programming mode (SFPM) is used to download Program and Data Memory into the onboard Flash Memory on the MSC120x. It is initiated by holding the P1.0/$\overline{\text{PROG}}$ pin low during the reset cycle, as shown in Figure 23. After the reset cycle, the host can communicate with the MSC120x through USART0. Refer to application note SBAA076 (www.ti.com) for serial programming commands and protocol.

In SFPM, the MSC120x uses the internal oscillator in low frequency mode (that is, the external clock is disabled). The internal oscillator frequency is affected by the power supply voltage and device temperature. Therefore, in order to avoid losing communication during programming, it is important to have a stable power supply and temperature environment during serial communication. The recommended baud rate range for SFPM is 2400 to 19200. If communication errors occur, decreasing the baud rate may improve communication performance.

Also note that in SFPM, the Brownout Detect circuit is disabled and AV_{DD} must be > 2.0V.

INTERRUPTS

The MSC120x use a three-priority interrupt system. As shown in Table 6, each interrupt source has an independent priority bit, flag, interrupt vector, and enable (except that nine interrupts share the Auxiliary Interrupt, AI, at the highest priority). In addition, interrupts can be globally enabled or disabled. The interrupt structure is compatible with the original 8051 family. All of the standard interrupts are available.

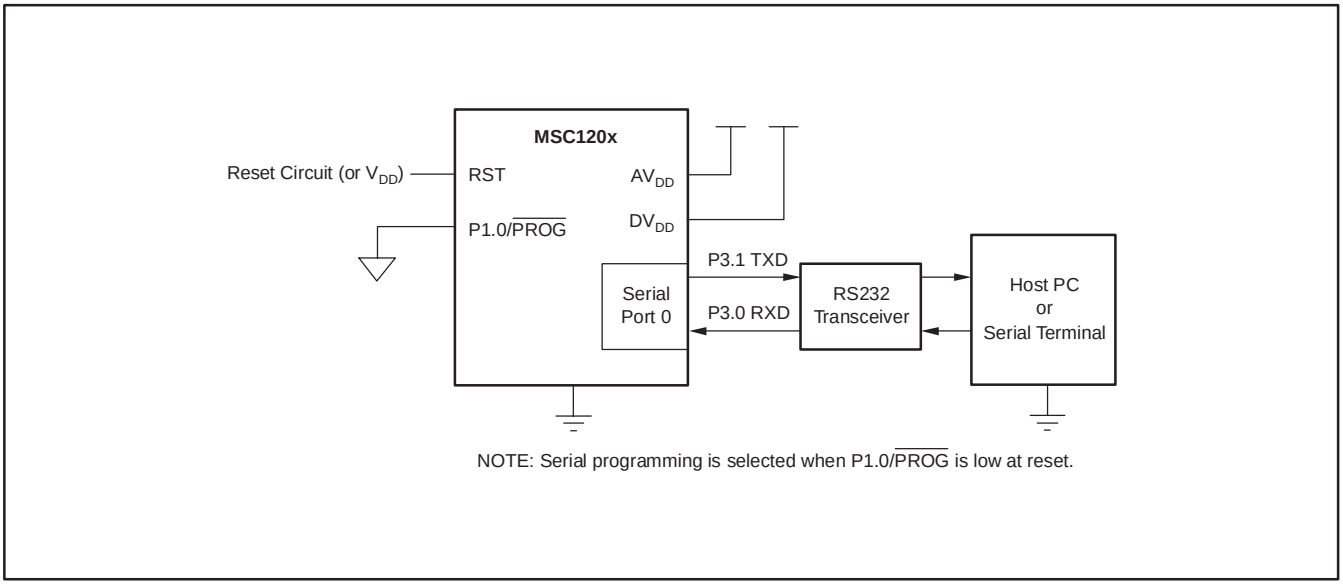


Figure 23. Serial Flash Programming Mode

Table 6. Interrupt Summary

INTERRUPT/EVENT	INTERRUPT ADDR	INTERRUPT NUM	PRIORITY	FLAG	ENABLE	PRIORITY CONTROL
AV_{DD} Low Voltage Detect	33h	6	High 0	ALVDIP (AIPOL.1)(1)	EALV (AIE.1)(1)	N/A
Count (SPI/I^2C)	33h	6	0	CNTIP (AIPOL.2)(1)	ECNT (AIE.2)(1)	N/A
I^2C Start/Stop	33h	6	0	I2CIP (AIPOL.3)(1)	EI2C (AIE.3)(1)	N/A
Milliseconds Timer	33h	6	0	MSECIP (AIPOL.4)(1)	EMSEC (AIE.4)(1)	N/A
ADC	33h	6	0	ADCIP (AIPOL.5)(1)	EADC (AIE.5)(1)	N/A
Summation Register	33h	6	0	SUMIP (AIPOL.6)(1)	ESUM (AIE.6)(1)	N/A
Seconds Timer	33h	6	0	SECIP (AIPOL.7)(1)	ESEC (AIE.7)(1)	N/A
External Interrupt 0	03h	0	1	IE0 (TCON.1)(2)	EX0 (IE.0)(4)	PX0 (IP.0)
Timer 0 Overflow	0Bh	1	2	TF0 (TCON.5)(3)	ET0 (IE.1)(4)	PT0 (IP.1)
External Interrupt 1	13h	2	3	IE1 (TCON.3)(2)	EX1 (IE.2)(4)	PX1 (IP.2)
Timer 1 Overflow	1Bh	3	4	TF1 (TCON.7)(3)	ET1 (IE.3)(4)	PT1 (IP.3)
Serial Port 0	23h	4	5	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)(4)	PS0 (IP.4)
External Interrupt 2	43h	8	6	IE2 (EXIF.4)	EX2 (EIE.0)(4)	PX2 (EIP.0)
External Interrupt 3	4Bh	9	7	IE3 (EXIF.5)	EX3 (EIE.1)(4)	PX3 (EIP.1)
External Interrupt 4	53h	10	8	IE4 (EXIF.6)	EX4 (EIE.2)(4)	PX4 (EIP.2)
External Interrupt 5	5Bh	11	9	IE5 (EXIF.7)	EX5 (EIE.3)(4)	PX5 (EIP.3)
Watchdog	63h	12	10 Low	WDTI (EICON.3)	EWDI (EIE.4)(4)	PWDI (EIP.4)

(1) These interrupts set the AI flag (EICON.4) and are enabled by EAI (EICON.5).
(2) If edge-triggered, cleared automatically by hardware when the service routine is vectored to. If level-triggered, the flag follows the state of the pin.
(3) Cleared automatically by hardware when interrupt vector occurs.
(4) Globally enabled by $\overline{EA}$ (IE.7).

Hardware Configuration Register 0 (HCR0)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CADDR 3Fh	EPMA	PML	RSL	EBR	EWDR	1	DFSEL1	DFSEL0

NOTE: HCR0 is programmable only in SFPM, but can be read in UAM using the **faddr_data_read** Boot ROM routine.

EPMA **Enable Program Memory Access (Security Bit).**
bit 7
0: After reset in programming modes, Flash Memory can only be accessed in UAM until a mass erase is done.
1: Fully Accessible (default)

PML **Program Memory Lock (PML has priority over RSL).**
bit 6
0: Enable read and write for Program Memory in UAM.
1: Enable Read-Only mode for Program Memory in UAM (default).

RSL **Reset Sector Lock.** The reset sector can be used to provide another method of Flash Memory programming, which allows Program Memory updates without changing the jumpers for in-circuit code updates or program development. The code in this boot sector would then provide the monitor and programming routines with the ability to jump into the main Flash code when programming is finished.
bit 5
0: Enable Reset Sector Writing
1: Enable Read-Only mode for reset sector (4kB) (default). Same effect as PML for the MSC120xY2.

EBR **Enable Boot ROM.** Boot ROM is 1kB of code located in ROM, not to be confused with the 4kB Boot Sector located in Flash Memory.
bit 4
0: Disable Internal Boot ROM
1: Enable Internal Boot ROM (default)

EWDR **Enable Watchdog Reset.**
bit 3
0: Disable Watchdog Reset
1: Enable Watchdog Reset (default)

DFSEL1−0 **Data Flash Memory Size (see Table 3).**
bits 1−0
00: 4kB Data Flash Memory (MSC120xY3 only)
01: 2kB Data Flash Memory
10: 1kB Data Flash Memory
11: No Data Flash Memory (default)

Hardware Configuration Register 1 (HCR1)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CADDR 3Eh	DBSEL3	DBSEL2	DBSEL1	DBSEL0	1	DDB	1	1

NOTE: HCR1 is programmable only in SFPM, but can be read in UAM using the **faddr_data_read** Boot ROM routine.

DBSEL3−0 **Digital Supply Brownout Level Select.** The values listed are nominal. The actual value will vary depending on device clock frequency and supply voltage. For high clock frequencies, the variation could be on the order of 10% below the nominal value.

bits 7−4
- 0000: 4.6V
- 0001: 4.2V
- 0010: 3.8V
- 0011: 3.6V
- 0100: 3.3V
- 0101: 3.1V
- 0110: 2.9V
- 0111: 2.7V
- 1000: 2.6V
- 1001: Reserved
- 1010: Reserved
- 1011: Reserved
- 1100: Reserved
- 1101: Reserved
- 1110: Reserved
- 1111: Reserved

DDB **Disable Digital Brownout Detection.**

bit 2
- 0: Enable Digital Brownout Detection
- 1: Disable Digital Brownout Detection (default)

Hardware Configuration Register 2 (HCR2)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CADDR 3Dh	0	0	0	0	0	CLKSEL2	CLKSEL1	CLKSEL0

NOTE: HCR2 is programmable only in SFPM, but can be read in UAM using the **faddr_data_read** Boot ROM routine.

CLKSEL2−1 **Clock Select.**

bits 2−0
- 000: Reserved
- 001: Reserved
- 010: Reserved
- 011: External Clock Mode
- 100: PLL High-Frequency (HF) Mode
- 101: PLL Low-Frequency (LF) Mode
- 110: Internal Oscillator High-Frequency (HF) Mode
- 111: Internal Oscillator Low-Frequency (LF) Mode

NOTE: Clock status can be verified reading PLLH in UAM.

Configuration Memory Programming

Hardware Configuration Memory can be changed only in Serial Flash Programming mode (SFPM).

Table 7. Special Function Registers

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
80h										
81h	SP									07h
82h	DPL0									00h
83h	DPH0									00h
84h	DPL1									00h
85h	DPH1									00h
86h	DPS	0	0	0	0	0	0	0	SEL	00h
87h	PCON	SMOD	0	1	1	GF1	GF0	STOP	IDLE	30h
88h	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
89h	TMOD	——— Timer 1 ———				——— Timer 0 ———				00h
		GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	
8Ah	TL0									00h
8Bh	TL1									00h
8Ch	TH0									00h
8Dh	TH1									00h
8Eh	CKCON	0	0	0	T1M	T0M	MD2	MD1	MD0	01h
8Fh	MWS	0	0	0	0	0	0	0	MXWS	00h
90h	P1	P1.7 $\overline{INT5}$	P1.6 INT4	P1.5 $\overline{INT3}$	P1.4 INT2/$\overline{SS}$	P1.3 DIN	P1.2 DOUT	P1.1	P1.0 $\overline{PROG}$	FFh
91h	EXIF	IE5	IE4	IE3	IE2	1	0	0	0	08h
92h										
93h	CADDR									00h
94h	CDATA									00h
95h										
96h										
97h										
98h	SCON0	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00h
99h	SBUF0									00h
9Ah	SPICON I2CCON	SBIT3 SBIT3	SBIT2 SBIT2	SBIT1 SBIT1	SBIT0 SBIT0	ORDER STOP	CPHA START	ESS DCS	CPOL CNTSEL	00h
9Bh	SPIDATA I2CDATA									00h
9Ch										
9Dh										
9Eh										
9Fh										
A0h										
A1h										
A2h										
A3h										
A4h	AIPOL	SECIP	SUMIP	ADCIP	MSECIP	I2CIP	CNTIP	ALVDIP	0	00h
A5h	PAI	0	0	0	0	PAI3	PAI2	PAI1	PAI0	00h
A6h	AIE	ESEC	ESUM	EADC	EMSEC	EI2C	ECNT	EALV	0	00h
A7h	AISTAT	SEC	SUM	ADC	MSEC	I2C	CNT	ALVD	0	00h
A8h	IE	EA	0	0	ES0	ET1	EX1	ET0	EX0	00h
A9h										

Table 7. Special Function Registers (continued)

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
AAh										
ABh										
ACh										
ADh										
AEh	P1DDRL	P13H	P13L	P12H	P12L	P11H	P11L	P10H	P10L	00h
AFh	P1DDRH	P17H	P17L	P16H	P16L	P15H	P15L	P14H	P14L	00h
B0h	P3	P3.7	P3.6 SCK/SCL/CLKS	P3.5 T1	P3.4 T0	$\overline{\text{P3.3}}$ $\overline{\text{INT1}}$	$\overline{\text{P3.2}}$ $\overline{\text{INT0}}$	P3.1 TXD0	P3.0 RXD0	FFh
B1h										
B2h										
B3h	P3DDRL	P33H	P33L	P32H	P32L	P31H	P31L	P30H	P30L	00h
B4h	P3DDRH	P37H	P37L	P36H	P36L	P35H	P35L	P34H	P34L	00h
B5h	IDAC									00h
B6h										
B7h										
B8h	IP	1	0	0	PS0	PT1	PX1	PT0	PX0	80h
B9h										
BAh										
BBh										
BCh										
BDh										
BEh										
BFh										
C0h										
C1h										
C2h										
C3h										
C4h										
C5h										
C6h	EWU						EWUWDT	EWUEX1	EWUEX0	00h
C7h	SYSCLK	0	0	DIVMOD1	DIVMOD0	0	DIV2	DIV1	DIV0	00h
C8h										
C9h										
CAh										
CBh										
CCh										
CDh										
CEh										
CFh										
D0h	PSW	CY	AC	F0	RS1	RS0	OV	F1	P	00h
D1h	OCL								LSB	00h
D2h	OCM									00h
D3h	OCH	MSB								00h
D4h	GCL								LSB	5Ah
D5h	GCM									ECh
D6h	GCH	MSB								5Fh

Table 7. Special Function Registers (continued)

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUE
D7h	ADMUX	INP3	INP2	INP1	INP0	INN3	INN2	INN1	INN0	01h
D8h	EICON	0	1	EAI	AI	WDTI	0	0	0	40h
D9h	ADRESL(1)								LSB(1)	00h
DAh	ADRESM(1)	MSB(1)								00h
DBh	ADRESH(1)	MSB(1)								00h
DCh	ADCON0		BOD	EVREF	VREFH	EBUF	PGA2	PGA1	PGA0	30h
DDh	ADCON1	OF_UF	POL	SM1	SM0	—	CAL2	CAL1	CAL0	00h
DEh	ADCON2	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	1Bh
DFh	ADCON3	0	0	0	0	0	DR10	DR9	DR8	06h
E0h	ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h
E1h	SSCON	SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	00h
E2h	SUMR0								LSB	00h
E3h	SUMR1									00h
E4h	SUMR2									00h
E5h	SUMR3	MSB								00h
E6h	ODAC									00h
E7h	LVDCON	ALVDIS	0	0	0	ALVD3	ALVD2	ALVD1	ALVD0	8Fh
E8h	EIE	1	1	1	EWDI	EX5	EX4	EX3	EX2	E0h
E9h	HWPC0	0	0	0	0	0	0	DEVICE	MEMORY	0000_00xxb
EAh	HWPC1	0	0	1	0	0	0	0	0	20h
EBh	HWVER									
ECh										
EDh										
EEh	FMCON	0	PGERA	0	FRCM	0	BUSY	SPM	FPM	02h
EFh	FTCON	FER3	FER2	FER1	FER0	FWR3	FWR2	FWR1	FWR0	A5h
F0h	B									00h
F1h	PDCON	PDICLK	PDIDAC	PDI2C	0	PDADC	PDWDT	PDST	PDSPI	6Fh
F2h	PASEL	PSEN4	PSEN3	PSEN2	PSEN1	PSEN0	0	0	0	00h
F3h										
F4h	PLLL	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0	xxh(2)
F5h	PLLH	CKSTAT2	CKSTAT1	CKSTAT0	PLLLOCK	0	0	PLL9	PLL8	xxh(2)
F6h	ACLK	0	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03h
F7h	SRST	0	0	0	0	0	0	0	RSTREQ	00h
F8h	EIP	1	1	1	PWDI	PX5	PX4	PX3	PX2	E0h
F9h	SECINT	WRT	SECINT6	SECINT5	SECINT4	SECINT3	SECINT2	SECINT1	SECINT0	7Fh
FAh	MSINT	WRT	MSINT6	MSINT5	MSINT4	MSINT3	MSINT2	MSINT1	MSINT0	7Fh
FBh	USEC	0	0	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03h
FCh	MSECL	MSECL7	MSECL6	MSECL5	MSECL4	MSECL3	MSECL2	MSECL1	MSECL0	9Fh
FDh	MSECH	MSECH7	MSECH6	MSECH5	MSECH4	MSECH3	MSECH2	MSECH1	MSECH0	0Fh
FEh	HMSEC	HMSEC7	HMSEC6	HMSEC5	HMSEC4	HMSEC3	HMSEC2	HMSEC1	HMSEC0	63h
FFh	WDTCON	EWDT	DWDT	RWDT	WDCNT4	WDCNT3	WDCNT2	WDCNT1	WDCNT0	00h

(1) For the MSC1200/01, the ADC result is contained in ADRESH, ADRESM, and ADRESL. For the MSC1202, the ADC result is contained in ADRESM and ADRESL (that is, shifted right one byte) and the MSB is sign-extended (Bipolar mode) or zero-padded (Unipolar mode) in ADRESH. Therefore, when migrating between the MSC1200/01 and MSC1202, the ADC result calculation must be adjusted accordingly. For all devices, the ADC interrupt is cleared by reading ADRESL.

(2) Dependent on active clock mode.

Table 8. Special Function Register Cross Reference

SFR	ADDRESS	FUNCTIONS	CPU	INTERRUPTS	PORTS	SERIAL COMM.	POWER AND CLOCKS	TIMER COUNTERS	FLASH MEMORY	ADC DACS
SP	81h	Stack Pointer	X							
DPL0	82h	Data Pointer Low 0	X							
DPH0	83h	Data Pointer High 0	X							
DPL1	84h	Data Pointer Low 1	X							
DPH1	85h	Data Pointer High 1	X							
DPS	86h	Data Pointer Select	X							
PCON	87h	Power Control					X			
TCON	88h	Timer/Counter Control				X		X		
TMOD	89h	Timer Mode Control				X		X		
TL0	8Ah	Timer0 LSB						X		
TL1	8Bh	Timer1 LSB						X		
TH0	8Ch	Timer0 MSB						X		
TH1	8Dh	Timer1 MSB						X		
CKCON	8Eh	Clock Control				X	X	X		
MWS	8Fh	Memory Write Select							X	
P1	90h	Port 1			X					
EXIF	91h	External Interrupt Flag		X						
CADDR	93h	Configuration Address							X	
CDATA	94h	Configuration Data							X	
SCON0	98h	Serial Port 0 Control				X				
SBUF0	99h	Serial Data Buffer 0				X				
SPICON	9Ah	SPI Control				X				
I2CCON		I^2C Control				X				
SPIDATA	9Bh	SPI Data				X				
I2CDATA		I^2C Data				X				
AIPOL	A4h	Auxiliary Interrupt Poll		X		X	X	X		X
PAI	A5h	Pending Auxiliary Interrupt		X		X	X	X		X
AIE	A6h	Auxiliary Interrupt Enable		X		X	X	X		X
AISTAT	A7h	Auxiliary Interrupt Status		X		X	X	X		X
IE	A8h	Interrupt Enable		X						
P1DDRL	AEh	Port 1 Data Direction Low			X					
P1DDRH	AFh	Port 1 Data Direction High			X					
P3	B0h	Port 3			X					
P3DDRL	B3h	Port 3 Data Direction Low			X					
P3DDRH	B4h	Port 3 Data Direction High			X					
IDAC	B5h	Current DAC								X
IP	B8h	Interrupt Priority		X						
EWU	C6h	Enable Wake Up		X			X			
SYSCLK	C7h	System Clock Divider				X	X	X	X	X
PSW	D0h	Program Status Word	X							
OCL	D1h	ADC Offset Calibration Low Byte								X
OCM	D2h	ADC Offset Calibration Mid Byte								X
OCH	D3h	ADC Offset Calibration High Byte								X
GCL	D4h	ADC Gain Calibration Low Byte								X
GCM	D5h	ADC Gain Calibration Mid Byte								X
GCH	D6h	ADC Gain Calibration High Byte								X
ADMUX	D7h	ADC Input Multiplexer								X
EICON	D8h	Enable Interrupt Control		X		X	X			X

Table 8. Special Function Register Cross Reference (continued)

SFR	ADDRESS	FUNCTIONS	CPU	INTERRUPTS	PORTS	SERIAL COMM.	POWER AND CLOCKS	TIMER COUNTERS	FLASH MEMORY	ADC DACS
ADRESL	D9h	ADC Results Low Byte								X
ADRESM	DAh	ADC Results Middle Byte								X
ADRESH	DBh	ADC Results High Byte								X
ADCON0	DCh	ADC Control 0								X
ADCON1	DDh	ADC Control 1								X
ADCON2	DEh	ADC Control 2								X
ADCON3	DFh	ADC Control 3								X
ACC	E0h	Accumulator	X							
SSCON	E1h	Summation/Shifter Control	X							X
SUMR0	E2h	Summation 0	X							X
SUMR1	E3h	Summation 1	X							X
SUMR2	E4h	Summation 2	X							X
SUMR3	E5h	Summation 3	X							X
ODAC	E6h	Offset DAC								X
LVDCON	E7h	Low Voltage Detect Control					X			
EIE	E8h	Extended Interrupt Enable		X						
HWPC0	E9h	Hardware Product Code 0	X							
HWPC1	EAh	Hardware Product Code 1	X							
HWVER	EBh	Hardware Version	X							
FMCON	EEh	Flash Memory Control							X	
FTCON	EFh	Flash Memory Timing Control							X	
B	F0h	Second Accumulator	X							
PDCON	F1h	Power Down Control				X	X	X		X
PASEL	F2h	$\overline{\text{PSEN}}$/ALE Select			X		X			
PLLL	F4h	Phase Lock Loop Low					X			
PLLH	F5h	Phase Lock Loop High					X			
ACLK	F6h	Analog Clock					X			X
SRST	F7h	System Reset	X				X			
EIP	F8h	Extended Interrupt Priority		X						
SECINT	F9h	Seconds Interrupt		X			X			
MSINT	FAh	Milliseconds Interrupt		X			X			
USEC	FBh	One Microsecond					X		X	
MSECL	FCh	One Millisecond Low					X		X	
MSECH	FDh	One Millisecond High					X		X	
HMSEC	FEh	One Hundred Millisecond					X			
WDTCON	FFh	Watchdog Timer	X				X			
HCR0	3Fh	Hardware Configuration Reg. 0							X	
HCR1	3Eh	Hardware Configuration Reg. 1					X			
HCR2	3Dh	Hardware Configuration Reg. 2					X			

Stack Pointer (SP)

	7	6	5	4	3	2	1	0	Reset Value
SFR 81h	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	07h

SP.7−0 bits 7−0 **Stack Pointer.** The stack pointer identifies the location where the stack will begin. The stack pointer is incremented before every PUSH or CALL operation and decremented after each POP or RET/RETI. This register defaults to 07h after reset.

Data Pointer Low 0 (DPL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 82h	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0	00h

DPL0.7−0 bits 7−0 **Data Pointer Low 0.** This register is the low byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86h).

Data Pointer High 0 (DPH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 83h	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0	00h

DPH0.7−0 bits 7−0 **Data Pointer High 0.** This register is the high byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86h).

Data Pointer Low 1 (DPL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 84h	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0	00h

DPL1.7−0 bits 7−0 **Data Pointer Low 1.** This register is the low byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86h) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer High 1 (DPH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 85h	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0	00h

DPH1.7−0 bits 7−0 **Data Pointer High.** This register is the high byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86h) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer Select (DPS)

	7	6	5	4	3	2	1	0	Reset Value
SFR 86h	0	0	0	0	0	0	0	SEL	00h

SEL bit 0 **Data Pointer Select.** This bit selects the active data pointer.
0: Instructions that use the DPTR will use DPL0 and DPH0.
1: Instructions that use the DPTR will use DPL1 and DPH1.

Power Control (PCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 87h	SMOD	0	1	1	GF1	GF0	STOP	IDLE	30h

SMOD bit 7 **Serial Port 0 Baud Rate Doubler Enable.** The serial baud rate doubling function for Serial Port 0.
0: Serial Port 0 baud rate will be a standard baud rate.
1: Serial Port 0 baud rate will be double that defined by baud rate generation equation.

GF1 bit 3 **General-Purpose User Flag 1.** This is a general-purpose flag for software control.

GF0 bit 2 **General-Purpose User Flag 0.** This is a general-purpose flag for software control.

STOP bit 1 **Stop Mode Select.** Setting this bit halts the internal oscillator and blocks external clocks. This bit always reads as 0. Exit with RESET. In this mode, internal peripherals are frozen and I/O pins are held in their current state. The ADC is frozen, but IDAC and VREF remain active.

IDLE bit 0 **Idle Mode Select.** Setting this bit freezes the CPU, Timer 0 and 1, and the USART; other peripherals remain active. This bit will always be read as a 0. Exit with AIE (A6h) and EWU (C6h) interrupts (refer to Figure 6 for clocks affected during Idle mode).

Timer/Counter Control (TCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1 bit 7 **Timer 1 Overflow Flag.** This bit indicates when Timer 1 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow has been detected.
1: Timer 1 has overflowed its maximum count.

TR1 bit 6 **Timer 1 Run Control.** This bit enables/disables the operation of Timer 1. Halting this timer preserves the current count in TH1, TL1.
0: Timer is halted.
1: Timer is enabled.

TF0 bit 5 **Timer 0 Overflow Flag.** This bit indicates when Timer 0 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow has been detected.
1: Timer 0 has overflowed its maximum count.

TR0 bit 4 **Timer 0 Run Control.** This bit enables/disables the operation of Timer 0. Halting this timer preserves the current count in TH0, TL0.
0: Timer is halted.
1: Timer is enabled.

IE1 bit 3 **Interrupt 1 Edge Detect.** This bit is set when an edge/level of the type defined by IT1 is detected. If IT1 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 1 service routine. If IT1 = 0, this bit will inversely reflect the state of the $\overline{\text{INT1}}$ pin.

IT1 bit 2 **Interrupt 1 Type Select.** This bit selects whether the $\overline{\text{INT1}}$ pin will detect edge- or level-triggered interrupts.
0: $\overline{\text{INT1}}$ is level-triggered.
1: $\overline{\text{INT1}}$ is edge-triggered.

IE0 bit 1 **Interrupt 0 Edge Detect.** This bit is set when an edge/level of the type defined by IT0 is detected. If IT0 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 0 service routine. If IT0 = 0, this bit will inversely reflect the state of the $\overline{\text{INT0}}$ pin.

IT0 bit 0 **Interrupt 0 Type Select.** This bit selects whether the $\overline{\text{INT0}}$ pin will detect edge- or level-triggered interrupts.
0: $\overline{\text{INT0}}$ is level-triggered.
1: $\overline{\text{INT0}}$ is edge-triggered.

Timer Mode Control (TMOD)

	7	6	5	4	3	2	1	0	Reset Value
SFR 89h	TIMER 1				TIMER 0				00h
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	

GATE bit 7 **Timer 1 Gate Control.** This bit enables/disables the ability of Timer 1 to increment.
0: Timer 1 will clock when TR1 = 1, regardless of the state of pin $\overline{INT1}$.
1: Timer 1 will clock only when TR1 = 1 and pin $\overline{INT1}$ = 1.

C/$\overline{T}$ bit 6 **Timer 1 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on T1 pin when TR1 (TCON.6, SFR 88h) is 1.

M1, M0 bits 5−4 **Timer 1 Mode Select.** These bits select the operating mode of Timer 1.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Timer 1 is halted, but holds its count.

GATE bit 3 **Timer 0 Gate Control.** This bit enables/disables the ability of Timer 0 to increment.
0: Timer 0 will clock when TR0 = 1, regardless of the state of pin $\overline{INT0}$ (software control).
1: Timer 0 will clock only when TR0 = 1 and pin $\overline{INT0}$ = 1 (hardware control).

C/$\overline{T}$ bit 2 **Timer 0 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on pin T0 when TR0 (TCON.4, SFR 88h) is 1.

M1, M0 bits 1−0 **Timer 0 Mode Select.** These bits select the operating mode of Timer 0.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Two 8-bit counters.

Timer 0 LSB (TL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Ah	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	00h

TL0.7−0 bits 7−0 **Timer 0 LSB.** This register contains the least significant byte of Timer 0.

Timer 1 LSB (TL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Bh	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	00h

TL1.7−0 bits 7−0 **Timer 1 LSB.** This register contains the least significant byte of Timer 1.

Timer 0 MSB (TH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Ch	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	00h

TH0.7−0 **Timer 0 MSB.** This register contains the most significant byte of Timer 0.
bits 7−0

Timer 1 MSB (TH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Dh	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	00h

TH1.7−0 **Timer 1 MSB.** This register contains the most significant byte of Timer 1.
bits 7−0

Clock Control (CKCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Eh	0	0	0	T1M	T0M	MD2	MD1	MD0	01h

T1M **Timer 1 Clock Select.** This bit controls the division of the system clock that drives Timer 1. Clearing this bit to 0
bit 4 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.
0: Timer 1 uses a divide-by-12 of the crystal frequency.
1: Timer 1 uses a divide-by-4 of the crystal frequency.

T0M **Timer 0 Clock Select.** This bit controls the division of the system clock that drives Timer 0. Clearing this bit to 0
bit 3 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.
0: Timer 0 uses a divide-by-12 of the crystal frequency.
1: Timer 0 uses a divide-by-4 of the crystal frequency.

MD2, MD1, MD0 **Stretch MOVX Select.** These bits select the time by which external MOVX cycles are to be stretched in the
bits 2−0 standard 8051 core. Since the MSC120x does not allow external memory access, these bits should be set to 000b to allow for the fastest Flash Data Memory access.

Memory Write Select (MWS)

	7	6	5	4	3	2	1	0	Reset Value
SFR 8Fh	0	0	0	0	0	0	0	MXWS	00h

MXWS **MOVX Write Select.** This allows writing to the internal Flash Program Memory.
bit 0 0: No writes are allowed to the internal Flash Program Memory.
1: Writing is allowed to the internal Flash Program Memory, unless PML or RSL (HCR0, CADDR 3Fh) are set.

Port 1 (P1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 90h	P1.7 $\overline{\text{INT5}}$	P1.6 INT4	P1.5 $\overline{\text{INT3}}$	P1.4 INT2/$\overline{\text{SS}}$	P1.3 DIN	P1.2 DOUT	P1.1	P1.0 $\overline{\text{PROG}}$	FFh

P1.7−0 bits 7−0 **General-Purpose I/O Port 1.** This register functions as a general-purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 1 latch bit must contain a logic '1' before the pin can be used in its alternate function capacity. To use the alternate function, set the appropriate mode in P1DDRL (SFR AEh), P1DDRH (SFR AFh).

$\overline{\text{INT5}}$ bit 7 **External Interrupt 5.** A falling edge on this pin will cause an external interrupt 5 if enabled.

INT4 bit 6 **External Interrupt 4.** A rising edge on this pin will cause an external interrupt 4 if enabled.

$\overline{\text{INT3}}$ bit 5 **External Interrupt 3.** A falling edge on this pin will cause an external interrupt 3 if enabled.

INT2/$\overline{\text{SS}}$ bit 4 **External Interrupt 2.** A rising edge on this pin will cause an external interrupt 2 if enabled. This pin can be used as slave select ($\overline{\text{SS}}$) in SPI slave mode.

DIN bit 3 **Serial Data In.** This pin receives serial data in SPI and I^2C modes (in I^2C mode, this pin should be configured as an input) or standard 8051.

DOUT bit 2 **Serial Data Out.** This pin transmits serial data in SPI and I^2C modes (in I^2C mode, this pin should be configured as an open drain) or standard 8051.

$\overline{\text{PROG}}$ bit 0 **Program Mode.** When this pin is pulled low at power-up, the device enters Serial Programming mode (refer to Figure 2).

External Interrupt Flag (EXIF)

	7	6	5	4	3	2	1	0	Reset Value
SFR 91h	IE5	IE4	IE3	IE2	1	0	0	0	08h

IE5 bit 7 **External Interrupt 5 Flag.** This bit will be set when a falling edge is detected on $\overline{\text{INT5}}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE4 bit 6 **External Interrupt 4 Flag.** This bit will be set when a rising edge is detected on INT4. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE3 bit 5 **External Interrupt 3 Flag.** This bit will be set when a falling edge is detected on $\overline{\text{INT3}}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE2 bit 4 **External Interrupt 2 Flag.** This bit will be set when a rising edge is detected on INT2. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

Configuration Address (CADDR) (write-only)

	7	6	5	4	3	2	1	0	Reset Value
SFR 93h									00h

CADDR bits 7−0 **Configuration Address.** This register supplies the address for reading bytes in the 128 bytes of Flash Configuration Memory. It is recommended that **faddr_data_read** be used when accessing Configuration memory.This register is also used as the address for the **sfr_read** and **sfr_write** routines, so it must be set prior to their use.

CAUTION: If this register is written to while executing from Flash Memory, the CDATA register will be incorrect.

Configuration Data (CDATA) (read-only)

	7	6	5	4	3	2	1	0	Reset Value
SFR 94h									00h

CDATA bits 7−0 **Configuration Data.** This register will contain the data in the 128 bytes of Flash Configuration Memory that is located at the last written address in the CADDR register. This is a read-only register.

Serial Port 0 Control (SCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 98h	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00h

SM0−2 bits 7−5 **Serial Port 0 Mode.** These bits control the mode of serial Port 0. Modes 1, 2, and 3 have 1 start and 1 stop bit in addition to the 8 or 9 data bits.

MODE	SM0	SM1	SM2	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 p_{CLK}(1)
0	0	0	1	Synchronous	8 bits	4 p_{CLK}(1)
1	0	1	0	Asynchronous	10 bits	Timer 1 Baud Rate Equation
1	0	1	1	Asynchronous−Valid Stop Required(2)	10 bits	Timer 1 Baud Rate Equation
2	1	0	0	Asynchronous	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
2	1	0	1	Asynchronous with Multiprocessor Communication	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
3	1	1	0	Asynchronous	11 bits	Timer 1 Baud Rate Equation
3	1	1	1	Asynchronous with Multiprocessor Communication(3)	11 bits	Timer 1 Baud Rate Equation

(1) p_{CLK} will be equal to t_{CLK}, except that p_{CLK} will stop for Idle mode.
(2) RI_0 will only be activated when a valid STOP is received.
(3) RI_0 will not be activated if bit 9 = 0.

REN_0 bit 4 **Receive Enable.** This bit enables/disables the serial Port 0 received shift register.
0: Serial Port 0 reception disabled.
1: Serial Port 0 received enabled (modes 1, 2, and 3). Initiate synchronous reception (mode 0).

TB8_0 bit 3 **9th Transmission Bit State.** This bit defines the state of the 9th transmission bit in serial Port 0 modes 2 and 3.

RB8_0 bit 2 **9th Received Bit State.** This bit identifies the state of the 9th reception bit of received data in serial Port 0 modes 2 and 3. In serial port mode 1, when SM2_0 = 0, RB8_0 is the state of the stop bit. RB8_0 is not used in mode 0.

TI_0 bit 1 **Transmitter Interrupt Flag.** This bit indicates that data in the serial Port 0 buffer has been completely shifted out. In serial port mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_0 bit 0 **Receiver Interrupt Flag.** This bit indicates that a byte of data has been received in the serial Port 0 buffer. In serial port mode 0, RI_0 is set at the end of the 8th bit. In serial port mode 1, RI_0 is set after the last sample of the incoming stop bit subject to the state of SM2_0. In modes 2 and 3, RI_0 is set after the last sample of RB8_0. This bit must be manually cleared by software.

Serial Data Buffer 0 (SBUF0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 99h									00h

SBUF0 bits 7−0 **Serial Data Buffer 0.** Data for Serial Port 0 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

SPI Control (SPICON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Ah	SBIT3	SBIT2	SBIT1	SBIT0	ORDER	CPHA	ESS	CPOL	00h

SBIT3−0 bits 7−4 **Serial Bit Count.** Number of bits transferred (read-only).

SBIT3:0	COUNT
0x00	0
0x01	1
0x03	2
0x02	3
0x06	4
0x07	5
0x05	6
0x04	7
0x0C	8

ORDER bit 3 **Set Bit Order for Transmit and Receive.**

0: Most significant bits first

1: Least significant bBits first

CPHA bit 2 **Serial Clock Phase Control.**

0: Valid data starting from half SCK period before the first edge of SCK

1: Valid data starting from the first edge of SCK

ESS bit 1 **Enable Slave Select.**

0: $\overline{SS}$ (P1.4) is configured as a general-purpose I/O (default).

1: $\overline{SS}$ (P1.4) is configured as $\overline{SS}$ for SPI mode. DOUT (P1.2) drives when $\overline{SS}$ is low, and DOUT (P1.2) is high-impedance when $\overline{SS}$ is high.

CPOL bit 0 **Serial Clock Polarity.**

0: SCK idle at logic low

1: SCK idle at logic high

I²C Control (I2CCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Ah	SBIT3	SBIT2	SBIT1	SBIT0	STOP	START	DCS	CNTSEL	00h

SBIT3−0 **Serial Bit Count.** Number of bits transferred (read-only).
bits 7−4

SBIT3:0	COUNT
0x00	0
0x01	1
0x03	2
0x02	3
0x06	4
0x07	5
0x05	6
0x04	7
0x0C	8

STOP **Stop-Bit Status.**
bit 3 0: No stop
1: Stop condition received and I2C (bit 3, SFR A7h) set (cleared on write to I2CDATA)

START **Start-Bit Status.**
bit 2 0: No stop
1: Start or repeated start condition received and I2C (bit 3, SFR A7h) set (cleared on write to I2CDATA)

DCS **Disable Serial Clock Stretch.**
bit 1 0: Enable SCL stretch (cleared by firmware or START condition)
1: Disable SCL stretch

CNTSEL **Counter Select.**
bit 0 0: Counter IRQ set for bit counter = 8 (default)
1: Counter IRQ set for bit counter = 1

SPI Data (SPIDATA) / I²C Data (I2CDATA)

	7	6	5	4	3	2	1	0	Reset Value
SFR 9Bh									00h

SPIDATA **SPI Data.** Data for SPI is read from or written to this location. The SPI transmit and receive buffers are
bits 7−0 separate registers, but both are addressed at this location. Read to clear the receive interrupt and write to clear the transmit interrupt.

I2CDATA **I2C Data.** Data for I²C is read from or written to this location. The I²C transmit and receive buffers are
bits 7−0 separate registers, but both are addressed at this location.

Auxiliary Interrupt Poll (AIPOL)

	7	6	5	4	3	2	1	0	Reset Value
SFR A4h	SECIP	SUMIP	ADCIP	MSECIP	I2CIP	CNTIP	ALVDIP	0	00h

Interrupts are enabled by EICON.4 (SFR D8h). The other interrupts are controlled by the IE and EIE registers.

SECIP **Second System Timer Interrupt Poll (before IRQ masking).**
bit 7 0 = Second system timer interrupt poll inactive
1 = Second system timer interrupt poll active

SUMIP **Summation Interrupt Poll (before IRQ masking).**
bit 6 0 = Summation interrupt poll inactive
1 = Summation interrupt poll active

ADCIP **ADC Interrupt Poll (before IRQ masking).**
bit 5 0 = ADC interrupt poll inactive
1 = ADC interrupt poll active

MSECIP **Millisecond System Timer Interrupt Poll (before IRQ masking).**
bit 4 0 = Millisecond system timer interrupt poll inactive
1 = Millisecond system timer interrupt poll active

I2CIP **I^2C Start/Stop Interrupt Poll (before IRQ masking).**
bit 3 0 = I^2C start/stop interrupt poll inactive
1 = I^2C start/stop interrupt poll active

CNTIP **Serial Bit Count Interrupt Poll (before IRQ masking).**
bit 2 0 = Serial bit count interrupt poll inactive
1 = Serial bit count interrupt poll active

ALVDIP **Analog Low Voltage Detect Interrupt Poll (before IRQ masking).**
bit 1 0 = Analog low voltage detect interrupt poll inactive (AV_{DD} > ALVD threshold; ALVD threshold set in LVDCON, E7h)
1 = Analog low voltage detect interrupt poll active (AV_{DD} < ALVD threshold; ALVD threshold set in LVDCON, E7h)

Pending Auxiliary Interrupt (PAI)

	7	6	5	4	3	2	1	0	Reset Value
SFR A5h	0	0	0	0	PAI3	PAI2	PAI1	PAI0	00h

PAI **Pending Auxiliary Interrupt Register.** The results of this register can be used as an index to vector to the
bits 3−0 appropriate interrupt routine. All of these interrupts vector through address 0033h.

PAI3	PAI2	PAI1	PAI0	AUXILIARY INTERRUPT STATUS
0	0	0	0	No Pending Auxiliary IRQ.
0	0	0	1	Reserved.
0	0	1	0	Analog Low Voltage Detect IRQ and Possible Lower Priority Pending.
0	0	1	1	I^2C IRQ and Possible Lower Priority Pending.
0	1	0	0	Serial Bit Count Interrupt and Possible Lower Priority Pending.
0	1	0	1	Millisecond System Timer IRQ and Possible Lower Priority Pending.
0	1	1	0	ADC IRQ and Possible Lower Priority Pending.
0	1	1	1	Summation IRQ and Possible Lower Priority Pending.
1	0	0	0	Second System Timer IRQ.

Auxiliary Interrupt Enable (AIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR A6h	ESEC	ESUM	EADC	EMSEC	EI2C	ECNT	EALV	0	00h

Interrupts are enabled by EICON.4 (SFR D8h). The other interrupts are controlled by the IE and EIE registers.

ESEC **Enable Second System Timer Interrupt (lowest priority auxiliary interrupt).**
bit 7 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Second Timer Interrupt** mask.

ESUM **Enable Summation Interrupt.**
bit 6 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Summation Interrupt** mask.

EADC **Enable ADC Interrupt.**
bit 5 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **ADC Interrupt** mask.

EMSEC **Enable Millisecond System Timer Interrupt.**
bit 4 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Millisecond System Timer Interrupt** mask.

EI2C **Enable I^2C Start/Stop Bit.**
bit 3 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **I^2C Start/Stop Bit** mask.

ECNT **Enable Serial Bit Count Interrupt.**
bit 2 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Serial Bit Count Interrupt** mask.

EALV **Enable Analog Low Voltage Interrupt.**
bit 1 Write: Set mask bit for this interrupt; 0 = masked, 1 = enabled.
Read: **Analog Low Voltage Detect Interrupt** mask.

Auxiliary Interrupt Status (AISTAT)

	7	6	5	4	3	2	1	0	Reset Value
SFR A7h	SEC	SUM	ADC	MSEC	I2C	CNT	ALVD	0	00h

SEC **Second System Timer Interrupt Status Flag (lowest priority AI).**

bit 7 0: SEC interrupt cleared or masked.

1: SEC Interrupt active (it is cleared by reading SECINT, SFR F9h).

SUM **Summation Register Interrupt Status Flag.**

bit 6 0: SUM interrupt cleared or masked.

1: SUM interrupt active (it is cleared by reading the lowest byte of SUMR0, SFR E2h).

ADC **ADC Interrupt Status Flag.**

bit 5 0: ADC interrupt cleared or masked.

1: ADC interrupt active (it is cleared by reading the lowest byte of ADRESL, SFR D9h; if active, no new data will be written to the ADC Results registers).

MSEC **Millisecond System Timer Interrupt Status Flag.**

bit 4 0: MSEC interrupt cleared or masked.

1: MSEC interrupt active (it is cleared by reading MSINT, SFR FAh).

I2C **I^2C Start/Stop Interrupt Status Flag.**

bit 3 0: I^2C start/stop interrupt cleared or masked.

1: I^2C start/stop interrupt active (it is cleared by writing to I2CDATA, SFR 9Bh).

CNT **CNT Interrupt Status Flag.**

bit 2 0: CNT Interrupt cleared or masked.

1: CNT Interrupt active (it is cleared by reading from or writing to SPIDATA/I2CDATA, SFR 9Bh).

ALVD **Analog Low Voltage Detect Interrupt Status Flag.**

bit 1 0: ALVD Interrupt cleared or masked.

1: ALVD Interrupt active (cleared in hardware if AV_{DD} exceeds ALVD threshold).

NOTE: If an interrupt is masked, the status can be read in AIPOL (SFR A4h).

Interrupt Enable (IE)

	7	6	5	4	3	2	1	0	Reset Value
SFR A8h	EA	0	0	ES0	ET1	EX1	ET0	EX0	00h

EA bit 7 — **Global Interrupt Enable.** This bit controls the global masking of all interrupts except those in AIE (SFR A6h).
0: Disable interrupt sources. This bit overrides individual interrupt mask settings for this register.
1: Enable all individual interrupt masks. Individual interrupts in this register will occur if enabled.

ES0 bit 4 — **Enable Serial Port 0 Interrupt.** This bit controls the masking of the serial Port 0 interrupt.
0: Disable all serial Port 0 interrupts.
1: Enable interrupt requests generated by the RI_0 (SCON0.0, SFR 98h) or TI_0 (SCON0.1, SFR 98h) flags.

ET1 bit 3 — **Enable Timer 1 Interrupt.** This bit controls the masking of the Timer 1 interrupt.
0: Disable Timer 1 interrupt.
1: Enable interrupt requests generated by the TF1 flag (TCON.7, SFR 88h).

EX1 bit 2 — **Enable External Interrupt 1.** This bit controls the masking of external interrupt 1.
0: Disable external interrupt 1.
1: Enable interrupt requests generated by the $\overline{\text{INT1}}$ pin.

ET0 bit 1 — **Enable Timer 0 Interrupt.** This bit controls the masking of the Timer 0 interrupt.
0: Disable all Timer 0 interrupts.
1: Enable interrupt requests generated by the TF0 flag (TCON.5, SFR 88h).

EX0 bit 0 — **Enable External Interrupt 0.** This bit controls the masking of external interrupt 0.
0: Disable external interrupt 0.
1: Enable interrupt requests generated by the $\overline{\text{INT0}}$ pin.

Port 1 Data Direction Low (P1DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR AEh	P13H	P13L	P12H	P12L	P11H	P11L	P10H	P10L	00h

P1.3 **Port 1 bit 3 control.**

bits 7−6

P13H	P13L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.2 **Port 1 bit 2 control.**

bits 5−4

P12H	P12L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.1 **Port 1 bit 1 control.**

bits 3−2

P11H	P11L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.0 **Port 1 bit 0 control.**

bits 1−0

P10H	P10L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 1 Data Direction High (P1DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR AFh	P17H	P17L	P16H	P16L	P15H	P15L	P14H	P14L	00h

P1.7 **Port 1 bit 7 control.**

bits 7−6

P17H	P17L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.6 **Port 1 bit 6 control.**

bits 5−4

P16H	P16L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.5 **Port 1 bit 5 control.**

bits 3−2

P15H	P15L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.4 **Port 1 bit 4 control.**

bits 1−0

P14H	P14L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 (P3)

	7	6	5	4	3	2	1	0	Reset Value
SFR B0h	P3.7	P3.6 SCK/SCL/CLKS	P3.5 T1	P3.4 T0	P3.3 $\overline{\text{INT1}}$	P3.2 $\overline{\text{INT0}}$	P3.1 TXD0	P3.0 RXD0	FFh

P3.7−0 bits 7−0 **General-Purpose I/O Port 3.** This register functions as a general-purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 3 latch bit must contain a logic ‘1’ before the pin can be used in its alternate function capacity.

SCK/SCL/CLKS bit 6 **Clock Source Select.** Refer to PASEL (SFR F2h).

T1 bit 5 **Timer/Counter 1 External Input.** A 1 to 0 transition on this pin will increment Timer 1.

T0 bit 4 **Timer/Counter 0 External Input.** A 1 to 0 transition on this pin will increment Timer 0.

$\overline{\text{INT1}}$ bit 3 **External Interrupt 1.** A falling edge/low level on this pin will cause an external interrupt 1 if enabled.

$\overline{\text{INT0}}$ bit 2 **External Interrupt 0.** A falling edge/low level on this pin will cause an external interrupt 0 if enabled.

TXD0 bit 1 **Serial Port 0 Transmit.** This pin transmits the serial Port 0 data in serial port modes 1, 2, 3, and emits the synchronizing clock in serial port mode 0.

RXD0 bit 0 **Serial Port 0 Receive.** This pin receives the serial Port 0 data in serial port modes 1, 2, 3, and is a bidirectional data transfer pin in serial port mode 0.

Port 3 Data Direction Low (P3DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR B3h	P33H	P33L	P32H	P32L	P31H	P31L	P30H	P30L	00h

P3.3 **Port 3 bit 3 control.**

bits 7−6

P33H	P33L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.2 **Port 3 bit 2 control.**

bits 5−4

P32H	P32L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.1 **Port 3 bit 1 control.**

bits 3−2

P31H	P31L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.0 **Port 3 bit 0 control.**

bits 1−0

P30H	P30L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 Data Direction High (P3DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR B4h	P37H	P37L	P36H	P36L	P35H	P35L	P34H	P34L	00h

P3.7 **Port 3 bit 7 control.**

bits 7−6

P37H	P37L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.7 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.6 **Port 3 bit 6 control.**

bits 5−4

P36H	P36L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.6 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.5 **Port 3 bit 5 control.**

bits 3−2

P35H	P35L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.4 **Port 3 bit 4 control.**

bits 1−0

P34H	P34L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

IDAC

	7	6	5	4	3	2	1	0	Reset Value
SFR B5h	MSB							LSB	00h

IDAC **Current DAC.**

bits 7−0 $IDAC_{OUT}$ = IDAC • 3.9µA (~1mA full-scale). Setting (PDCON.PDIDAC) will shut down IDAC and float the IDAC pin.

Interrupt Priority (IP)

	7	6	5	4	3	2	1	0	Reset Value
SFR B8h	1	0	0	PS0	PT1	PX1	PT0	PX0	80h

PS0 **Serial Port 0 Interrupt.** This bit controls the priority of the serial Port 0 interrupt.

bit 4 0 = Serial Port 0 priority is determined by the natural priority order.
1 = Serial Port 0 is a high-priority interrupt.

PT1 **Timer 1 Interrupt.** This bit controls the priority of the Timer 1 interrupt.

bit 3 0 = Timer 1 priority is determined by the natural priority order.
1 = Timer 1 priority is a high-priority interrupt.

PX1 **External Interrupt 1.** This bit controls the priority of external interrupt 1.

bit 2 0 = External interrupt 1 priority is determined by the natural priority order.
1 = External interrupt 1 is a high-priority interrupt.

PT0 **Timer 0 Interrupt.** This bit controls the priority of the Timer 0 interrupt.

bit 1 0 = Timer 0 priority is determined by the natural priority order.
1 = Timer 0 priority is a high-priority interrupt.

PX0 **External Interrupt 0.** This bit controls the priority of external interrupt 0.

bit 0 0 = External interrupt 0 priority is determined by the natural priority order.
1 = External interrupt 0 is a high-priority interrupt.

Enable Wake Up (EWU) (Waking Up from Idle Mode)

	7	6	5	4	3	2	1	0	Reset Value
SFR C6h	—	—	—	—	—	EWUWDT	EWUEX1	EWUEX0	00h

Auxiliary interrupts will wake up from Idle mode. They are enabled with EAI (EICON.5).

EWUWDT **Enable Wake Up Watchdog Timer.** Wake using watchdog timer interrupt.

bit 2 0 = Do not wake up on watchdog timer interrupt.
1 = Wake up on watchdog timer interrupt.

EWUEX1 **Enable Wake Up External 1.** Wake using external interrupt source 1.

bit 1 0 = Do not wake up on external interrupt source 1.
1 = Wake up on external interrupt source 1.

EWUEX0 **Enable Wake Up External 0.** Wake using external interrupt source 0.

bit 0 0 = Do not wake up on external interrupt source 0.
1 = Wake up on external interrupt source 0.

System Clock Divider (SYSCLK)

	7	6	5	4	3	2	1	0	Reset Value
SFR C7h	0	0	DIVMOD1	DIVMOD0	0	DIV2	DIV1	DIV0	00h

NOTE: Changing the SYSCLK registers affects all internal clocks, including the ADC clock.

DIVMOD1−0 Clock Divide Mode

bits 5−4 Write:

DIVMOD	DIVIDE MODE
00	Normal mode (default, no divide).
01	Immediate mode: start divide immediately; return to Normal mode on Idle mode wakeup condition, or by direct write to SFR.
10	Delay mode: same as Immediate mode, except that the mode changes with the millisecond interrupt (MSINT). If MSINT is enabled, the divide will start on the next MSINT and return to normal mode on the following MSINT. If MSINT is not enabled, the divide will start on the next MSINT condition (even if masked) but will not leave the divide mode until the MSINT counter overflows, which follows a wakeup condition. Can exit by directly writing to SFR.
11	Manual mode: start divide immediately; exit mode only by directly writing to SFR. Same as immediate mode, but cannot return to Normal mode on Idle mode wakeup condition; only by directly writing to SFR.

Read:

DIVMOD	DIVIDE MODE STATUS
00	No divide
01	Divider is in Immediate mode
10	Divider is in Delay mode
11	Manual mode

DIV2−0 Divide Mode

bit 2−0

DIV	DIVISOR	f_{CLK} FREQUENCY
000	Divide by 2 (default)	$f_{CLK} = f_{SYS}/2$
001	Divide by 4	$f_{CLK} = f_{SYS}/4$
010	Divide by 8	$f_{CLK} = f_{SYS}/8$
011	Divide by 16	$f_{CLK} = f_{SYS}/16$
100	Divide by 32	$f_{CLK} = f_{SYS}/32$
101	Divide by 1024	$f_{CLK} = f_{SYS}/1024$
110	Divide by 2048	$f_{CLK} = f_{SYS}/2048$
111	Divide by 4096	$f_{CLK} = f_{SYS}/4096$

Program Status Word (PSW)

	7	6	5	4	3	2	1	0	Reset Value
SFR D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00h

CY bit 7 — **Carry Flag.** This bit is set when the last arithmetic operation resulted in a carry (during addition) or a borrow (during subtraction). Otherwise, it is cleared to ‘0’ by all arithmetic operations.

AC bit 6 — **Auxiliary Carry Flag.** This bit is set to ‘1’ if the last arithmetic operation resulted in a carry into (during addition), or a borrow (during subtraction) from the high order nibble. Otherwise, it is cleared to ‘0’ by all arithmetic operations.

F0 bit 5 — **User Flag 0.** This is a bit-addressable, general-purpose flag for software control.

RS1, RS0 bits 4−3 — **Register Bank Select 1−0.** These bits select which register bank is addressed during register accesses.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00h − 07h
0	1	1	08h − 0Fh
1	0	2	10h − 17h
1	1	3	18h − 1Fh

OV bit 2 — **Overflow Flag.** This bit is set to ‘1’ if the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise, it is cleared to ‘0’ by all arithmetic operations.

F1 bit 1 — **User Flag 1.** This is a bit-addressable, general-purpose flag for software control.

P bit 0 — **Parity Flag.** This bit is set to ‘1’ if the modulo-2 sum of the 8 bits of the accumulator is 1 (odd parity), and cleared to ‘0’ on even parity.

ADC Offset Calibration Low Byte (OCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR D1h								LSB	00h

All MSC120x devices support 24-bit calibration values.

OCL bits 7−0 **ADC Offset Calibration Low Byte.** This is the low byte of the 24-bit word that contains the ADC offset calibration. This value is written by the device after performing a calibration. This register is read/writable, so it can be used for setting calibration values independent of the hardware-generated calibration values.

ADC Offset Calibration Middle Byte (OCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR D2h									00h

All MSC120x devices support 24-bit calibration values.

OCM bits 7−0 **ADC Offset Calibration Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC offset calibration. This value is written by the device after performing a calibration. This register is read/writable, so it can be used for setting calibration values independent of the hardware-generated calibration values.

ADC Offset Calibration High Byte (OCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR D3h	MSB								00h

All MSC120x devices support 24-bit calibration values.

OCH bits 7−0 **ADC Offset Calibration High Byte.** This is the high byte of the 24-bit word that contains the ADC offset calibration. This value is written by the device after performing a calibration. This register is read/writable, so it can be used for setting calibration values independent of the hardware-generated calibration values.

ADC Gain Calibration Low Byte (GCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR D4h								LSB	5Ah

All MSC120x devices support 24-bit calibration values.

GCL bits 7−0 **ADC Gain Calibration Low Byte.** This is the low byte of the 24-bit word that contains the ADC gain calibration. This value is written by the device after performing a calibration. This register is read/writable, so it can be used for setting calibration values independent of the hardware-generated calibration values.

ADC Gain Calibration Middle Byte (GCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR D5h									ECh

All MSC120x devices support 24-bit calibration values.

GCM bits 7−0 **ADC Gain Calibration Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC gain calibration. This value is written by the device after performing a calibration. This register is read/writable, so it can be used for setting calibration values independent of the hardware-generated calibration values.

ADC Gain Calibration High Byte (GCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR D6h	MSB								5Fh

All MSC120x devices support 24-bit calibration values.

GCH bits 7−0 **ADC Gain Calibration High Byte.** This is the high byte of the 24-bit word that contains the ADC gain calibration. This value is written by the device after performing a calibration. This register is read/writable, so it can be used for setting calibration values independent of the hardware-generated calibration values.

ADC Input Multiplexer (ADMUX)

	7	6	5	4	3	2	1	0	Reset Value
SFR D7h	INP3	INP2	INP1	INP0	INN3	INN2	INN1	INN0	01h

INP3−0 bits 7−4 **Input Multiplexer Positive Input.** This selects the positive signal input.

INP3	INP2	INP1	INP0	POSITIVE INPUT
0	0	0	0	AIN0 (default)
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6 (MSC1200 only; for the MSC1201/02, this pin is internally tied to REFIN−)
0	1	1	1	AIN7 (MSC1200 only; for the MSC1201/02, this pin is internally tied to REFIN−)
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (requires ADMUX = FFh)

INN3−0 bits 3−0 **Input Multiplexer Negative Input.** This selects the negative signal input.

INN3	INN2	INN1	INN0	NEGATIVE INPUT
0	0	0	0	AIN0
0	0	0	1	AIN1 (default)
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6 (MSC1200 Only)
0	1	1	1	AIN7 (MSC1200 Only)
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (requires ADMUX = FFh)

Enable Interrupt Control (EICON)

	7	6	5	4	3	2	1	0	Reset Value
SFR D8h	0	1	EAI	AI	WDTI	0	0	0	40h

EAI bit 5 — **Enable Auxiliary Interrupt.** The Auxiliary Interrupt accesses nine different interrupts which are masked and identified by SFR registers PAI (SFR A5h), AIE (SFR A6h), and AISTAT (SFR A7h).

0 = Auxiliary Interrupt disabled (default).

1 = Auxiliary Interrupt enabled.

AI bit 4 — **Auxiliary Interrupt Flag.** AI must be cleared by software before exiting the interrupt service routine, after the source of the interrupt is cleared. Otherwise, the interrupt occurs again. Setting AI in software generates an Auxiliary Interrupt, if enabled.

0 = No Auxiliary Interrupt detected (default).

1 = Auxiliary Interrupt detected.

WDTI bit 3 — **Watchdog Timer Interrupt Flag.** WDTI must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting WDTI in software generates a watchdog time interrupt, if enabled. The Watchdog timer can generate an interrupt or reset. The interrupt is available only if the reset action is disabled in HCR0.

0 = No Watchdog Timer Interrupt Detected (default).

1 = Watchdog Timer Interrupt Detected.

ADC Results Low Byte (ADRESL)

	7	6	5	4	3	2	1	0	Reset Value
SFR D9h								LSB	00h

ADRESL bits 7−0 — **ADC Results Low Byte.** This is the low byte of the ADC results.

Reading from this register clears the ADC interrupt; however, AI in EICON (SFR D8) must also be cleared.

ADC Results Middle Byte (ADRESM)

	7	6	5	4	3	2	1	0	Reset Value
SFR DAh									00h

ADRESM bits 7−0 — **ADC Results Middle Byte.** This is the middle byte of the ADC results for the MSC1200/01 and the most significant byte for the MSC1202.

ADC Results High Byte (ADRESH)

	7	6	5	4	3	2	1	0	Reset Value
SFR DBh	MSB								00h

ADRESH bits 7−0 — **ADC Results High Byte.** This is the high byte and most significant byte of the ADC results for the MSC1200/01.

This is a sign-extended (Bipolar mode) or zero-padded (Unipolar mode) byte for the MSC1202 (that is, all 0s for positive ADC or unipolar results and all 1s for negative ADC results).

ADC Control 0 (ADCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR DCh	—	BOD	EVREF	VREFH	EBUF	PGA2	PGA1	PGA0	30h

BOD bit 6 — **Burnout Detect.** When enabled, this connects a positive current source to the positive channel and a negative current source to the negative channel. If the channel is open circuit, then the ADC results will be full-scale (buffer must be enabled).

0 = Burnout Current Sources Off (default).

1 = Burnout Current Sources On.

EVREF bit 5 — **Enable Internal Voltage Reference.** If an external voltage is used, the internal voltage reference should be disabled.

0 = Internal Voltage Reference Off for external reference.

1 = Internal Voltage Reference On (default). Note that in this mode, REFIN− must be connected to AGND.

VREFH bit 4 — **Voltage Reference High Select.** The internal voltage reference can be selected to be 2.5V or 1.25V.

0 = REFOUT/REF IN+ is 1.25V.

1 = REFOUT/REF IN+ is 2.5V (default).

EBUF bit 3 — **Enable Buffer.** Enables the input buffer to provide higher input impedance but limits the input voltage range and dissipates more power.

0 = Buffer disabled (default).

1 = Buffer enabled. Input signal limited to AV_{DD} − 1.5V.

PGA2−0 bits 2−0 — **Programmable Gain Amplifier.** Sets the gain for the PGA from 1 to 128.

PGA2	PGA1	PGA0	GAIN
0	0	0	1 (default)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Control 1 (ADCON1)

	7	6	5	4	3	2	1	0	Reset Value
SFR DDh	OF_UF	POL	SM1	SM0	—	CAL2	CAL1	CAL0	00h

OF_UF bit 6 — **Overflow/Underflow.** If this bit is set, the data in the Summation register is invalid; either an overflow or underflow occurred. This bit is cleared by writing a '0' to it.

POL bit 6 — **Polarity.** Polarity of the ADC result and Summation register.
0 = Bipolar.
1 = Unipolar.

POL	ANALOG INPUT	DIGITAL OUTPUT (ADRESH:ADRESM:ADRESL)	
		MSC1200 MSC1201	MSC1202(1)
0	+FSR	7FFFFFh	007FFFh
	ZERO	000000h	000000h
	−FSR	800000h	FF8000h
1	+FSR	FFFFFFh	00FFFFh
	ZERO	000000h	000000h
	−FSR	000000h	000000h

(1) The MSC1202 ADC result is sign-extended into ADRESH.

SM1−0 bits 5−4 — **Settling Mode.** Selects the type of filter or auto-select which defines the digital filter settling characteristics.

SM1	SM0	SETTLING MODE
0	0	Auto
0	1	Fast Settling Filter
1	0	$Sinc^2$ Filter
1	1	$Sinc^3$ Filter

CAL2−0 bits 2−0 — **Calibration Mode Control Bits.** Writing to this register initiates calibration.

CAL2	CAL1	CAL0	CALIBRATION MODE
0	0	0	No Calibration (default)
0	0	1	Self-Calibration, Offset and Gain
0	1	0	Self-Calibration, Offset only
0	1	1	Self-Calibration, Gain only
1	0	0	System Calibration, Offset only (requires external signal)
1	0	1	System Calibration, Gain only (requires external signal)
1	1	0	Reserved
1	1	1	Reserved

NOTE: Read value—000b.

ADC Control 2 (ADCON2)

	7	6	5	4	3	2	1	0	Reset Value
SFR DEh	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	1Bh

DR7−0 **Decimation Ratio LSB (refer to ADCON3, SFR DFh).**

bits 7−0

ADC Control 3 (ADCON3)

	7	6	5	4	3	2	1	0	Reset Value
SFR DFh	—	—	—	—	—	DR10	DR9	DR8	06h

DR10−8 **Decimation Ratio Most Significant 3 Bits.**

bits 2−0 The ADC output data rate is: $\frac{f_{MOD}}{\text{Decimation Ratio}}$ where $f_{MOD} = \frac{f_{CLK}}{(ACLK + 1) \cdot 64}$.

Accumulator (A or ACC)

	7	6	5	4	3	2	1	0	Reset Value
SFR E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h

ACC.7−0 **Accumulator.** This register serves as the accumulator for arithmetic and logic operations.

bits 7−0

Summation/Shifter Control (SSCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR E1h	SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	00h

The Summation register is powered down when the ADC is powered down. If all zeroes are written to this register, the 32-bit SUMR3−0 registers will be cleared. The Summation registers will do sign-extend if Bipolar Mode is selected in ADCON1.

SSCON1−0 Summation/Shift Count.

bits 7−6

SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	DESCRIPTION
0	0	0	0	0	0	0	0	Clear Summation Register
0	0	0	1	0	0	0	0	CPU Summation on Write to SUMR0 (sum count/shift ignored)
0	0	1	0	0	0	0	0	CPU Subtraction on Write to SUMR0 (sum count/shift ignored)
1	0	x	x	x	Note (1)	Note (1)	Note (1)	CPU Shift only
0	1	Note (1)	Note (1)	Note (1)	x	x	x	ADC Summation only
1	1	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	ADC Summation completes, then shift completes

(1) Refer to register bit definition.

SCNT2−0 bits 5−3 **Summation Count.** When the summation is complete an interrupt will be generated unless masked. Reading the SUMR0 register clears the interrupt.

SCNT2	SCNT1	SCNT0	SUMMATION COUNT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

SHF2−0 Shift Count.

bits 2−0

SHF2	SHF1	SHF0	SHIFT	DIVIDE
0	0	0	1	2
0	0	1	2	4
0	1	0	3	8
0	1	1	4	16
1	0	0	5	32
1	0	1	6	64
1	1	0	7	128
1	1	1	8	256

Summation 0 (SUMR0)

	7	6	5	4	3	2	1	0	Reset Value
SFR E2h								LSB	00h

SUMR0 **Summation 0.** This is the least significant byte of the 32-bit summation register, or bits 0 to 7.
bits 7−0 Write: Will cause values in SUMR3−0 to be added to the summation register.
Read: Will clear the Summation Interrupt.

Summation 1 (SUMR1)

	7	6	5	4	3	2	1	0	Reset Value
SFR E3h									00h

SUMR1 **Summation 1.** This is the most significant byte of the lowest 16 bits of the summation register, or bits 8−15.
bits 7−0

Summation 2 (SUMR2)

	7	6	5	4	3	2	1	0	Reset Value
SFR E4h									00h

SUMR2 **Summation 2.** This is the most significant byte of the lowest 24 bits of the summation register, or bits 16−23.
bits 7−0

Summation 3 (SUMR3)

	7	6	5	4	3	2	1	0	Reset Value
SFR E5h	MSB								00h

SUMR3 **Summation 3.** This is the most significant byte of the 32-bit summation register, or bits 24−31.
bits 7−0

Offset DAC (ODAC)

	7	6	5	4	3	2	1	0	Reset Value
SFR E6h									00h

ODAC **Offset DAC.** This register will shift the input by up to half of the ADC full-scale input range. The Offset DAC
bits 7−0 value is summed into the ADC prior to conversion. Writing 00h or 80h to ODAC turns off the Offset DAC. The offset DAC should be cleared prior to calibration, since the offset DAC analog output is applied directly to the ADC input.

bit 7 Offset DAC Sign Bit.
0 = Positive
1 = Negative

bit 6−0 $$\text{Offset} = \frac{-V_{REF}}{2 \cdot PGA} \cdot \left(\frac{ODAC\,[6:0]}{127}\right) \cdot (-1)^{bit7}$$

NOTE: ODAC cannot be used to offset the analog inputs so that the buffer can be used for signals within 50mV of AGND.

Low Voltage Detect Control (LVDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR E7h	ALVDIS	0	0	0	ALVD3	ALVD2	ALVD1	ALVD0	8Fh

ALVDIS **Analog Low Voltage Detect Disable.**

bit 7 0 = Enable Detection of Low Analog Supply Voltage (ALVD flag and interrupt are set when AV_{DD} < ALVD threshold)

1 = Disable Detection of Low Analog Supply Voltage

ALVD3−0 **Analog Low Voltage Detect.** Sets ALVD threshold.

bits 7−4 0000: 4.6V
0001: 4.2V
0010: 3.8V
0011: 3.6V
0100: 3.3V
0101: 3.1V
0110: 2.9V
0111: 2.7V
1000: Reserved
1001: Reserved
1010: Reserved
1011: Reserved
1100: Reserved
1101: Reserved
1110: Reserved
1111: Reserved

Extended Interrupt Enable (EIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR E8h	1	1	1	EWDI	EX5	EX4	EX3	EX2	E0h

EWDI **Enable Watchdog Interrupt.** This bit enables/disables the watchdog interrupt. The Watchdog timer is enabled by the WDTCON (SFR FFh) and PDCON (SFR F1h) registers.

bit 4 0 = Disable the Watchdog Interrupt

1 = Enable Interrupt Request Generated by the Watchdog Timer

EX5 **External Interrupt 5 Enable.** This bit enables/disables external interrupt 5.

bit 3 0 = Disable External Interrupt 5

1 = Enable External Interrupt 5

EX4 **External Interrupt 4 Enable.** This bit enables/disables external interrupt 4.

bit 2 0 = Disable External Interrupt 4

1 = Enable External Interrupt 4

EX3 **External Interrupt 3 Enable.** This bit enables/disables external interrupt 3.

bit 1 0 = Disable External Interrupt 3

1 = Enable External Interrupt 3

EX2 **External Interrupt 2 Enable.** This bit enables/disables external interrupt 2.

bit 0 0 = Disable External Interrupt 2

1 = Enable External Interrupt 2

Hardware Product Code 0 (HWPC0) (read-only)

	7	6	5	4	3	2	1	0	Reset Value
SFR E9h	0	0	0	0	0	0	DEVICE	MEMORY	0000_00xxb

HWPC0.7−0 Hardware Product Code LSB. Read-only.

bits 7−0

DEVICE	MEMORY	MODEL	FLASH MEMORY
0	0	MSC1200Y2, MSC1201Y2	4kB
0	1	MSC1200Y3, MSC1201Y3	8kB
1	0	MSC1202Y2	4kB
1	1	MSC1202Y3	8kB

Hardware Product Code 1 (HWPC1) (read-only)

	7	6	5	4	3	2	1	0	Reset Value
SFR EAh	0	0	1	0	0	0	0	0	20h

HWPC1.7−0 Hardware Product Code MSB. Read-only.

bits 7−0

Hardware Version (HWVER)

	7	6	5	4	3	2	1	0	Reset Value
SFR EBh									

Flash Memory Control (FMCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EEh	0	PGERA	0	FRCM	0	BUSY	SPM	FPM	02h

PGERA bit 6 — **Page Erase.** Available in both user and program modes.
0 = Disable Page Erase Mode
1 = Enable Page Erase Mode (automatically set by **page_erase** Boot ROM routine)

FRCM bit 4 — **Frequency Control Mode.**
0 = Bypass (default)
1 = Use Delay Line. Recommended for saving power.

BUSY bit 2 — **Write/Erase BUSY Signal.**
0 = Idle or Available
1 = Busy

SPM bit 1 — **Serial Programming Mode.** Read-only.
0 = Indicates the device is not in serial programming mode.
1 = Indicates the device is in serial programming mode (if FPM also = 1).

FPM bit 0 — **Flash Programming Mode.** Read-only.
0 = Indicates the device is operating in UAM.
1 = Indicates the device is operating in programming mode.

Flash Memory Timing Control (FTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EFh	FER3	FER2	FER1	FER0	FWR3	FWR2	FWR1	FWR0	A5h

Refer to *Flash Memory Characteristics*.

FER3−0 bits 7−4 — **Set Erase.** Flash Erase Time = (1 + FER) • (MSEC + 1) • t_{CLK}. This can be broken into multiple, shorter erase times. For more Information, see Application Report SBAA137, *Incremental Flash Memory Page Erase*, available for download from www.ti.com.
Industrial temperature range: 11ms
Commercial temperature range: 5ms

FWR3−0 bits 3−0 — **Set Write.** Set Flash Write Time = (1 + FWR) • (USEC + 1) • 5 • t_{CLK}. Total writing time will be longer. For more Information, see Application Report SBAA087, *In-Application Flash Programming*, available for download from www.ti.com.
Range: 30µs to 40µs.

B Register (B)

	7	6	5	4	3	2	1	0	Reset Value
SFR F0h									00h

B.7−0 bits 7−0 — **B Register.** This register serves as a second accumulator for certain arithmetic operations.

Power-Down Control (PDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR F1h	PDICLK	PDIDAC	PDI2C	0	PDADC	PDWDT	PDST	PDSPI	6Fh

Turning peripheral modules off puts the MSC120x in the lowest power mode.

PDICLK **Internal Clock Control.**

bit 7 0 = Internal Oscillator and PLL On (Internal Oscillator or PLL mode)

1 = Internal Oscillator and PLL Power Down (External Clock mode). Bit is not active on IOM or PLL mode.

PDIDAC **IDAC Control.**

bit 6 0 = IDAC On

1 = IDAC Power Down (default)

PDI2C **I2C Control.**

bit 5 0 = I^2C On (only when PDSPI = 1)

1 = I^2C Power Down (default)

PDADC **ADC Control.**

bit 3 0 = ADC On

1 = ADC, V_{REF}, and Summation registers are powered down (default).

PDWDT **Watchdog Timer Control.**

bit 2 0 = Watchdog Timer On

1 = Watchdog Timer Power Down (default)

PDST **System Timer Control.**

bit 1 0 = System Timer On

1 = System Timer Power Down (default)

PDSPI **SPI System Control.**

bit 0 0 = SPI System On

1 = SPI System Power Down (default)

$\overline{\text{PSEN}}$/ALE Select (PASEL)

	7	6	5	4	3	2	1	0	Reset Value
SFR F2h	PSEN4	PSEN3	PSEN2	PSEN1	PSEN0	0	0	0	00h

PSEN2−0 **$\overline{\text{PSEN}}$ Mode Select.** Defines the output on P3.6 in UAM or SFPM.

bits 7−3
- 00000: General-purpose I/O (default)
- 00001: SYSCLK
- 00011: Internal $\overline{\text{PSEN}}$ (refer to Figure 5 for timing)
- 00101: Internal ALE (refer to Figure 5 for timing)
- 00111: f_{OSC} (buffered XIN oscillator clock)
- 01001: Memory $\overline{\text{WR}}$ (MOVX write)
- 01011: T0 Out (overflow)(1)
- 01101: T1 Out (overflow)(1)
- 01111: f_{MOD}(2)
- 10001: SYSCLK/2 (toggles on rising edge)(2)
- 10011: Internal $\overline{\text{PSEN}}$/2(2)
- 10101: Internal ALE/2(2)
- 10111: f_{OSC}(2)
- 11001: Memory $\overline{\text{WR}}$/2 (MOVX write)(2)
- 11011: T0 Out/2 (overflow)(2)
- 11101: T1 Out/2 (overflow)(2)
- 11111: f_{MOD}/2(2)

(1) One period of these signals equal to t_{CLK}.
(2) Duty cycle is 50%.

Phase Lock Loop Low (PLLL)

	7	6	5	4	3	2	1	0	Reset Value
SFR F4h	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0	xxh

PLL7−0 **PLL Counter Value Least Significant Bit.**

bits 7−0 PLL Frequency = External Crystal Frequency • (PLL9:0 + 1).

Phase Lock Loop High (PLLH)

	7	6	5	4	3	2	1	0	Reset Value
SFR F5h	CLKSTAT2	CLKSTAT1	CLKSTAT0	PLLLOCK	0	0	PLL9	PLL8	xxh

CLKSTAT2−0 **Active Clock Status (read-only).** Derived from HCR2 setting; refer to Table 3.

bits 7−5

000: Reserved
001: Reserved
010: Reserved
011: External Clock Mode
100: PLL High-Frequency (HF) Mode (must read PLLLOCK to determine active clock status)
101: PLL Low-Frequency (LF) Mode (must read PLLLOCK to determine active clock status)
110: Internal Oscillator High-Frequency (HF) Mode
111: Internal Oscillator Low-Frequency (LF) Mode

PLLLOCK **PLL Lock Status and Status Enable.**

bit 4

For Write (PLL Lock Status Enable):
0 = No Effect
1 = Enable PLL Lock Detection (must wait 20ms before PLLLOCK read status is valid).
For Read (PLL Lock Status):
0 = PLL Not Locked (PLL may be inactive; refer to Table 3 for active clock mode)
1 = PLL Locked (PLL is active clock).

PLL9−8 **PLL Counter Value Most Significant 2 Bits (refer to PLLL, SFR F4h).**

bits 1−0

Analog Clock (ACLK)

	7	6	5	4	3	2	1	0	Reset Value
SFR F6h	0	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03h

FREQ6−0 **Clock Frequency − 1.** This value + 1 divides the system clock to create the ADC clock.

bits 6−0

$$f_{ACLK} = \frac{f_{CLK}}{ACLK + 1}, \text{ where } f_{CLK} = \frac{f_{OSC}}{SYSCLK\ divider}.$$

$$f_{MOD} = \frac{f_{ACLK}}{64}$$

$$\text{ADC Data Rate} = f_{DATA} = \frac{f_{MOD}}{\text{Decimation Ratio}}$$

System Reset (SRST)

	7	6	5	4	3	2	1	0	Reset Value
SFR F7h	0	0	0	0	0	0	0	RSTREQ	00h

RSTREQ **Reset Request.** Setting this bit to ‘1’ and then clearing to ‘0’ will generate a system reset.

bit 0

Extended Interrupt Priority (EIP)

	7	6	5	4	3	2	1	0	Reset Value
SFR F8h	1	1	1	PWDI	PX5	PX4	PX3	PX2	E0h

PWDI **Watchdog Interrupt Priority.** This bit controls the priority of the watchdog interrupt.
bit 4 0 = The watchdog interrupt is low priority.
1 = The watchdog interrupt is high priority.

PX5 **External Interrupt 5 Priority.** This bit controls the priority of external interrupt 5.
bit 3 0 = External interrupt 5 is low priority.
1 = External interrupt 5 is high priority.

PX4 **External Interrupt 4 Priority.** This bit controls the priority of external interrupt 4.
bit 2 0 = External interrupt 4 is low priority.
1 = External interrupt 4 is high priority.

PX3 **External Interrupt 3 Priority.** This bit controls the priority of external interrupt 3.
bit 1 0 = External interrupt 3 is low priority.
1 = External interrupt 3 is high priority.

PX2 **External Interrupt 2 Priority.** This bit controls the priority of external interrupt 2.
bit 0 0 = External interrupt 2 is low priority.
1 = External interrupt 2 is high priority.

Seconds Timer Interrupt (SECINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR F9h	WRT	SECINT6	SECINT5	SECINT4	SECINT3	SECINT2	SECINT1	SECINT0	7Fh

This system clock is divided by the value of the 16-bit register MSECH:MSECL. Then, that 1ms timer tick is divided by the register HMSEC which provides the 100ms signal used by this seconds timer. Therefore, this seconds timer can generate an interrupt which occurs from 100ms to 12.8 seconds. Reading this register will clear the Seconds Interrupt. This Interrupt can be monitored in the AIE register.

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished.
bit 7 Read = 0.
0 = Delay Write Operation. The SEC value is loaded when the current count expires.
1 = Write Immediately. The counter is loaded once the CPU completes the write operation.

SECINT6−0 **Seconds Count.** Normal operation would use 100ms as the clock interval.
bits 6−0 Seconds Interrupt = (1 + SEC) • (HMSEC + 1) • (MSEC + 1) • t_{CLK}.

Milliseconds TImer Interrupt (MSINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR FAh	WRT	MSINT6	MSINT5	MSINT4	MSINT3	MSINT2	MSINT1	MSINT0	7Fh

The clock used for this timer is the 1ms clock, which results from dividing the system clock by the values in registers MSECH:MSECL. Reading this register is necessary for clearing the interrupt; however, AI in EICON (SFR D8h) must also be cleared.

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished.
bit 7 Read = 0.
0 = Delay Write Operation. The MSINT value is loaded when the current count expires.
1 = Write Immediately. The MSINT counter is loaded once the CPU completes the write operation.

MSINT6−0 **Milliseconds Count.** Normal operation would use 1ms as the clock interval.
bits 6−0 MS Interrupt Interval = (1 + MSINT) • (MSEC + 1) • t_{CLK}

One Microsecond Timer (USEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FBh	0	0	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03h

FREQ5−0 **Clock Frequency − 1.** This value + 1 divides the system clock to create a 1µs Clock.
bits 5−0 USEC = CLK/(FREQ + 1). This clock is used to set Flash write time. See FTCON (SFR EFh).

One Millisecond TImer Low Byte (MSECL)

	7	6	5	4	3	2	1	0	Reset Value
SFR FCh	MSECL7	MSECL6	MSECL5	MSECL4	MSECL3	MSECL2	MSECL1	MSECL0	9Fh

MSECL7−0 **One Millisecond Timer Low Byte.** This value in combination with the next register is used to create a 1ms clock.
bits 7−0 1ms = (MSECH • 256 + MSECL + 1) • t_{CLK}. This clock is used to set Flash erase time. See FTCON (SFR EFh).

One Millisecond Timer High Byte (MSECH)

	7	6	5	4	3	2	1	0	Reset Value
SFR FDh	MSECH7	MSECH6	MSECH5	MSECH4	MSECH3	MSECH2	MSECH1	MSECH0	0Fh

MSECH7−0 **One Millisecond Timer High Byte.** This value in combination with the previous register is used to create a 1ms clock.
bits 7−0 1ms = (MSECH • 256 + MSECL + 1) • t_{CLK}.

One Hundred Millisecond Timer (HMSEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FEh	HMSEC7	HMSEC6	HMSEC5	HMSEC4	HMSEC3	HMSEC2	HMSEC1	HMSEC0	63h

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished.
Read = 0.

HMSEC7−0 **One Hundred Millisecond Timer.** This clock divides the 1ms clock to create a 100ms clock.
bits 7−0 100ms = (MSECH • 256 + MSECL + 1) • (HMSEC + 1) • t_{CLK}.

Watchdog Timer (WDTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR FFh	EWDT	DWDT	RWDT	WDCNT4	WDCNT3	WDCNT2	WDCNT1	WDCNT0	00h

EWDT **Enable Watchdog (R/W).**

bit 7 Write 1/Write 0 sequence sets the Watchdog Enable Counting bit.

DWDT **Disable Watchdog (R/W).**

bit 6 Write 1/Write 0 sequence clears the Watchdog Enable Counting bit.

RWDT **Reset Watchdog (R/W).**

bit 5 Write 1/Write 0 sequence restarts the Watchdog Counter.

WDCNT4−0 **Watchdog Count (R/W).**

bits 4−0 Watchdog expires in (WDCNT + 1) • HMSEC to (WDCNT + 2) • HMSEC, if the sequence is not asserted. There is an uncertainty of 1 count.

NOTE: If HCR0.3 (EWDR) is set and the watchdog timer expires, a system reset is generated. If HCR0.3 (EWDR) is cleared and the watchdog timer expires, an interrupt is generated (see Table 6).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSC1200Y2PFBT	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSC1200Y2	Samples
MSC1200Y3PFBT	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSC1200Y3	Samples
MSC1202Y2RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSC 1202Y2	Samples
MSC1202Y2RHHTG4	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSC 1202Y2	Samples
MSC1202Y3RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSC 1202Y3	Samples
MSC1202Y3RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSC 1202Y3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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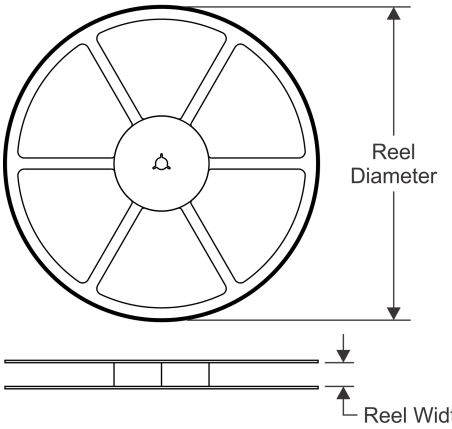
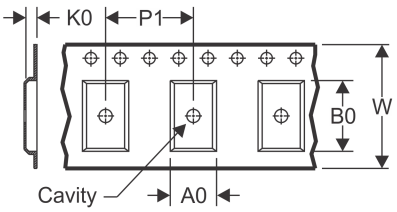
TAPE AND REEL INFORMATION

REEL DIMENSIONS

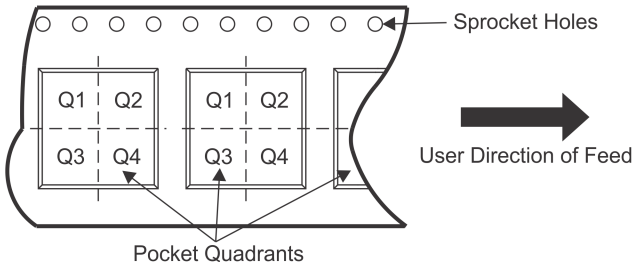


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

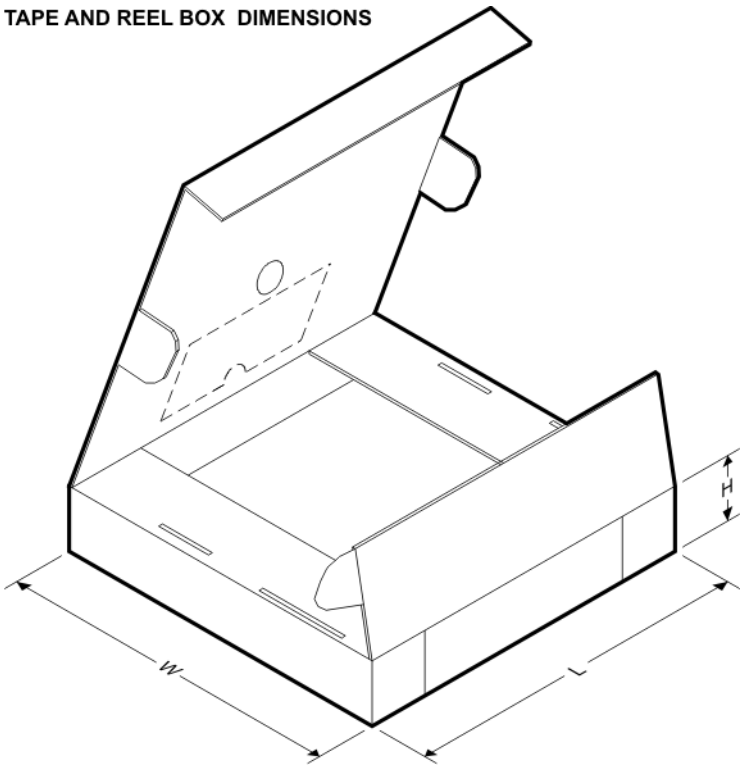
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSC1200Y2PFBT	TQFP	PFB	48	250	180.0	17.0	9.6	9.6	1.5	12.0	16.0	Q2
MSC1200Y3PFBT	TQFP	PFB	48	250	180.0	17.0	9.6	9.6	1.5	12.0	16.0	Q2
MSC1202Y2RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSC1202Y3RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSC1202Y3RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

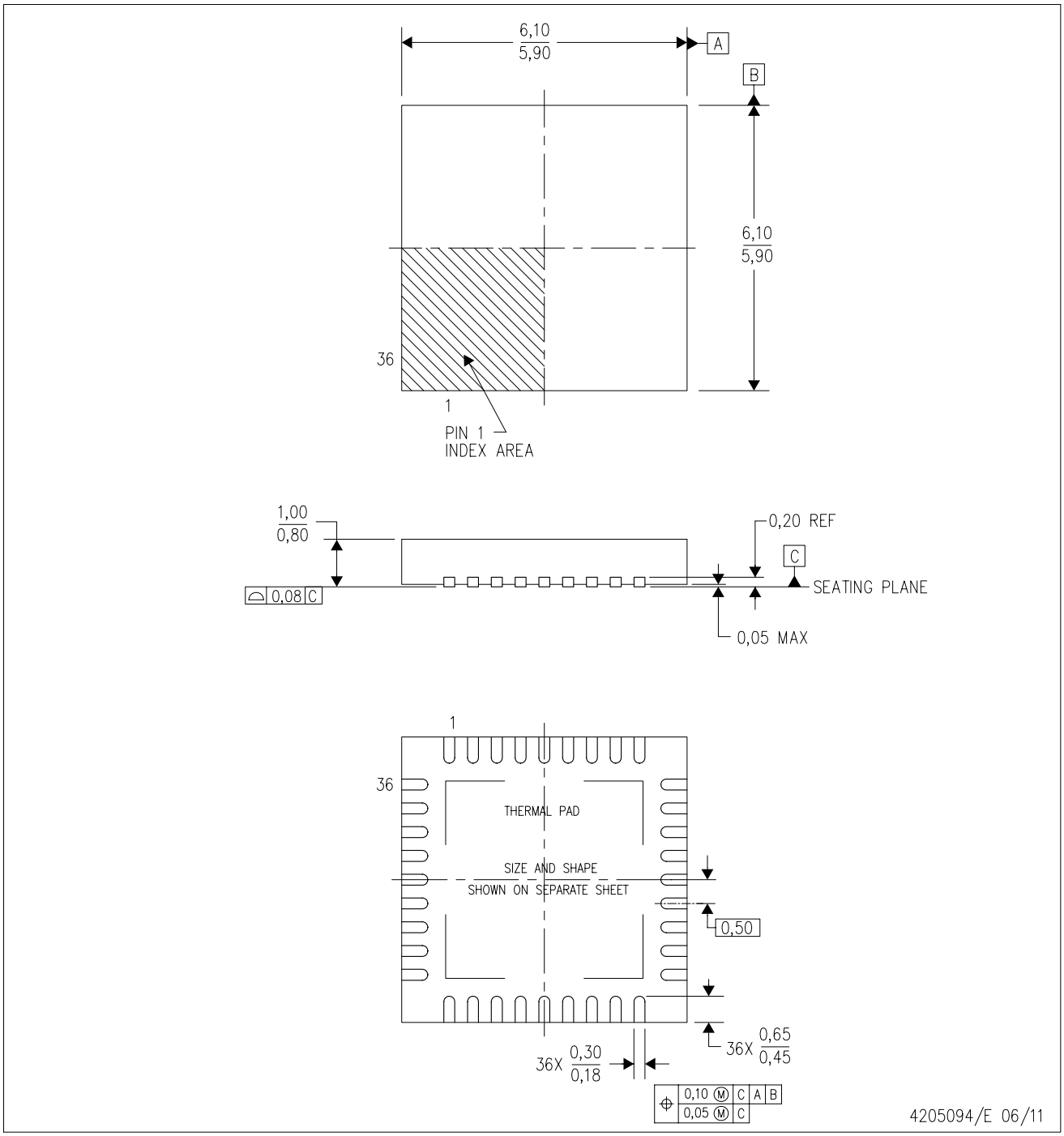
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSC1200Y2PFBT	TQFP	PFB	48	250	210.0	185.0	35.0
MSC1200Y3PFBT	TQFP	PFB	48	250	210.0	185.0	35.0
MSC1202Y2RHHT	VQFN	RHH	36	250	210.0	185.0	35.0
MSC1202Y3RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
MSC1202Y3RHHT	VQFN	RHH	36	250	210.0	185.0	35.0

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

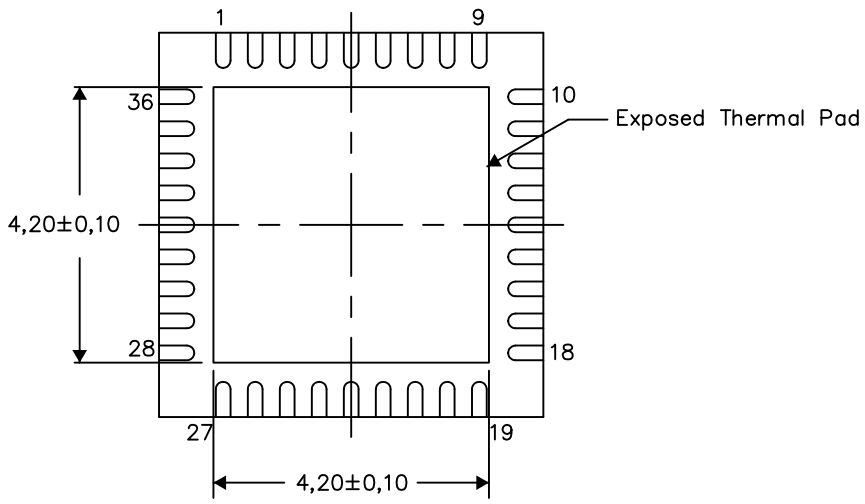
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

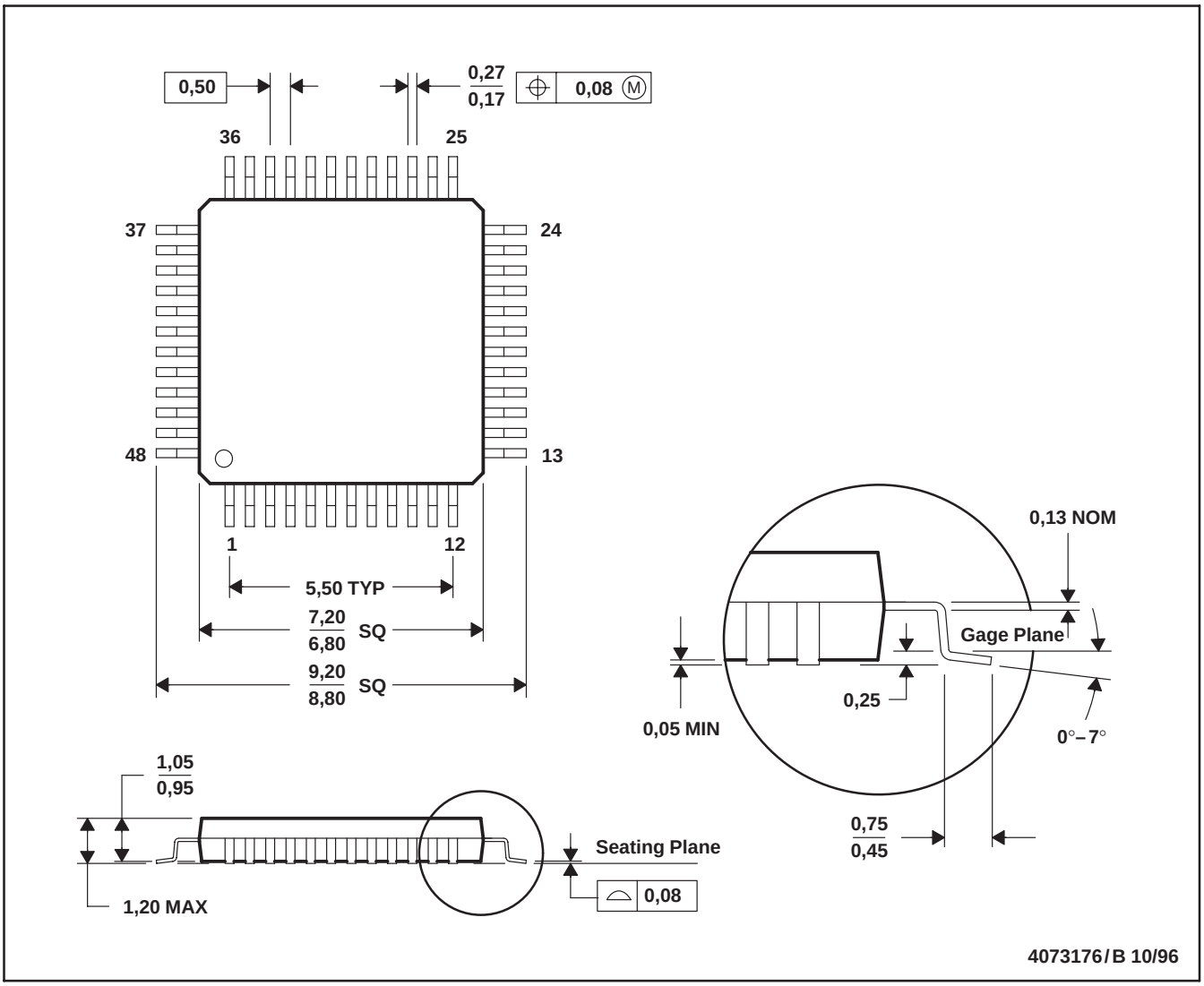
Exposed Thermal Pad Dimensions

4206362–2/M 11/13

NOTE: All linear dimensions are in millimeters

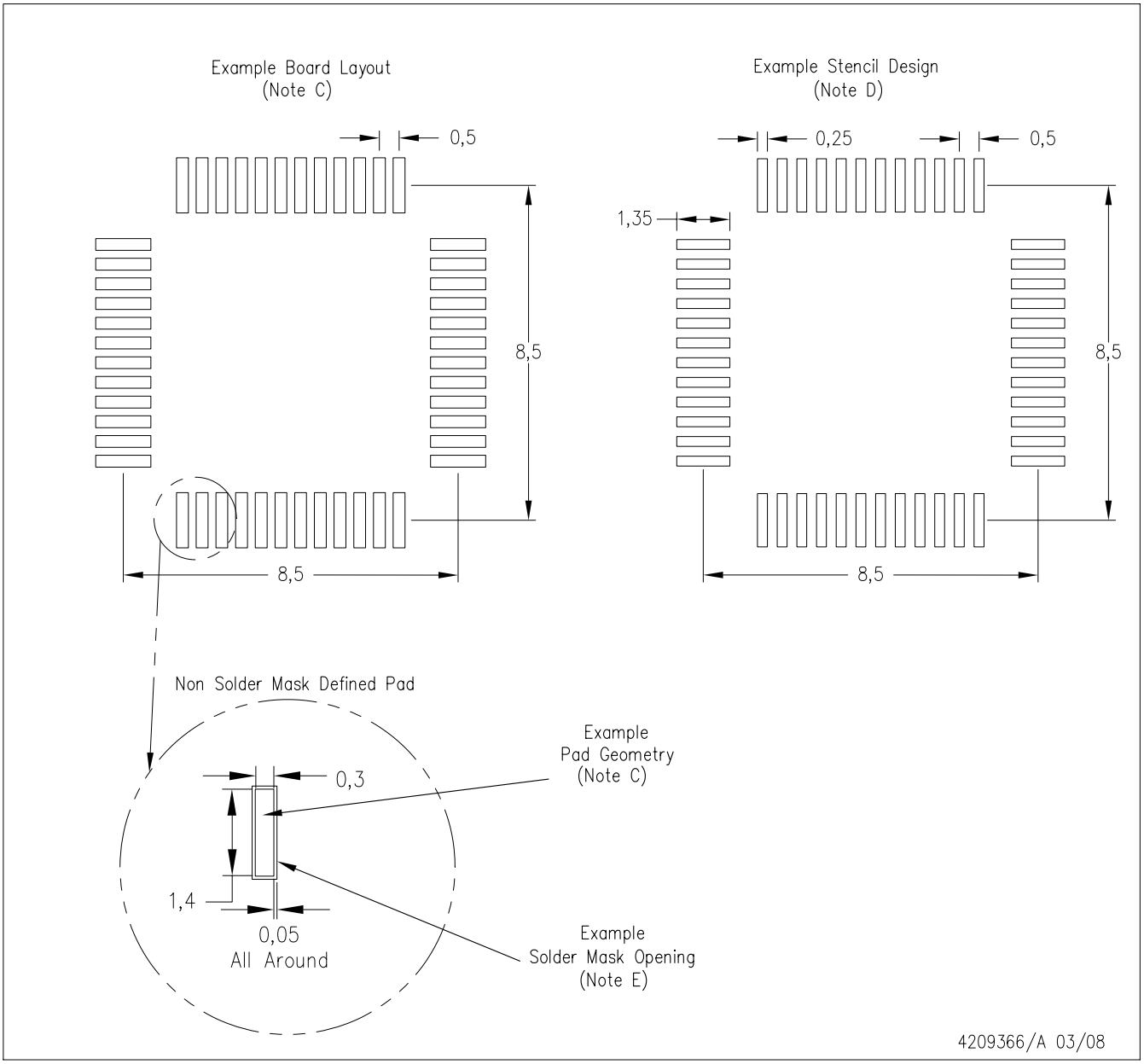
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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