WINSOURCE ELECTRONICS

THE DATASHEET OF

MSP430F1101AIPWR

SLAS241I – SEPTEMBER 1999 – REVISED DECEMBER 2008

- **Low Supply Voltage Range 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode: 160 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **16-Bit RISC Architecture, 125 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Various Internal Resistors**
  - **Single External Resistor**
  - **32-kHz Crystal**
  - **High-Frequency Crystal**
  - **Resonator**
  - **External Clock Source**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Family Members Include**
  MSP430C1101: 1KB ROM, 128B RAM
  MSP430C1111: 2KB ROM, 128B RAM
  MSP430C1121: 4KB ROM, 256B RAM
  MSP430F1101A: 1KB + 128B Flash Memory 128B RAM
  MSP430F1111A: 2KB + 256B Flash Memory 128B RAM
  MSP430F1121A: 4KB + 256B Flash Memory 256B RAM
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package, 20-Pin Plastic Small-Outline Thin Package, 20-Pin TVSOP (F11x1A only), and 24-Pin QFN**
- **For Complete Module Descriptions, Refer to the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

The MSP430x11x1(A) series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer, versatile analog comparator and fourteen I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand alone radio frequency (RF) sensor front end is another area of application. The I/O port inputs provide single slope A/D conversion capability on resistive sensors.

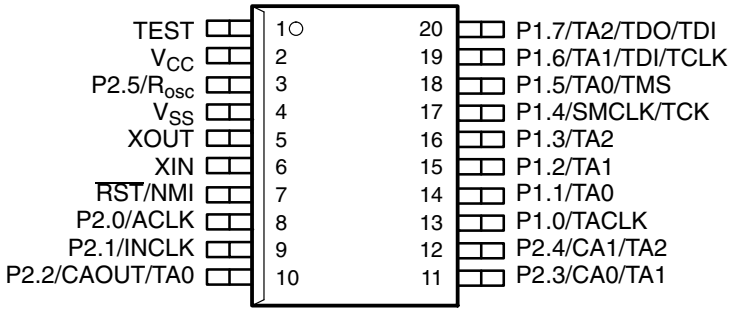
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

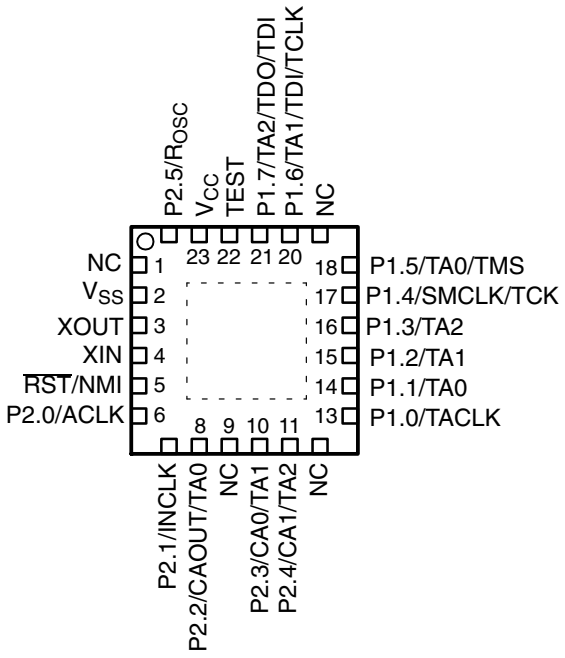
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	PLASTIC 20-PIN SOWB (DW)	**PLASTIC 20-PIN TSSOP (PW)**	**PLASTIC 20-PIN TVSOP (DGV)**	**PLASTIC 24-PIN QFN (RGE)**
–40°C to 85°C	MSP430C1101IDW MSP430C1111IDW MSP430C1121IDW MSP430F1101AIDW MSP430F1111AIDW MSP430F1121AIDW	MSP430C1101IPW MSP430C1111IPW MSP430C1121IPW MSP430F1101AIPW MSP430F1111AIPW MSP430F1121AIPW	MSP430F1101AIDGV MSP430F1111AIDGV MSP430F1121AIDGV	MSP430C1101IRGE MSP430C1111IRGE MSP430C1121IRGE MSP430F1101AIRGE MSP430F1111AIRGE MSP430F1121AIRGE

DW, PW, or DGV PACKAGE
(TOP VIEW)

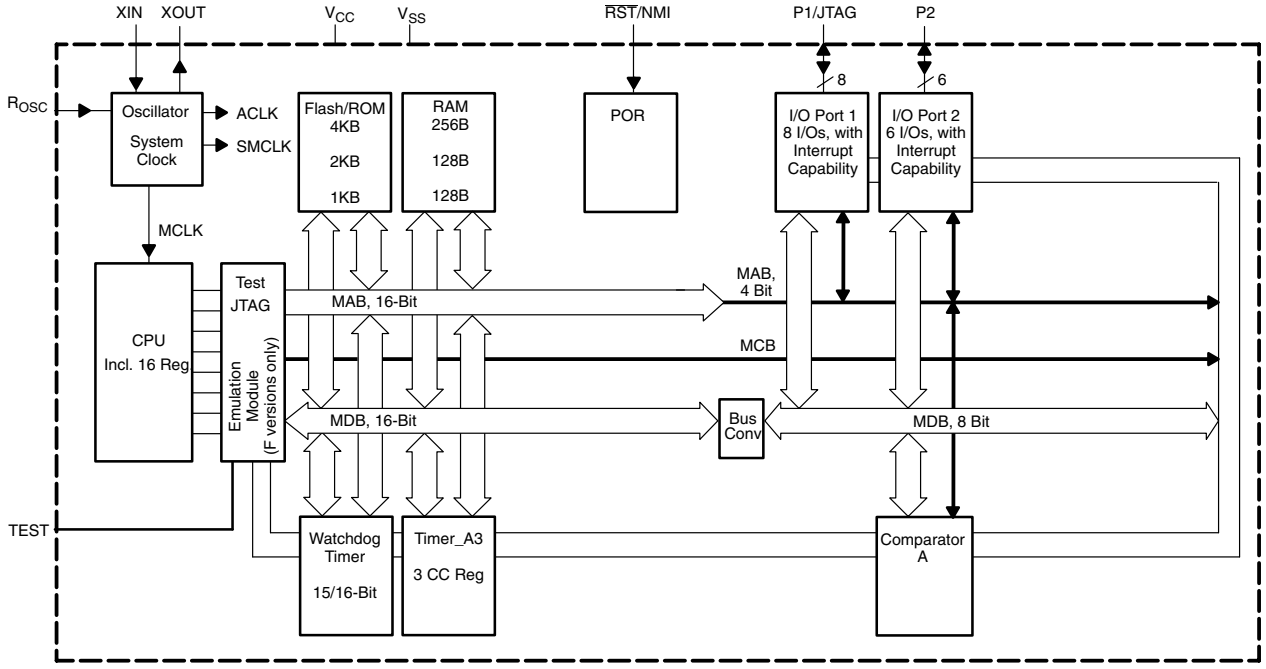


RGE PACKAGE
(TOP VIEW)



Note: NC pins not internally connected
Power Pad connection to V_{SS} recommended

functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DW, PW, OR DGV	RGE		
P1.0/TACLK	13	13	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	14	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	15	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	16	16	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK/TCK	17	17	I/O	General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test
P1.5/TA0/TMS	18	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test
P1.6/TA1/TDI/TCLK	19	20	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input or test clock input
P1.7/TA2/TDO/TDI†	20	21	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or data input during programming
P2.0/ACLK	8	6	I/O	General-purpose digital I/O pin/ACLK output
P2.1/INCLK	9	7	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	10	8	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/ comparator_A, output/BSL receive
P2.3/CA0/TA1	11	10	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/ comparator_A, input
P2.4/CA1/TA2	12	11	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/ comparator_A, input
P2.5/R_{OSC}	3	24	I/O	General-purpose digital I/O pin/input for external resistor that defines the DCO nominal frequency
$\overline{RST}$/NMI	7	5	I	Reset or nonmaskable interrupt input
TEST	1	22	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST.
V_{CC}	2	23		Supply voltage
V_{SS}	4	2		Ground reference
XIN	6	4	I	Input terminal of crystal oscillator
XOUT	5	3	O	Output terminal of crystal oscillator
QFN Pad	NA	Package Pad	NA	QFN package pad connection to V_{SS} recommended.

† TDO or TDI is selected via JTAG instruction.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 –––> R5
Single operands, destination only	e.g., CALL R8	PC –––>(TOS), R8–––> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 –––> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)–––> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) –––> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) –––> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) –––> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) –––> R11 R10 + 2–––> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 –––> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
  - DCO's dc generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO's dc generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO's dc generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DCO's dc generator is disabled.
  - Crystal oscillator is stopped.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash Memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 1 and 4)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
Comparator_A	CAIFG	maskable	0FFF6h	11
Watchdog Timer	WDTIFG	maskable	0FFF4h	10
Timer_A3	TACCR0 CCIFG (see Note 2)	maskable	0FFF2h	9
Timer_A3	TACCR1 CCIFG. TACCR2 CCIFG TAIFG (see Notes 1 and 2)	maskable	0FFF0h	8
			0FFEEh	7
			0FFECh	6
			0FFEAh	5
			0FFE8h	4
I/O Port P2 (eight flags; see Note 3)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	maskable	0FFE6h	3
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	maskable	0FFE4h	2
			0FFE2h	1
			0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module
3. There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0–5) implemented on the ’C11x1 and ’F11x1A devices.
4. (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE: Oscillator fault enable
NMIIE: (Non)maskable interrupt enable
ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-(0)

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG: Flag set on oscillator fault
NMIIFG: Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h								

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

memory organization

		MSP430C1101	MSP430C1111	MSP430C1121
Memory Main: interrupt vector Main: code memory	Size ROM ROM	1KB ROM 0FFFFh–0FFE0h 0FFFFh–0FC00h	2KB ROM 0FFFFh–0FFE0h 0FFFFh–0F800h	4KB ROM 0FFFFh–0FFE0h 0FFFFh–0F000h
Information memory	Size Flash	Not applicable	Not applicable	Not applicable
Boot memory	Size ROM	Not applicable	Not applicable	Not applicable
RAM	Size	128 Byte 027Fh – 0200h	128 Byte 027Fh – 0200h	256 Byte 02FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

		MSP430F1101A	MSP430F1111A	MSP430F1121A
Memory Main: interrupt vector Main: code memory	Size Flash Flash	1KB Flash 0FFFFh–0FFE0h 0FFFFh–0FC00h	2KB Flash 0FFFFh–0FFE0h 0FFFFh–0F800h	4KB Flash 0FFFFh–0FFE0h 0FFFFh–0F000h
Information memory	Size Flash	128 Byte 010FFh – 01080h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM	Size	128 Byte 027Fh – 0200h	128 Byte 027Fh – 0200h	256 Byte 02FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

bootstrap loader (BSL)

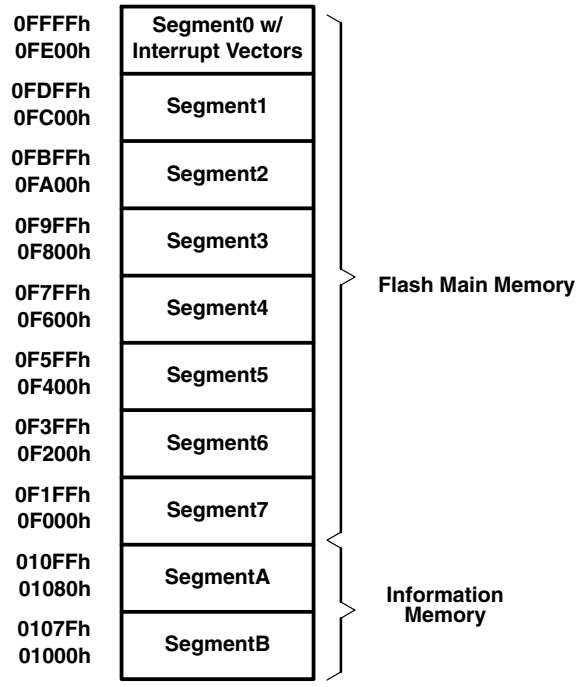
The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSL FUNCTION	DW, PW, AND DGV PACKAGE PINS	RGE PACKAGE PINS
Data Transmit	14 - P1.1	14 - P1.1
Data Receive	10 - P2.2	8 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



NOTE: All segments not implemented on all devices.

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x1xx Family User's Guide*, literature number SLAU049.

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules

digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2 (only six P2 I/O signals are available on external pins):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and six bits of port P2.
- Read/write access to port-control registers is supported by all instructions.

NOTE:

Only six bits of port P2 (P2.0 to P2.5) are available on external pins, but all control and data bits for port P2 are implemented.

watchdog timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Comparator_A

The primary function of the Comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS							
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
DW, PW, DGV	RGE					DW, PW, DGV	RGE
13 - P1.0	13 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	INCLK	INCLK				
14 - P1.1	14 - P1.1	TA0	CCI0A	CCR0	TA0	14 - P1.1	14 - P1.1
10 - P2.2	8 - P2.2	TA0	CCI0B			18 - P1.5	18 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
15 - P1.2	15 - P1.2	TA1	CCI1A	CCR1	TA1	11 - P2.3	10 - P2.3
		CAOUT (internal)	CCI1B			15 - P1.2	15 - P1.2
		V_{SS}	GND			19 - P1.6	20 - P1.6
		V_{CC}	V_{CC}				
16 - P1.3	16 - P1.3	TA2	CCI2A	CCR2	TA2	12 - P2.4	11 - P2.4
		ACLK (internal)	CCI2B			16 - P1.3	16 - P1.3
		V_{SS}	GND			20 - P1.7	21 - P1.7
		V_{CC}	V_{CC}				

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Timer_A	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register	TACCR2	0176h
	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h
	Capture/compare control	TACCTL2	0166h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
Basic Clock	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note) . . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature, T_{stg} (programmed device) . . . . . –40°C to 85°C

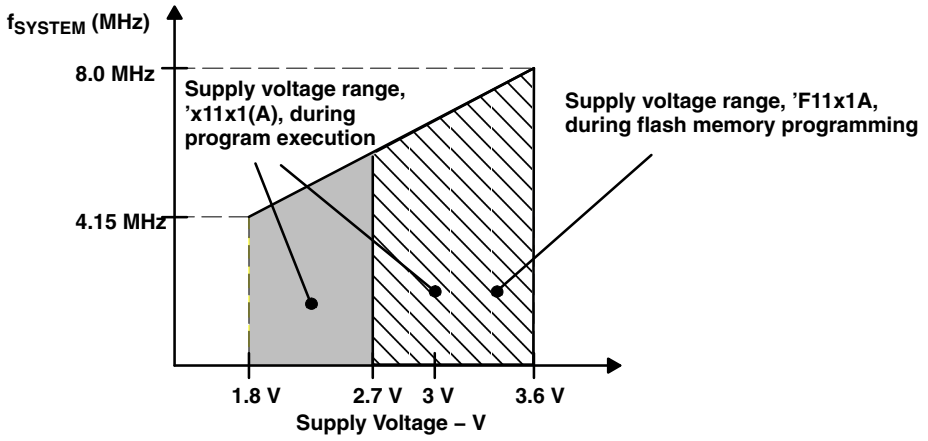
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (see Note 1)		MSP430C11x1	1.8		3.6	V
		MSP430F11x1A	1.8		3.6	
Supply voltage during program/erase flash memory, V_{CC}		MSP430F11x1A	2.7		3.6	V
Supply voltage, V_{SS}				0		V
Operating free-air temperature range, T_A		MSP430x11x1(A)	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 1 and 2)	LF mode selected, XTS=0	Watch crystal		32768		Hz
	XT1 mode selected, XTS=1	Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency $f_{(system)}$ (MCLK signal)		V_{CC} = 1.8 V, MSP430x11x1(A)	dc		4.15	MHz
		V_{CC} = 3.6 V, MSP430x11x1(A)	dc		8	

NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal. A 5.1MΩ resistor from XOUT to V_{SS} is recommended when V_{CC} < 2.5 V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 4.15MHz at $V_{CC} \geq$ 2.2 V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 8 MHz at $V_{CC} \geq$ 2.8 V.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.7 V.

Figure 1. Frequency vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into V_{CC}) excluding external current

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode	C11x1	T_A = –40°C to 85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		2.2 V		160	200	µA
					3 V		240	300	
			T_A = –40°C to 85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz		2.2 V		1.3	2	
					3 V		2.5	3.2	
		F11x1A	T_A = –40°C to 85°C, $f_{MCLK} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, Program executes in flash		2.2 V		200	250	
					3 V		300	350	
			T_A = –40°C to 85°C, Program executes in flash $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz		2.2 V		3	5	
					3 V		11	18	
$I_{(CPUOff)}$	Low-power mode (LPM0)	C11x1	T_A = –40°C to 85°C, $f_{(MCLK)}$ = 0, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		2.2 V		30	40	µA
					3 V		51	60	
		F11x1A	T_A = –40°C to 85°C, $f_{(MCLK)}$ = 0, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		2.2 V		32	45	
					3 V		55	70	
$I_{(LPM2)}$	Low-power mode (LPM2)		T_A = –40°C to 85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0		2.2 V		11	14	µA
					3 V		17	22	
$I_{(LPM3)}$	Low-power mode (LPM3)	C11x1	T_A = –40°C to 85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1		2.2 V		1.2	1.7	µA
					3 V		2	2.7	
		F11x1A	T_A = –40°C	$f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1	2.2 V		0.8	1.2	
			T_A = 25°C				0.7	1	
			T_A = 85°C				1.6	2.3	
			T_A = –40°C		3 V		1.8	2.2	
			T_A = 25°C				1.6	1.9	
			T_A = 85°C				2.3	3.4	
$I_{(LPM4)}$	Low-power mode (LPM4)	C11x1	T_A = –40°C	$f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	2.2 V/3 V		0.1	0.5	µA
			T_A = 25°C				0.1	0.5	
			T_A = 85°C				0.4	0.8	
		F11x1A	T_A = –40°C		2.2 V/3 V		0.1	0.5	
			T_A = 25°C				0.1	0.5	
			T_A = 85°C				0.8	1.9	

NOTE: All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

current consumption of active mode versus system frequency, C version, F version

$$I_{AM} = I_{AM[1\ MHz]} \times f_{system}\ [MHz]$$

current consumption of active mode versus supply voltage, C version

$$I_{AM} = I_{AM[3\ V]} + 105\ \mu A/V \times (V_{CC} - 3\ V)$$

current consumption of active mode versus supply voltage, F version

$$I_{AM} = I_{AM[3\ V]} + 120\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1 (P1.0 to P1.7) and P2 (P2.0 to P2.5)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	2.2 V	1.1		1.5	V
		3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	2.2 V	0.4		0.9	V
		3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	2.2 V	0.3		1.1	V
		3 V	0.5		1	

standard inputs – $\overline{\text{RST}}$/NMI, JTAG (TCK, TMS, TDI/TCLK)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.

leakage current

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	Port P1: P1.x, $0 \le x \le 7$ (see Notes 1 and 2)	2.2 V/3 V			±50	nA
		Port P2: P2.x, $0 \le x \le 5$ (see Notes 1 and 2)	2.2 V/3 V			±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1 (P1.0 to P1.7) and P2 (P2.0 to P2.5)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage Port 1 and Port 2 (C11x1) Port 1 (F11x1A)	$I_{(OHmax)}$ = –1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{(OHmax)}$ = –6 mA		See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{(OHmax)}$ = –1.5 mA	V_{CC} = 3 V	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA		See Note 2	V_{CC}–0.6		V_{CC}	
V_{OH}	High-level output voltage Port 2 (F11x1A)	$I_{(OHmax)}$ = –1 mA	V_{CC} = 2.2 V	See Note 3	V_{CC}–0.25		V_{CC}	V
		$I_{(OHmax)}$ = –3.4 mA		See Note 3	V_{CC}–0.6		V_{CC}	
		$I_{(OHmax)}$ = –1 mA	V_{CC} = 3 V	See Note 3	V_{CC}–0.25		V_{CC}	
		$I_{(OHmax)}$ = –3.4 mA		See Note 3	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage Port 1 and Port 2 (C11x1, F11x1A)	$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 3 V	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
3. One output loaded at a time.

output frequency

PARAMETER		TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT
f_{P20}	Output frequency	P2.0/ACLK, C_L = 20 pF		2.2 V/3 V			f_{System}	MHz
f_{TAx}		TA0, TA1, TA2, C_L = 20 pF Internal clock source, SMCLK signal applied (see Note 1)		2.2 V/3 V	dc		f_{System}	
t_{Xdc}	Duty cycle of O/P frequency	P1.4/SMCLK, C_L = 20 pF	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$		35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$		50%– 15 ns	50%	50%+ 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	2.2 V/3 V	50%– 15 ns	50%	50%+ 15 ns	
		P2.0/ACLK, C_L = 20 pF	$f_{P20} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{P20} = f_{LFXT1} = f_{LF}$		30%		70%	
			$f_{P20} = f_{LFXT1/n}$			50%		
t_{TAdc}		TA0, TA1, TA2, C_L = 20 pF, duty cycle = 50%		2.2 V/3 V		0	±50	ns

NOTE 1: The limits of the system clock MCLK has to be met. MCLK and SMCLK can have different frequencies.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1 and P2 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

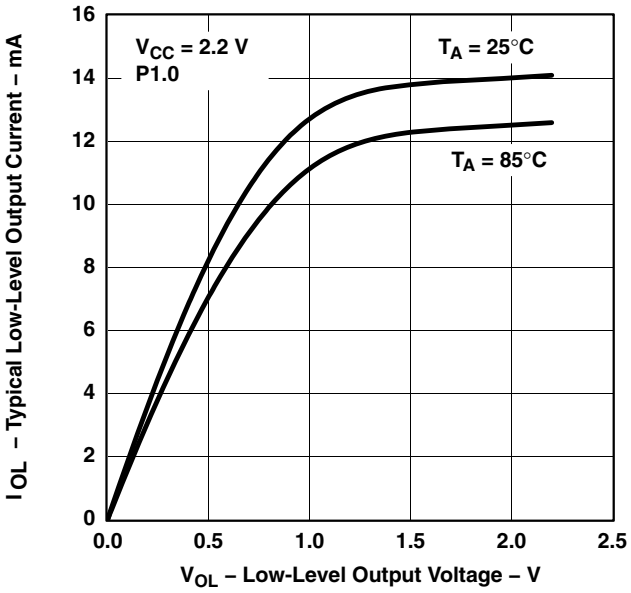


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

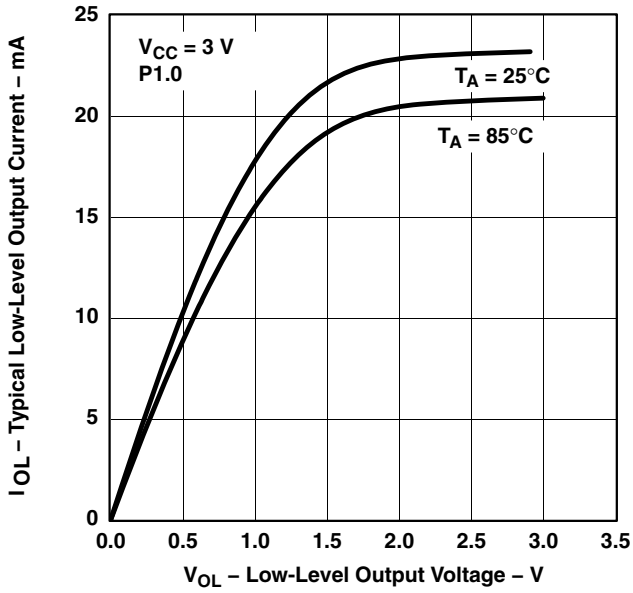


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

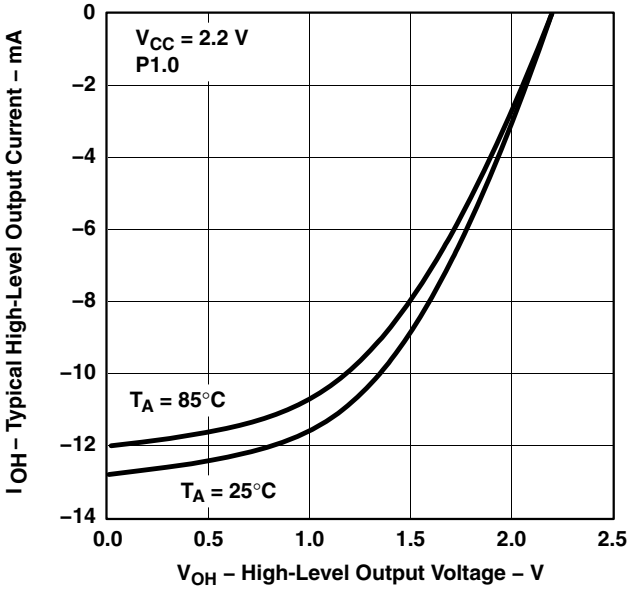


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

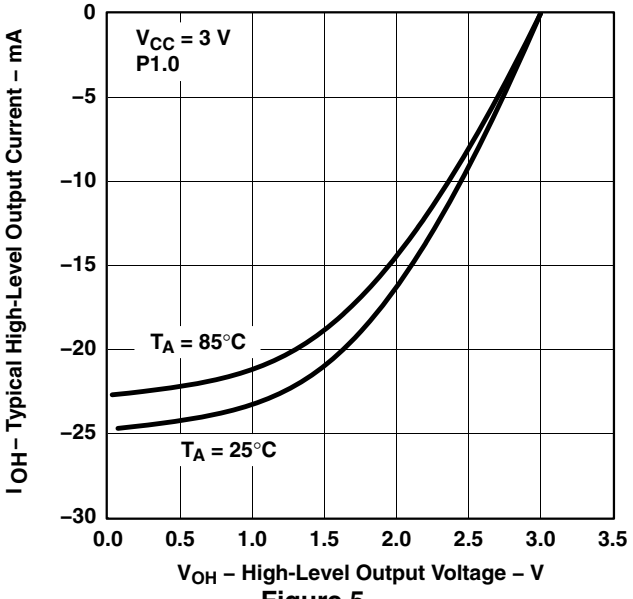


Figure 5

NOTE: One output loaded at a time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

optional resistors, individually programmable with ROM code (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(opt1)}$	Resistors, individually programmable with ROM code, all port pins, values applicable for pulldown and pullup	V_{CC} = 2.2 V/3 V	2.5	5	10	kΩ
$R_{(opt2)}$			3.8	7.7	15	kΩ
$R_{(opt3)}$			7.6	15	31	kΩ
$R_{(opt4)}$			11.5	23	46	kΩ
$R_{(opt5)}$			23	45	90	kΩ
$R_{(opt6)}$			46	90	180	kΩ
$R_{(opt7)}$			70	140	280	kΩ
$R_{(opt8)}$			115	230	460	kΩ
$R_{(opt9)}$			160	320	640	kΩ
$R_{(opt10)}$			205	420	830	kΩ

NOTE 1: Optional resistors R_{optx} for pulldown or pullup are not available in standard flash memory device MSP430F11x1A.

wake-up from low-power modes (LPMx)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(LPM0)}$	Delay time (see Note 1)	V_{CC} = 2.2 V/3 V			100		ns
$t_{(LPM2)}$		V_{CC} = 2.2 V/3 V			100		ns
$t_{(LPM3)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	µs
$t_{(LPM4)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	µs

NOTE 1: Parameter applicable only if DCOCLK is used for MCLK.

RAM

PARAMETER		MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1	V_{CC} = 2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ } 0.25\ V_{CC}\text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ } 0.5V_{CC}\text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	(see Figure 6 and Figure 7)	PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	V_{CC} = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	V_{CC} = 2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	90	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

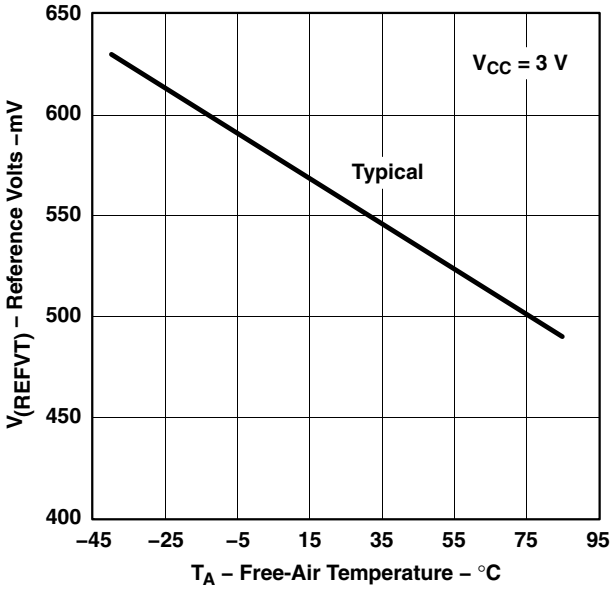


Figure 6. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

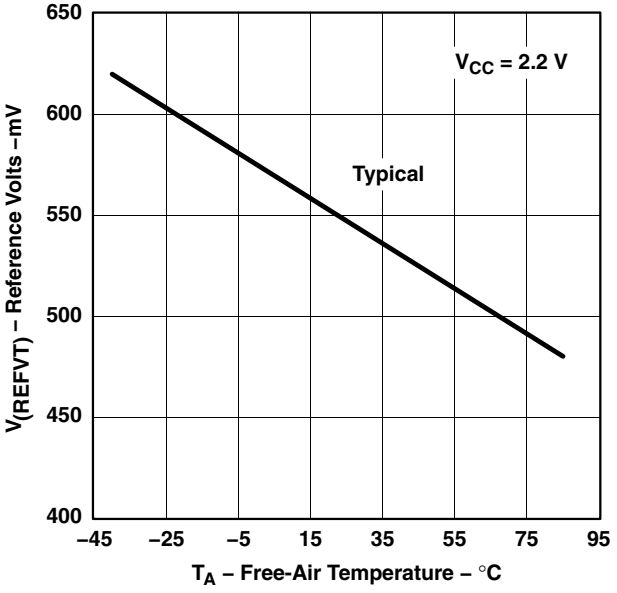


Figure 7. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

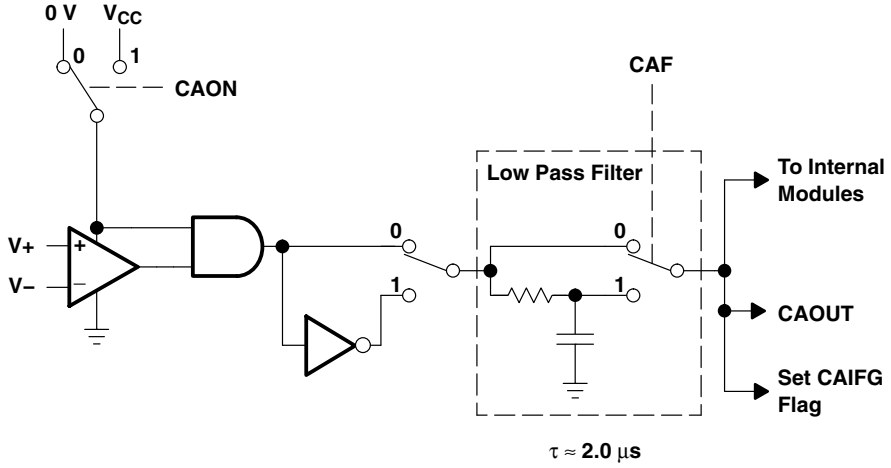


Figure 8. Block Diagram of Comparator_A Module

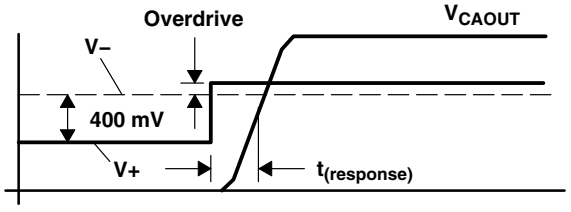


Figure 9. Overdrive Definition

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PUC/POR

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(POR\_Delay)}$	Internal time delay to release POR		V_{CC} = 2.2 V/3 V		150	250	µs
V_{POR}	V_{CC} threshold at which POR release delay time begins (see Note 1)	T_A = –40°C		1.4		1.8	V
		T_A = 25°C		1.1		1.5	
		T_A = 85°C		0.8		1.2	
$V_{(min)}$	V_{CC} threshold required to generate a POR (see Note 2)	V_{CC} |dV/dt| ≥ 1V/ms		0.2			V
$t_{(reset)}$	$\overline{RST}$/NMI low time for PUC/POR	Reset is accepted internally		2			µs

NOTES: 1. V_{CC} rise time dV/dt ≥ 1V/ms.
2. When driving V_{CC} low in order to generate a POR condition, V_{CC} should be driven to 200mV or lower with a dV/dt equal to or less than –1V/ms. The corresponding rising V_{CC} must also meet the dV/dt requirement equal to or greater than +1V/ms.

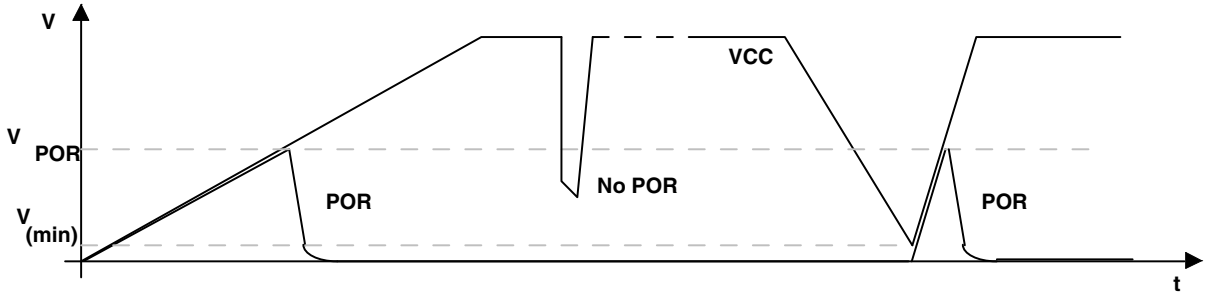


Figure 10. Power-On Reset (POR) vs Supply Voltage

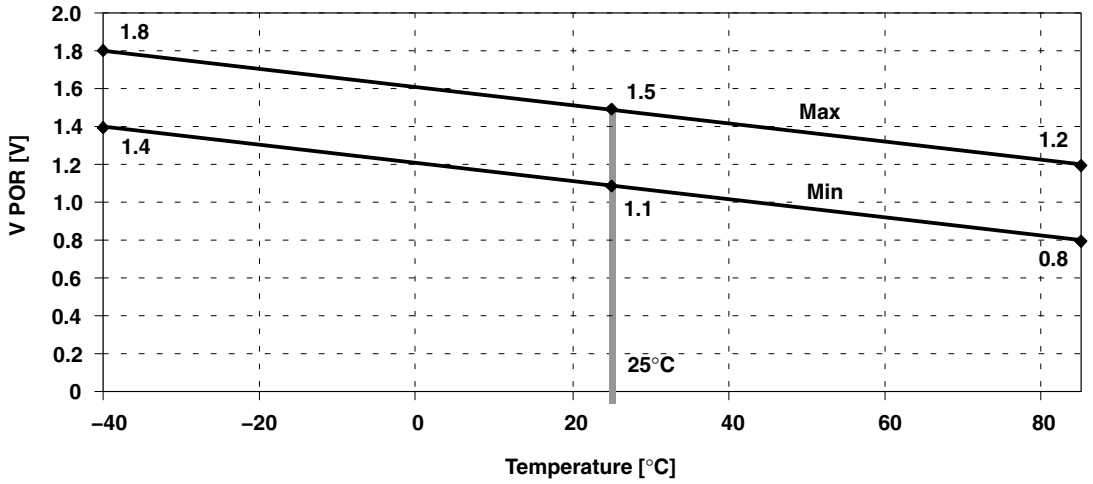


Figure 11. V_{POR} vs Temperature

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.08	0.12	0.15	MHz
		3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.14	0.19	0.23	MHz
		3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.22	0.30	0.36	MHz
		3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.37	0.49	0.59	MHz
		3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	0.61	0.77	0.93	MHz
		3 V	0.61	0.75	0.9	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	1	1.2	1.5	MHz
		3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	1.6	1.9	2.2	MHz
		3 V	1.69	2	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	2.4	2.9	3.4	MHz
		3 V	2.7	3.2	3.65	
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V	4	4.5	4.9	MHz
		3 V	4.4	4.9	5.4	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V/3 V	f_{DCO40} x1.7	f_{DCO40} x2.1	f_{DCO40} x2.5	MHz
$S_{(Rsel)}$	$S_R = f_{Rsel+1}/f_{Rsel}$	2.2 V/3 V	1.35	1.65	2	ratio
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1}/f_{DCO}$	2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	2.2 V	–0.31	–0.36	–0.40	%/°C
		3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	2.2 V/3 V	0	5	10	%/V

NOTE 1: These parameters are not production tested.

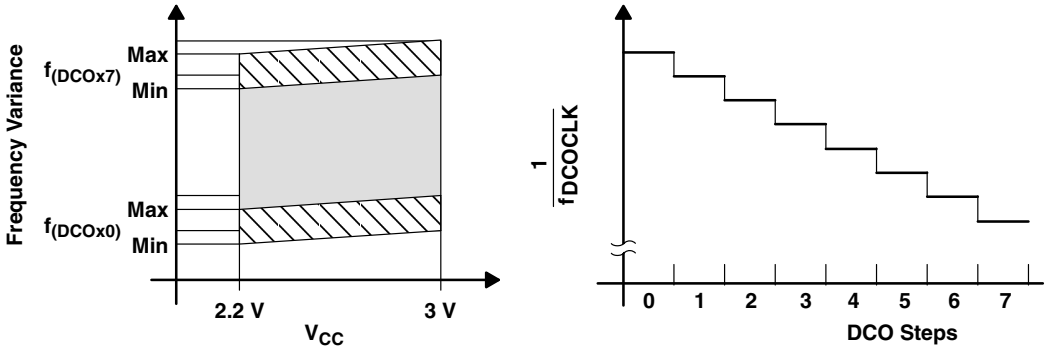


Figure 12. DCO Characteristics

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for $f_{(DCOx0)}$ to $f_{(DCOx7)}$ are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps Rsel1, ... Rsel6 overlaps Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often $f_{(DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{(DCO)} \times f_{(DCO+1)}}{MOD \times f_{(DCO)} + (32 - MOD) \times f_{(DCO+1)}}$$

DCO when using R_{OSC} (see Note 1)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{DCO}, DCO output frequency	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 1, T_A = 25°C	2.2 V		1.8±15%		MHz
		3 V		1.95±15%		MHz
D_t, Temperature drift	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V/3 V		±0.1		%/°C
D_v, Drift with V_{CC} variation	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V/3 V		10		%/V

NOTES: 1. R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50ppm/°C.

crystal oscillator, LFXT1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Input capacitance	XTS=0, LF mode selected, V_{CC} = 2.2 V / 3 V		12		pF
		XTS=1, XT1 mode selected, V_{CC} = 2.2 V / 3 V (see Note 1)		2		
C_{XOUT}	Output capacitance	XTS=0, LF mode selected, V_{CC} = 2.2 V / 3 V		12		pF
		XTS=1, XT1 mode selected, V_{CC} = 2.2 V / 3 V (see Note 1)		2		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 2)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	See Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time	See Note 2	2.7 V/ 3.6 V	200			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TEST pull-down resistor implemented in all versions.

JTAG fuse (see Note 1)

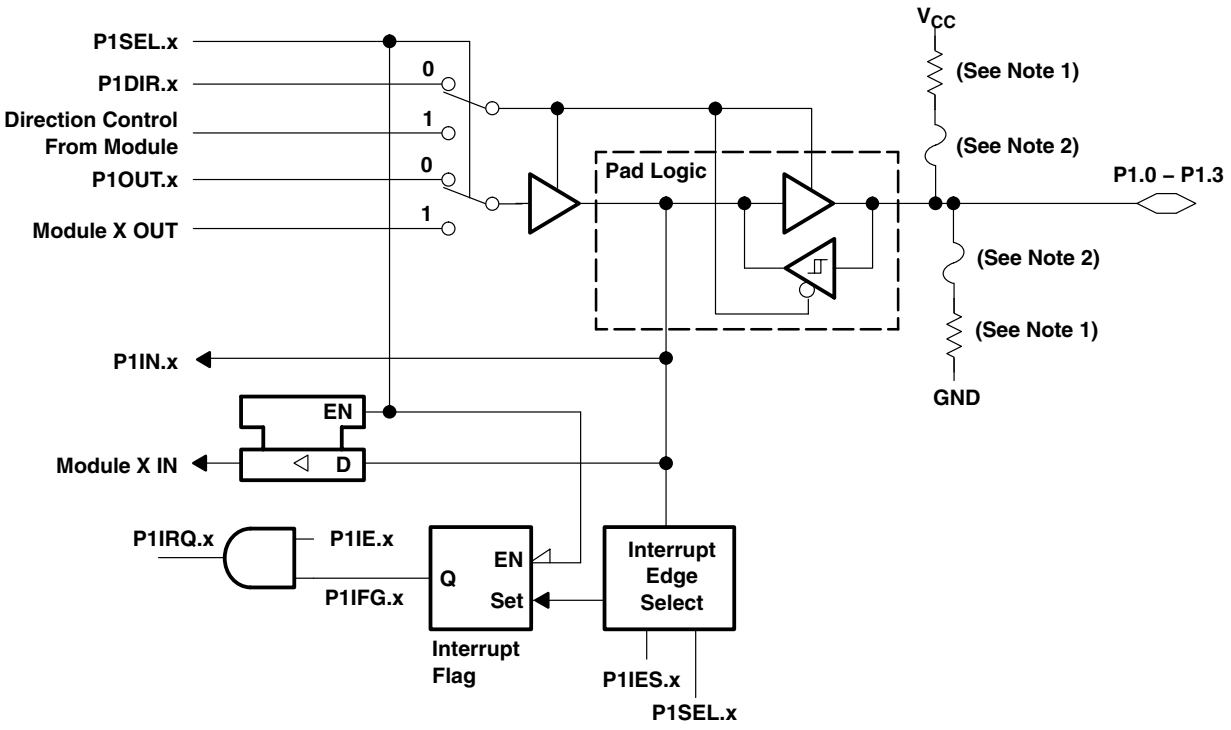
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TEST for fuse blow ('C11x1)			3.5		3.9	V
	Voltage level on TEST for fuse blow ('F11x1A)			6		7	V
I_{FB}	Supply current into TEST during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation (F versions only) features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.3, input/output with Schmitt trigger



NOTE: x = Bit/identifier, 0 to 3 for port P1

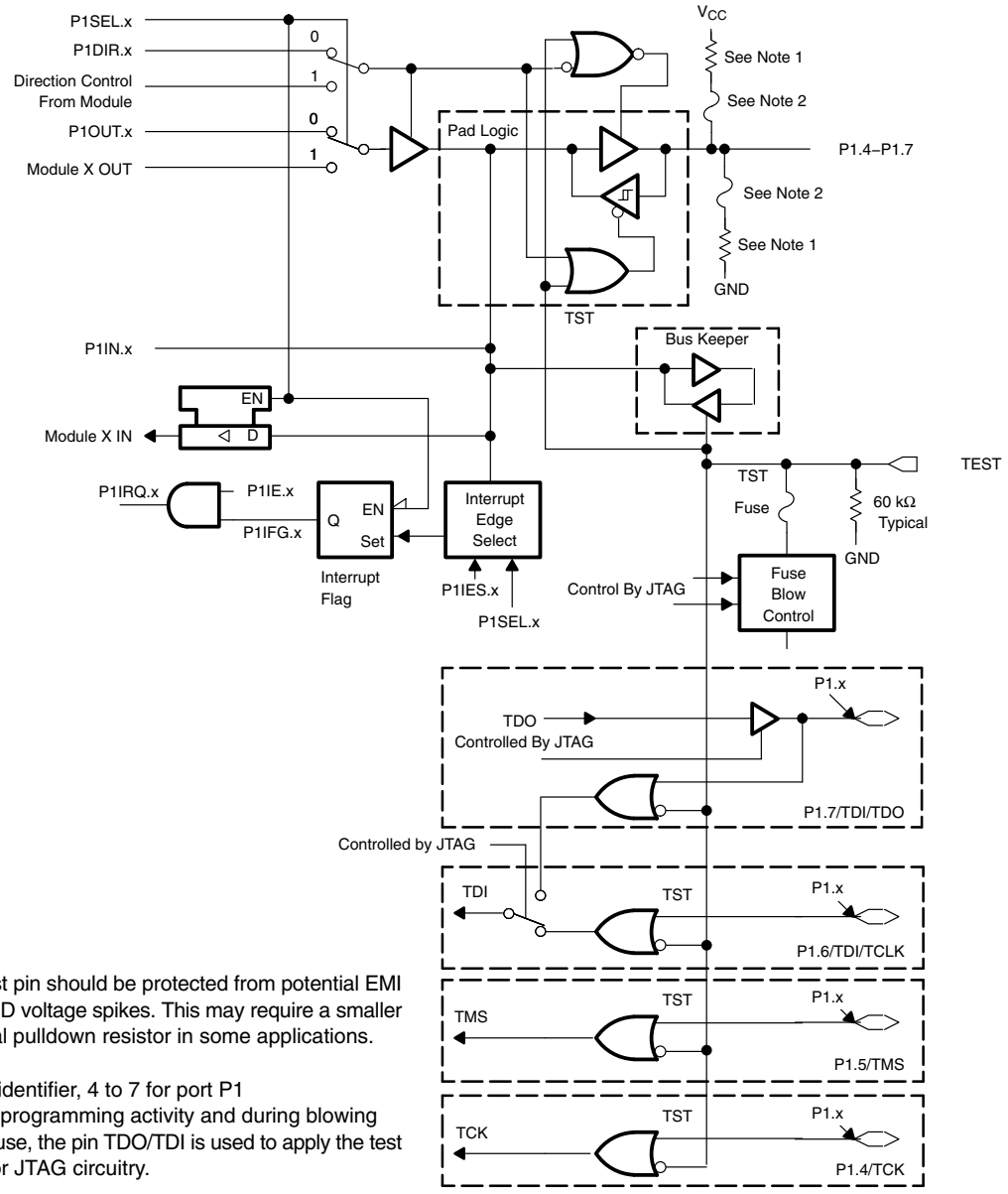
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	V_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3

† Signal from or to Timer_A

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P1, P1.4 to P1.7, input/output with Schmitt trigger and in-system access features



NOTE: The test pin should be protected from potential EMI and ESD voltage spikes. This may require a smaller external pulldown resistor in some applications.

x = Bit identifier, 4 to 7 for port P1
During programming activity and during blowing of the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

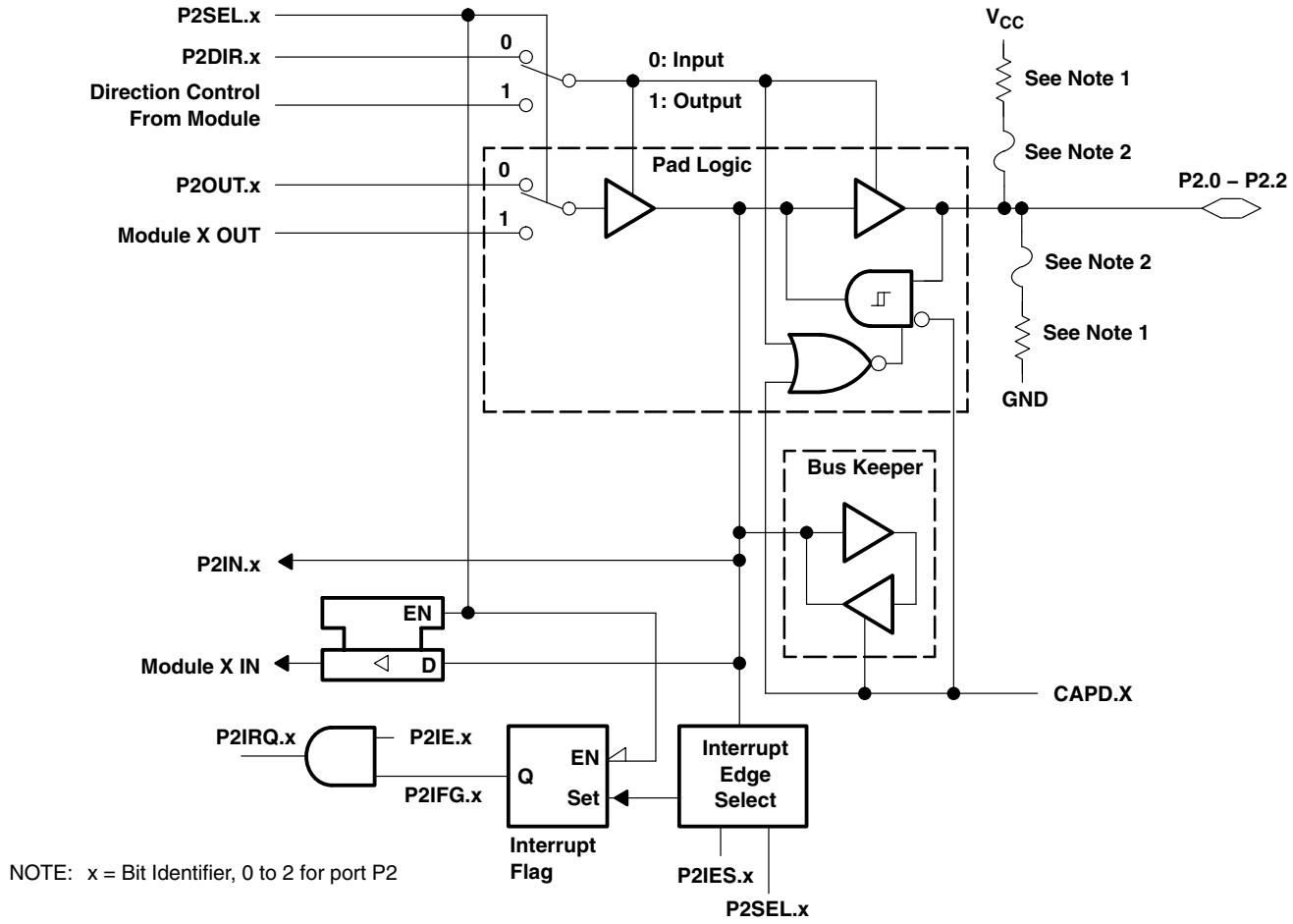
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P2, P2.0 to P2.2, input/output with Schmitt trigger



NOTE: x = Bit Identifier, 0 to 2 for port P2

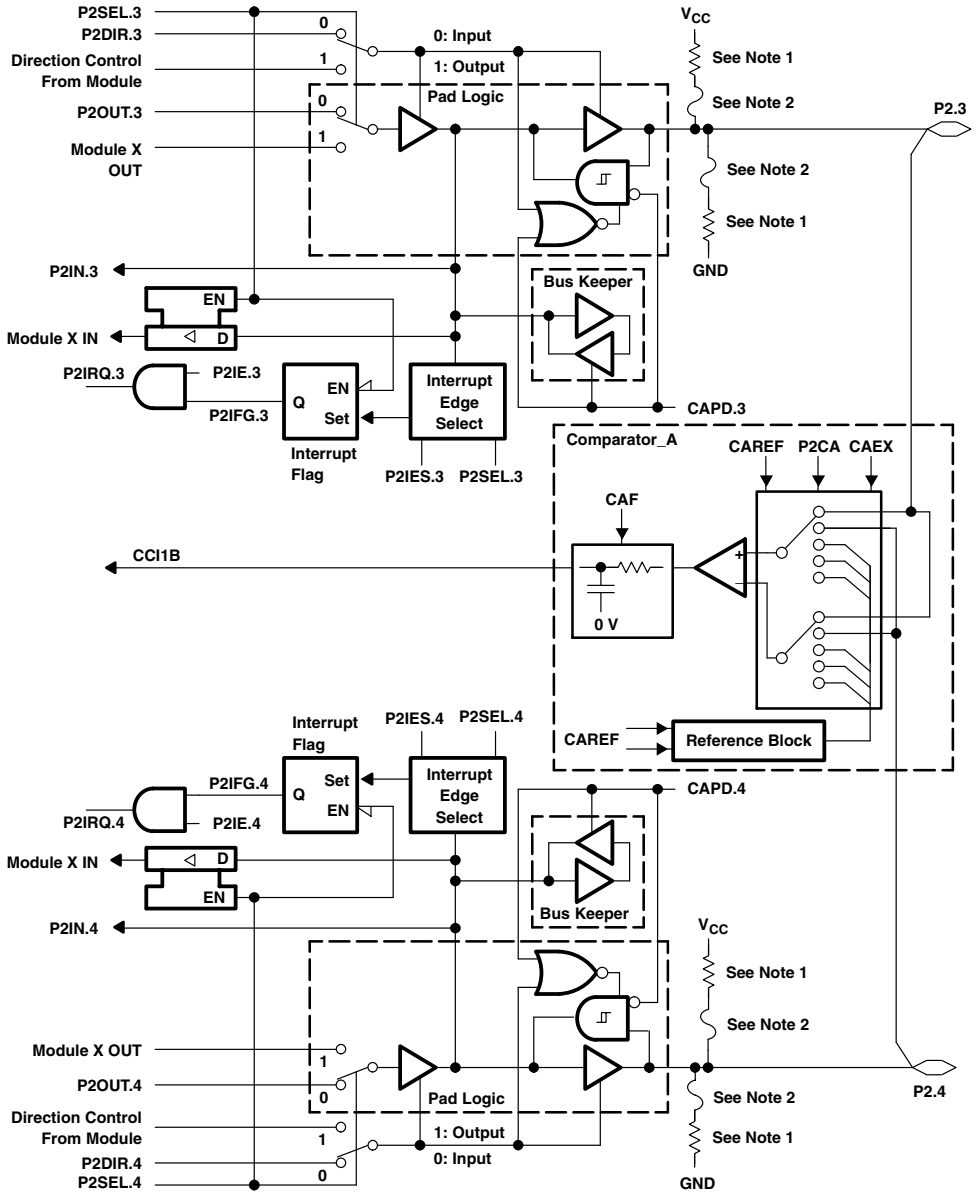
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P1IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	V_{SS}	P2IN.1	INCLK†	P2IE.1	P2IFG.1	P1IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT	P2IN.2	CCI0B†	P2IE.2	P2IFG.2	P1IES.2

† Signal from or to Timer_A

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P2, P2.3 to P2.4, input/output with Schmitt trigger



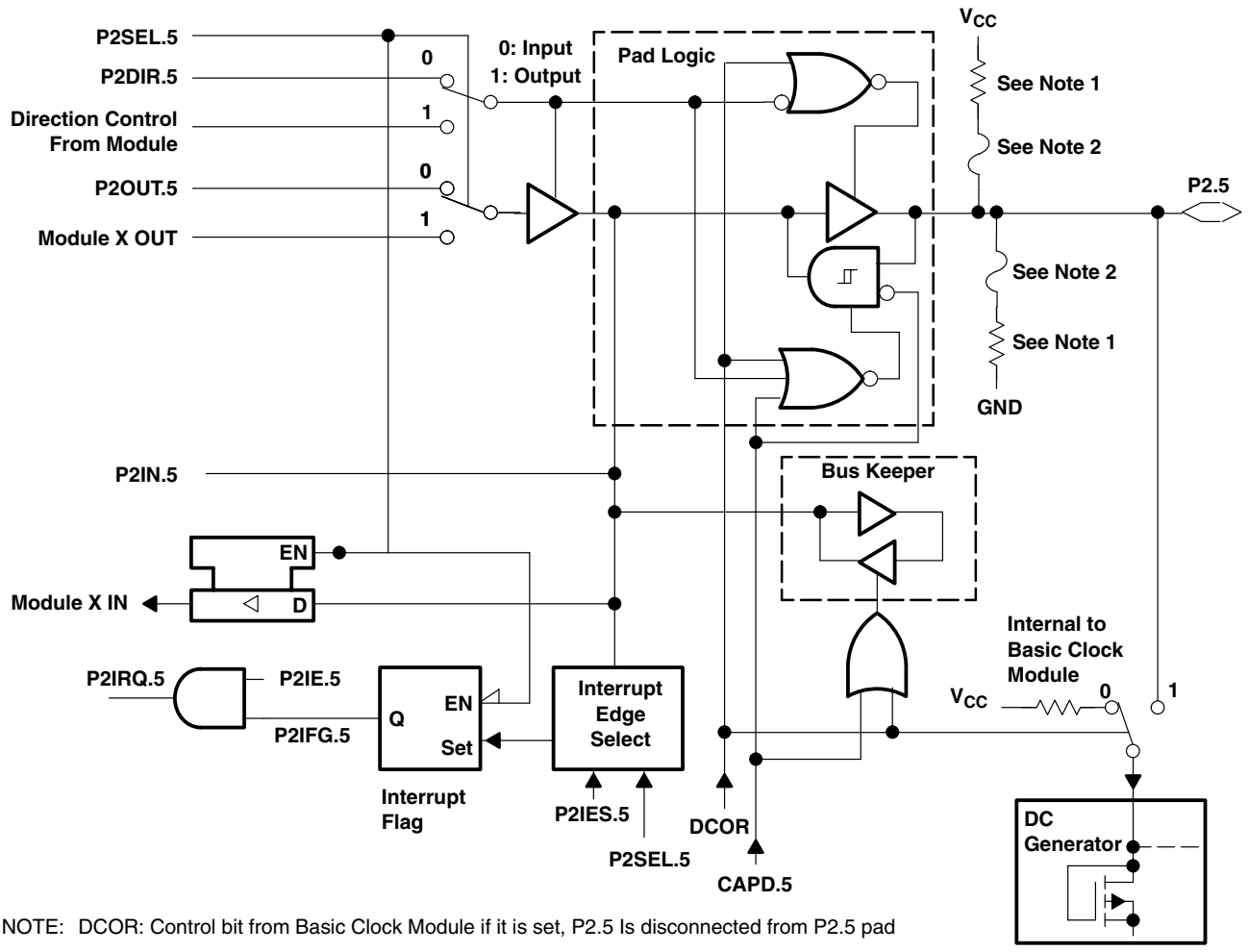
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P1IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P1IES.4

† Signal from Timer_A

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P2, P2.5, input/output with Schmitt trigger and R_{OSC} function for the Basic Clock module



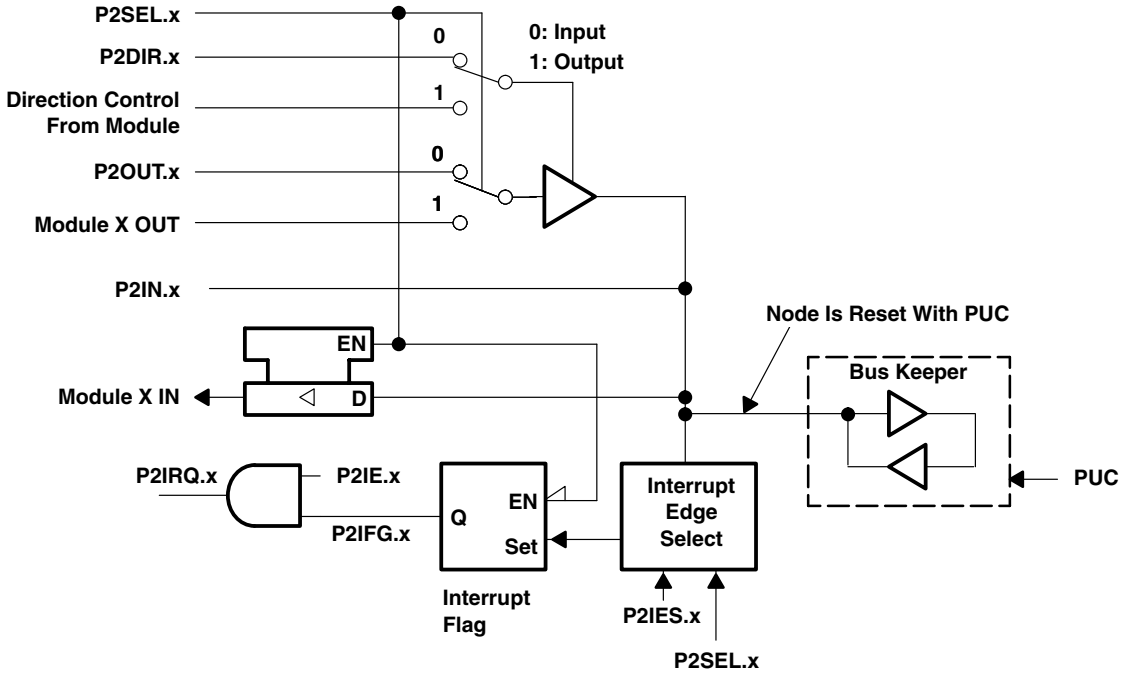
NOTE: DCOR: Control bit from Basic Clock Module if it is set, P2.5 Is disconnected from P2.5 pad

PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	V_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P2, unbonded bits P2.6 and P2.7



NOTE: x = Bit/identifier, 6 to 7 for port P2 without external pins

P2Sel.x	P2DIR.x	Direction control from module	P2OUT.x	Module X OUT	P2IN.x	Module X IN	P2IE.x	P2IFG.x	P2IES.x
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	V_{SS}	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	V_{SS}	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

NOTE 1: Unbonded bits 6 and 7 of port P2 can be used as software interrupt flags. The interrupt flags can only be influenced by software. They work then as a software interrupt.

JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is taken back low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 13). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

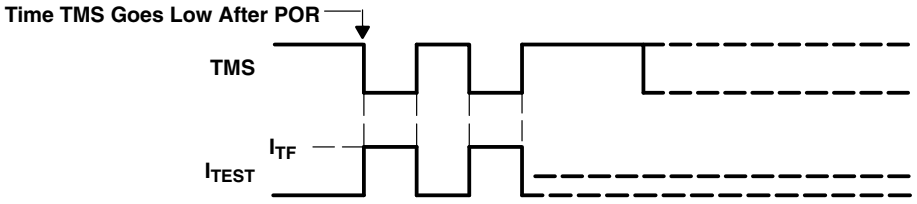


Figure 13. Fuse Check Mode Current, MSP430F11x1A and MSP430C11x1

NOTE:
The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the *bootstrap loader* section for more information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F1101AIDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F1101A	Samples
MSP430F1101AIDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F1101A	Samples
MSP430F1101AIDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1101A	Samples
MSP430F1101AIDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1101A	Samples
MSP430F1101AIPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1101A	Samples
MSP430F1101AIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1101A	Samples
MSP430F1101AIRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 1101A	Samples
MSP430F1101AIRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 1101A	Samples
MSP430F1101IDWR	NRND	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1101	
MSP430F1111AIDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F1111A	Samples
MSP430F1111AIDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1111A	Samples
MSP430F1111AIDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1111A	Samples
MSP430F1111AIPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1111A	Samples
MSP430F1111AIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1111A	Samples
MSP430F1111AIRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 1111A	Samples
MSP430F1111AIRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 1111A	Samples
MSP430F1121AIDGV	ACTIVE	TVSOP	DGV	20	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F1121A	Samples
MSP430F1121AIDGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4F1121A	Samples
MSP430F1121AIDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1121A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F1121AIDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1121A	Samples
MSP430F1121AIPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1121A	Samples
MSP430F1121AIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1121A	Samples
MSP430F1121AIRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 1121A	Samples
MSP430F1121AIRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F 1121A	Samples
MSP430F1121IDW	NRND	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1121	
MSP430F1121IDWR	NRND	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430F1121	
MSP430F1121IPW	NRND	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1121	
MSP430F1121IPWR	NRND	TSSOP	PW	20	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430F1121	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

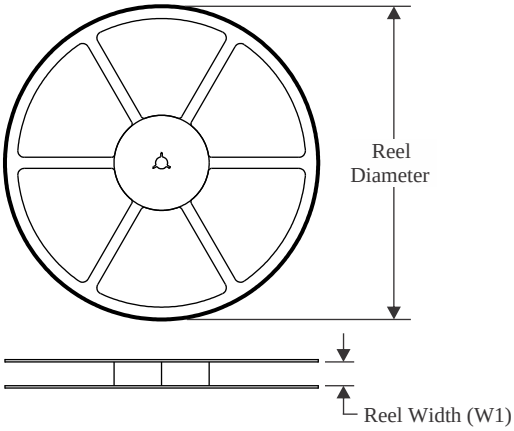
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

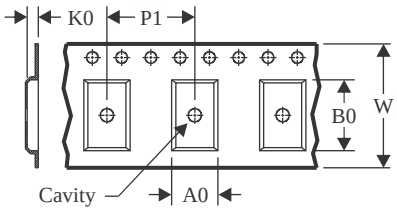
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

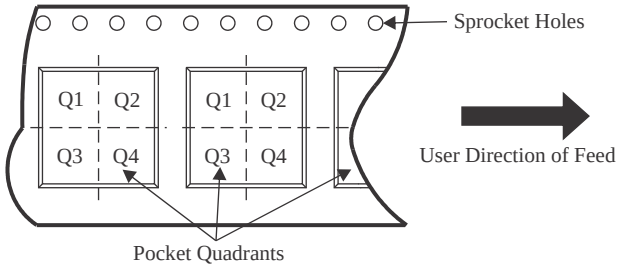


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

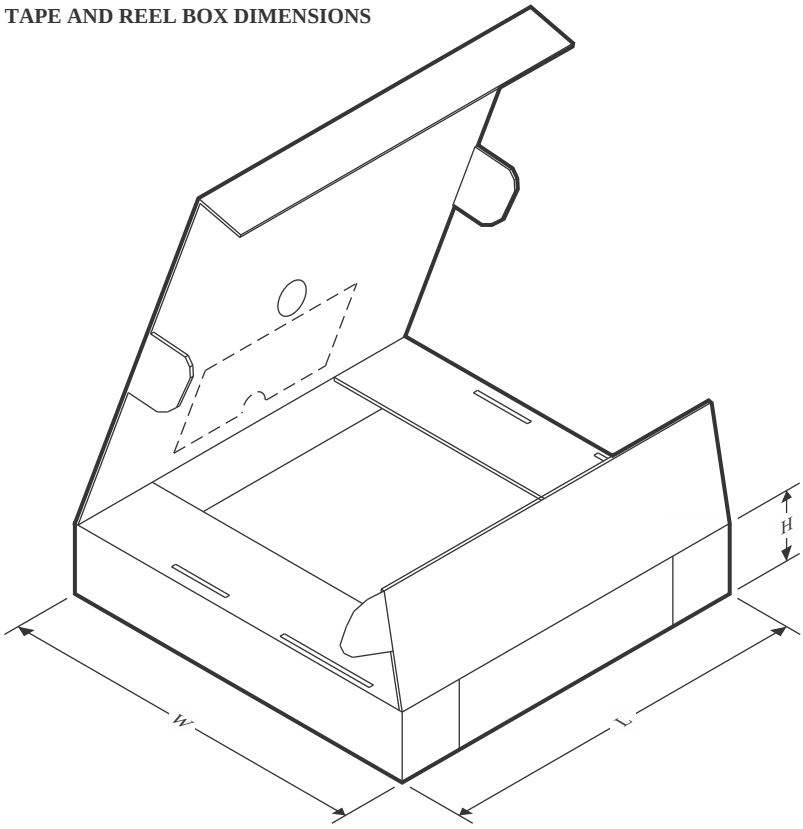


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F1101AIDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F1101AIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F1101AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F1101AIRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F1101AIRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F1101IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F1111AIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F1111AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F1111AIRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F1111AIRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F1121AIDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430F1121AIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MSP430F1121AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430F1121AIRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F1121AIRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430F1121IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F1121IPWR	TSSOP	PW	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

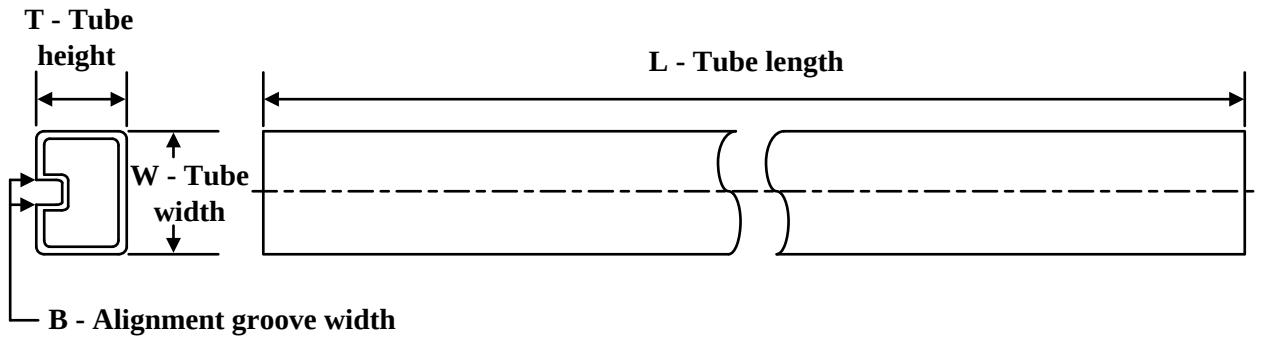
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F1101AIDGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
MSP430F1101AIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F1101AIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MSP430F1101AIRGER	VQFN	RGE	24	3000	356.0	356.0	35.0
MSP430F1101AIRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F1101IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F1111AIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F1111AIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MSP430F1111AIRGER	VQFN	RGE	24	3000	356.0	356.0	35.0
MSP430F1111AIRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F1121AIDGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
MSP430F1121AIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F1121AIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MSP430F1121AIRGER	VQFN	RGE	24	3000	356.0	356.0	35.0
MSP430F1121AIRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430F1121IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MSP430F1121IPWR	TSSOP	PW	20	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

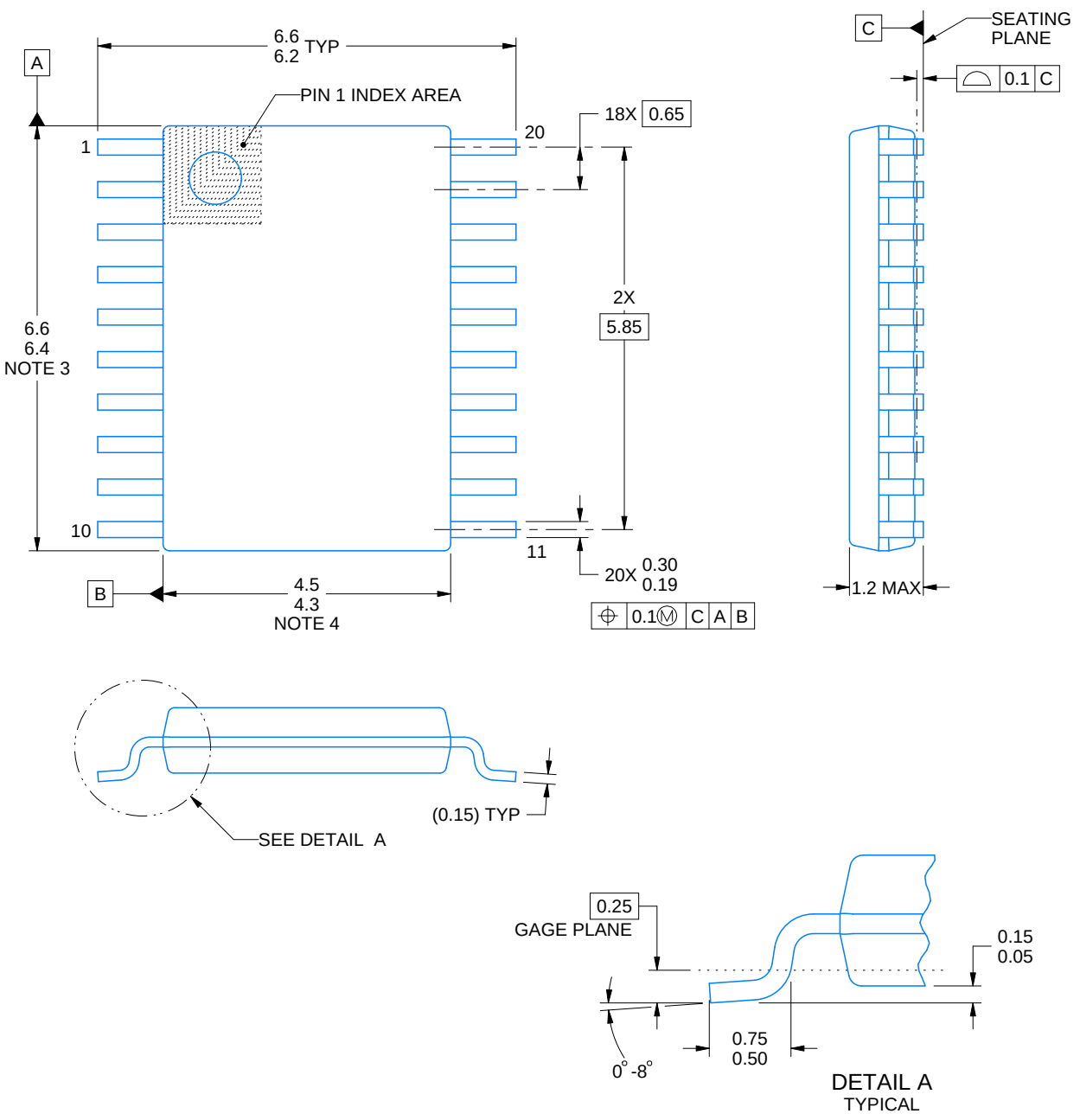
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430F1101AIDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F1101AIDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F1101AIPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F1111AIDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F1111AIDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F1111AIPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F1121AIDGV	DGV	TVSOP	20	90	530	10.2	3600	3.5
MSP430F1121AIDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F1121AIPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MSP430F1121IDW	DW	SOIC	20	25	507	12.83	5080	6.6
MSP430F1121IPW	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

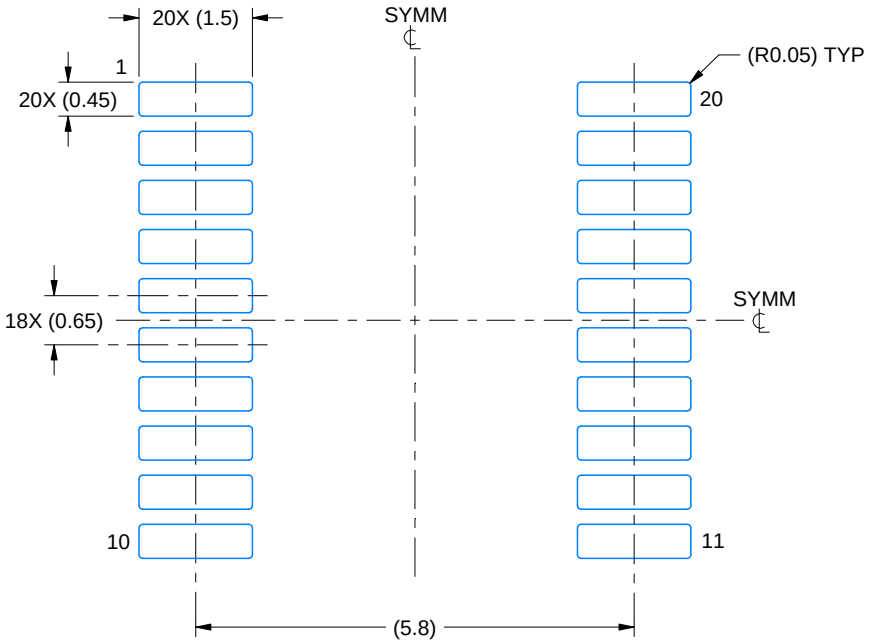
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



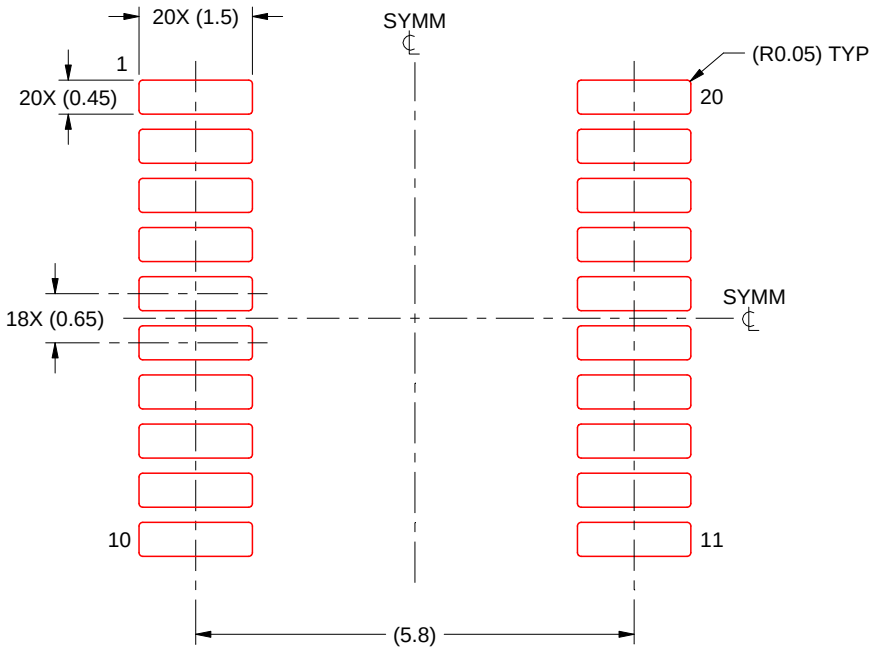
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



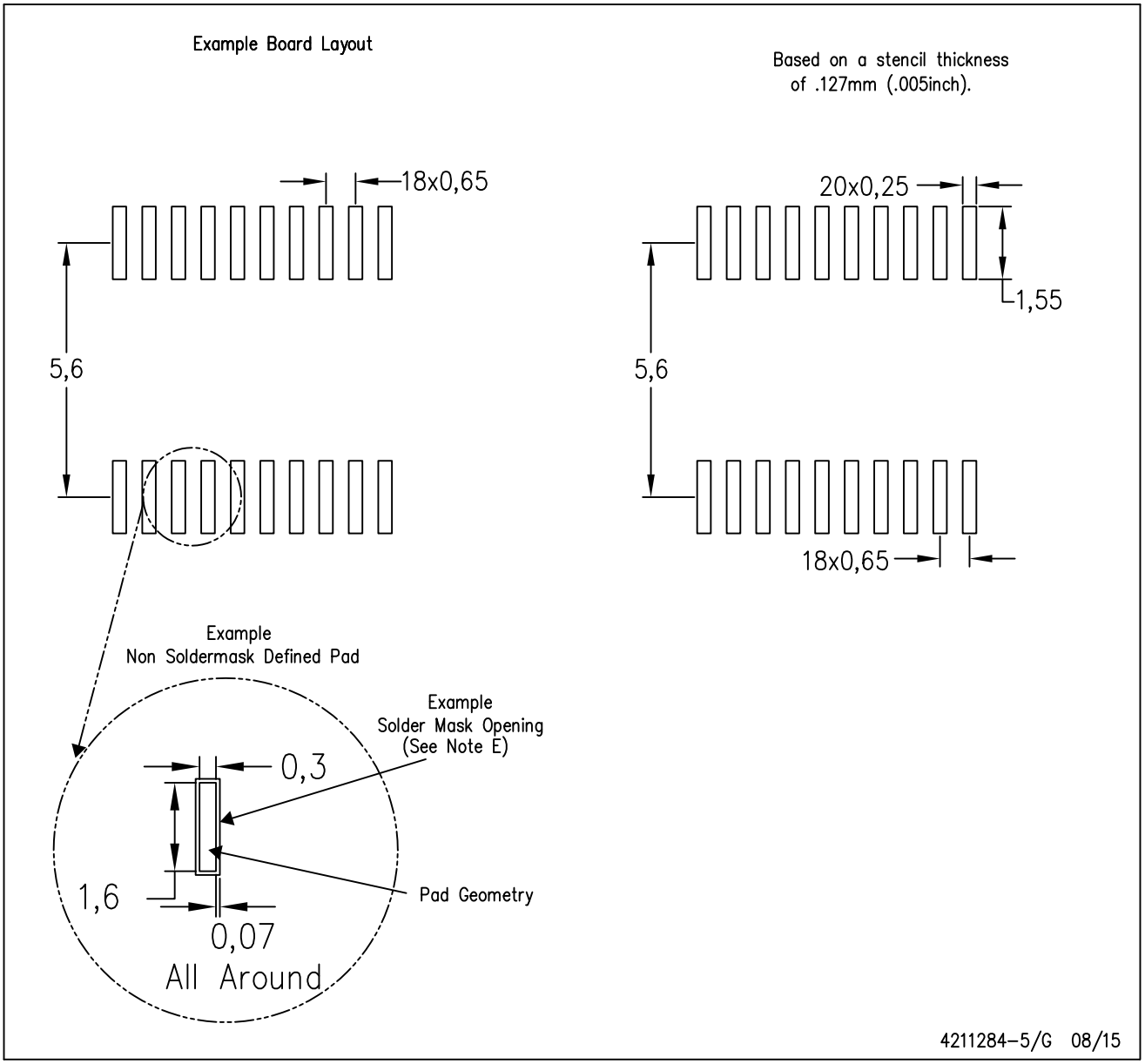
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE

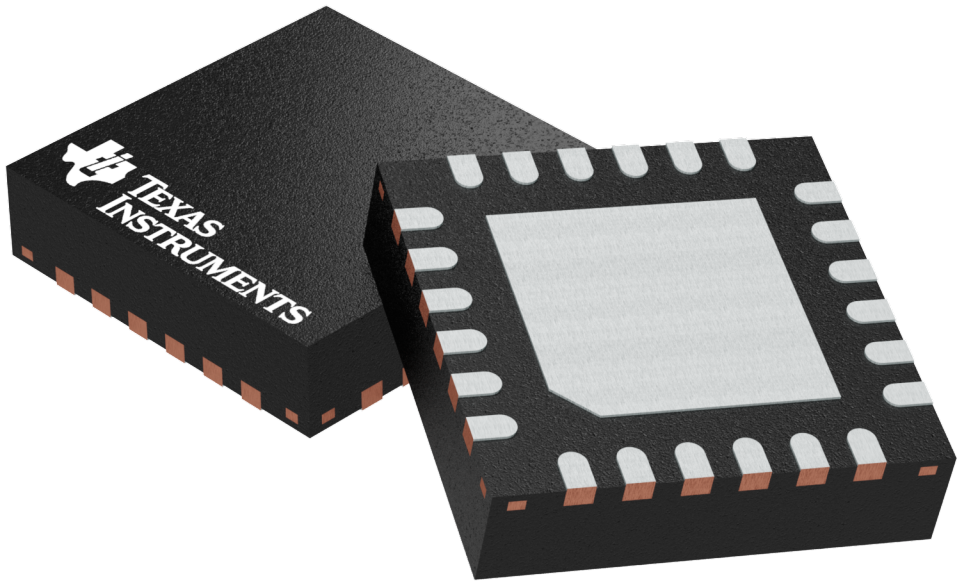


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

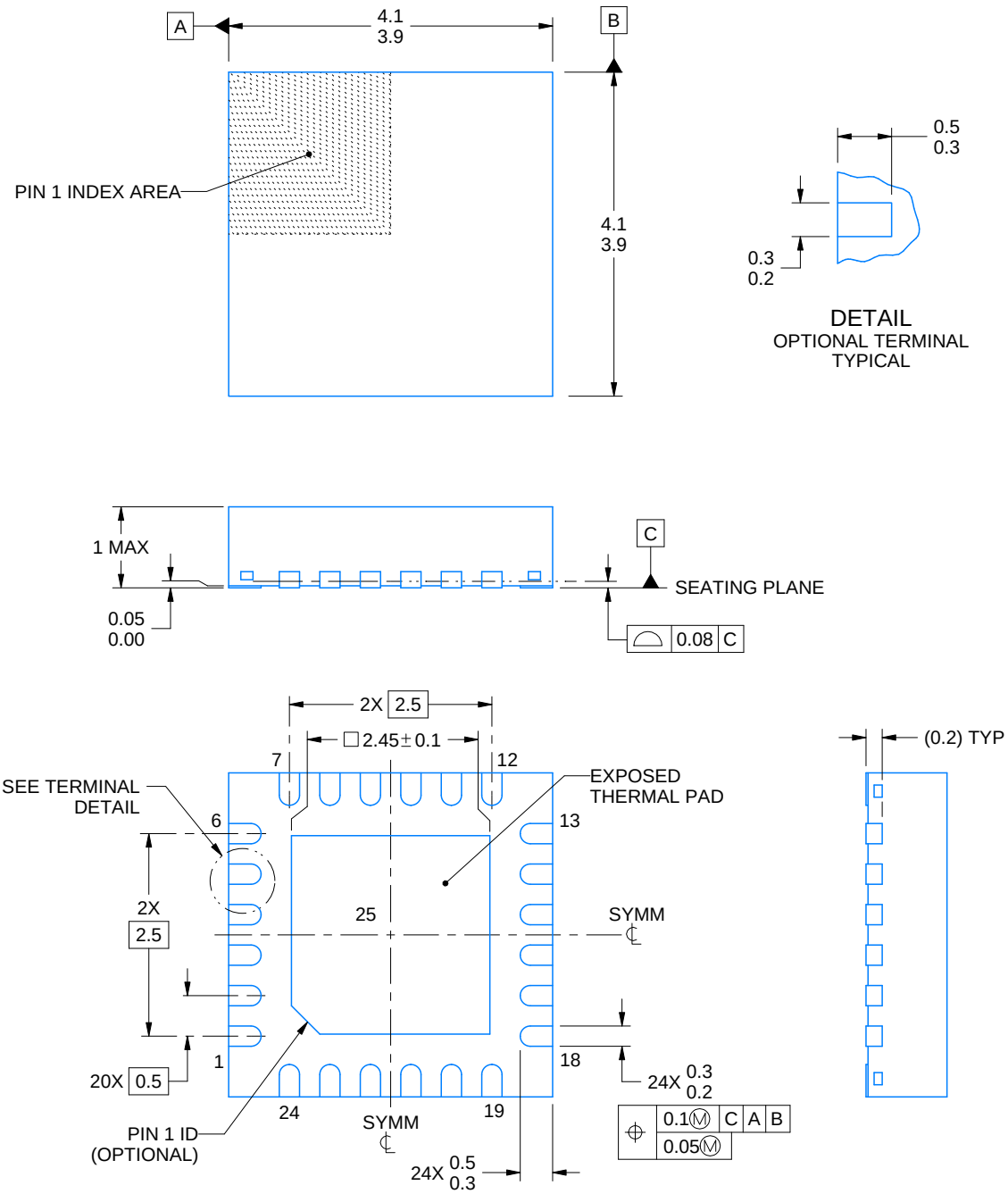
4204104/H

PACKAGE OUTLINE

RGE0024B

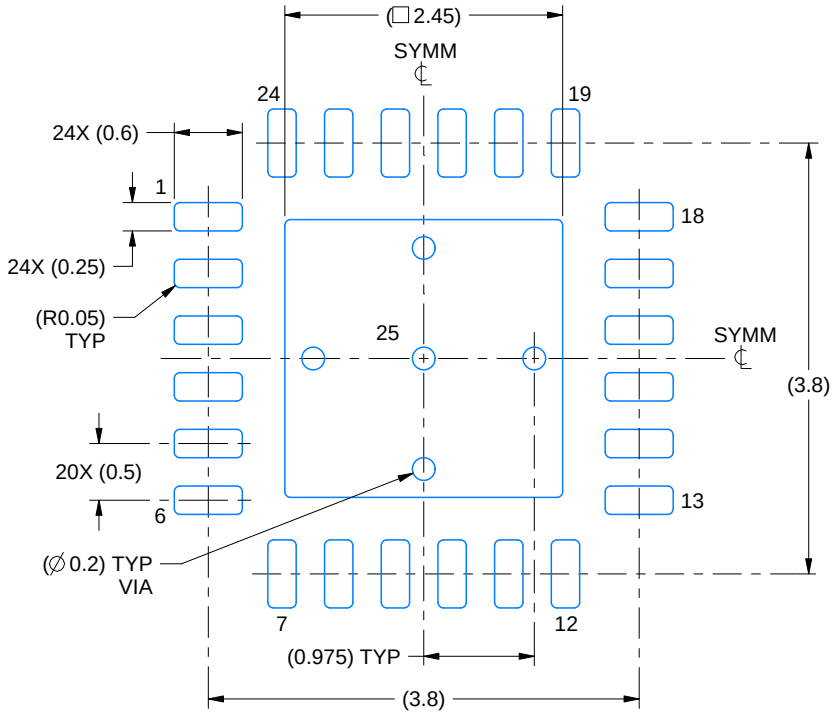
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

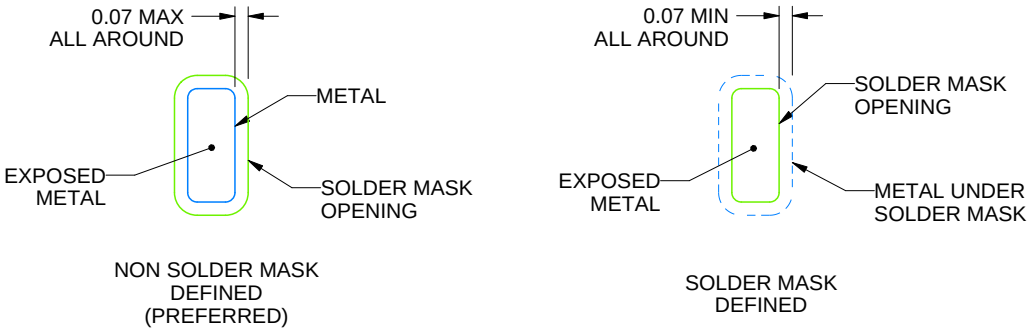


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

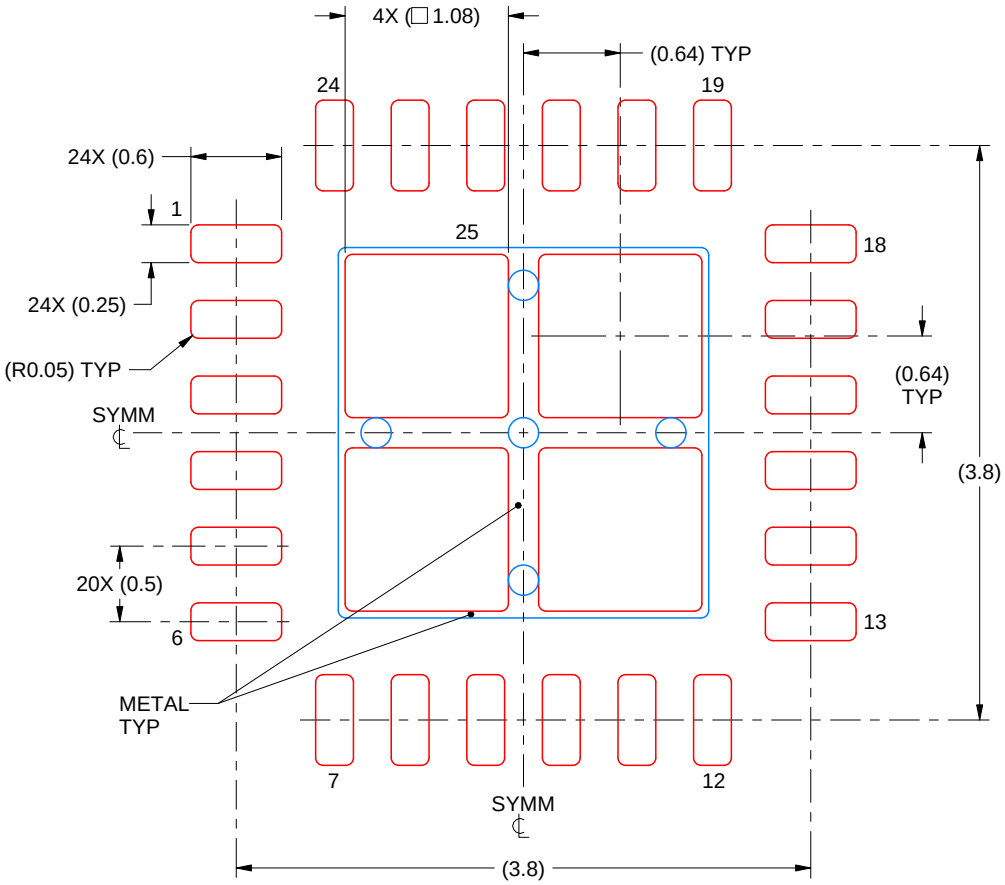


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



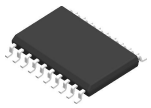
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

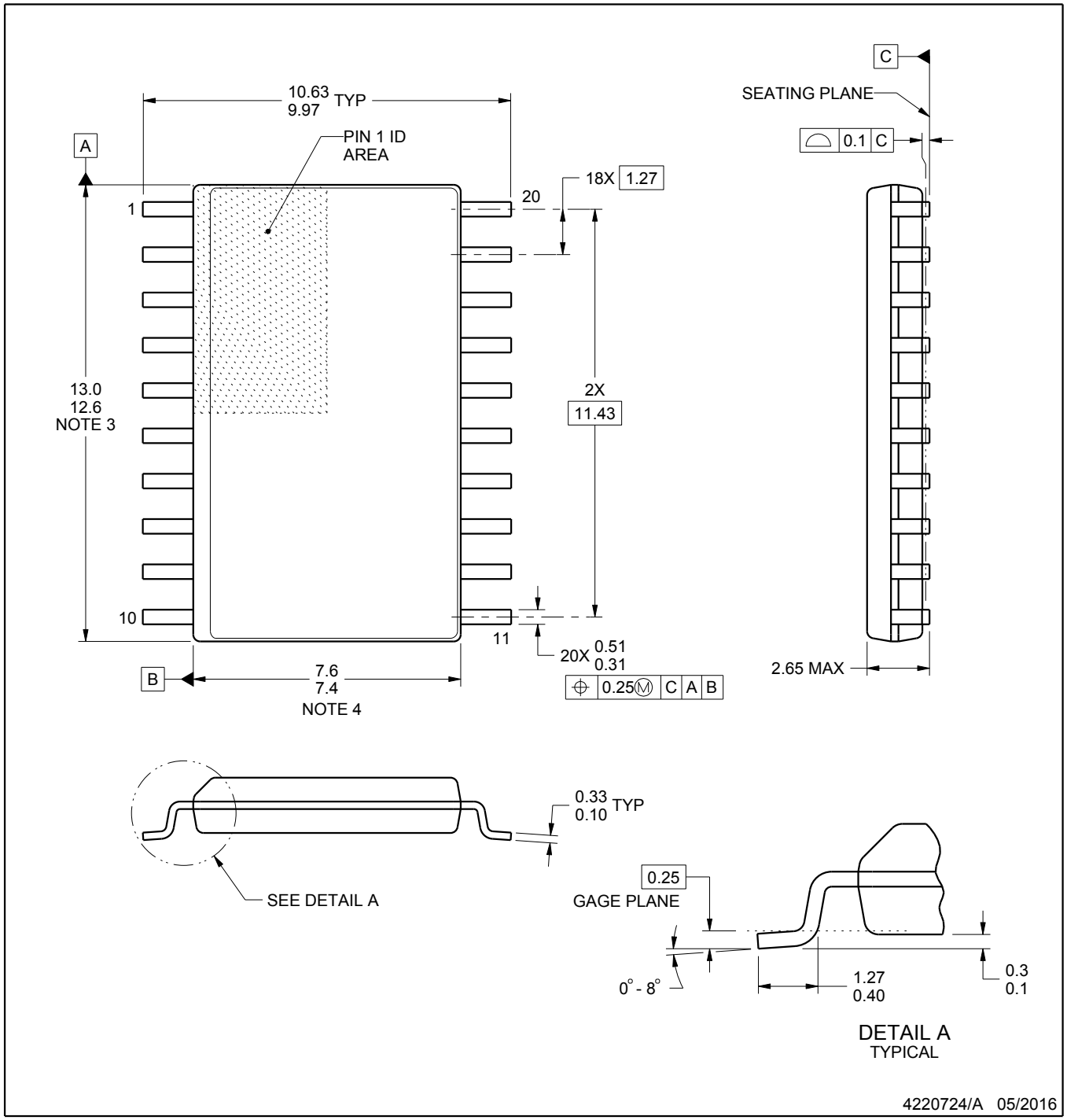


PACKAGE OUTLINE

DW0020A

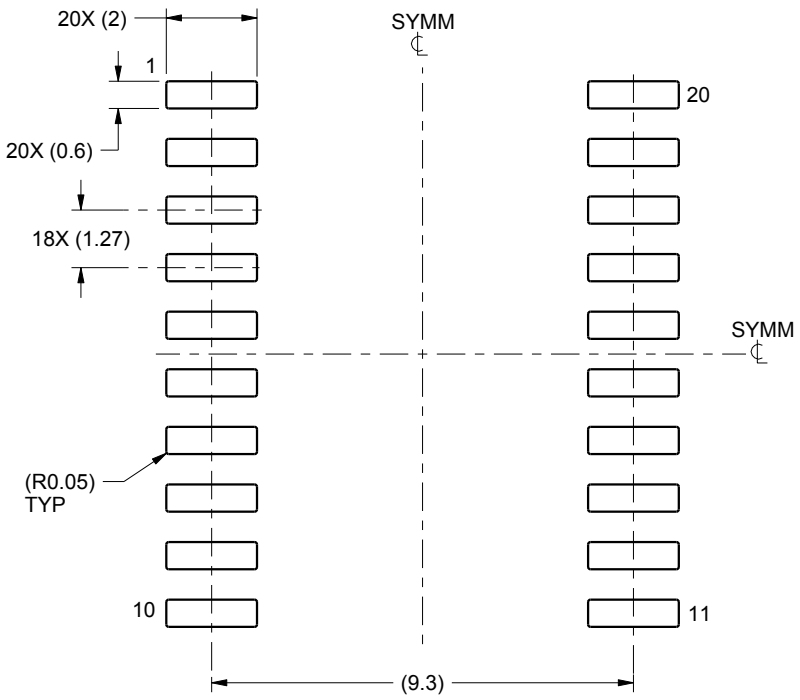
SOIC - 2.65 mm max height

SOIC

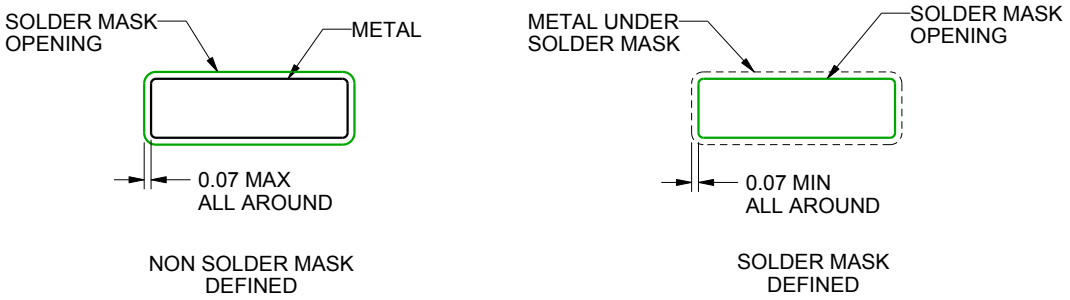


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

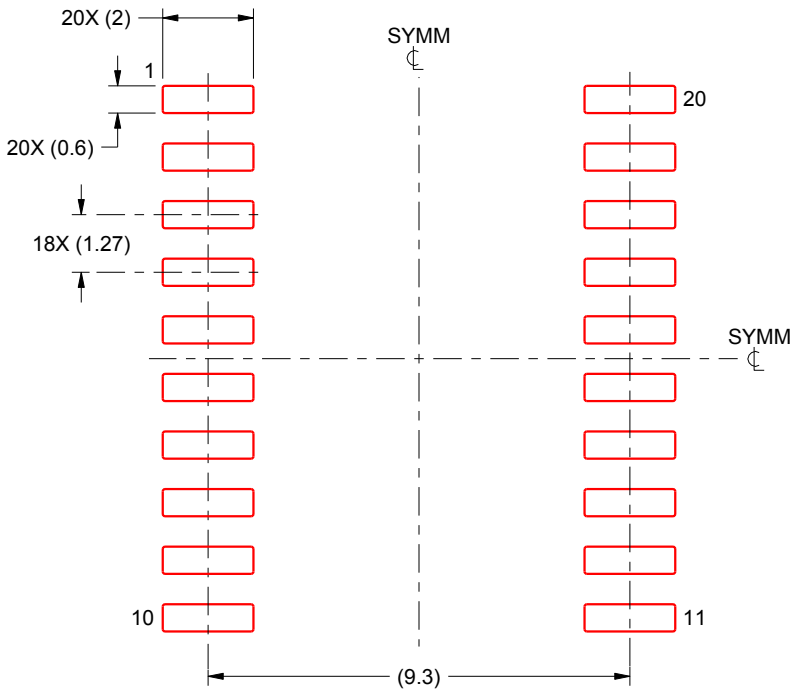


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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