



THE DATASHEET OF MSP430F413IPM



- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow Power Consumption
 - Active Mode: 200 μ A at 1 MHz, 2.2 V
 - Standby Mode: 0.7 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Five Power-Saving Modes
- Wake-Up From Standby Mode in Less Than 6 μ s
- Frequency-Locked Loop (FLL+)
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- 16-Bit Timer_A With Three or Five[†] Capture/Compare Registers
- Integrated LCD Driver for 96 Segments
- On-Chip Comparator
- Brownout Detector
- Supply Voltage Supervisor/Monitor – Programmable Level Detection on MSP430F415/417 Devices Only
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Bootstrap Loader in Flash Devices
- Family Members Include:
 - MSP430C412: 4KB ROM, 256B RAM
 - MSP430C413: 8KB ROM, 256B RAM
 - MSP430F412: 4KB + 256B Flash 256B RAM
 - MSP430F413: 8KB + 256B Flash 256B RAM
 - MSP430F415: 16KB + 256B Flash 512B RAM
 - MSP430F417: 32KB + 256B Flash 1KB RAM
- Available in 64-Pin QFP (PM) and 64-Pin QFN (RTD/RGC) Packages
- For Complete Module Descriptions, See the *MSP430x4xx Family User's Guide*, Literature Number SLAU056

[†] Timer_A5 in 'F415 and 'F417 devices only

description

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μ s.

The MSP430x41x series are microcontroller configurations with one or two built-in 16-bit timers, a comparator, 96 LCD segment drive capability, and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process the data and transmit them to a host system. The comparator and timer make the configurations ideal for industrial meters, counter applications, handheld meters, etc.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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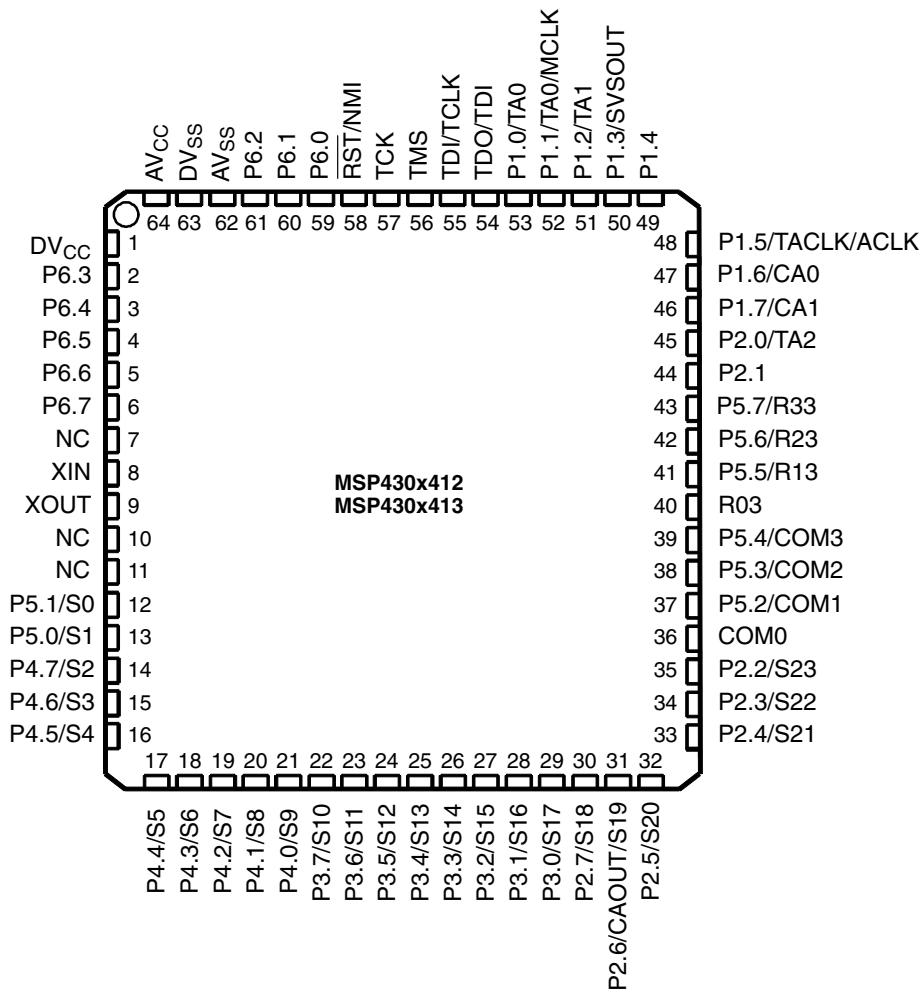
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AVAILABLE OPTIONS

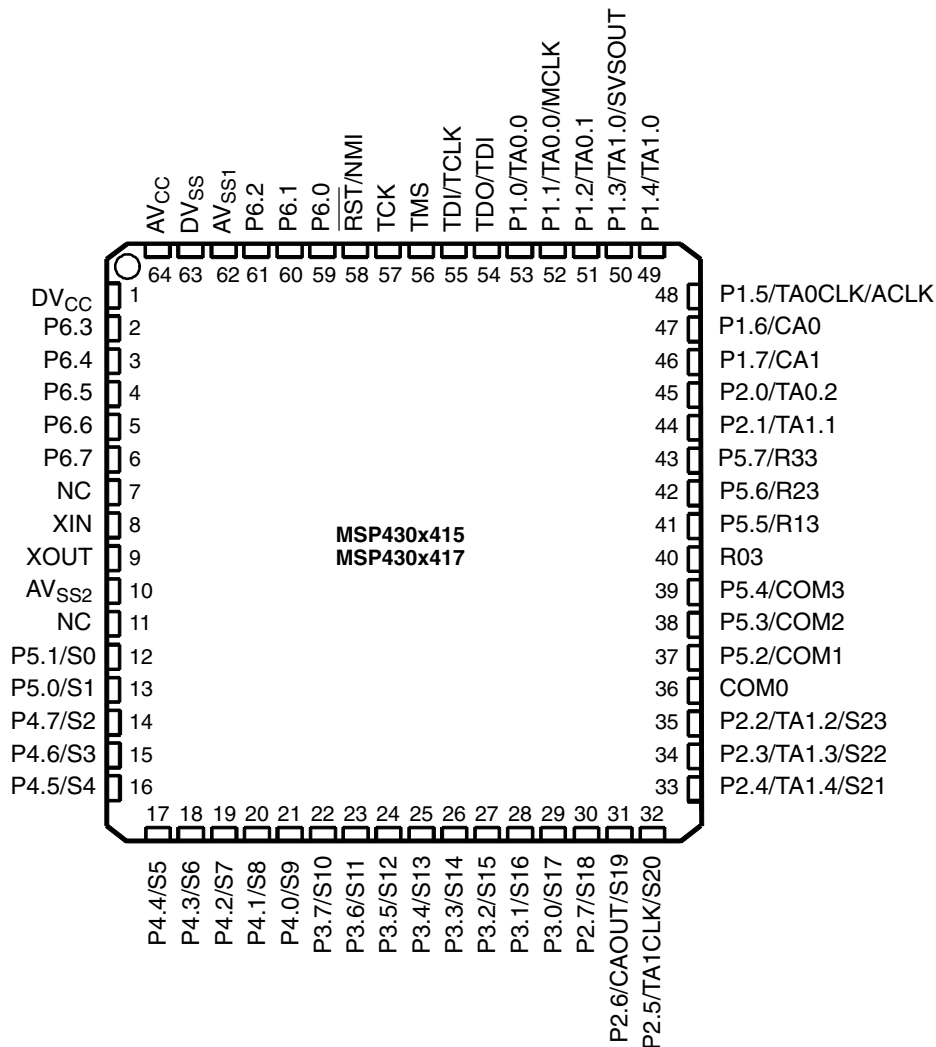
| T _A | PACKAGED DEVICES | |
|----------------|--|--|
| | PLASTIC 64-PIN QFP (PM) | PLASTIC 64-PIN QFN (RTD/RGC) |
| -40°C to 85°C | MSP430C412IPM MSP430C413IPM MSP430F412IPM MSP430F413IPM MSP430F415IPM MSP430F417IPM | MSP430C412IRGC MSP430C413IRGC MSP430F412IRTD MSP430F413IRTD MSP430F415IRTD MSP430F417IRTD |

pin designation – MSP430x412, MSP430x413



NC – No internal connection. External connection to V_{SS} recommended.

pin designation – MSP430x415, MSP430x417

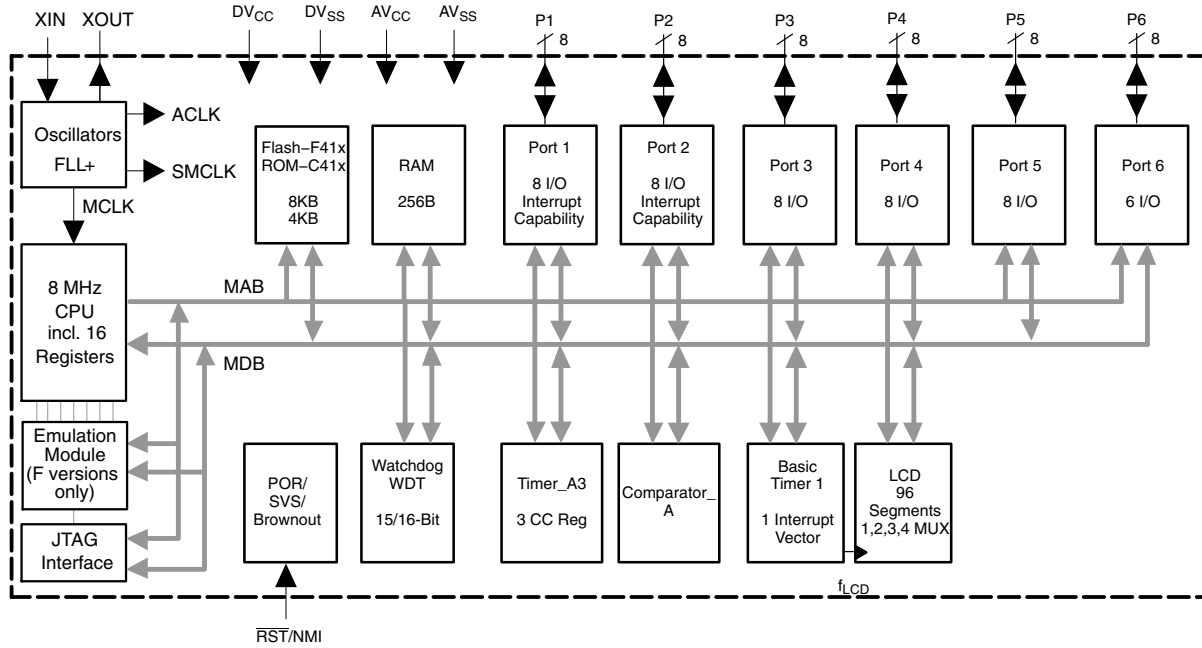


NC – No internal connection. External connection to V_{SS} recommended.

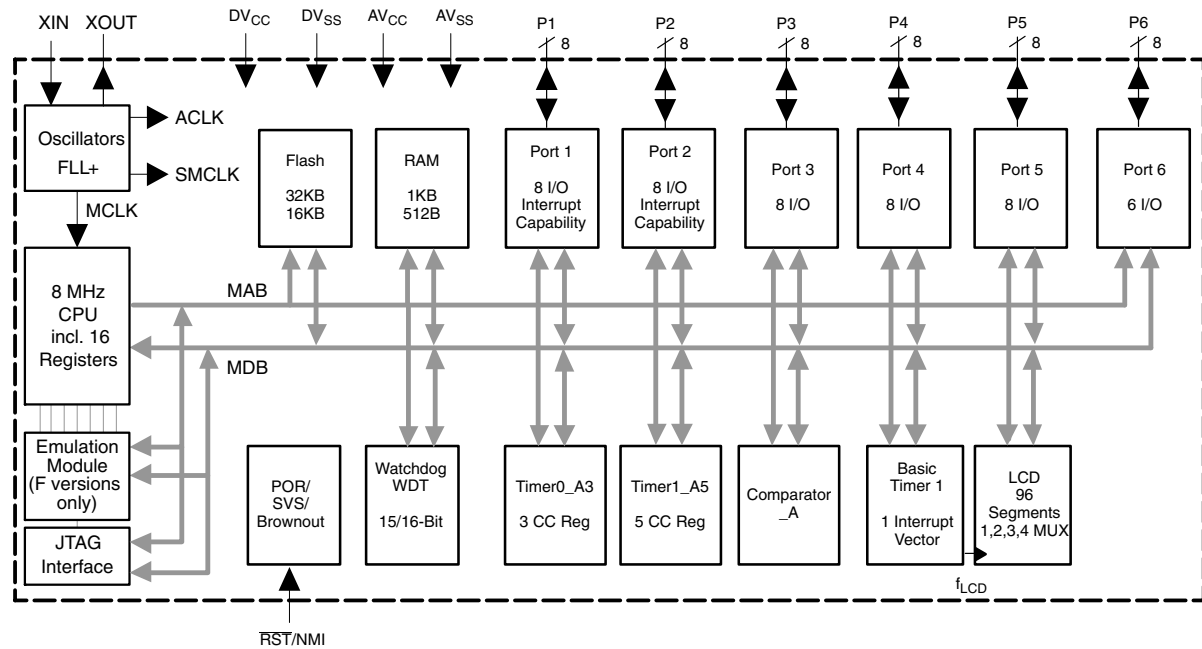
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functional block diagram – MSP430x412, MSP430x413



functional block diagram – MSP430x415, MSP430x417



Terminal Functions – MSP430x412, MSP430x413

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|------------------|-----------|-----|---|
| AV _{CC} | 64 | | Positive terminal that supplies SVS, brownout, oscillator, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV _{CC} . |
| AV _{SS} | 62 | | Negative terminal that supplies SVS, brownout, oscillator, comparator_A. Needs to be externally connected to DV _{SS} . |
| DV _{CC} | 1 | | Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AV _{CC} . |
| DV _{SS} | 63 | | Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV _{CC} /AV _{SS} . |
| NC | 7, 10, 11 | | Not internally connected. Connection to V _{SS} recommended. |
| P1.0/TA0 | 53 | I/O | General-purpose digital I/O / Timer_A, Capture: CCI0A input, compare: Out0 output/BSL transmit |
| P1.1/TA0/MCLK | 52 | I/O | General-purpose digital I/O / Timer_A, Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin/BSL receive. |
| P1.2/TA1 | 51 | I/O | General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output |
| P1.3/SVSOUT | 50 | I/O | General-purpose digital I/O / SVS: output of SVS comparator |
| P1.4 | 49 | I/O | General-purpose digital I/O |
| P1.5/TACLK/ ACLK | 48 | I/O | General-purpose digital I/O / Input of Timer_A clock/output of ACLK |
| P1.6/CA0 | 47 | I/O | General-purpose digital I/O / Comparator_A input |
| P1.7/CA1 | 46 | I/O | General-purpose digital I/O / Comparator_A input |
| P2.0/TA2 | 45 | I/O | General-purpose digital I/O / Timer_A capture: CCI2A input, compare: Out2 output |
| P2.1 | 44 | I/O | General-purpose digital I/O |
| P2.2/S23 | 35 | I/O | General-purpose digital I/O / LCD segment output 23 (see Note 1) |
| P2.3/S22 | 34 | I/O | General-purpose digital I/O / LCD segment output 22 (see Note 1) |
| P2.4/S21 | 33 | I/O | General-purpose digital I/O / LCD segment output 21 (see Note 1) |
| P2.5/S20 | 32 | I/O | General-purpose digital I/O / LCD segment output 20 (see Note 1) |
| P2.6/CAOUT/S19 | 31 | I/O | General-purpose digital I/O / Comparator_A output/LCD segment output 19 (see Note 1) |
| P2.7/S18 | 30 | I/O | General-purpose digital I/O / LCD segment output 18 (see Note 1) |
| P3.0/S17 | 29 | I/O | General-purpose digital I/O / LCD segment output 17 (see Note 1) |
| P3.1/S16 | 28 | I/O | General-purpose digital I/O / LCD segment output 16 (see Note 1) |
| P3.2/S15 | 27 | I/O | General-purpose digital I/O / LCD segment output 15 (see Note 1) |
| P3.3/S14 | 26 | I/O | General-purpose digital I/O / LCD segment output 14 (see Note 1) |
| P3.4/S13 | 25 | I/O | General-purpose digital I/O / LCD segment output 13 (see Note 1) |
| P3.5/S12 | 24 | I/O | General-purpose digital I/O / LCD segment output 12 (see Note 1) |
| P3.6/S11 | 23 | I/O | General-purpose digital I/O / LCD segment output 11 (see Note 1) |
| P3.7/S10 | 22 | I/O | General-purpose digital I/O / LCD segment output 10 (see Note 1) |

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

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Terminal Functions – MSP430x412, MSP430x413 (Continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-----|-----|---|
| P4.0/S9 | 21 | I/O | General-purpose digital I/O / LCD segment output 9 (see Note 1) |
| P4.1/S8 | 20 | I/O | General-purpose digital I/O / LCD segment output 8 (see Note 1) |
| P4.2/S7 | 19 | I/O | General-purpose digital I/O / LCD segment output 7 (see Note 1) |
| P4.3/S6 | 18 | I/O | General-purpose digital I/O / LCD segment output 6 (see Note 1) |
| P4.4/S5 | 17 | I/O | General-purpose digital I/O / LCD segment output 5 (see Note 1) |
| P4.5/S4 | 16 | I/O | General-purpose digital I/O / LCD segment output 4 (see Note 1) |
| P4.6/S3 | 15 | I/O | General-purpose digital I/O / LCD segment output 3 (see Note 1) |
| P4.7/S2 | 14 | I/O | General-purpose digital I/O / LCD segment output 2 (see Note 1) |
| P5.0/S1 | 13 | I/O | General-purpose digital I/O / LCD segment output 1 (see Note 1) |
| P5.1/S0 | 12 | I/O | General-purpose digital I/O / LCD segment output 0 (see Note 1) |
| COM0 | 36 | O | Common output. COM0–3 are used for LCD backplanes |
| P5.2/COM1 | 37 | I/O | General-purpose digital I/O / Common output. COM0–3 are used for LCD backplanes. |
| P5.3/COM2 | 38 | I/O | General-purpose digital I/O / Common output. COM0–3 are used for LCD backplanes. |
| P5.4/COM3 | 39 | I/O | General-purpose digital I/O / Common output. COM0–3 are used for LCD backplanes. |
| R03 | 40 | I | Input port of fourth positive (lowest) analog LCD level (V5) |
| P5.5/R13 | 41 | I/O | General-purpose digital I/O / Input port of third most positive analog LCD level (V4 or V3) |
| P5.6/R23 | 42 | I/O | General-purpose digital I/O / Input port of second most positive analog LCD level (V2) |
| P5.7/R33 | 43 | I/O | General-purpose digital I/O / Output port of most positive analog LCD level (V1) |
| P6.0 | 59 | I/O | General-purpose digital I/O |
| P6.1 | 60 | I/O | General-purpose digital I/O |
| P6.2 | 61 | I/O | General-purpose digital I/O |
| P6.3 | 2 | I/O | General-purpose digital I/O |
| P6.4 | 3 | I/O | General-purpose digital I/O |
| P6.5 | 4 | I/O | General-purpose digital I/O |
| P6.6 | 5 | I/O | General-purpose digital I/O |
| P6.7 | 6 | I/O | General-purpose digital I/O |
| RST/NMI | 58 | I | Reset input / Nonmaskable interrupt input |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming and test. |
| TDI/TCLK | 55 | I | Test data input / Test clock input. The device protection fuse is connected to TDI. |
| TDO/TDI | 54 | I/O | Test data output port. TDO/TDI data output or programming data input terminal. |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device programming and test. |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1. |
| QFN Pad | NA | NA | QFN package pad connection to V _{SS} recommended. |

NOTE 2: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.



Terminal Functions – MSP430x415, MSP430x417

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-----------------------|-------|-----|---|
| AV _{CC} | 64 | | Positive terminal that supplies SVS, brownout, oscillator, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV _{CC} . |
| AV _{SS1} | 62 | | Negative terminal that supplies SVS, brownout, oscillator, comparator_A. Needs to be externally connected to DV _{SS} . |
| DV _{CC} | 1 | | Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AV _{CC} . |
| DV _{SS} | 63 | | Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV _{CC} /AV _{SS} . |
| AV _{SS2} | 10 | | Negative terminal that supplies SVS, brownout, oscillator, comparator_A. Needs to be externally connected to DV _{SS} . |
| NC | 7, 11 | | Not internally connected. Connection to V _{SS} recommended. |
| P1.0/TA0.0 | 53 | I/O | General-purpose digital I/O / Timer0_A. Capture: CCI0A input, compare: Out0 output/BSL transmit |
| P1.1/TA0.0/MCLK | 52 | I/O | General-purpose digital I/O / Timer0_A. Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin/BSL receive |
| P1.2/TA0.1 | 51 | I/O | General-purpose digital I/O / Timer0_A, capture: CCI1A input, compare: Out1 output |
| P1.3/TA1.0/ SVSOUT | 50 | I/O | General-purpose digital I/O / Timer1_A, capture: CCI0B input/SVS: output of SVS comparator |
| P1.4/TA1.0 | 49 | I/O | General-purpose digital I/O / Timer1_A, capture: CCI0A input, compare: Out0 output |
| P1.5/TA0CLK/ ACLK | 48 | I/O | General-purpose digital I/O / input of Timer0_A clock/output of ACLK |
| P1.6/CA0 | 47 | I/O | General-purpose digital I/O / Comparator_A input |
| P1.7/CA1 | 46 | I/O | General-purpose digital I/O / Comparator_A input |
| P2.0/TA0.2 | 45 | I/O | General-purpose digital I/O / Timer0_A capture: CCI2A input, compare: Out2 output |
| P2.1/TA1.1 | 44 | I/O | General-purpose digital I/O / Timer1_A, capture: CCI1A input, compare: Out1 output |
| P2.2/TA1.2/S23 | 35 | I/O | General-purpose digital I/O / Timer1_A, capture: CCI2A input, compare: Out2 output/LCD segment output 23 (see Note 1) |
| P2.3/TA1.3/S22 | 34 | I/O | General-purpose digital I/O / Timer1_A, capture: CCI3A input, compare: Out3 output/LCD segment output 22 (see Note 1) |
| P2.4/TA1.4/S21 | 33 | I/O | General-purpose digital I/O / Timer1_A, capture: CCI4A input, compare: Out4 output/LCD segment output 21 (see Note 1) |
| P2.5/TA1CLK/S20 | 32 | I/O | General-purpose digital I/O / input of Timer1_A clock/LCD segment output 20 (see Note 1) |
| P2.6/CAOUT/S19 | 31 | I/O | General-purpose digital I/O / Comparator_A output/LCD segment output 19 (see Note 1) |
| P2.7/S18 | 30 | I/O | General-purpose digital I/O / LCD segment output 18 (see Note 1) |
| P3.0/S17 | 29 | I/O | General-purpose digital I/O / LCD segment output 17 (see Note 1) |
| P3.1/S16 | 28 | I/O | General-purpose digital I/O / LCD segment output 16 (see Note 1) |
| P3.2/S15 | 27 | I/O | General-purpose digital I/O / LCD segment output 15 (see Note 1) |
| P3.3/S14 | 26 | I/O | General-purpose digital I/O / LCD segment output 14 (see Note 1) |
| P3.4/S13 | 25 | I/O | General-purpose digital I/O / LCD segment output 13 (see Note 1) |
| P3.5/S12 | 24 | I/O | General-purpose digital I/O / LCD segment output 12 (see Note 1) |
| P3.6/S11 | 23 | I/O | General-purpose digital I/O / LCD segment output 11 (see Note 1) |
| P3.7/S10 | 22 | I/O | General-purpose digital I/O / LCD segment output 10 (see Note 1) |

NOTE 3: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

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Terminal Functions – MSP430x415, MSP430x417 (Continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-----|-----|---|
| P4.0/S9 | 21 | I/O | General-purpose digital I/O / LCD segment output 9 (see Note 1) |
| P4.1/S8 | 20 | I/O | General-purpose digital I/O / LCD segment output 8 (see Note 1) |
| P4.2/S7 | 19 | I/O | General-purpose digital I/O / LCD segment output 7 (see Note 1) |
| P4.3/S6 | 18 | I/O | General-purpose digital I/O / LCD segment output 6 (see Note 1) |
| P4.4/S5 | 17 | I/O | General-purpose digital I/O / LCD segment output 5 (see Note 1) |
| P4.5/S4 | 16 | I/O | General-purpose digital I/O / LCD segment output 4 (see Note 1) |
| P4.6/S3 | 15 | I/O | General-purpose digital I/O / LCD segment output 3 (see Note 1) |
| P4.7/S2 | 14 | I/O | General-purpose digital I/O / LCD segment output 2 (see Note 1) |
| P5.0/S1 | 13 | I/O | General-purpose digital I/O / LCD segment output 1 (see Note 1) |
| P5.1/S0 | 12 | I/O | General-purpose digital I/O / LCD segment output 0 (see Note 1) |
| COM0 | 36 | O | Common output. COM0–3 are used for LCD backplanes. |
| P5.2/COM1 | 37 | I/O | General-purpose digital I/O / common output. COM0–3 are used for LCD backplanes. |
| P5.3/COM2 | 38 | I/O | General-purpose digital I/O / common output. COM0–3 are used for LCD backplanes. |
| P5.4/COM3 | 39 | I/O | General-purpose digital I/O / common output. COM0–3 are used for LCD backplanes. |
| R03 | 40 | I | Input port of fourth positive (lowest) analog LCD level (V5) |
| P5.5/R13 | 41 | I/O | General-purpose digital I/O / input port of third most positive analog LCD level (V4 or V3) |
| P5.6/R23 | 42 | I/O | General-purpose digital I/O / input port of second most positive analog LCD level (V2) |
| P5.7/R33 | 43 | I/O | General-purpose digital I/O / output port of most positive analog LCD level (V1) |
| P6.0 | 59 | I/O | General-purpose digital I/O |
| P6.1 | 60 | I/O | General-purpose digital I/O |
| P6.2 | 61 | I/O | General-purpose digital I/O |
| P6.3 | 2 | I/O | General-purpose digital I/O |
| P6.4 | 3 | I/O | General-purpose digital I/O |
| P6.5 | 4 | I/O | General-purpose digital I/O |
| P6.6 | 5 | I/O | General-purpose digital I/O |
| P6.7/SVSIN | 6 | I/O | General-purpose digital I/O / SVS, analog input |
| RST/NMI | 58 | I | Reset input / Nonmaskable interrupt input port |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming and test. |
| TDI/TCLK | 55 | I | Test data input / Test clock input. The device protection fuse is connected to TDI. |
| TDO/TDI | 54 | I/O | Test data output port. TDO/TDI data output or programming data input terminal. |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device programming and test. |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1. |
| QFN Pad | NA | NA | QFN package pad connection to V _{SS} recommended |

NOTE 4: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.



short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

| | | |
|-----------------------------------|----------------|-------------------------|
| Dual operands, source-destination | e.g. ADD R4,R5 | R4 + R5 ----> R5 |
| Single operands, destination only | e.g. CALL R8 | PC --->(TOS), R8---> PC |
| Relative jump, un/conditional | e.g. JNE | Jump-on-equal bit = 0 |

Table 2. Address Mode Descriptions

| ADDRESS MODE | S | D | SYNTAX | EXAMPLE | OPERATION |
|------------------------|---|---|-----------------|------------------|------------------------------------|
| Register | ● | ● | MOV Rs,Rd | MOV R10,R11 | R10 ---> R11 |
| Indexed | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5)---> M(6+R6) |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI | | M(EDE) ---> M(TONI) |
| Absolute | ● | ● | MOV &MEM,&TCDAT | | M(MEM) ---> M(TCDAT) |
| Indirect | ● | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) ---> M(Tab+R6) |
| Indirect autoincrement | ● | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) ---> R11 R10 + 2---> R10 |
| Immediate | ● | | MOV #X,TONI | MOV #45,TONI | #45 ---> M(TONI) |

NOTE: S = source D = destination

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operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active.
- Low-power mode 0 (LPM0)
 - CPU is disabled.
 - ACLK and SMCLK remain active, MCLK is available to modules.
 - FLL+ loop control remains active.
- Low-power mode 1 (LPM1)
 - CPU is disabled.
 - ACLK and SMCLK remain active. MCLK is available to modules.
 - FLL+ loop control is disabled.
- Low-power mode 2 (LPM2)
 - CPU is disabled.
 - MCLK, FLL+ loop control, and DCOCLK are disabled.
 - DCO's dc generator remains enabled.
 - ACLK remains active.
- Low-power mode 3 (LPM3)
 - CPU is disabled.
 - MCLK, FLL+ loop control, and DCOCLK are disabled.
 - DCO's dc generator is disabled.
 - ACLK remains active.
- Low-power mode 4 (LPM4)
 - CPU is disabled.
 - ACLK is disabled.
 - MCLK, FLL+ loop control, and DCOCLK are disabled.
 - DCO's dc generator is disabled.
 - Crystal oscillator is stopped.



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interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|---|--------------|-------------|
| Power-up External reset Watchdog Flash memory | WDTIFG KEYV (see Note 1) | Reset | 0FFFEh | 15, highest |
| NMI Oscillator fault Flash memory access violation | NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3) | (Non)maskable (Non)maskable (Non)maskable | 0FFFCh | 14 |
| Timer1_A5 (see Note 4) | TA1CCR0 CCIFG (see Note 2) | Maskable | 0FFFAh | 13 |
| Timer1_A5 (see Note 4) | TA1CCR1 to TA1CCR4 CCIFGs and TA1CTL TAIFG (see Notes 1 and 2) | Maskable | 0FFF8h | 12 |
| Comparator_A | CMPAIFG | Maskable | 0FFF6h | 11 |
| Watchdog timer | WDTIFG | Maskable | 0FFF4h | 10 |
| | | | 0FFF2h | 9 |
| | | | 0FFF0h | 8 |
| | | | 0FFEEh | 7 |
| Timer_A3/Timer0_A3 | TACCR0/TA0CCR0 CCIFG (see Note 2) | Maskable | 0FFEEh | 6 |
| Timer_A3/Timer0_A3 | TACCR1/TA0CCR1, TACCR2/TA0CCR2 CCIFGs and TACL1/TA0CTL TAIFG (see Notes 1 and 2) | Maskable | 0FFEAh | 5 |
| I/O port P1 (eight flags) | P1IFG.0 to P1IFG.7 (see Notes 1 and 2) | Maskable | 0FFE8h | 4 |
| | | | 0FFE6h | 3 |
| | | | 0FFE4h | 2 |
| I/O port P2 (eight flags) | P2IFG.0 to P2IFG.7 (see Notes 1 and 2) | Maskable | 0FFE2h | 1 |
| Basic Timer1 | BTIFG | Maskable | 0FFE0h | 0, lowest |

- NOTES: 1. Multiple source flags
 2. Interrupt flags are located in the module.
 3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt-enable cannot.
 4. Implemented in MSP430x415 and MSP430x417 devices only

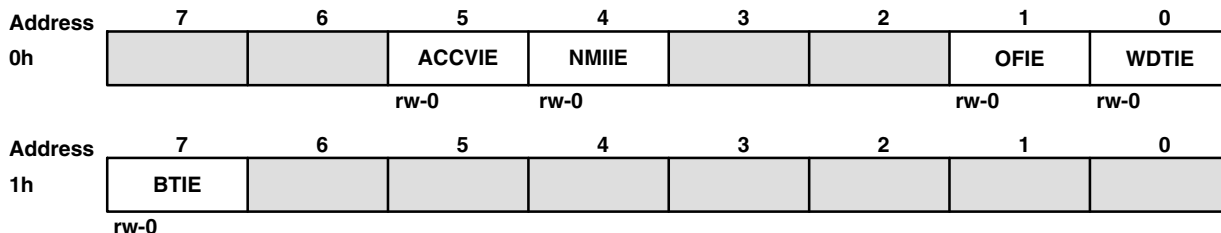
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special function registers

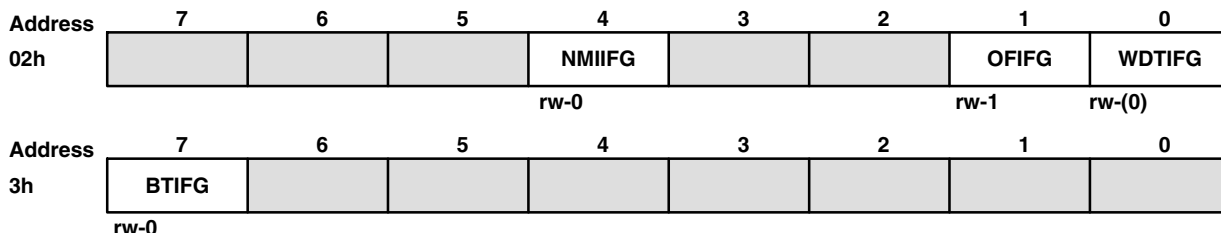
Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2



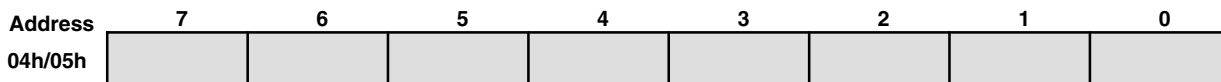
- WDTIE: Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
- OFIE: Oscillator fault interrupt enable
- NMIIE: Nonmaskable interrupt enable
- ACCVIE: Flash access violation interrupt enable
- BTIE: Basic Timer1 interrupt enable

interrupt flag register 1 and 2



- WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation. Reset with V_{CC} power-up, or a reset condition at the \overline{RST}/NMI pin in reset mode.
- OFIFG: Flag set on oscillator fault
- NMIIFG: Set via \overline{RST}/NMI pin
- BTIFG: Basic Timer1 interrupt flag

module enable registers 1 and 2



- Legend: **rw-0,1:** Bit Can Be Read and Written. It Is Reset or Set by PUC.
rw-(0,1): Bit Can Be Read and Written. It Is Reset or Set by POR.
 SFR Bit Not Present in Device.



memory organization

| | | MSP430F412 | MSP430F413 | MSP430F415 | MSP430F417 |
|--------------------|-----------|----------------------------|----------------------------|----------------------------|------------------------|
| Memory | Size | 4KB | 8KB | 16KB | 32KB |
| Interrupt vector | Flash | 0FFFFh to 0FFE0h | 0FFFFh to 0FFE0h | 0FFFFh to 0FFE0h | 0FFFFh to 0FFE0h |
| Code memory | Flash | 0FFFFh to 0F000h | 0FFFFh to 0E000h | 0FFFFh to 0C000h | 0FFFFh to 08000h |
| Information memory | Size | 256 Byte | 256 Byte | 256 Byte | 256 Byte |
| | Flash | 010FFh to 01000h | 010FFh to 01000h | 010FFh to 01000h | 010FFh to 01000h |
| Boot memory | Size | 1KB | 1KB | 1KB | 1KB |
| | ROM | 0FFFh to 0C00h | 0FFFh to 0C00h | 0FFFh to 0C00h | 0FFFh to 0C00h |
| RAM | Size | 256 Byte 02FFh to 0200h | 256 Byte 02FFh to 0200h | 512 Byte 03FFh to 0200h | 1 KB 05FFh to 0200h |
| Peripherals | 16-bit | 01FFh to 0100h | 01FFh to 0100h | 01FFh to 0100h | 01FFh to 0100h |
| | 8-bit | 0FFh to 010h | 0FFh to 010h | 0FFh to 010h | 0FFh to 010h |
| | 8-bit SFR | 0Fh to 00h | 0Fh to 00h | 0Fh to 00h | 0Fh to 00h |

| | | MSP430C412 | MSP430C413 |
|--------------------|-----------|----------------------------|----------------------------|
| Memory | Size | 4KB | 8KB |
| Interrupt vector | ROM | 0FFFFh to 0FFE0h | 0FFFFh to 0FFE0h |
| Code memory | ROM | 0FFFFh to 0F000h | 0FFFFh to 0E000h |
| Information memory | Size | NA | NA |
| Boot memory | Size | NA | NA |
| RAM | Size | 256 Byte 02FFh to 0200h | 256 Byte 02FFh to 0200h |
| Peripherals | 16-bit | 01FFh to 0100h | 01FFh to 0100h |
| | 8-bit | 0FFh to 010h | 0FFh to 010h |
| | 8-bit SFR | 0Fh to 00h | 0Fh to 00h |

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

| BSL FUNCTION | PM, RTD, RGC PACKAGE PINS |
|---------------------|----------------------------------|
| Data Transmit | 53 - P1.0 |
| Data Receive | 52 - P1.1 |

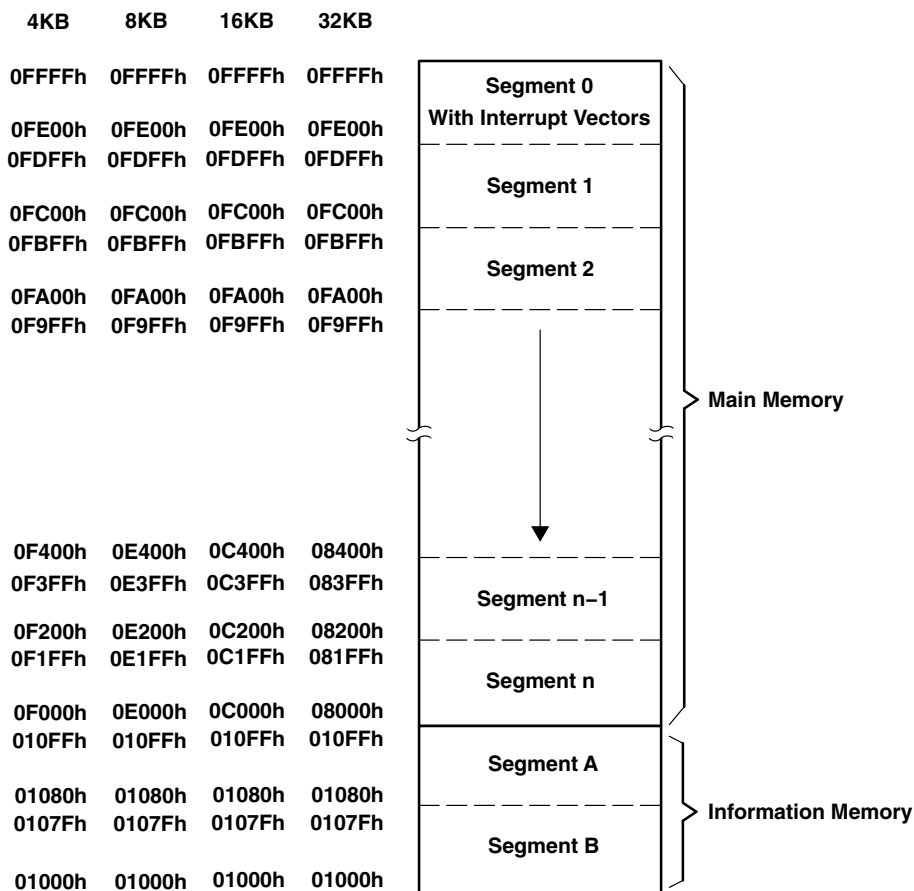
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flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*, literature number SLAU056.

oscillator and system clock

The clock system in the MSP430x41x family of devices is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μ s. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a fixed level or user selectable level (MSP430x415 & MSP430x417 only) and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

Basic Timer1

Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

LCD driver

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

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watchdog timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

Timer_A3/Timer0_A3

Timer_A3/Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3/Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3/Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_A3/TIMER0_A3 SIGNAL CONNECTIONS | | | | | |
|---------------------------------------|---------------------|-------------------|--------------|----------------------|-------------------|
| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
| 48 - P1.5 | TACLK/TA0CLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 48 - P1.5 | TACLK/TA0CLK | INCLK | | | |
| 53 - P1.0 | TA0/TA0.0 | CCI0A | CCR0 | TA0/TA0.0 | 53 - P1.0 |
| 52 - P1.1 | TA0/TA0.0 | CCI0B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 51 - P1.2 | TA1/TA0.1 | CCI1A | CCR1 | TA1/TA0.1 | 51 - P1.2 |
| | CAOUT (internal) | CCI1B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 45 - P2.0 | TA2/TA0.2 | CCI2A | CCR2 | TA2/TA0.2 | 45 - P2.0 |
| | ACLK (internal) | CCI2B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |



Timer1_A5 (MSP430x415 and MSP430x417 only)

Timer1_A5 is a 16-bit timer/counter with five capture/compare registers. Timer1_A5 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A5 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER1_A5 SIGNAL CONNECTIONS | | | | | |
|------------------------------|----------------------------|-------------------|--------------|----------------------|-------------------|
| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
| 32 - P2.5 | TA1CLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 32 - P2.5 | $\overline{\text{TA1CLK}}$ | INCLK | | | |
| 49 - P1.4 | TA1.0 | CCI0A | CCR0 | TA1.0 | 49 - P1.4 |
| 50 - P1.3 | TA1.0 | CCI0B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 44 - P2.1 | TA1.1 | CCI1A | CCR1 | TA1.1 | 44 - P2.1 |
| | CAOUT (internal) | CCI1B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 35 - P2.2 | TA1.2 | CCI2A | CCR2 | TA1.2 | 35 - P2.2 |
| | Not Connected | CCI2B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 34 - P2.3 | TA1.3 | CCI3A | CCR3 | TA1.3 | 34 - P2.3 |
| | Not Connected | CCI3B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 33 - P2.4 | TA1.4 | CCI4A | CCR4 | TA1.4 | 33 - P2.4 |
| | Not Connected | CCI4B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |

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peripheral file map

| PERIPHERALS WITH WORD ACCESS | | | |
|---|-----------------------------------|------------------|-------|
| Watchdog | Watchdog Timer control | WDTCTL | 0120h |
| Timer1_A5 (MSP430x415 and MSP430x417 only) | Timer1_A interrupt vector | TA1IV | 011Eh |
| | Timer1_A control | TA1CTL | 0180h |
| | Capture/compare control 0 | TA1CCTL0 | 0182h |
| | Capture/compare control 1 | TA1CCTL1 | 0184h |
| | Capture/compare control 2 | TA1CCTL2 | 0186h |
| | Capture/compare control 3 | TA1CCTL3 | 0188h |
| | Capture/compare control 4 | TA1CCTL4 | 018Ah |
| | Reserved | | 018Ch |
| | Reserved | | 018Eh |
| | Timer1_A register | TA1R | 0190h |
| | Capture/compare register 0 | TA1CCR0 | 0192h |
| | Capture/compare register 1 | TA1CCR1 | 0194h |
| | Capture/compare register 2 | TA1CCR2 | 0196h |
| | Capture/compare register 3 | TA1CCR3 | 0198h |
| | Capture/compare register 4 | TA1CCR4 | 019Ah |
| Reserved | | 019Ch | |
| Reserved | | 019Eh | |
| Timer_A3/Timer0_A3 | Timer_A/Timer0_A interrupt vector | TAIV/TA0IV | 012Eh |
| | Timer_A/Timer0_A control | TACTL/TA0CTL | 0160h |
| | Capture/compare control 0 | TACCTL0/TA0CCTL0 | 0162h |
| | Capture/compare control 1 | TACCTL1/TA0CCTL1 | 0164h |
| | Capture/compare control 2 | TACCTL2/TA0CCTL2 | 0166h |
| | Reserved | | 0168h |
| | Reserved | | 016Ah |
| | Reserved | | 016Ch |
| | Reserved | | 016Eh |
| | Timer_A/Timer0_A register | TAR/TA0R | 0170h |
| | Capture/compare register 0 | TACCR0/TA0CCR0 | 0172h |
| | Capture/compare register 1 | TACCR1/TA0CCR1 | 0174h |
| | Capture/compare register 2 | TACCR2/TA0CCR2 | 0176h |
| | Reserved | | 0178h |
| | Reserved | | 017Ah |
| Reserved | | 017Ch | |
| Reserved | | 017Eh | |
| Flash | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |



peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS | | | |
|-------------------------------------|--------------------------------------|-----------------|--------------|
| LCD | LCD memory 20 | LCDM20 | 0A4h |
| | : | : | : |
| | LCD memory 16 | LCDM16 | 0A0h |
| | LCD memory 15 | LCDM15 | 09Fh |
| | : | : | : |
| | LCD memory 1 LCD control and mode | LCDM1 LCDCTL | 091h 090h |
| Comparator_A | Comparator_A port disable | CAPD | 05Bh |
| | Comparator_A control2 | CACTL2 | 05Ah |
| | Comparator_A control1 | CACTL1 | 059h |
| Brownout, SVS | SVS control register | SVSCTL | 056h |
| FLL+ Clock | FLL+ Control1 | FLL_CTL1 | 054h |
| | FLL+ Control0 | FLL_CTL0 | 053h |
| | System clock frequency control | SCFQCTL | 052h |
| | System clock frequency integrator | SCFI1 | 051h |
| | System clock frequency integrator | SCFI0 | 050h |
| Basic Timer1 | BT counter2 | BTCNT2 | 047h |
| | BT counter1 | BTCNT1 | 046h |
| | BT control | BTCTL | 040h |
| Port P6 | Port P6 selection | P6SEL | 037h |
| | Port P6 direction | P6DIR | 036h |
| | Port P6 output | P6OUT | 035h |
| | Port P6 input | P6IN | 034h |
| Port P5 | Port P5 selection | P5SEL | 033h |
| | Port P5 direction | P5DIR | 032h |
| | Port P5 output | P5OUT | 031h |
| | Port P5 input | P5IN | 030h |
| Port P4 | Port P4 selection | P4SEL | 01Fh |
| | Port P4 direction | P4DIR | 01Eh |
| | Port P4 output | P4OUT | 01Dh |
| | Port P4 input | P4IN | 01Ch |
| Port P3 | Port P3 selection | P3SEL | 01Bh |
| | Port P3 direction | P3DIR | 01Ah |
| | Port P3 output | P3OUT | 019h |
| | Port P3 input | P3IN | 018h |
| Port P2 | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt-edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |

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peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) | | | |
|--|-------------------------------|-------|------|
| Port P1 | Port P1 selection | P1SEL | 026h |
| | Port P1 interrupt enable | P1IE | 025h |
| | Port P1 interrupt-edge select | P1IES | 024h |
| | Port P1 interrupt flag | P1IFG | 023h |
| | Port P1 direction | P1DIR | 022h |
| | Port P1 output | P1OUT | 021h |
| | Port P1 input | P1IN | 020h |
| Special Functions | SFR module enable 2 | ME2 | 005h |
| | SFR module enable 1 | ME1 | 004h |
| | SFR interrupt flag2 | IFG2 | 003h |
| | SFR interrupt flag1 | IFG1 | 002h |
| | SFR interrupt enable2 | IE2 | 001h |
| | SFR interrupt enable1 | IE1 | 000h |

absolute maximum ratings†

| | |
|--|----------------------------|
| Voltage applied at V_{CC} to V_{SS} | -0.3 V to + 4.1 V |
| Voltage applied to any pin (see Note 1) | -0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device terminal | ± 2 mA |
| Storage temperature: Unprogrammed device | -55°C to 150°C |
| Programmed device | -40°C to 85°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.



recommended operating conditions

| PARAMETER | | MIN | NOM | MAX | UNITS | |
|---|-------------------------|-------------------|-----|-------|-------|-----|
| Supply voltage during program execution, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) (see Note 1) | MSP430x41x | 1.8 | | 3.6 | V | |
| Supply voltage during program execution, SVS enabled and PORON = 1, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) (see Note 1 and Note 2) | MSP430x412/413 | 2.2 | | 3.6 | V | |
| | MSP430x415/417 | 2.0 | | 3.6 | | |
| Supply voltage during programming of flash memory, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$) | MSP430F41x | 2.7 | | 3.6 | V | |
| Supply voltage, V_{SS} ($AV_{SS1/2} = DV_{SS} = V_{SS}$) | | 0 | | 0 | V | |
| Operating free-air temperature range, T_A | MSP430x41x | -40 | | 85 | °C | |
| LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 3) | LF selected, XTS_FLL=0 | Watch crystal | | 32768 | Hz | |
| | XT1 selected, XTS_FLL=1 | Ceramic resonator | | 450 | 8000 | kHz |
| | XT1 selected, XTS_FLL=1 | Crystal | | 1000 | 8000 | |
| Processor frequency (signal MCLK), $f_{(System)}$ | $V_{CC} = 1.8$ V | DC | | 4.15 | MHz | |
| | $V_{CC} = 3.6$ V | DC | | 8 | | |

- NOTES:
1. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
 2. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised above minimum supply voltage plus the hysteresis of the SVS circuitry.
 3. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

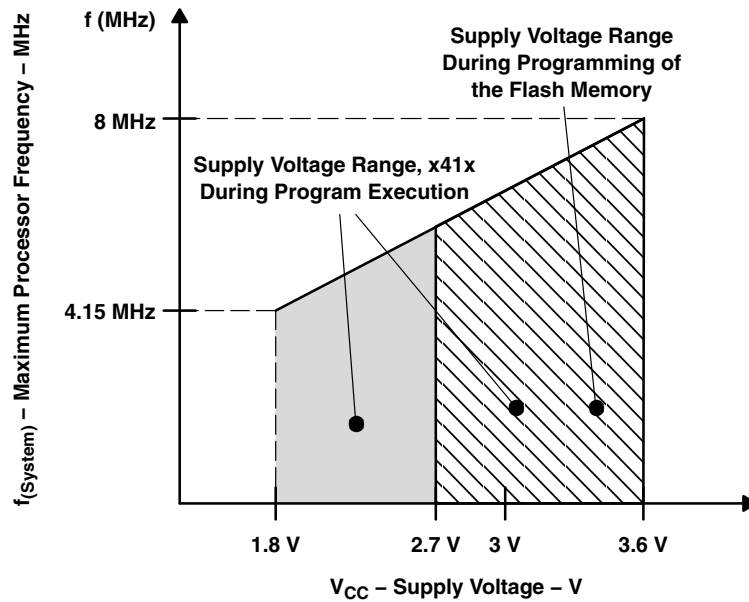


Figure 1. Frequency vs Supply Voltage

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current (see Note 1)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|--------------------------------|-----------------|-----|------|-----|------|
| I _(AM) | Active mode, f _(MCLK) = f _(SMCLK) = f _(DCO) = 1 MHz, f _(ACLK) = 32,768 Hz, XTS_FLL = 0 (F41x: Program executes in flash) | T _A = -40°C to 85°C | 2.2 V | | 160 | 200 | μA |
| | | | 3 V | | 240 | 300 | |
| | | | 2.2 V | | 200 | 250 | |
| | | | 3 V | | 300 | 350 | |
| I _(LPM0) | Low-power mode (LPM0) f _(MCLK) = f _(SMCLK) = f _(DCO) = 0.5 MHz, f _(ACLK) = 32,768 Hz, XTS_FLL = 0 FN_8=FN_4=FN_3=FN_2=0 (see Note 3) | T _A = -40°C to 85°C | 2.2 V | | 32 | 45 | μA |
| | | | 3 V | | 55 | 70 | |
| | 2.2 V | | | 57 | 70 | | |
| | 3 V | | | 92 | 100 | | |
| I _(LPM2) | Low-power mode (LPM2) (see Note 3) | T _A = -40°C to 85°C | 2.2 V | | 11 | 14 | μA |
| | | | 3 V | | 17 | 22 | |
| I _(LPM3) | Low-power mode (LPM3) (see Note 2 and Note 3) | T _A = -40°C | 2.2 V | | 0.95 | 1.4 | μA |
| | | T _A = -10°C | | | 0.8 | 1.3 | |
| | | T _A = 25°C | | | 0.7 | 1.2 | |
| | | T _A = 60°C | | | 0.95 | 1.4 | |
| | | T _A = 85°C | | | 1.6 | 2.3 | |
| | | T _A = -40°C | 3 V | | 1.1 | 1.7 | |
| | | T _A = -10°C | | | 1.0 | 1.6 | |
| | | T _A = 25°C | | | 0.9 | 1.5 | |
| | | T _A = 60°C | | | 1.1 | 1.7 | |
| | | T _A = 85°C | | | 2.0 | 2.6 | |
| I _(LPM4) | Low-power mode (LPM4) (see Note 3) | T _A = -40°C | 2.2 V/3 V | | 0.1 | 0.5 | μA |
| | | T _A = 25°C | | | 0.1 | 0.5 | |
| | | T _A = 85°C | | | 0.8 | 2.5 | |

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current. The current consumption is measured with active Basic Timer1 and LCD (ACLK selected).

The current consumption of the Comparator_A and the SVS module are specified in the respective sections.

2. The LPM3 currents are characterized with a KDS Daishinku DT-38 (6 pF) crystal.

3. Current for brownout included.

current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f_{(\text{System})} [\text{MHz}]$$

current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 140 \mu\text{A/V} \times (V_{CC} - 3 \text{ V})$$



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – ports P1, P2, P3, P4, P5, and P6

| PARAMETER | | V _{CC} | MIN | MAX | UNIT |
|------------------|---|-----------------|------|-----|------|
| V _{IT+} | Positive-going input threshold voltage | 2.2 V | 1.1 | 1.5 | V |
| | | 3 V | 1.5 | 1.9 | |
| V _{IT-} | Negative-going input threshold voltage | 2.2 V | 0.4 | 0.9 | V |
| | | 3 V | 0.9 | 1.3 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | 2.2 V | 0.3 | 1.1 | V |
| | | 3 V | 0.45 | 1 | |

standard inputs – $\overline{\text{RST}}$ /NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

| PARAMETER | | V _{CC} | MIN | MAX | UNIT |
|-----------------|--------------------------|-----------------|---------------------|----------------------|------|
| V _{IL} | Low-level input voltage | 2.2 V/3 V | V _{SS} | V _{SS} +0.6 | V |
| V _{IH} | High-level input voltage | | 0.8×V _{CC} | V _{CC} | V |

inputs P_{x.x}, TAx/TAx.x

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|----------------------|---|--|-----------------|-----|-----|-------|
| t _(int) | External interrupt timing | Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag (see Note 1) | 2.2 V/3 V | 1.5 | | cycle |
| | | | 2.2 V | 62 | | ns |
| | | | 3 V | 50 | | |
| t _(cap) | Timer_A, capture timing | TAx/TAx.y | 2.2 V | 62 | | ns |
| | | | 3 V | 50 | | |
| f _(TAext) | Timer_A clock frequency externally applied to pin | TACLK/TAxCLK, INCLK t _(H) = t _(L) | 2.2 V | | 8 | MHz |
| | | | 3 V | | 10 | |
| f _(TAint) | Timer_A clock frequency | SMCLK or ACLK signal selected | 2.2 V | | 8 | MHz |
| | | | 3 V | | 10 | |

NOTES: 1. The external signal sets the interrupt flag every time the minimum t_(int) cycle and time parameters are met. It may be set even with trigger signals shorter than t_(int). Both the cycle and timing specifications must be met to ensure the flag is set. t_(int) is measured in MCLK cycles.

leakage current (see Note 1)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-------------------------|-----------------|--|-----------------|-----|-----|------|
| I _{lkg} (P1.x) | Leakage current | Port P1 V _(P1.x) (see Note 2) | 2.2 V/3 V | | ±50 | nA |
| I _{lkg} (P2.x) | | Port P2 V _(P2.x) (see Note 2) | | | ±50 | |
| I _{lkg} (P3.x) | | Port P3 V _(P3.x) (see Note 2) | | | ±50 | |
| I _{lkg} (P4.x) | | Port P4 V _(P4.x) (see Note 2) | | | ±50 | |
| I _{lkg} (P5.x) | | Port P5 V _(P5.x) (see Note 2) | | | ±50 | |
| I _{lkg} (P6.x) | | Port P6 V _(P6.x) (see Note 2) | | | ±50 | |

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as an input.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P3, P4, P5, and P6

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|--|-----------------|-----------------------|-----------------------|------|
| V _{OH} | High-level output voltage | I _{OH(max)} = -1.5 mA, See Note 1 | 2.2 V | V _{CC} -0.25 | V _{CC} | V |
| | | I _{OH(max)} = -6 mA, See Note 2 | 2.2 V | V _{CC} -0.6 | V _{CC} | |
| | | I _{OH(max)} = -1.5 mA, See Note 1 | 3 V | V _{CC} -0.25 | V _{CC} | |
| | | I _{OH(max)} = -6 mA, See Note 2 | 3 V | V _{CC} -0.6 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _{OL(max)} = 1.5 mA, See Note 1 | 2.2 V | V _{SS} | V _{SS} +0.25 | V |
| | | I _{OL(max)} = 6 mA, See Note 2 | 2.2 V | V _{SS} | V _{SS} +0.6 | |
| | | I _{OL(max)} = 1.5 mA, See Note 1 | 3 V | V _{SS} | V _{SS} +0.25 | |
| | | I _{OL(max)} = 6 mA, See Note 2 | 3 V | V _{SS} | V _{SS} +0.6 | |

NOTES: 1. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
 2. The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±24 mA to satisfy the maximum specified voltage drop.

output frequency

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------------|---|---|---------------|-----|------|
| f _{Px.y} | (1 ≤ x ≤ 6, 0 ≤ y ≤ 7) | C _L = 20 pF, I _L = ± 1.5mA | V _{CC} = 2.2 V | DC | 10 | MHz |
| | | | V _{CC} = 3 V | DC | 12 | |
| f _{ACLK} , f _{MCLK} , f _{SMCLK} | P1.1/TA0/MCLK, P1.5/TACLK/ACLK | C _L = 20 pF | V _{CC} = 2.2 V | | 8 | MHz |
| | | | V _{CC} = 3 V | | 12 | |
| t _{Xdc} | Duty cycle of output frequency | P1.5/TACLK/ACLK, C _L = 20 pF V _{CC} = 2.2 V / 3 V | f _{ACLK} = f _{LFXT1} = f _{XT1} | 40% | 60% | |
| | | | f _{ACLK} = f _{LFXT1} = f _{LF} | 30% | 70% | |
| | | | f _{ACLK} = f _{LFXT1/n} | 50% | | |
| | | P1.1/TA0/MCLK, C _L = 20 pF, V _{CC} = 2.2 V / 3 V | f _{MCLK} = f _{LFXT1/n} | 50%– 15 ns | 50% | |
| f _{MCLK} = f _{DCOCLK} | 50%– 15 ns | | 50% | 50%+ 15 ns | | |



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

MSP430x412, MSP430x413 outputs – ports P1, P2, P3, P4, P5, and P6 (see Note A)

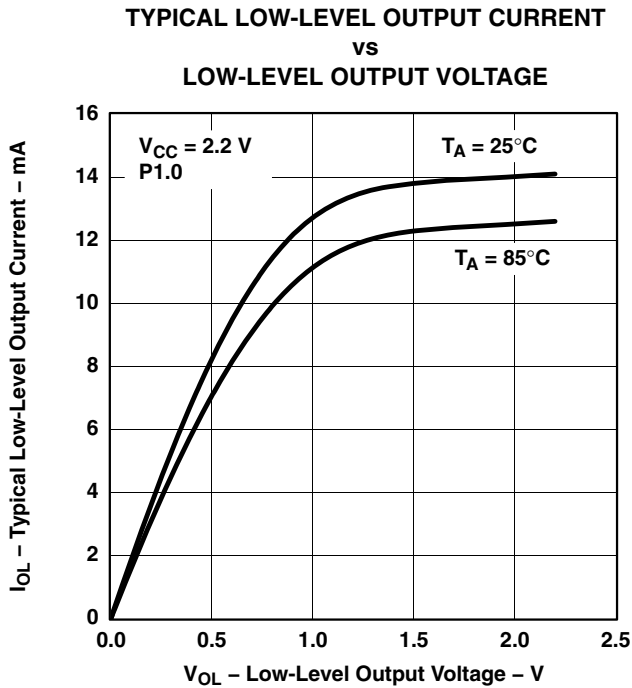


Figure 2

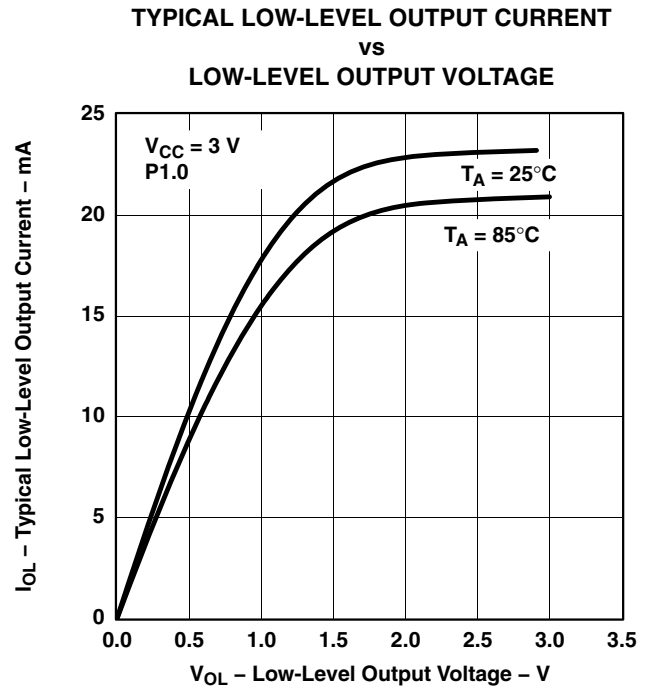


Figure 3

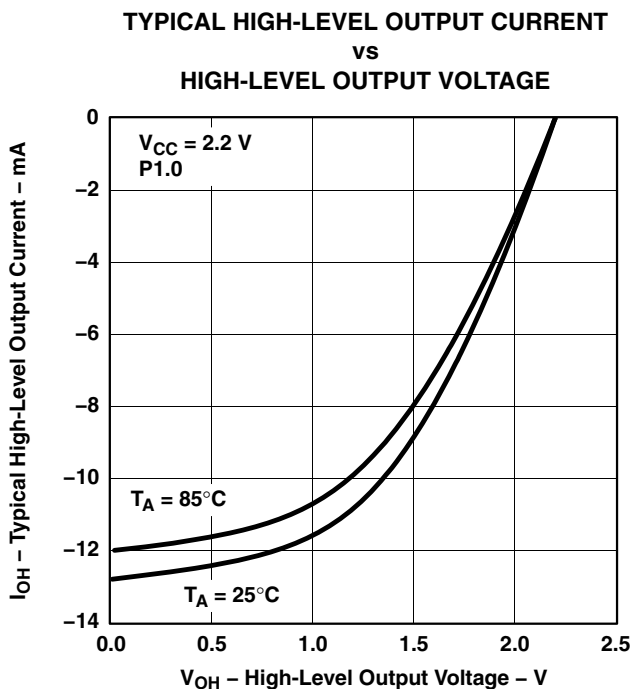


Figure 4

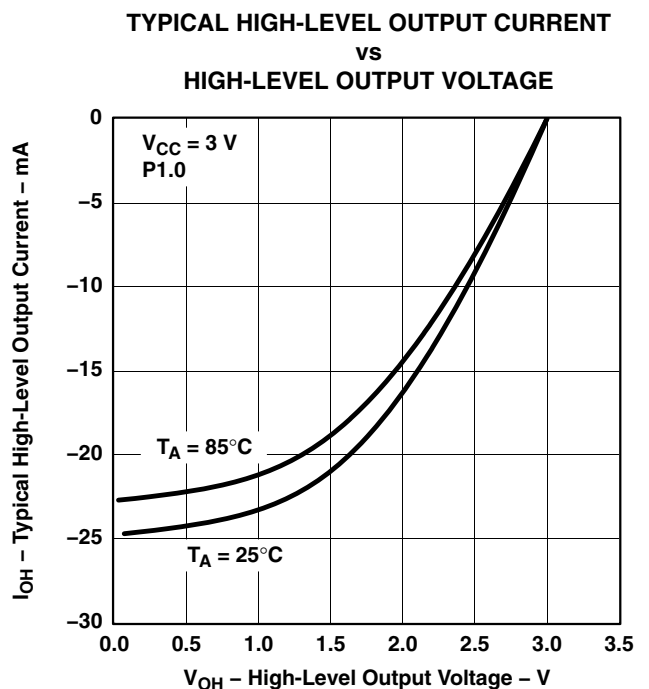


Figure 5

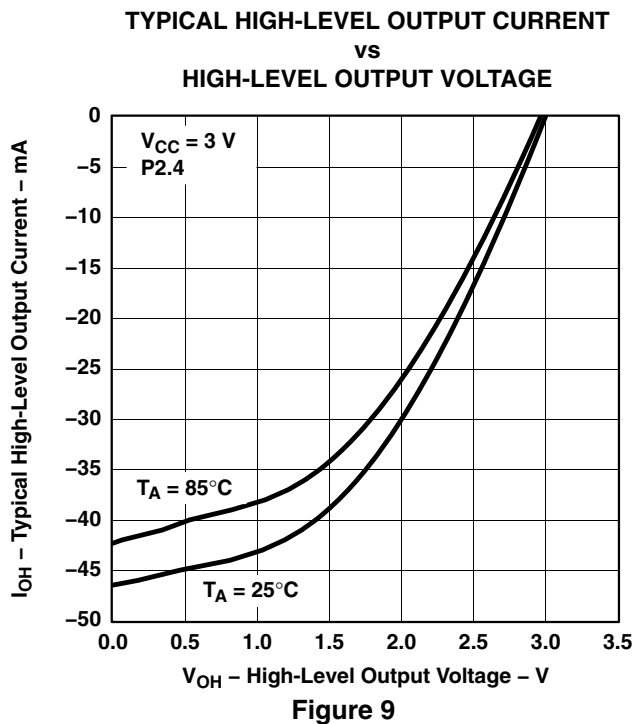
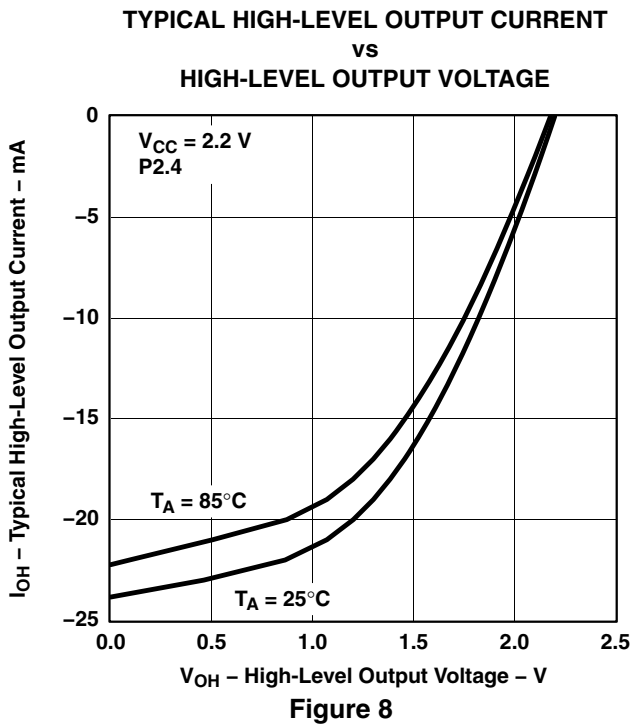
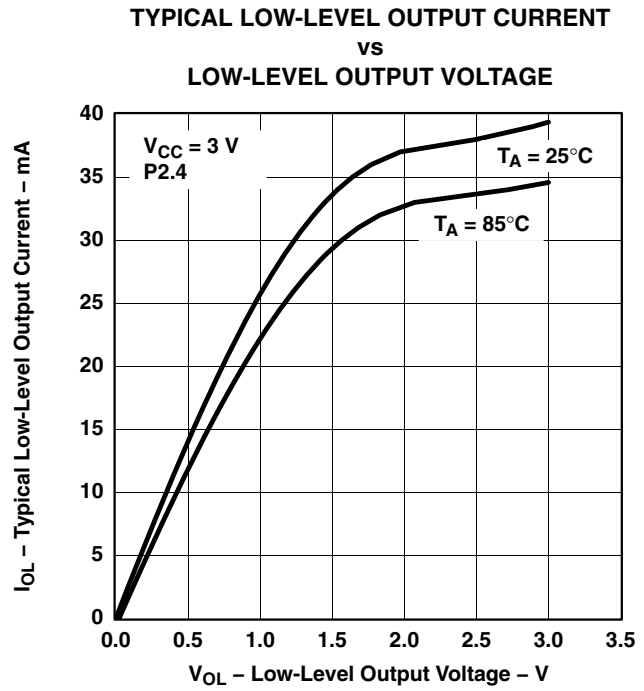
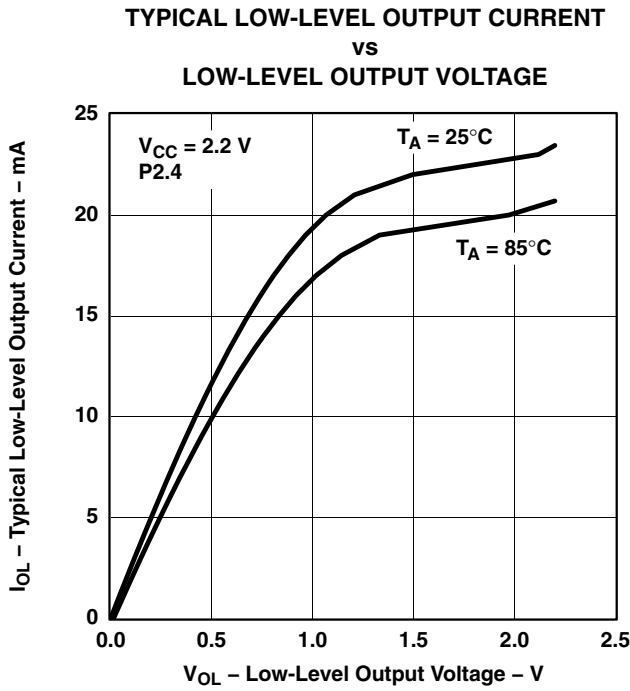
NOTE A: One output loaded at a time

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

MSP430x415, MSP430x417 outputs – ports P1, P2, P3, P4, P5, and P6 (see Note A)



NOTE B: One output loaded at a time



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---------------|------------|-----------------|----------------------|-----|-----|---------|
| $t_{d(LPM3)}$ | Delay time | f = 1 MHz | $V_{CC} = 2.2 V/3 V$ | | 6 | μs |
| | | f = 2 MHz | | 6 | | |
| | | f = 3 MHz | | 6 | | |

RAM (see Note 1)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------|-------------------------|-----|-----|------|
| V_{RAMh} | CPU halted (see Note 1) | 1.6 | | V |

NOTE 1: This parameter defines the minimum supply voltage when the data in the program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------|----------------------|--------------------------------|--|---|------------------|------------------|------|
| $V_{(33)}$ | Analog voltage | Voltage at P5.7/R33 | $V_{CC} = 3 V$ | 2.5 | | $V_{CC} + 0.2$ | V |
| $V_{(23)}$ | | Voltage at P5.6/R23 | | $(V_{33} - V_{03}) \times 2/3 + V_{03}$ | | | |
| $V_{(13)}$ | | Voltage at P5.5/R13 | | $(V_{(33)} - V_{(03)}) \times 1/3 + V_{(03)}$ | | | |
| $V_{(33)} - V_{(03)}$ | | Voltage at R33/R03 | | 2.5 | $V_{CC} + 0.2$ | | |
| $I_{(R03)}$ | Input leakage | $R03 = V_{SS}$ | No load at all segment and common lines, $V_{CC} = 3 V$ | | | ± 20 | nA |
| $I_{(R13)}$ | | $P5.5/R13 = V_{CC}/3$ | | | ± 20 | | |
| $I_{(R23)}$ | | $P5.6/R23 = 2 \times V_{CC}/3$ | | | ± 20 | | |
| $V_{(Sxx0)}$ | Segment line voltage | $I_{(Sxx)} = -3 \mu A,$ | $V_{CC} = 3 V$ | $V_{(03)}$ | | $V_{(03)} - 0.1$ | V |
| $V_{(Sxx1)}$ | | | | $V_{(13)}$ | $V_{(13)} - 0.1$ | | |
| $V_{(Sxx2)}$ | | | | $V_{(23)}$ | $V_{(23)} - 0.1$ | | |
| $V_{(Sxx3)}$ | | | | $V_{(33)}$ | $V_{(33)} + 0.1$ | | |

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------------------|---|-----------------|------|------|----------------------|------|
| I _(CC) | CAON = 1, CARSEL = 0, CAREF = 0 | 2.2 V | | 25 | 40 | μA |
| | | 3 V | | 45 | 60 | |
| I _(Ref ladder/RefDiode) | CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.6/CA0 and P1.7/CA1 | 2.2 V | | 30 | 50 | μA |
| | | 3 V | | 45 | 71 | |
| V _(Ref025) | $\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$ PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1 | 2.2 V / 3 V | 0.23 | 0.24 | 0.25 | |
| V _(Ref050) | $\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$ PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1 | 2.2V / 3 V | 0.47 | 0.48 | 0.50 | |
| V _(RefVT) | See Figure 10 and Figure 11 PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1; T _A = 85°C | 2.2 V | 390 | 480 | 540 | mV |
| | | 3 V | 400 | 490 | 550 | |
| V _(IC) | Common-mode input voltage range CAON = 1 | 2.2 V/3 V | 0 | | V _{CC} -1.0 | V |
| V _(offset) | Offset voltage See Note 2 | 2.2 V/3 V | -30 | | 30 | mV |
| V _(hys) | Input hysteresis CAON = 1 | 2.2 V/3 V | 0 | 0.7 | 1.4 | mV |
| t _(response LH) | T _A = 25°C, Overdrive 10 mV, Without filter: CAF = 0 | 2.2 V | 160 | 210 | 300 | ns |
| | | 3 V | 80 | 150 | 240 | |
| | T _A = 25°C Overdrive 10 mV, With filter: CAF = 1 | 2.2 V | 1.4 | 1.9 | 3.4 | μs |
| | | 3 V | 0.9 | 1.5 | 2.6 | |
| t _(response HL) | T _A = 25°C Overdrive 10 mV, Without filter: CAF = 0 | 2.2 V | 130 | 210 | 300 | ns |
| | | 3 V | 80 | 150 | 240 | |
| | T _A = 25°C, Overdrive 10 mV, With filter: CAF = 1 | 2.2 V | 1.4 | 1.9 | 3.4 | μs |
| | | 3 V | 0.9 | 1.5 | 2.6 | |

- NOTES: 1. The leakage current for the Comparator_A terminals is identical to I_{kg(Px.x)} specification.
 2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

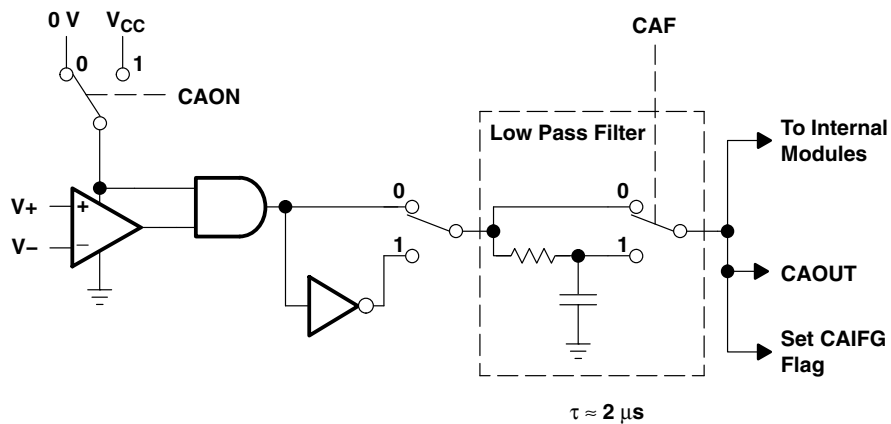
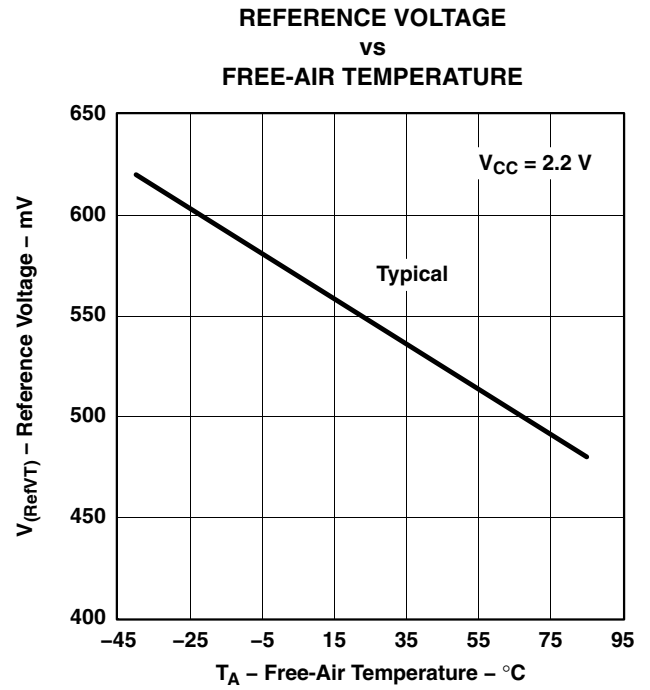
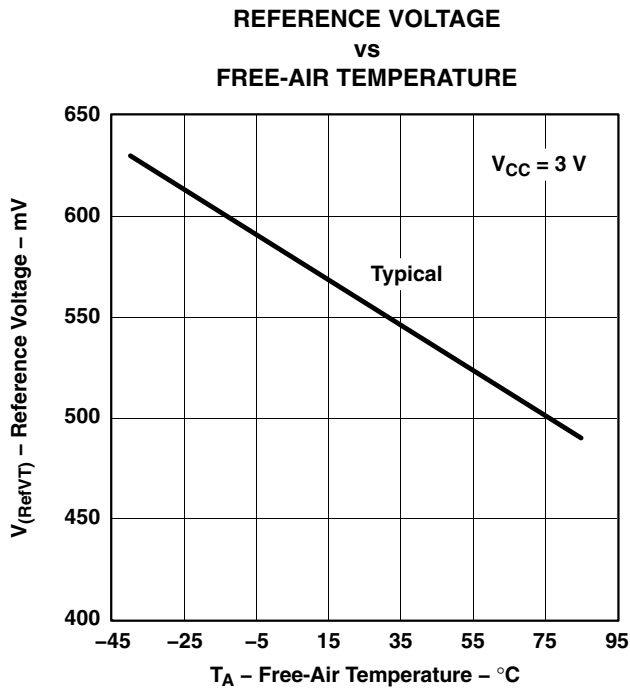


Figure 12. Comparator_A Module Block Diagram

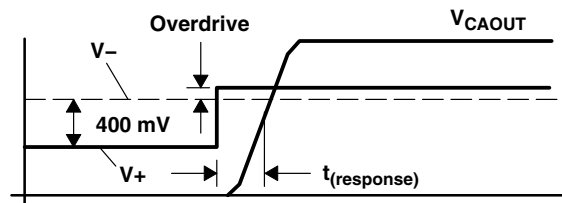


Figure 13. Overdrive Definition

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR brownout, reset (see Notes 1 and 2)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|-----|---------------------------|------|---------|
| $t_{d(BOR)}$ | | | | 2000 | μs |
| $V_{CC(start)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 14) | | $0.7 \times V_{(B_IT-)}$ | | V |
| $V_{(B_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 14, Figure 15, Figure 16) | | | 1.71 | V |
| $V_{hys(B_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 14) | 70 | 130 | 180 | mV |
| $t_{(reset)}$ | Pulse length needed at $\overline{RST/NMI}$ pin to accepted reset internally, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | 2 | | | μs |

- NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)} + V_{hys(B_IT-)}$ is $\leq 1.8 \text{ V}$.
2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \geq V_{CC(min)}$. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout/SVS circuit.

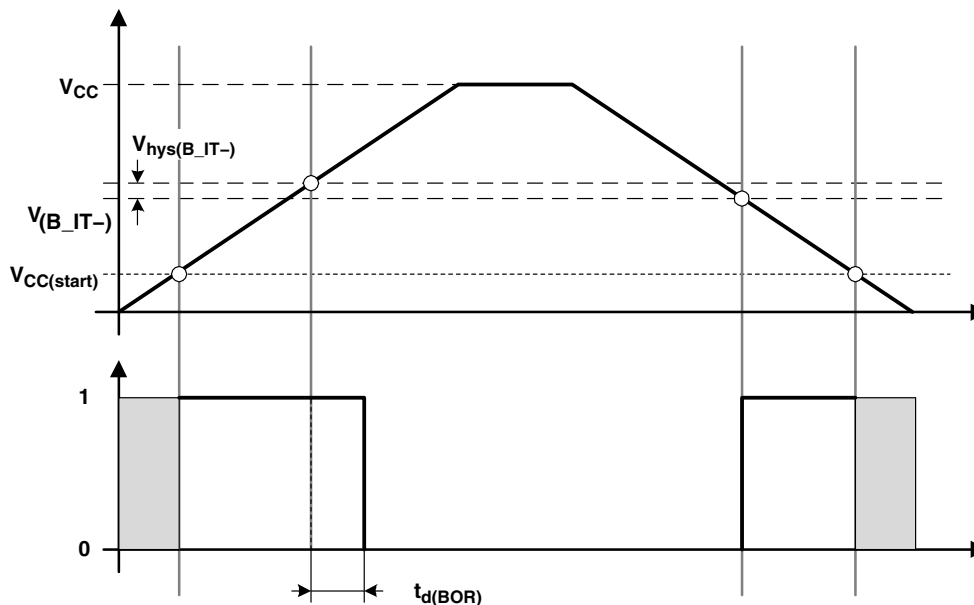


Figure 14. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

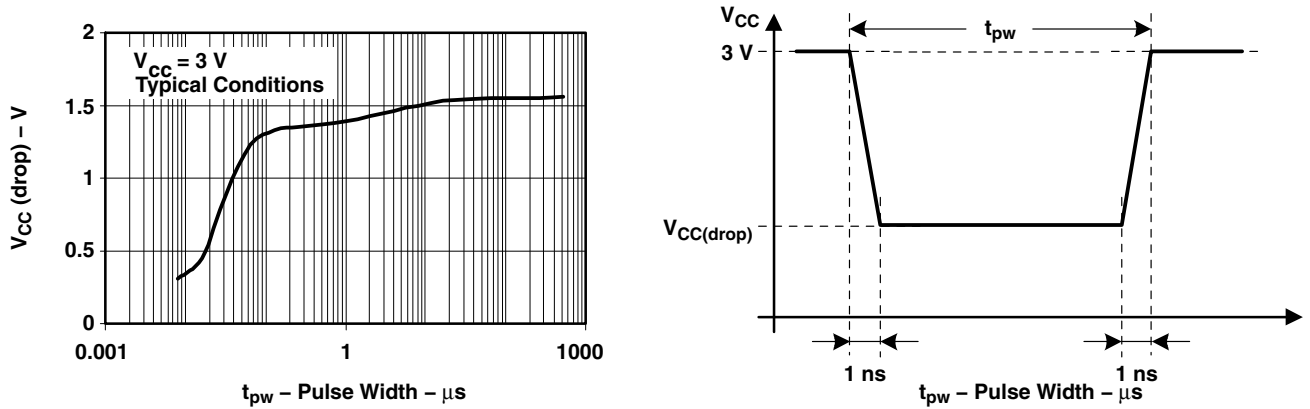


Figure 15. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

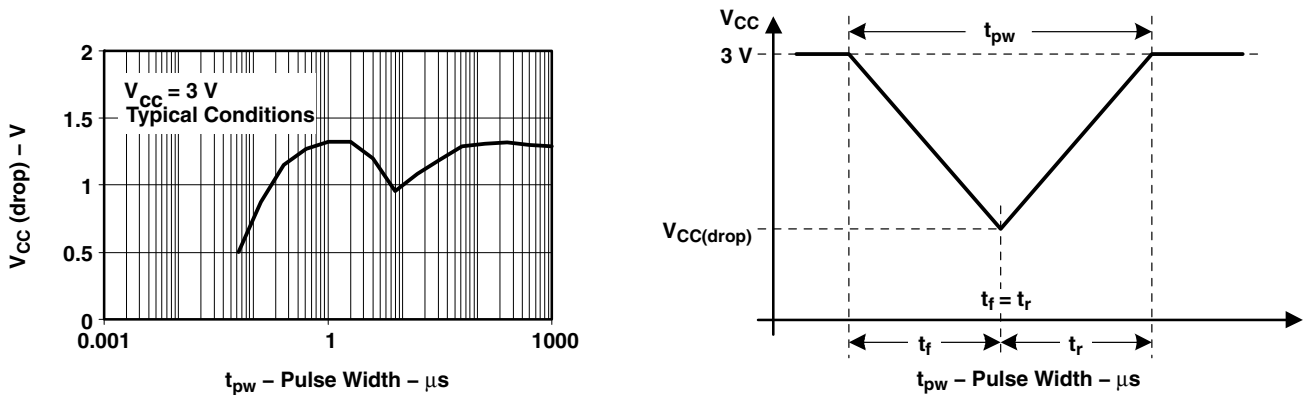


Figure 16. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

SVS (supply voltage supervisor/monitor) (MSP430x412, MSP430x413 only) (see Notes 1 and 2)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|-----|------|------|---------|
| $t_d(SVSR)$ | $dV_{CC}/dt > 30$ V/ms (see Note 2) | 5 | | 150 | μ s |
| | $dV_{CC}/dt \leq 30$ V/ms (see Note 2) | | | 2000 | μ s |
| $t_d(SV_{Son})$ | SV _{Son} , switch from 0 to 1, $V_{CC} = 3$ V (see Note 2) | 20 | | 150 | μ s |
| $V(SV_{Sstart})$ | $dV_{CC}/dt \leq 3$ V/s (see Figure 17) | | 1.55 | 1.7 | V |
| $V(SV_{S_IT-})$ | $dV_{CC}/dt \leq 3$ V/s (see Figure 17) | 1.8 | 1.95 | 2.2 | V |
| $V_{hys}(SV_{S_IT-})$ | $dV_{CC}/dt \leq 3$ V/s (see Figure 17) | 70 | 100 | 155 | mV |
| $I_{CC}(SVS)$ (see Note 1) | VLD \neq 0 (VLD bits are in SVSCTL register), $V_{CC} = 2.2$ V/3 V | | 10 | 15 | μ A |

- NOTES: 1. The current consumption of the SVS module is not included in the I_{CC} current consumption data.
2. The SVS is not active at power up.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SVS (supply voltage supervisor/monitor) (MSP430x415, MSP430x417 only) (see Notes 1 and 2)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT | |
|--|--|---------------|-------------------------------|-------------------|-------------------------------|----|
| $t_{d(SVSR)}$ | $dV_{CC}/dt > 30 \text{ V/ms}$ (see Figure 17) | 5 | | 150 | μs | |
| | $dV_{CC}/dt \leq 30 \text{ V/ms}$ | | | 2000 | | |
| $t_{d(SVSON)}$ | SVSON, switch from VLD=0 to VLD \neq 0, $V_{CC} = 3 \text{ V}$ | 20 | | 150 | μs | |
| t_{settle} | VLD \neq 0 [†] | | | 12 | μs | |
| $V_{(SVSstart)}$ | VLD \neq 0, $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 17) | | 1.55 | 1.7 | V | |
| $V_{\text{hys}(SVS_IT-)}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 17) | VLD = 1 | 70 | 120 | 155 | mV |
| | | VLD = 2 to 14 | $V_{(SVS_IT-)} \times 0.004$ | | $V_{(SVS_IT-)} \times 0.008$ | |
| | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 17), External voltage applied on SVSIN | VLD = 15 | 4.4 | | 10.4 | mV |
| $V_{(SVS_IT-)}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 17) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | 1.94 | 2.1 | 2.25 | |
| | | VLD = 3 | 2.05 | 2.2 | 2.37 | |
| | | VLD = 4 | 2.14 | 2.3 | 2.48 | |
| | | VLD = 5 | 2.24 | 2.4 | 2.6 | |
| | | VLD = 6 | 2.33 | 2.5 | 2.71 | |
| | | VLD = 7 | 2.46 | 2.65 | 2.86 | |
| | | VLD = 8 | 2.58 | 2.8 | 3 | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | 2.83 | 3.05 | 3.29 | |
| | | VLD = 11 | 2.94 | 3.2 | 3.42 | |
| | | VLD = 12 | 3.11 | 3.35 | 3.61 [†] | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76 [†] | |
| | VLD = 14 | 3.43 | 3.7 [†] | 3.99 [†] | | |
| $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 17), External voltage applied on SVSIN | VLD = 15 | 1.1 | 1.2 | 1.3 | | |
| $I_{CC(SVS)}$ (see Note 1) | VLD \neq 0, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | | 10 | 15 | μA | |

[†] The recommended operating voltage range is limited to 3.6 V.

[‡] t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD \neq 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be $> 50 \text{ mV}$.

NOTES: 1. The current consumption of the SVS module is not included in the I_{CC} current consumption data.
2. The SVS is not active at power up.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

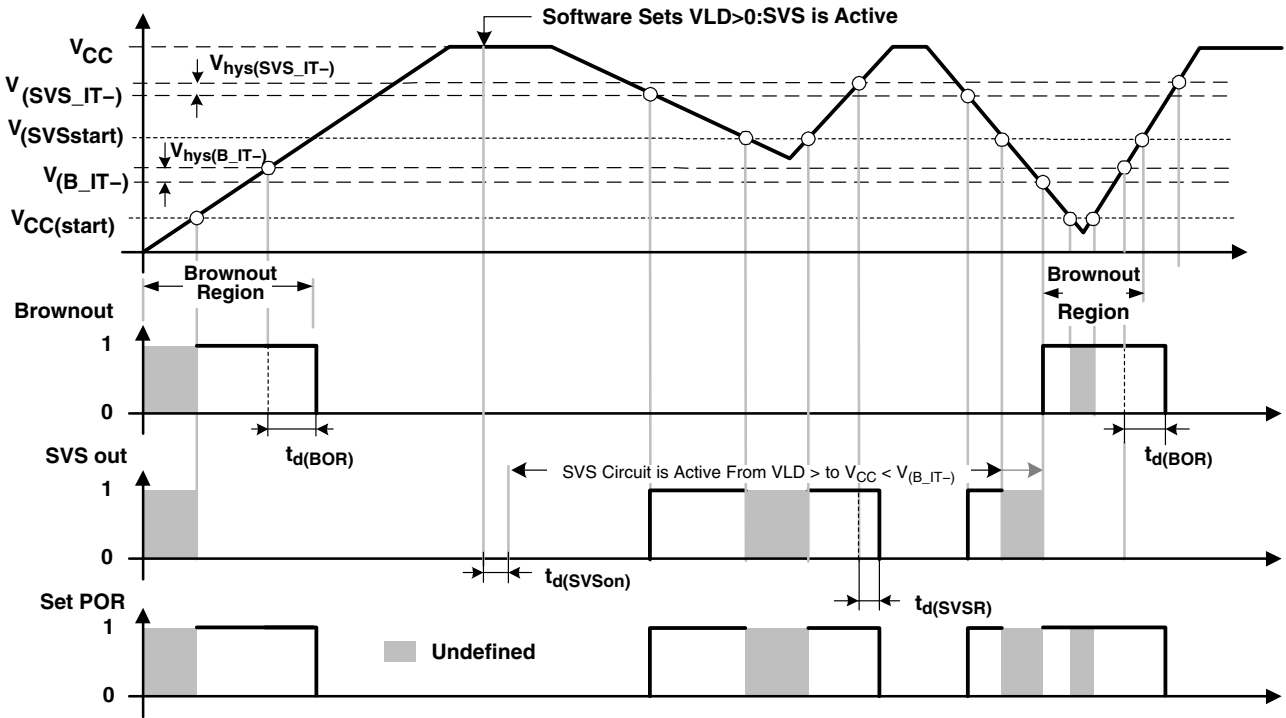


Figure 17. SVS Reset (SVSR) vs Supply Voltage

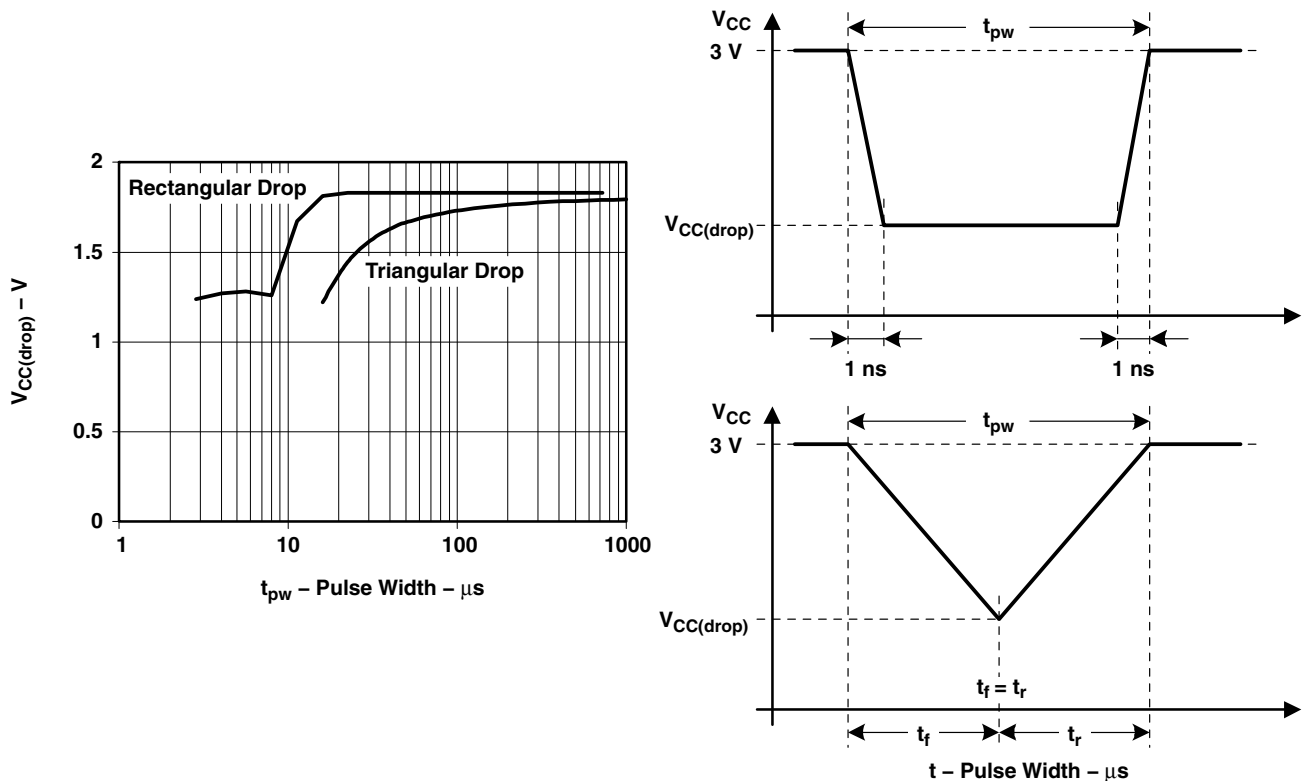


Figure 18. $V_{CC(drop)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|------|------|------|-------------------|
| f _(DCOCLK) | N _(DCO) = 01Eh, FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, D = 2, DCOPLUS = 0, f _{Crystal} = 32.768 kHz | 2.2 V/3 V | | 1 | | MHz |
| f _(DCO=2) | FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, DCOPLUS = 1 | 2.2 V | 0.3 | 0.65 | 1.25 | MHz |
| | | 3 V | 0.3 | 0.7 | 1.3 | |
| f _(DCO=27) | FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, DCOPLUS = 1 | 2.2 V | 2.5 | 5.6 | 10.5 | MHz |
| | | 3 V | 2.7 | 6.1 | 11.3 | |
| f _(DCO=2) | FN ₈ = FN ₄ = FN ₃ = 0, FN ₂ = 1, DCOPLUS = 1 | 2.2 V | 0.7 | 1.3 | 2.3 | MHz |
| | | 3 V | 0.8 | 1.5 | 2.5 | |
| f _(DCO=27) | FN ₈ = FN ₄ = FN ₃ = 0, FN ₂ = 1, DCOPLUS = 1 | 2.2 V | 5.7 | 10.8 | 18 | MHz |
| | | 3 V | 6.5 | 12.1 | 20 | |
| f _(DCO=2) | FN ₈ = FN ₄ = 0, FN ₃ = 1, FN ₂ = x, DCOPLUS = 1 | 2.2 V | 1.2 | 2 | 3 | MHz |
| | | 3 V | 1.3 | 2.2 | 3.5 | |
| f _(DCO=27) | FN ₈ = FN ₄ = 0, FN ₃ = 1, FN ₂ = x; DCOPLUS = 1 | 2.2 V | 9 | 15.5 | 25 | MHz |
| | | 3 V | 10.3 | 17.9 | 28.5 | |
| f _(DCO=2) | FN ₈ = 0, FN ₄ = 1, FN ₃ = FN ₂ = x, DCOPLUS = 1 | 2.2 V | 1.8 | 2.8 | 4.2 | MHz |
| | | 3 V | 2.1 | 3.4 | 5.2 | |
| f _(DCO=27) | FN ₈ = 0, FN ₄ = 1, FN ₃ = FN ₂ = x, DCOPLUS = 1 | 2.2 V | 13.5 | 21.5 | 33 | MHz |
| | | 3 V | 16 | 26.6 | 41 | |
| f _(DCO=2) | FN ₈ = 1, FN ₄ = FN ₃ = FN ₂ = x, DCOPLUS = 1 | 2.2 V | 2.8 | 4.2 | 6.2 | MHz |
| | | 3 V | 4.2 | 6.3 | 9.2 | |
| f _(DCO=27) | FN ₈ = 1, FN ₄ = FN ₃ = FN ₂ = x, DCOPLUS = 1 | 2.2 V | 21 | 32 | 46 | MHz |
| | | 3 V | 30 | 46 | 70 | |
| S _n | Step size between adjacent DCO taps: S _n = f _{DCO(Tap n+1)} / f _{DCO(Tap n)} (see Figure 20 for taps 21 to 27) | 1 < TAP ≤ 20 | | 1.06 | 1.11 | |
| | | TAP = 27 | | 1.07 | 1.17 | |
| D _t | Temperature drift, N _(DCO) = 01Eh, FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, D = 2, DCOPLUS = 0 | 2.2 V | -0.2 | -0.3 | -0.4 | %/ ^o C |
| | | 3 V | -0.2 | -0.3 | -0.4 | |
| D _V | Drift with V _{CC} variation, N _(DCO) = 01Eh, FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, D = 2, DCOPLUS = 0 | | 0 | 5 | 15 | %/V |

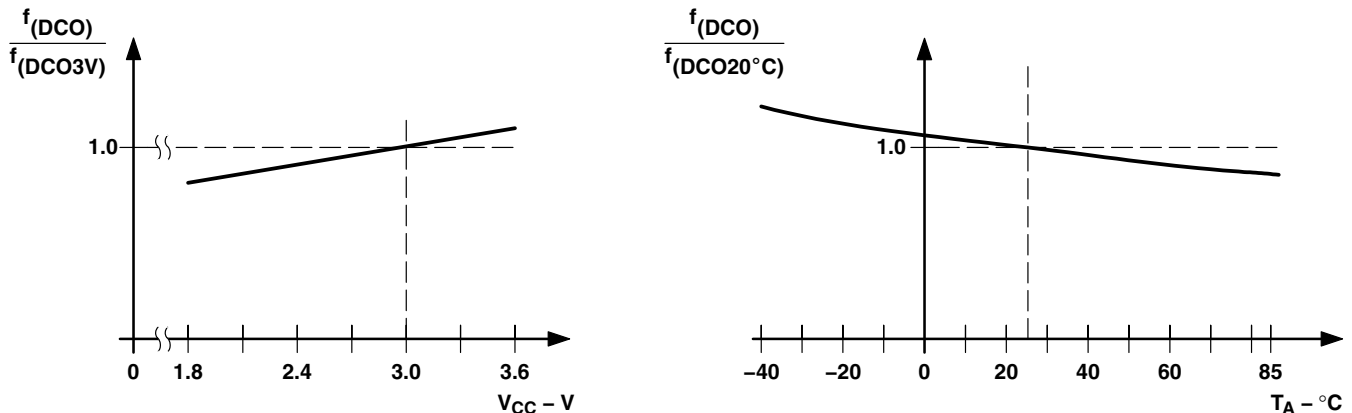


Figure 19. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

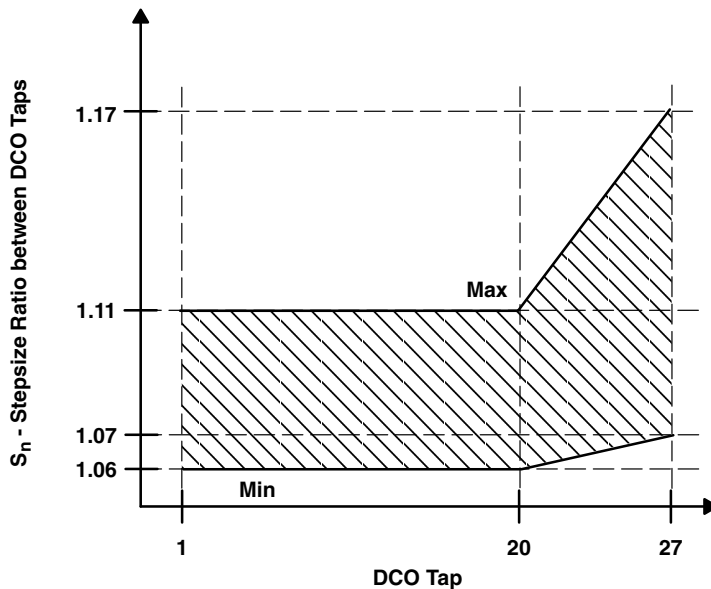


Figure 20. DCO Tap Step Size

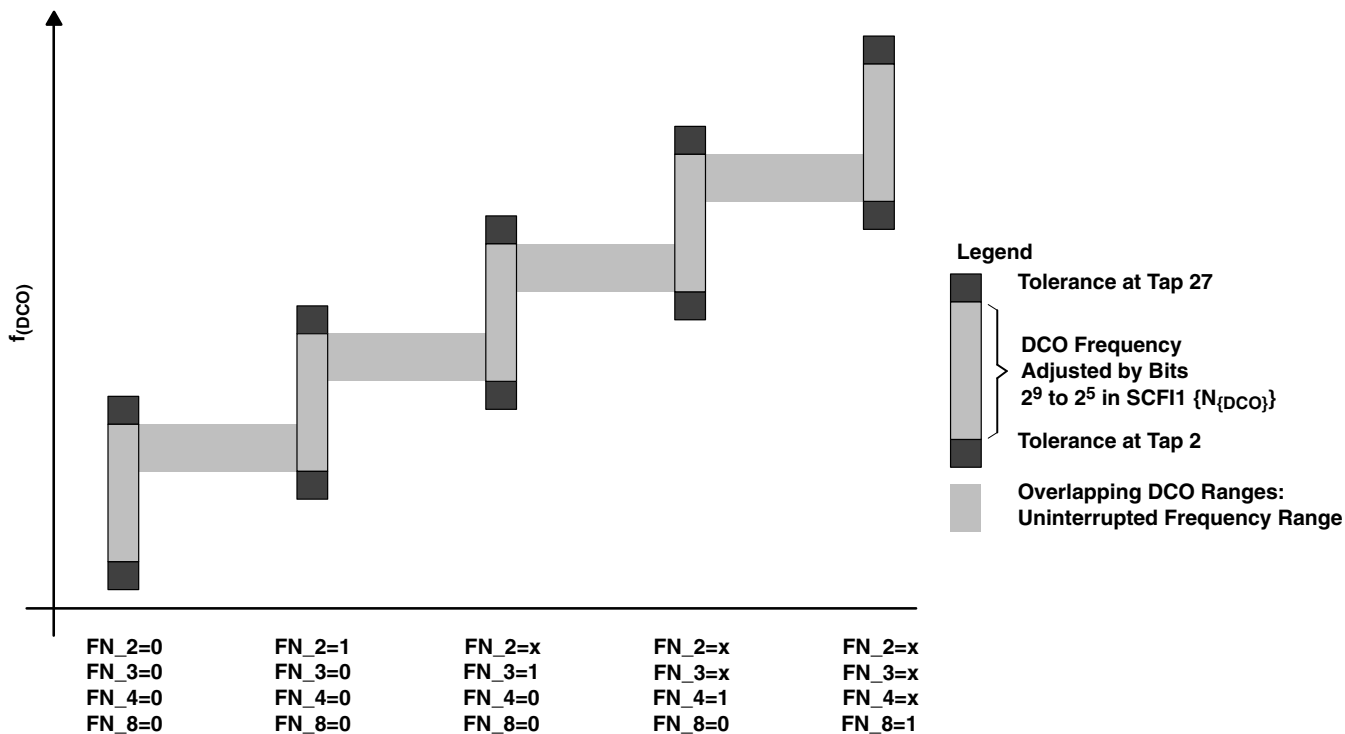


Figure 21. Five Overlapping DCO Ranges Controlled by FN_x Bits

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|-----------------------------|-----------------|-----------------|---------------------|-----|---------------------|------|
| C _{XIN} | Integrated load capacitance | OSCCAPx = 0h | 2.2 V/3 V | | 0 | | pF |
| | | OSCCAPx = 1h | | | 10 | | |
| | | OSCCAPx = 2h | | | 14 | | |
| | | OSCCAPx = 3h | | | 18 | | |
| C _{XOUT} | Integrated load capacitance | OSCCAPx = 0h | 2.2 V/3 V | | 0 | | pF |
| | | OSCCAPx = 1h | | | 10 | | |
| | | OSCCAPx = 2h | | | 14 | | |
| | | OSCCAPx = 3h | | | 18 | | |
| V _{IL} | Input levels at XIN | see Note 3 | 2.2 V/3 V | V _{SS} | | 0.2×V _{CC} | V |
| V _{IH} | | | 2.2 V/3 V | 0.8×V _{CC} | | V _{CC} | |

- NOTES:
- The parasitic capacitance from the package and board may be estimated to be 2pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. It is independent of XTS_FLL.
 - To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines must be observed:
 - Keep the trace between the MSP430x41x and the crystal as short as possible.
 - Design a good ground plane around oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to XIN and XOUT pins.
 - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
 - Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
 - External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

flash memory

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V _{CC(PGM/ERASE)} | Program and erase supply voltage | | | 2.7 | | 3.6 | V |
| f _{FTG} | Flash timing generator frequency | | | 257 | | 476 | kHz |
| I _{PGM} | Supply current from DV _{CC} during program | | 2.7 V/ 3.6 V | | 3 | 5 | mA |
| I _{ERASE} | Supply current from DV _{CC} during erase | | 2.7 V/ 3.6 V | | 3 | 7 | mA |
| t _{CPT} | Cumulative program time | See Note 1 | 2.7 V/ 3.6 V | | | 10 | ms |
| t _{CMErase} | Cumulative mass erase time | See Note 2 | 2.7 V/ 3.6 V | 200 | | | ms |
| | Program/erase endurance | | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | | 100 | | | years |
| t _{Word} | Word or byte program time | See Note 3 | | | 35 | | t _{FTG} |
| t _{Block, 0} | Block program time for 1 st byte or word | | | | 30 | | |
| t _{Block, 1-63} | Block program time for each additional byte or word | | | | 21 | | |
| t _{Block, End} | Block program end-sequence wait time | | | | 6 | | |
| t _{Mass Erase} | Mass erase time | | | | 5297 | | |
| t _{Seg Erase} | Segment erase time | | | | 4819 | | |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 2. The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297x1/f_{FTG,max} = 5297x1/476kHz). To achieve the required cumulative mass erase time the flash controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
 3. These values are hardwired into the flash controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG interface

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------------|-----------------|-----|-----|-----|------|
| f _{TCK} | TCK input frequency | see Note 1 | 2.2 V | 0 | | 5 | MHz |
| | | | 3 V | 0 | | 10 | MHz |
| R _{Internal} | Internal pull-up resistance on TMS, TCK, TDI/TCLK | see Note 2 | 2.2 V/ 3 V | 25 | 60 | 90 | kΩ |

- NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
 2. TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

JTAG fuse (see Note 1)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------------|-----|-----|------|
| V _{CC(FB)} | Supply voltage during fuse-blow condition | T _A = 25°C | 2.5 | | V |
| V _{FB} | Voltage level on TDI/TCLK for fuse-blow | MSP430C41x | 3.5 | 3.9 | V |
| | | MSP430F41x | 6 | 7 | V |
| I _{FB} | Supply current into TDI/TCLK during fuse blow | | | 100 | mA |
| t _{FB} | Time to blow fuse | | | 1 | ms |

- NOTES: 1. Once the fuse is blown, no further access to the MSP430 via JTAG/Test is possible. The JTAG block is switched to bypass mode.

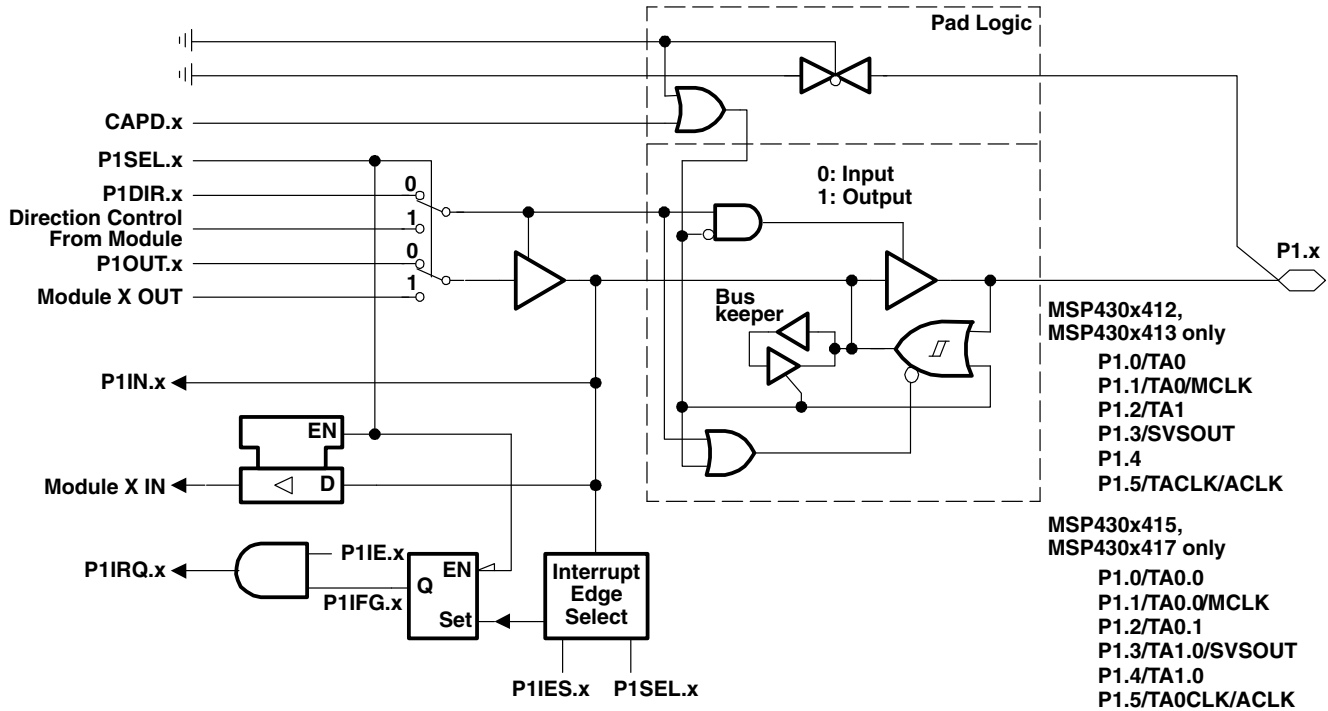
MSP430x41x MIXED SIGNAL MICROCONTROLLER

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APPLICATION INFORMATION

input/output schematics

Port P1, P1.0 to P1.5, input/output with Schmitt trigger



NOTE: $0 \leq x \leq 5$.
Port Function is Active if CAPD.x = 0

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|---|--------|---|--------|---------|---------|
| P1SEL.0 | P1DIR.0 | P1DIR.0 | P1OUT.0 | Out0 Sig. [†] | P1IN.0 | CCI0A [†] | P1IE.0 | P1IFG.0 | P1IES.0 |
| P1SEL.1 | P1DIR.1 | P1DIR.1 | P1OUT.1 | MCLK | P1IN.1 | CCI0B [†] | P1IE.1 | P1IFG.1 | P1IES.1 |
| P1SEL.2 | P1DIR.2 | P1DIR.2 | P1OUT.2 | Out1 Sig. [†] | P1IN.2 | CCI1A [†] | P1IE.2 | P1IFG.2 | P1IES.2 |
| P1SEL.3 | P1DIR.3 | P1DIR.3 | P1OUT.3 | SVSOUT | P1IN.3 | Unused | P1IE.3 | P1IFG.3 | P1IES.3 |
| P1SEL.4 | P1DIR.4 | P1DIR.4 | P1OUT.4 | DVSS [§] Out0 Sig. [‡] | P1IN.4 | Unused [§] CCI0A [†] | P1IE.4 | P1IFG.4 | P1IES.4 |
| P1SEL.5 | P1DIR.5 | P1DIR.5 | P1OUT.5 | ACLK | P1IN.5 | TACLK [†] | P1IE.5 | P1IFG.5 | P1IES.5 |

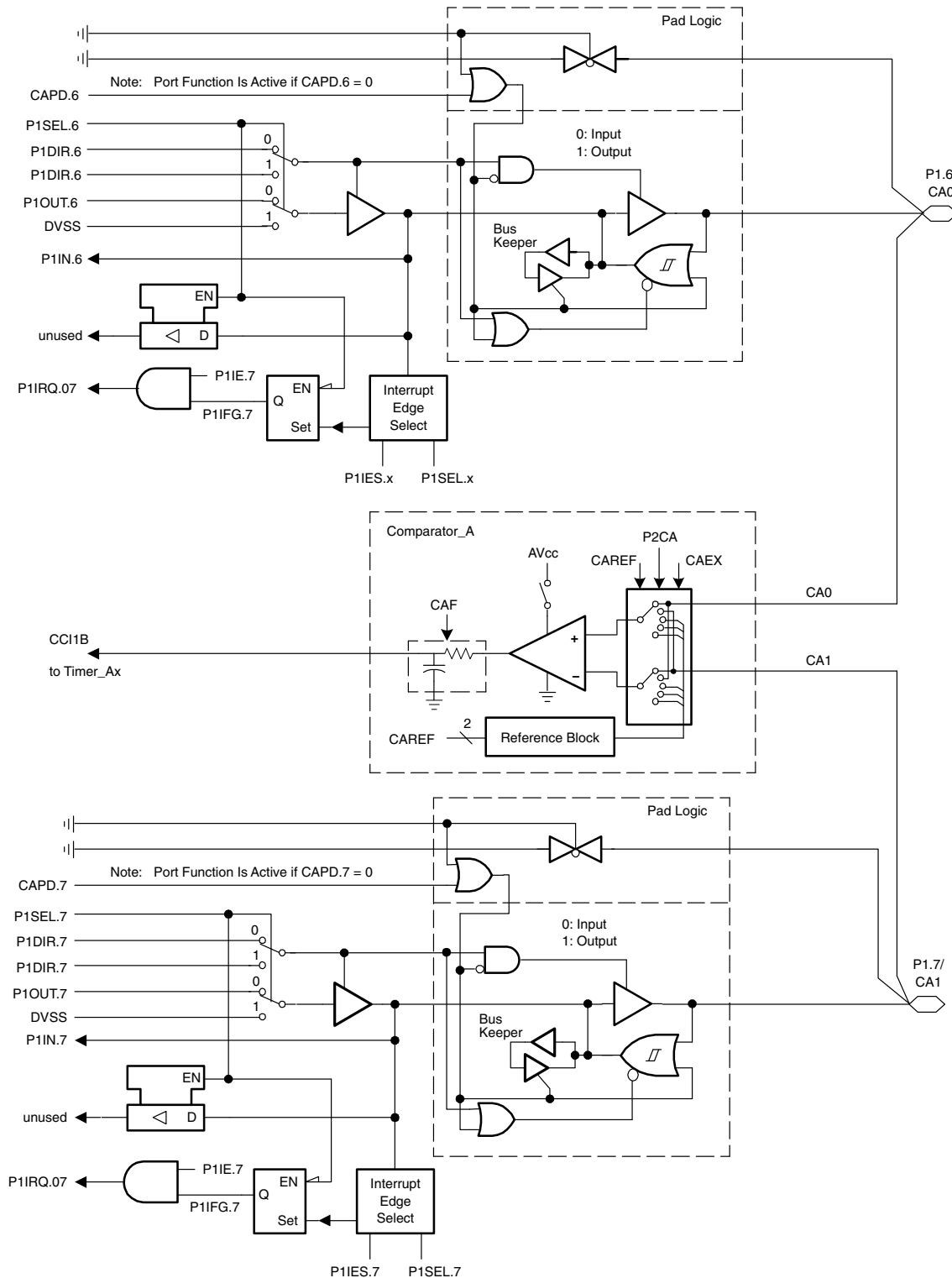
[†] Timer_A3/Timer0_A3

[‡] Timer1_A5 (MSP430x415, MSP430x417 only)

[§] MSP430x412, MSP430x413 only

APPLICATION INFORMATION

Port P1, P1.6, P1.7 input/output with Schmitt trigger

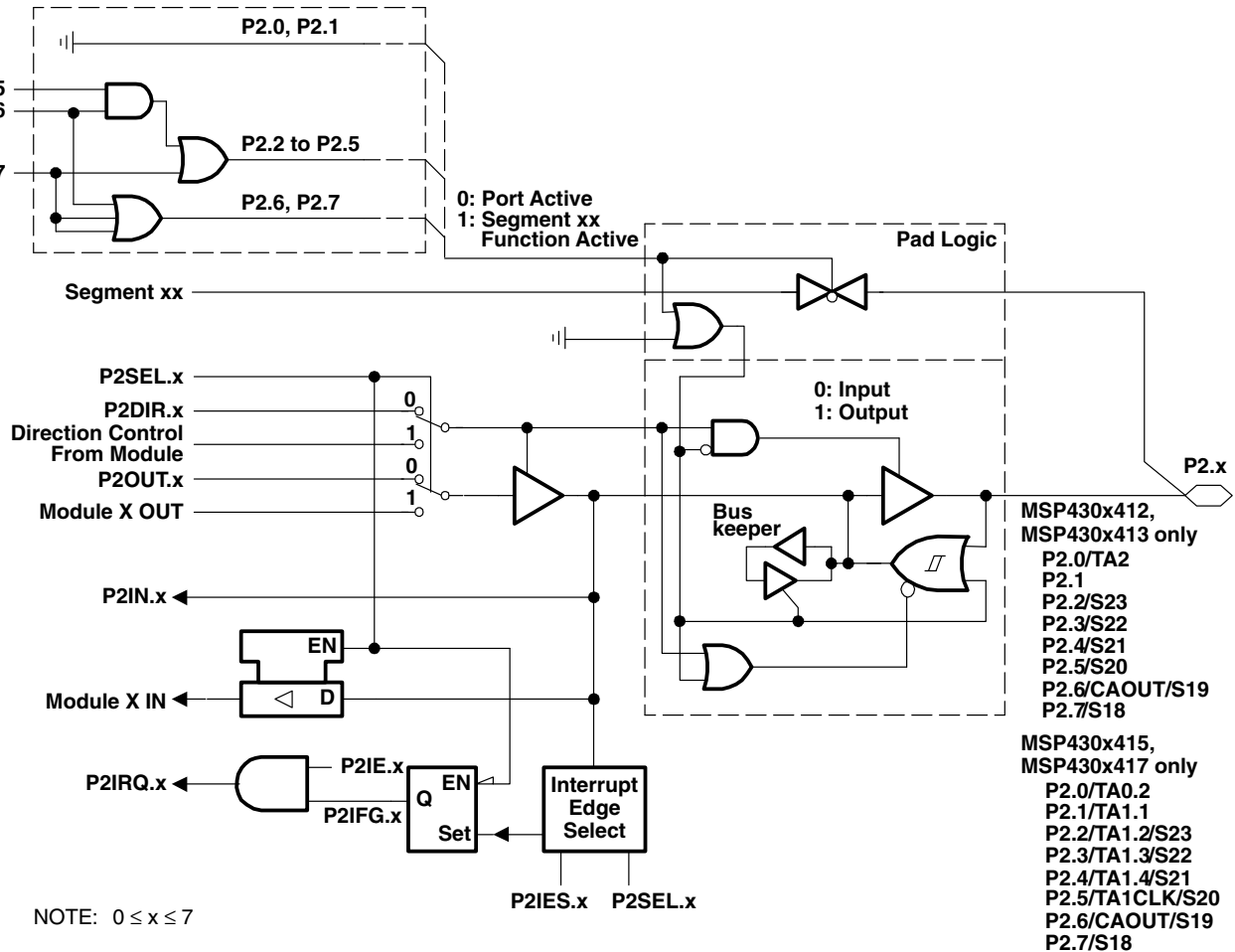


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APPLICATION INFORMATION

port P2, P2.0 to P2.7, input/output with Schmitt trigger



NOTE: $0 \leq x \leq 7$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x |
|---------|---------|-------------------------------|---------|---|--------|--|--------|---------|---------|
| P2SEL.0 | P2DIR.0 | P2DIR.0 | P2OUT.0 | Out2 Sig. [†] | P2IN.0 | CC12A [†] | P2IE.0 | P2IFG.0 | P2IES.0 |
| P2SEL.1 | P2DIR.1 | P2DIR.1 | P2OUT.1 | DVSS [§] Out1 Sig. [‡] | P2IN.1 | Unused [§] CC11A [†] | P2IE.1 | P2IFG.1 | P2IES.1 |
| P2SEL.2 | P2DIR.2 | P2DIR.2 | P2OUT.2 | DVSS [§] Out2 Sig. [‡] | P2IN.2 | Unused [§] CC12A [†] | P2IE.2 | P2IFG.2 | P2IES.2 |
| P2SEL.3 | P2DIR.3 | P2DIR.3 | P2OUT.3 | DVSS [§] Out3 Sig. [‡] | P2IN.3 | Unused [§] CC13A [†] | P2IE.3 | P2IFG.3 | P2IES.3 |
| P2SEL.4 | P2DIR.4 | P2DIR.4 | P2OUT.4 | DVSS [§] Out4 Sig. [‡] | P2IN.4 | Unused [§] CC14A [†] | P2IE.4 | P2IFG.4 | P2IES.4 |
| P2SEL.5 | P2DIR.5 | P2DIR.5 | P2OUT.5 | DVSS | P2IN.5 | Unused [§] TA1CLK [†] | P2IE.5 | P2IFG.5 | P2IES.5 |
| P2SEL.6 | P2DIR.6 | P2DIR.6 | P2OUT.6 | CAOUT | P2IN.6 | Unused | P2IE.6 | P2IFG.6 | P2IES.6 |
| P2SEL.7 | P2DIR.7 | P2DIR.7 | P2OUT.7 | DVSS | P2IN.7 | Unused | P2IE.7 | P2IFG.7 | P2IES.7 |

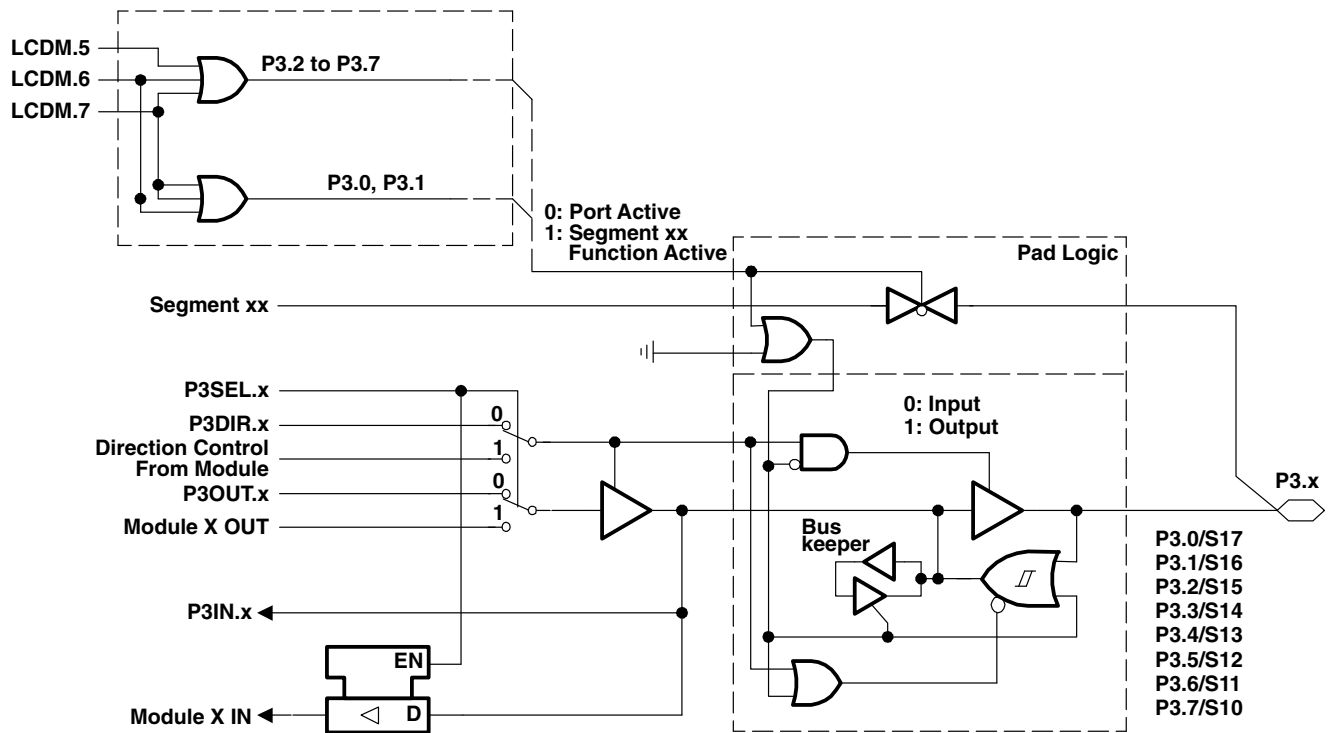
[†] Timer_A3/Timer0_A3

[‡] Timer1_A5 (MSP430x415, MSP430x417 only)

[§] MSP430x412, MSP430x413 only

APPLICATION INFORMATION

port P3, P3.0 to P3.7, input/output with Schmitt trigger



NOTE: $0 \leq x \leq 7$

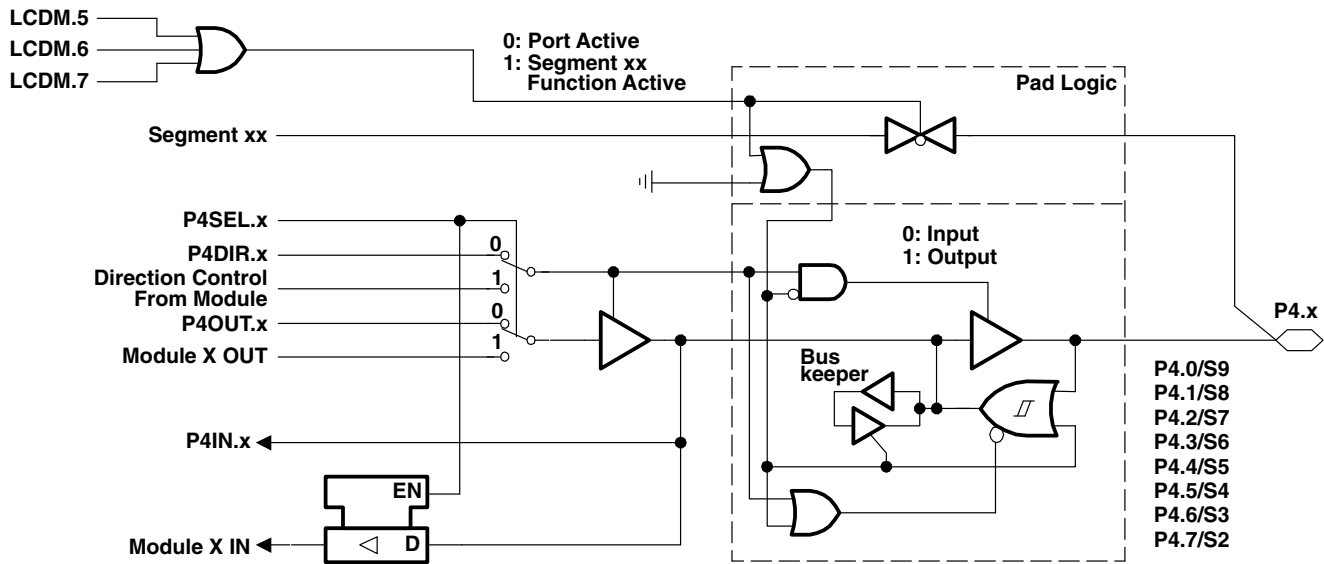
| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P3SEL.0 | P3DIR.0 | P3DIR.0 | P3OUT.0 | DVSS | P3IN.0 | Unused |
| P3SEL.1 | P3DIR.1 | P3DIR.1 | P3OUT.1 | DVSS | P3IN.1 | Unused |
| P3SEL.2 | P3DIR.2 | P3DIR.2 | P3OUT.2 | DVSS | P3IN.2 | Unused |
| P3SEL.3 | P3DIR.3 | P3DIR.3 | P3OUT.3 | DVSS | P3IN.3 | Unused |
| P3SEL.4 | P3DIR.4 | P3DIR.4 | P3OUT.4 | DVSS | P3IN.4 | Unused |
| P3SEL.5 | P3DIR.5 | P3DIR.5 | P3OUT.5 | DVSS | P3IN.5 | Unused |
| P3SEL.6 | P3DIR.6 | P3DIR.6 | P3OUT.6 | DVSS | P3IN.6 | Unused |
| P3SEL.7 | P3DIR.7 | P3DIR.7 | P3OUT.7 | DVSS | P3IN.7 | Unused |

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APPLICATION INFORMATION

port P4, P4.0 to P4.7, input/output with Schmitt trigger

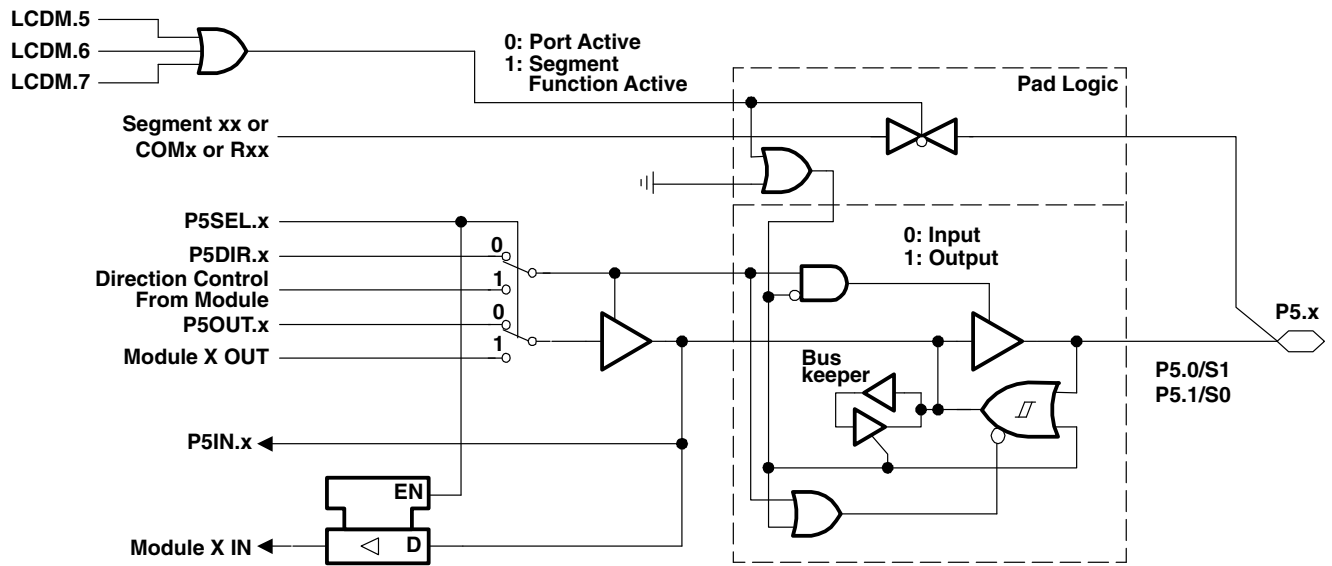


NOTE: $0 \leq x \leq 7$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P4SEL.0 | P4DIR.0 | P4DIR.0 | P4OUT.0 | DVSS | P4IN.0 | Unused |
| P4SEL.1 | P4DIR.1 | P4DIR.1 | P4OUT.1 | DVSS | P4IN.1 | Unused |
| P4SEL.2 | P4DIR.2 | P4DIR.2 | P4OUT.2 | DVSS | P4IN.2 | Unused |
| P4SEL.3 | P4DIR.3 | P4DIR.3 | P4OUT.3 | DVSS | P4IN.3 | Unused |
| P4SEL.4 | P4DIR.4 | P4DIR.4 | P4OUT.4 | DVSS | P4IN.4 | Unused |
| P4SEL.5 | P4DIR.5 | P4DIR.5 | P4OUT.5 | DVSS | P4IN.5 | Unused |
| P4SEL.6 | P4DIR.6 | P4DIR.6 | P4OUT.6 | DVSS | P4IN.6 | Unused |
| P4SEL.7 | P4DIR.7 | P4DIR.7 | P4OUT.7 | DVSS | P4IN.7 | Unused |

APPLICATION INFORMATION

port P5, P5.0, P5.1, input/output with Schmitt trigger



NOTE: x = 0, 1

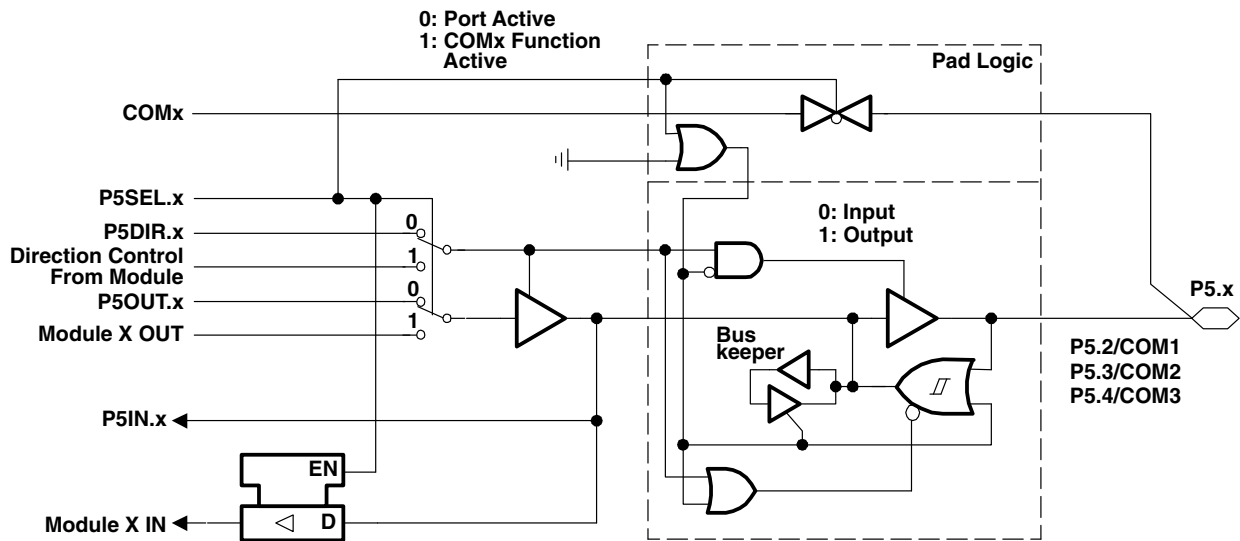
| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | Segment |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|---------|
| P5SEL.0 | P5DIR.0 | P5DIR.0 | P5OUT.0 | DVSS | P5IN.0 | Unused | S1 |
| P5SEL.1 | P5DIR.1 | P5DIR.1 | P5OUT.1 | DVSS | P5IN.1 | Unused | S0 |

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APPLICATION INFORMATION

port P5, P5.2 to P5.4, input/output with Schmitt trigger



NOTE: $2 \leq x \leq 4$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | COMx |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|------|
| P5SEL.2 | P5DIR.2 | P5DIR.2 | P5OUT.2 | DVSS | P5IN.2 | Unused | COM1 |
| P5SEL.3 | P5DIR.3 | P5DIR.3 | P5OUT.3 | DVSS | P5IN.3 | Unused | COM2 |
| P5SEL.4 | P5DIR.4 | P5DIR.4 | P5OUT.4 | DVSS | P5IN.4 | Unused | COM3 |

NOTE:

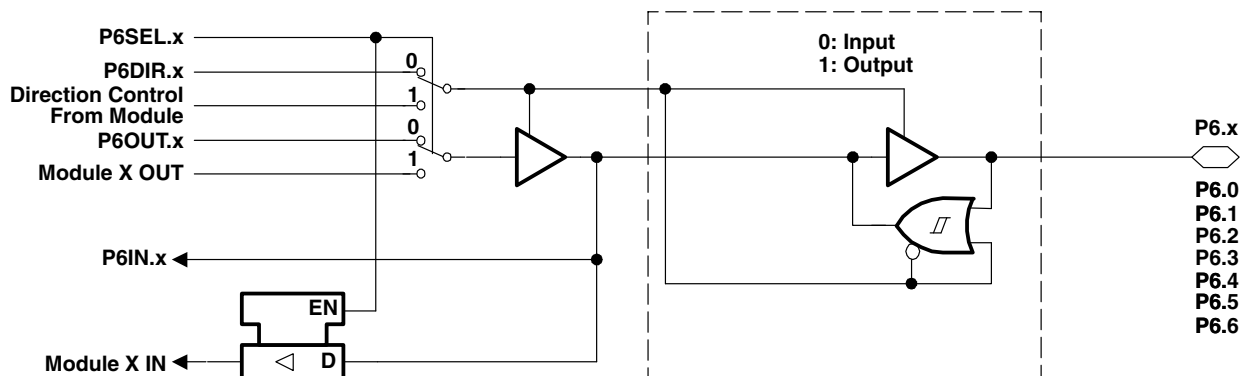
The direction control bits P5SEL.2, P5SEL.3, and P5SEL.4 are used to distinguish between port and common functions. Note that a 4MUX LCD requires all common signals COM3 to COM0, a 3MUX LCD requires COM2 to COM0, 2MUX LCD requires COM1 to COM0, and a static LCD requires only COM0.

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APPLICATION INFORMATION

port P6, P6.0 to P6.6, input/output with Schmitt trigger

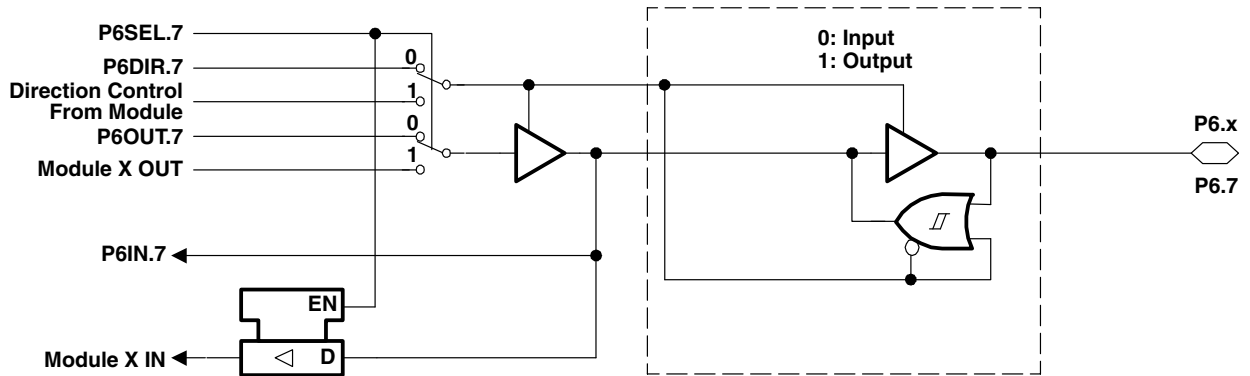


NOTE: $0 \leq x \leq 6$

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P6SEL.0 | P6DIR.0 | P6DIR.0 | P6OUT.0 | DVSS | P6IN.0 | Unused |
| P6SEL.1 | P6DIR.1 | P6DIR.1 | P6OUT.1 | DVSS | P6IN.1 | Unused |
| P6SEL.2 | P6DIR.2 | P6DIR.2 | P6OUT.2 | DVSS | P6IN.2 | Unused |
| P6SEL.3 | P6DIR.3 | P6DIR.3 | P6OUT.3 | DVSS | P6IN.3 | Unused |
| P6SEL.4 | P6DIR.4 | P6DIR.4 | P6OUT.4 | DVSS | P6IN.4 | Unused |
| P6SEL.5 | P6DIR.5 | P6DIR.5 | P6OUT.5 | DVSS | P6IN.5 | Unused |
| P6SEL.6 | P6DIR.6 | P6DIR.6 | P6OUT.6 | DVSS | P6IN.6 | Unused |

APPLICATION INFORMATION

port P6, P6.7 input/output with Schmitt trigger (MSP430x412/413 only)



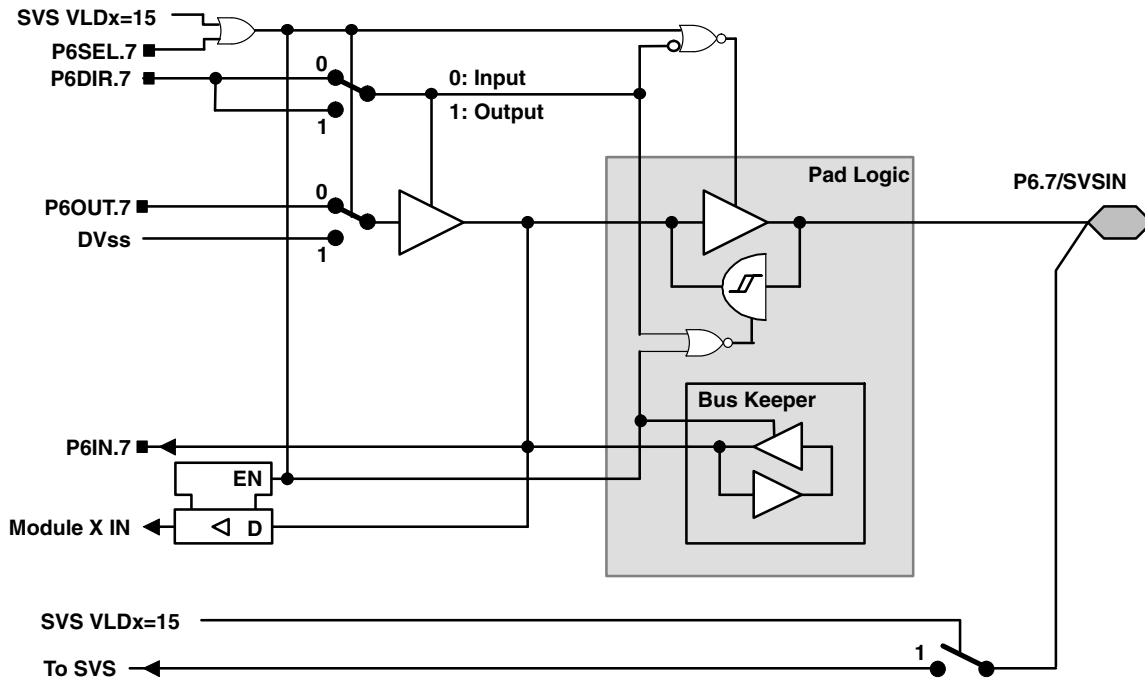
| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|
| P6SEL.7 | P6DIR.7 | P6DIR.7 | P6OUT.7 | DVSS | P6IN.7 | Unused |

MSP430x41x MIXED SIGNAL MICROCONTROLLER

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APPLICATION INFORMATION

port P6, P6.7 input/output with Schmitt trigger (MSP430F415/417 only)



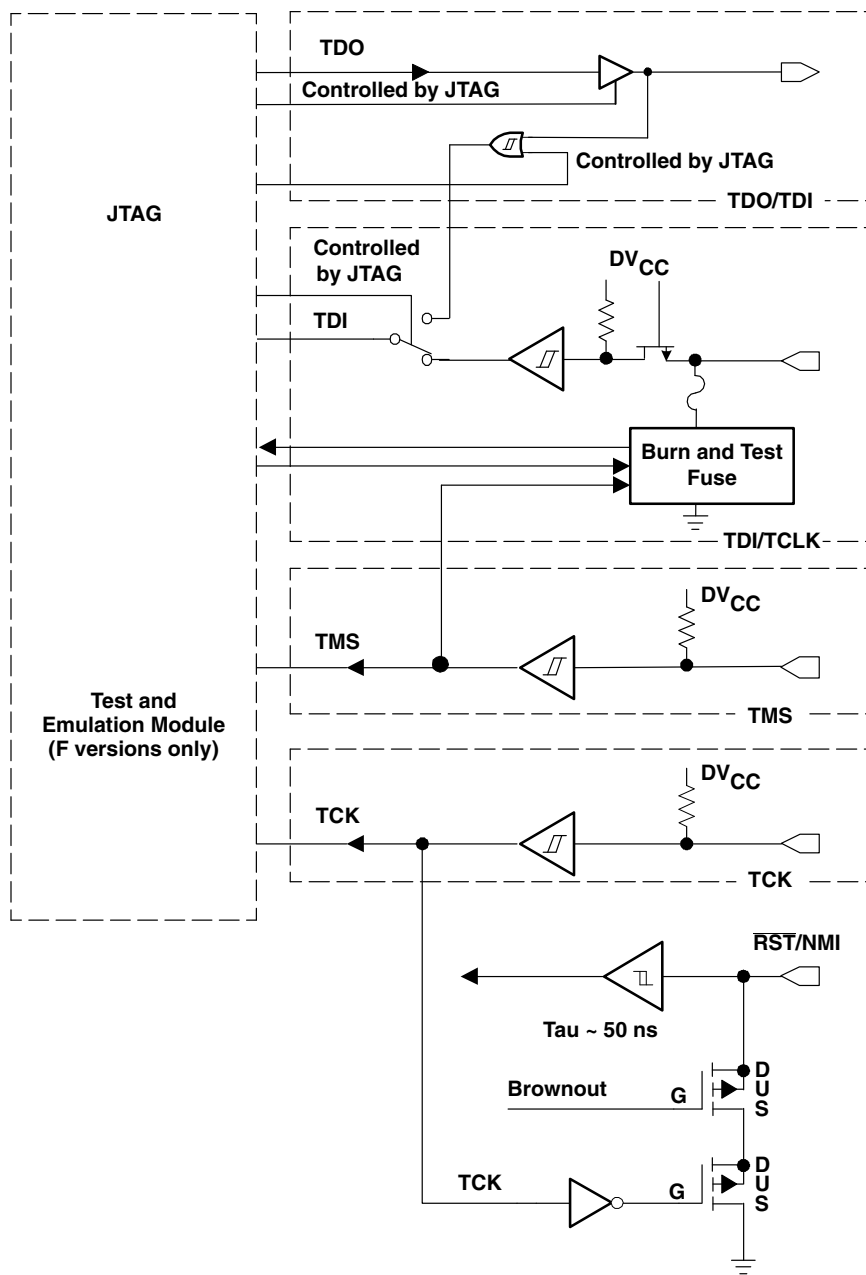
NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 μ A.

Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, if an analog signal is applied to the pin.

| SWS VLDx = 15 | P6SEL.7 | P6DIR.7 | Port Function |
|---------------|---------|---------|---------------|
| 0 | 0 | 0 | P6.7 Input |
| 0 | 0 | 1 | P6.7 Output |
| 0 | 1 | X | Undefined |
| 1 | X | X | SVSIN |

APPLICATION INFORMATION

JTAG pins (TMS, TCK, TDI/TCLK, TDO/TDI), input/output with Schmitt trigger or output



APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1.8 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 22). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

The JTAG pins are terminated internally, and therefore do not require external termination.

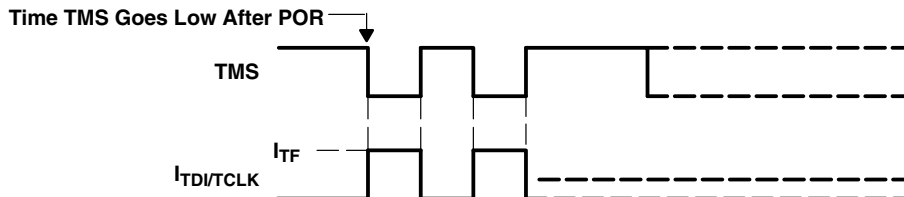


Figure 22. Fuse Check Mode Current, MSP430C41x, MSP430F41x

Data Sheet Revision History

| Literature Number | Summary |
|-------------------|--|
| SLAS340H | Updated functional block diagrams (page 4) Clarified test conditions in recommended operating conditions table (page 21) Split Supply voltage during program execution for MSP430x412/413 and MSP430x415/417 (page 21) Clarified test conditions for $I_{(LPM0)}$ in supply current into $AV_{CC} + DV_{CC}$ table (page 22) Added P2–P5 to leakage current table (page 23) Changed t_{CP_T} maximum value from 4 ms to 10 ms in Flash memory table (page 37) |
| SLAS340I | Changed all RTD package options for MSP430C41x to RGC package. |

NOTE: Page and figure numbers refer to the respective document revision.

Corrections to MSP430x41x Data Sheet (SLAS340J)

Document Being Updated: *MSP430x41x Mixed Signal Microcontroller*

Literature Number Being Updated: SLAS340J

Page Change or Add

- 40 In top left of the figure:
LCDM.5 should be changed to **bit 0 of LCDPx**, which is bit 5 of the LCDCTL register.
LCDM.6 should be changed to **bit 1 of LCDPx**, which is bit 6 of the LCDCTL register.
LCDM.7 should be changed to **bit 2 of LCDPx**, which is bit 7 of the LCDCTL register.
- 41 In top left of the figure:
LCDM.5 should be changed to **bit 0 of LCDPx**, which is bit 5 of the LCDCTL register.
LCDM.6 should be changed to **bit 1 of LCDPx**, which is bit 6 of the LCDCTL register.
LCDM.7 should be changed to **bit 2 of LCDPx**, which is bit 7 of the LCDCTL register.
- 42 In top left of the figure:
LCDM.5 should be changed to **bit 0 of LCDPx**, which is bit 5 of the LCDCTL register.
LCDM.6 should be changed to **bit 1 of LCDPx**, which is bit 6 of the LCDCTL register.
LCDM.7 should be changed to **bit 2 of LCDPx**, which is bit 7 of the LCDCTL register.
- 43 In top left of the figure:
LCDM.5 should be changed to **bit 0 of LCDPx**, which is bit 5 of the LCDCTL register.
LCDM.6 should be changed to **bit 1 of LCDPx**, which is bit 6 of the LCDCTL register.
LCDM.7 should be changed to **bit 2 of LCDPx**, which is bit 7 of the LCDCTL register.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F412IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F412 REV # | Samples |
| MSP430F412IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F412 REV # | Samples |
| MSP430F412IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F412 | Samples |
| MSP430F412IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F412 | Samples |
| MSP430F413IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F413 REV # | Samples |
| MSP430F413IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F413 REV # | Samples |
| MSP430F413IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F413 | Samples |
| MSP430F413IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F413 | Samples |
| MSP430F415IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F415 | Samples |
| MSP430F415IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F415 | Samples |
| MSP430F415IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F415 | Samples |
| MSP430F415IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F415 | Samples |
| MSP430F417IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F417 | Samples |
| MSP430F417IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F417 | Samples |
| MSP430F417IRTDR | ACTIVE | VQFN | RTD | 64 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F417 | Samples |
| MSP430F417IRTD | ACTIVE | VQFN | RTD | 64 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 85 | M430F417 | Samples |

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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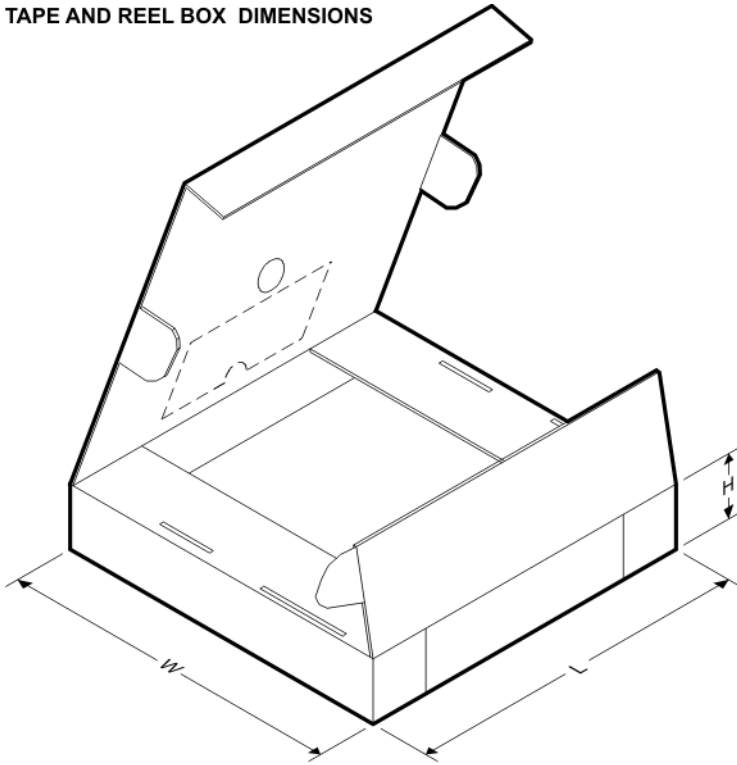
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F412IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F412IRTD | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F412IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F413IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F413IRTD | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F413IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F415IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F415IRTD | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F415IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F417IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430F417IRTD | VQFN | RTD | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| MSP430F417IRTD | VQFN | RTD | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

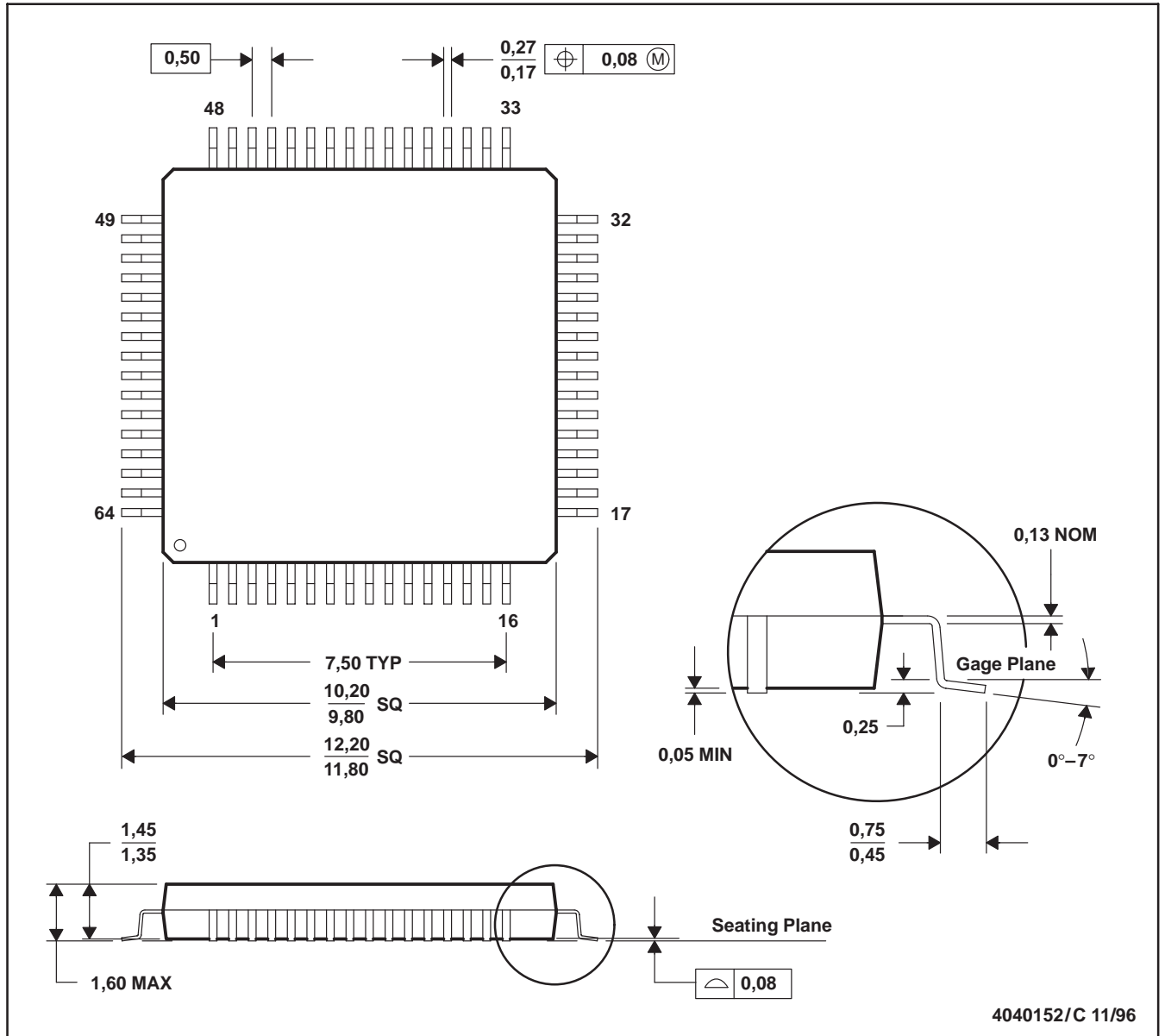
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F412IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F412IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F412IRTD | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F413IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F413IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F413IRTD | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F415IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F415IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F415IRTD | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F417IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430F417IRTDR | VQFN | RTD | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F417IRTD | VQFN | RTD | 64 | 250 | 210.0 | 185.0 | 35.0 |

PM (S-PQFP-G64)

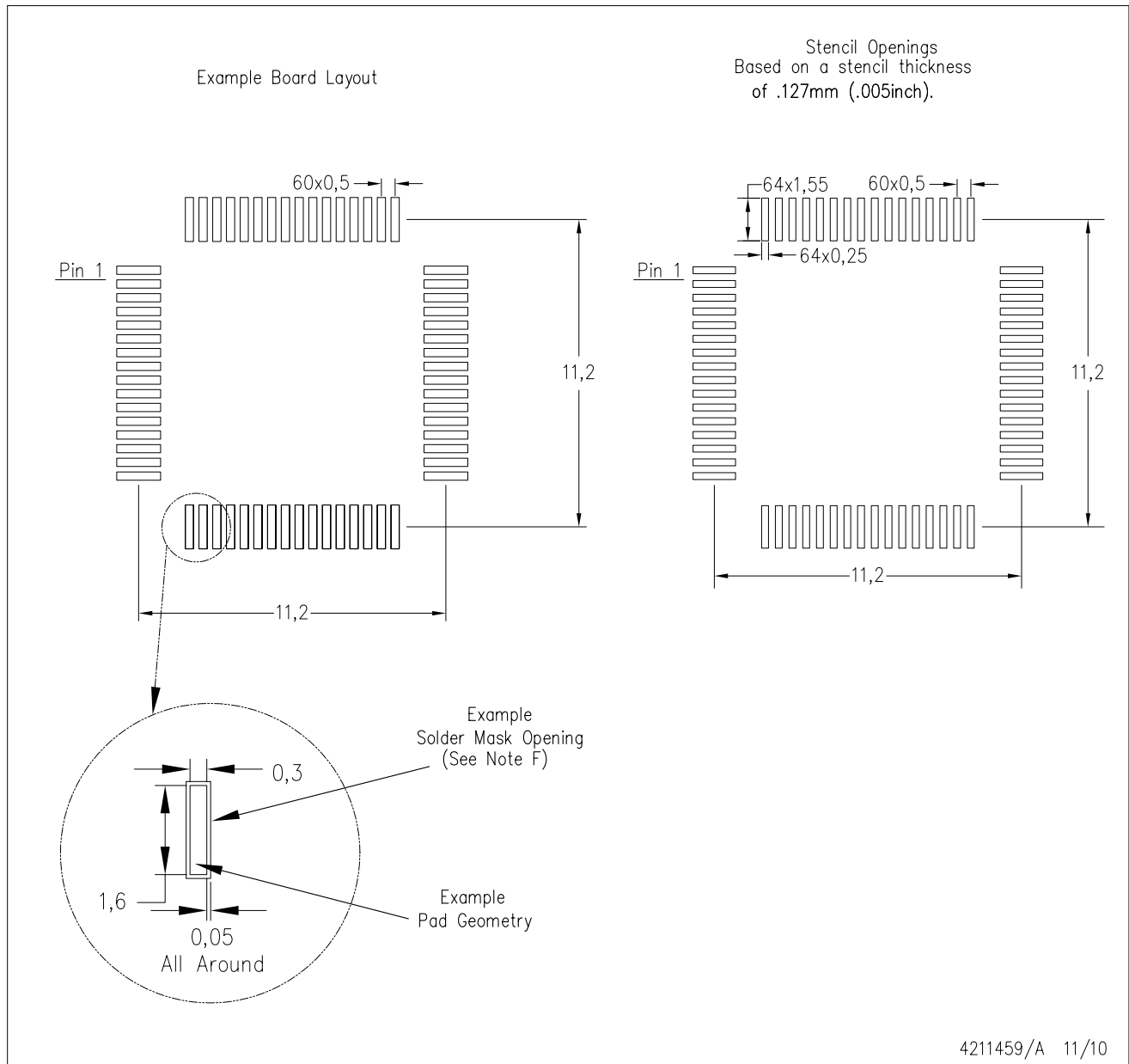
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



4211459/A 11/10

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

RTD 64

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



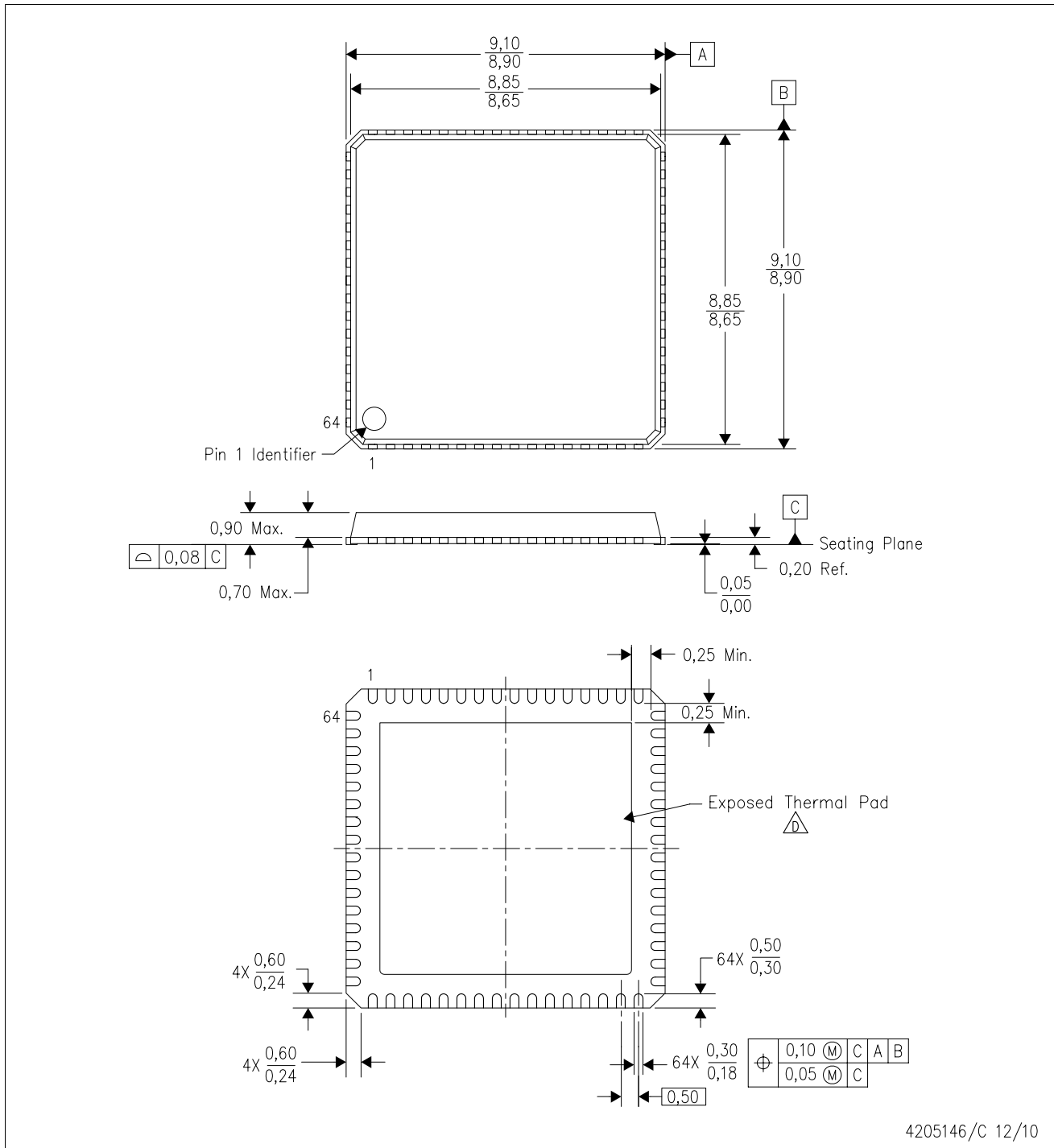
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.


4205146/D

MECHANICAL DATA

RTD (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

RTD (S-PVQFN-N64)

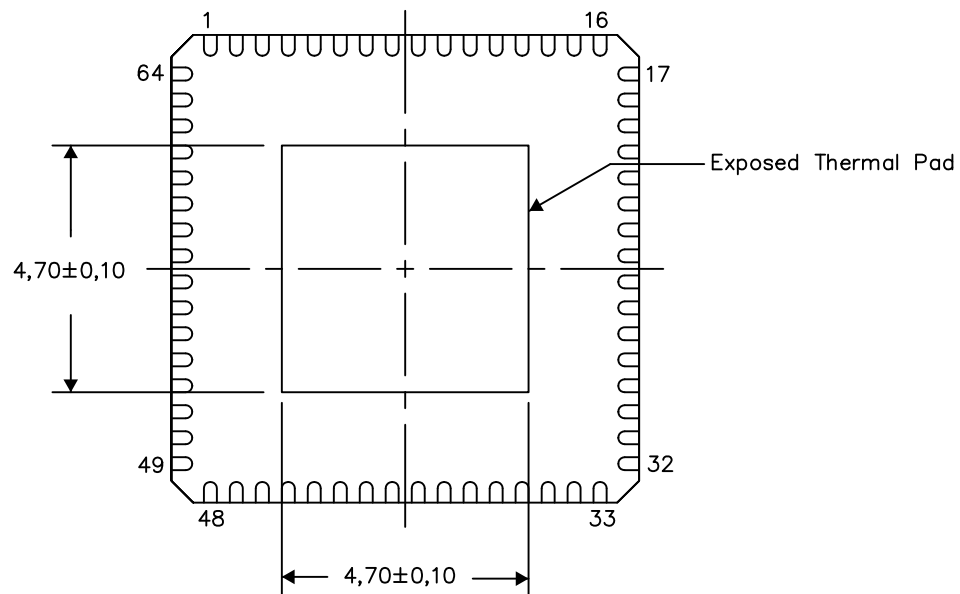
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

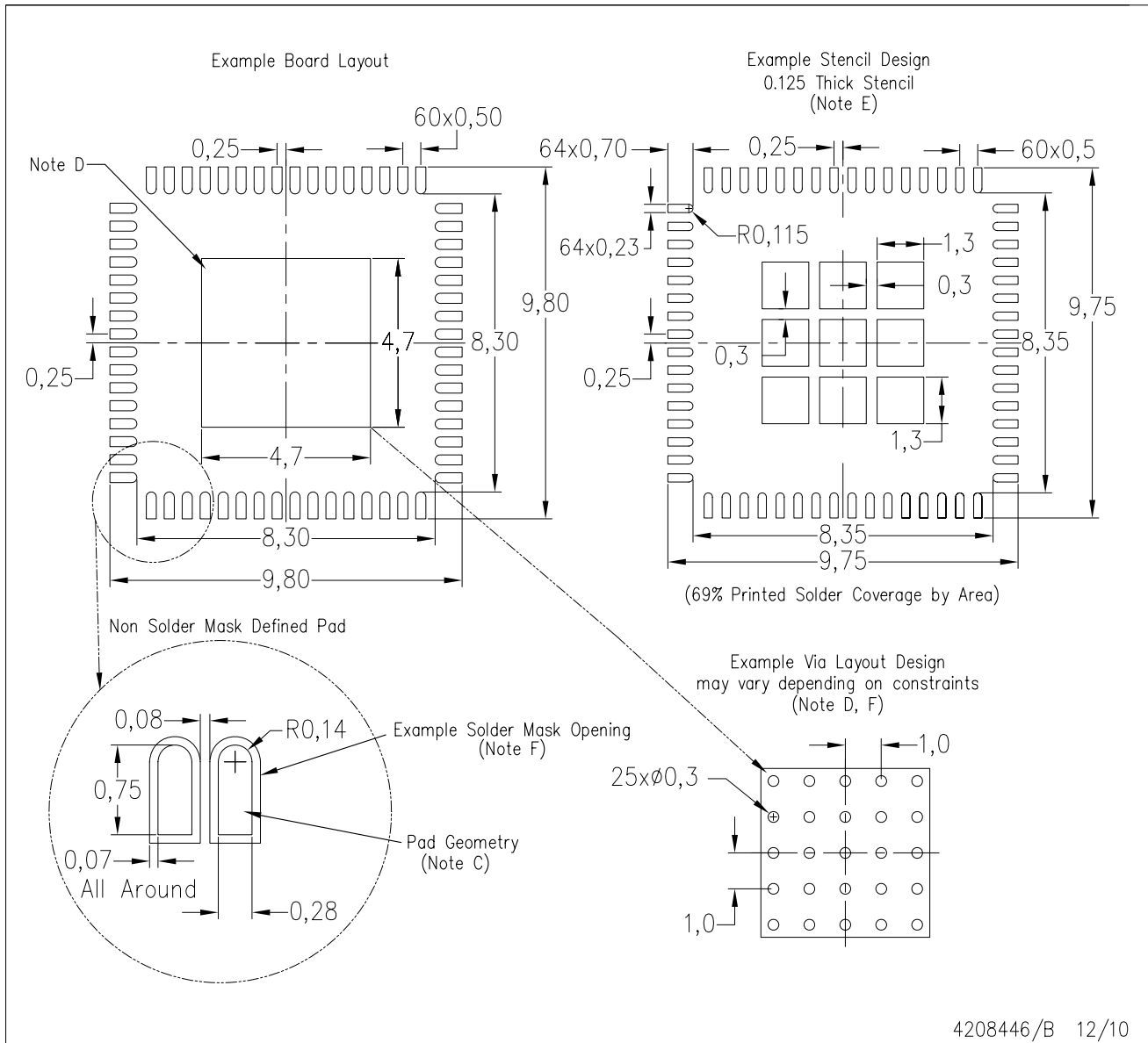


4206338-3/F 09/14

NOTE: A. All linear dimensions are in millimeters

RTD (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Package, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed into the thermal pad.

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