# THE DATASHEET OF

# MSP430F47193IPZR

www.win-source.net 0086-755-83957316

SLAS626C – OCTOBER 2008 – REVISED MARCH 2011

- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode: 350 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.1 μA**
  - **Off Mode (RAM Retention): 0.2 μA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Three-Channel Internal DMA**
- **Three, Six or Seven 16-Bit Sigma-Delta Analog-to-Digital (A/D) Converters With Differential PGA Inputs**
- **16-Bit Timer_B With Three Capture/Compare-With-Shadow Registers**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator**
- **Four Universal Serial Communication Interface (USCI) Modules**
  - **USCI_A0 and USCI_A1**
    - **Enhanced UART Supporting Auto-Baudrate Detection**
    - **IrDA Encoder and Decoder**
    - **Synchronous SPI**
  - **USCI_B0 and USCI_B1**
    - **I2C**
    - **Synchronous SPI**
- **Integrated LCD Driver With Contrast Control for Up to 160 Segments**
- **Basic Timer With Real-Time Clock Feature**
- **32-Bit Hardware Multiplier**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On-Chip Emulation Module**
- **Family Members Include**
  - **MSP430F47163: 92KB Flash, 4KB RAM, 3 Sigma-Delta ADCs**
  - **MSP430F47173: 92KB Flash, 8KB RAM, 3 Sigma-Delta ADCs**
  - **MSP430F47183: 116KB Flash, 8KB RAM, 3 Sigma-Delta ADCs**
  - **MSP430F47193: 120KB Flash, 4KB RAM, 3 Sigma-Delta ADCs**
  - **MSP430F47126: 56KB Flash, 4KB RAM, 6 Sigma-Delta ADCs**
  - **MSP430F47166: 92KB Flash, 4KB RAM, 6 Sigma-Delta ADCs**
  - **MSP430F47176: 92KB Flash, 8KB RAM, 6 Sigma-Delta ADCs**
  - **MSP430F47186: 116KB Flash, 8KB RAM, 6 Sigma-Delta ADCs**
  - **MSP430F47196: 120KB Flash, 4KB RAM, 6 Sigma-Delta ADCs**
  - **MSP430F47127: 56KB Flash, 4KB RAM, 7 Sigma-Delta ADCs**
  - **MSP430F47167: 92KB Flash, 4KB RAM, 7 Sigma-Delta ADCs**
  - **MSP430F47177: 92KB Flash, 8KB RAM, 7 Sigma-Delta ADCs**
  - **MSP430F47187: 116KB Flash, 8KB RAM, 7 Sigma-Delta ADCs**
  - **MSP430F47197: 120KB Flash, 4KB RAM, 7 Sigma-Delta ADCs**
- **Available in a 100-Pin Plastic Quad Flatpack (QFP) Package**
- **For Complete Module Descriptions, See the *MSP430x4xx Family User's Guide*, Literature Number SLAU056**
- **For E-Meter Reference Design and Software, See *Implementation of a Three-Phase Electronic Watt-Hour Meter using the MSP430F471xx*, Literature Number SLAA409**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

Copyright © 2011, Texas Instruments Incorporated

## description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The devices feature a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6μs.

The MSP430F471xx series are microcontroller configurations targeted to single-phase and poly-phase electricity meters with three, six, or seven 16-bit sigma-delta A/D converters. Each channel has a differential input pair and programmable input gain. Also integrated are two 16-bit timers, four universal serial communication interfaces (USCI), DMA, 68 I/O pins, and a liquid crystal driver (LCD) with integrated contrast control.

**AVAILABLE OPTIONS**[†]

| $T_A$ | PACKAGED DEVICES[‡] |
|---|---|
| | PLASTIC 100-PIN QFP (PZ) |
| –40°C to 85°C | MSP430F47127IPZ<br>MSP430F47167IPZ<br>MSP430F47177IPZ<br>MSP430F47187IPZ<br>MSP430F47197IPZ |
| | MSP430F47126IPZ<br>MSP430F47166IPZ<br>MSP430F47176IPZ<br>MSP430F47186IPZ<br>MSP430F47196IPZ |
| | MSP430F47163IPZ<br>MSP430F47173IPZ<br>MSP430F47183IPZ<br>MSP430F47193IPZ |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

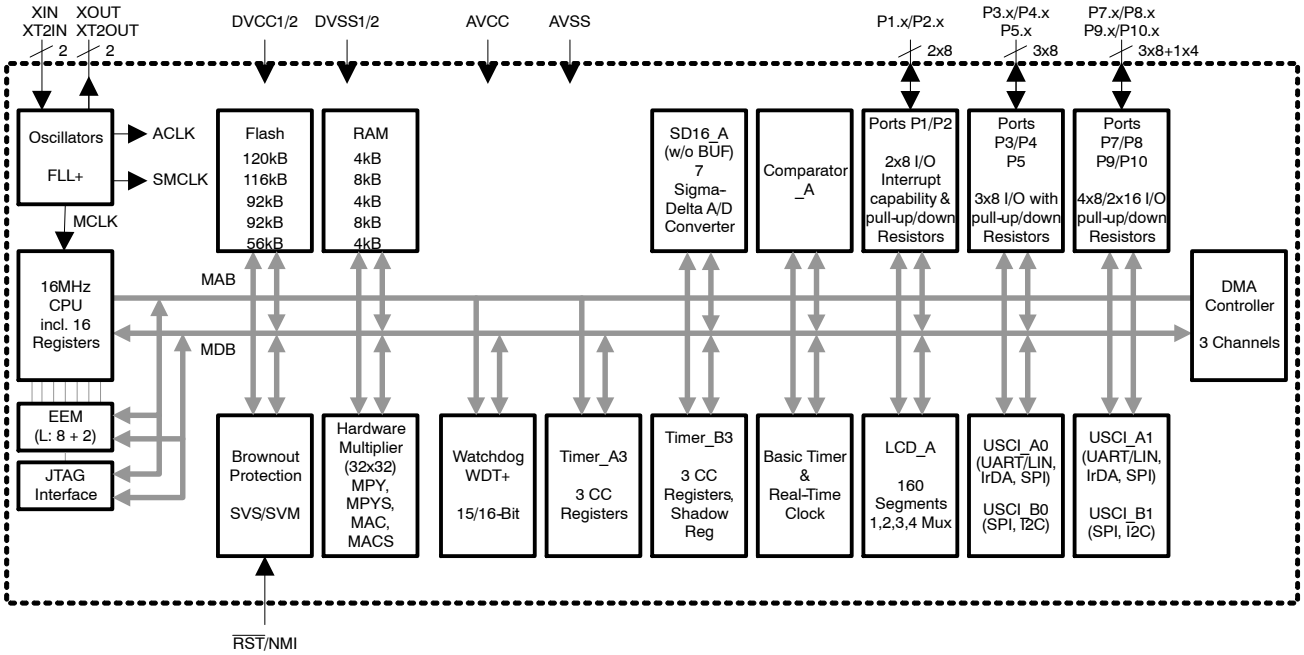
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## DEVELOPMENT TOOL SUPPORT

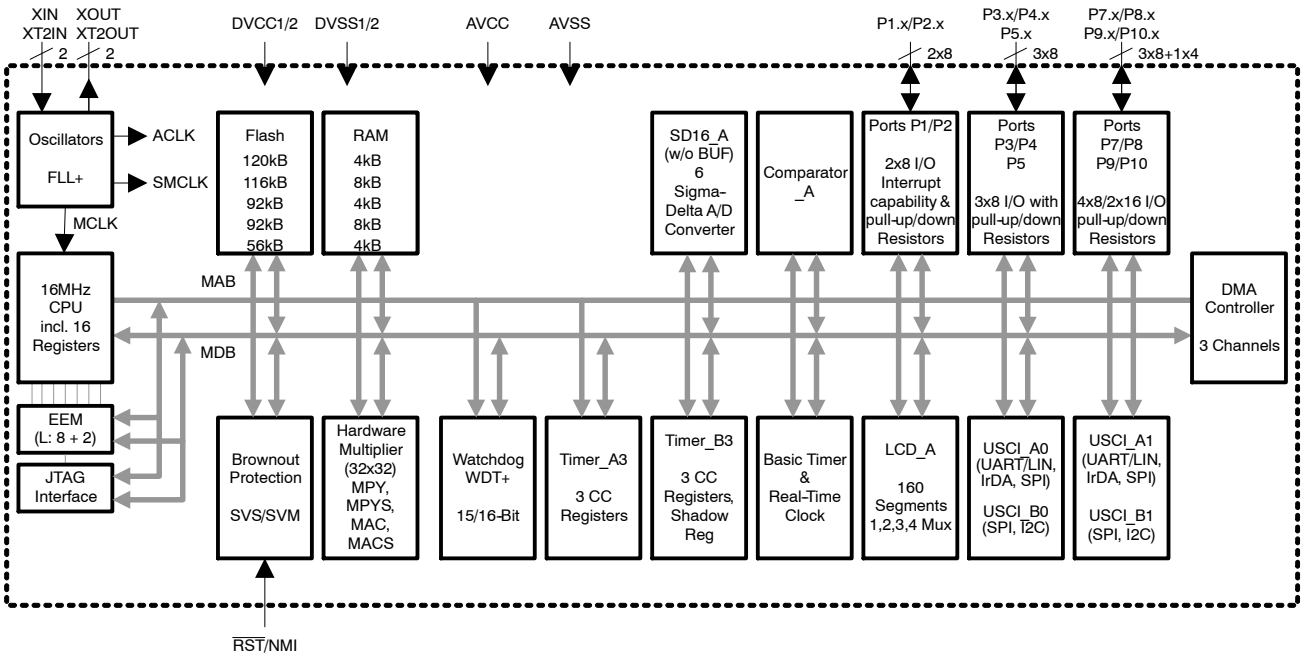
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U100
- Stand-Alone Target Board
  - MSP-TS430PZ100
- Production Programmer
  - MSP-GANG430

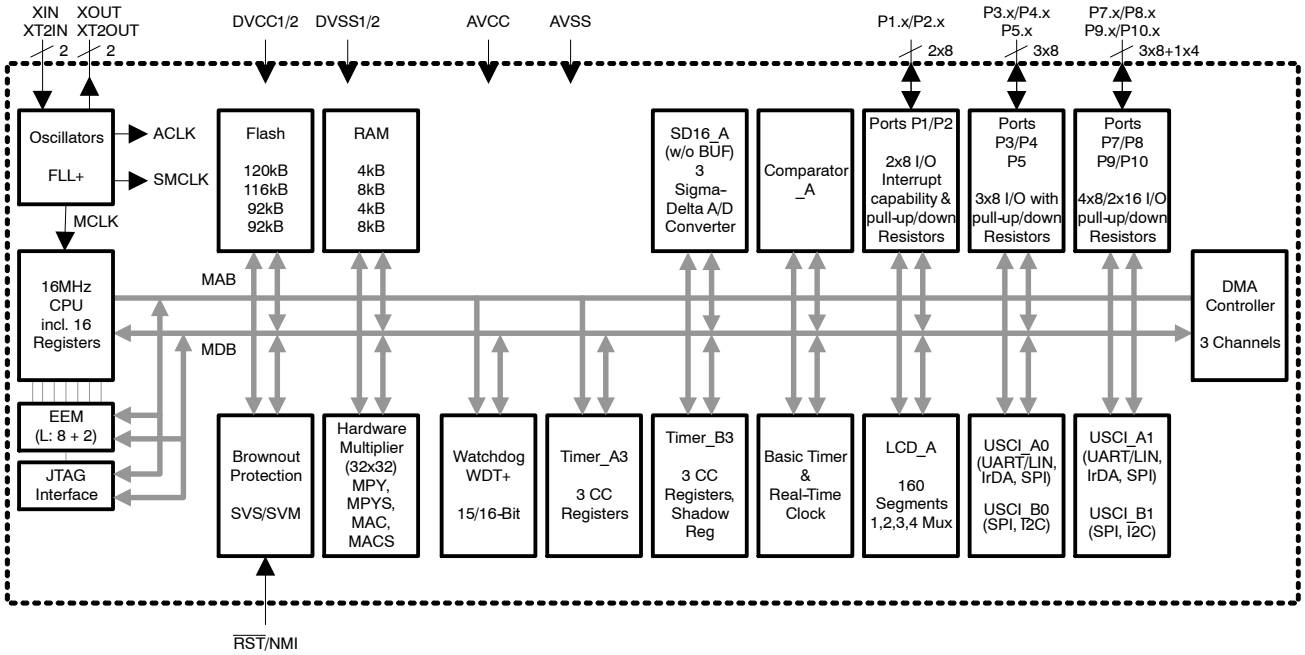
## functional block diagram, MSP430F471x7



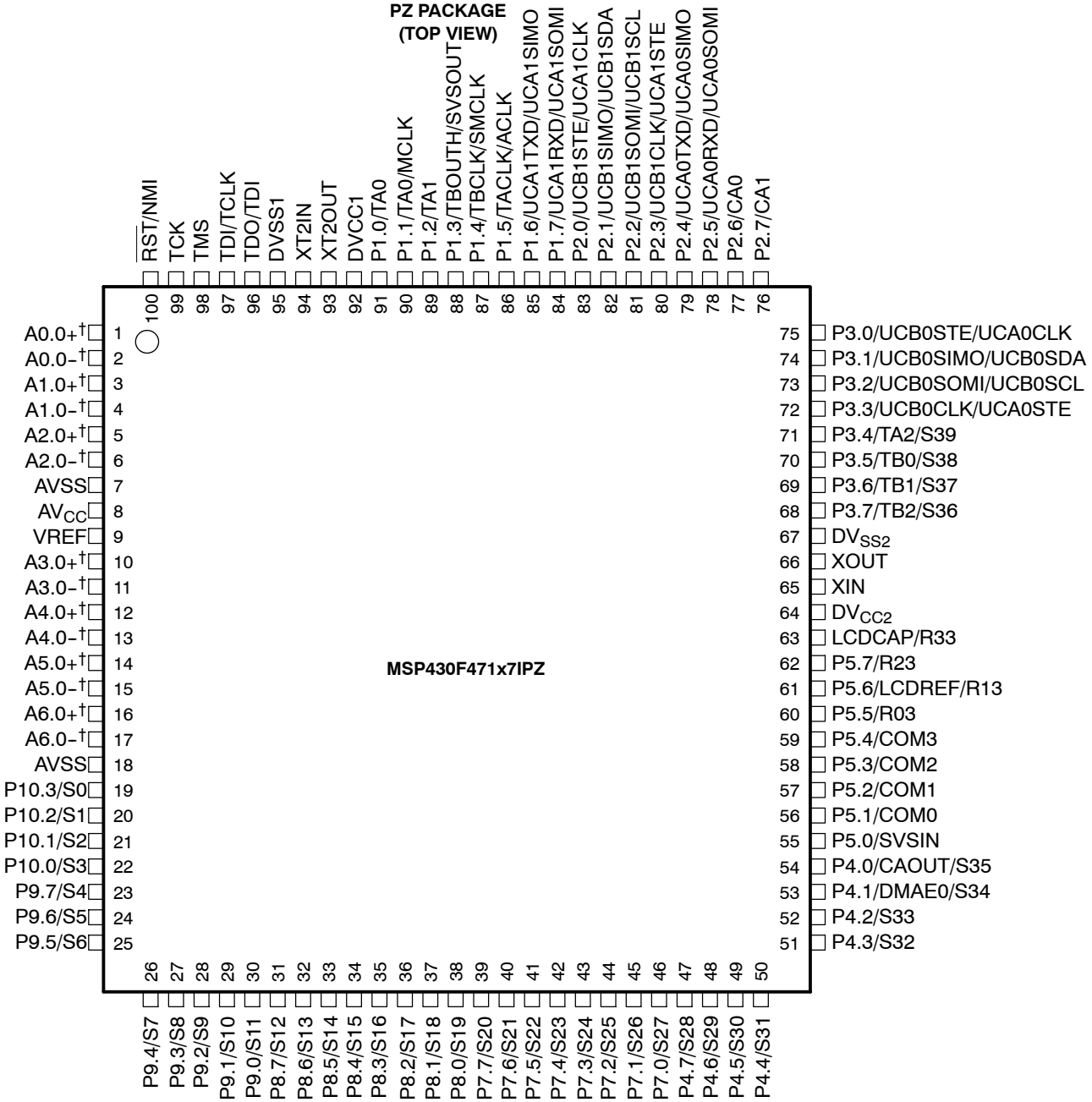

## functional block diagram, MSP430F471x6



## functional block diagram, MSP430F471x3

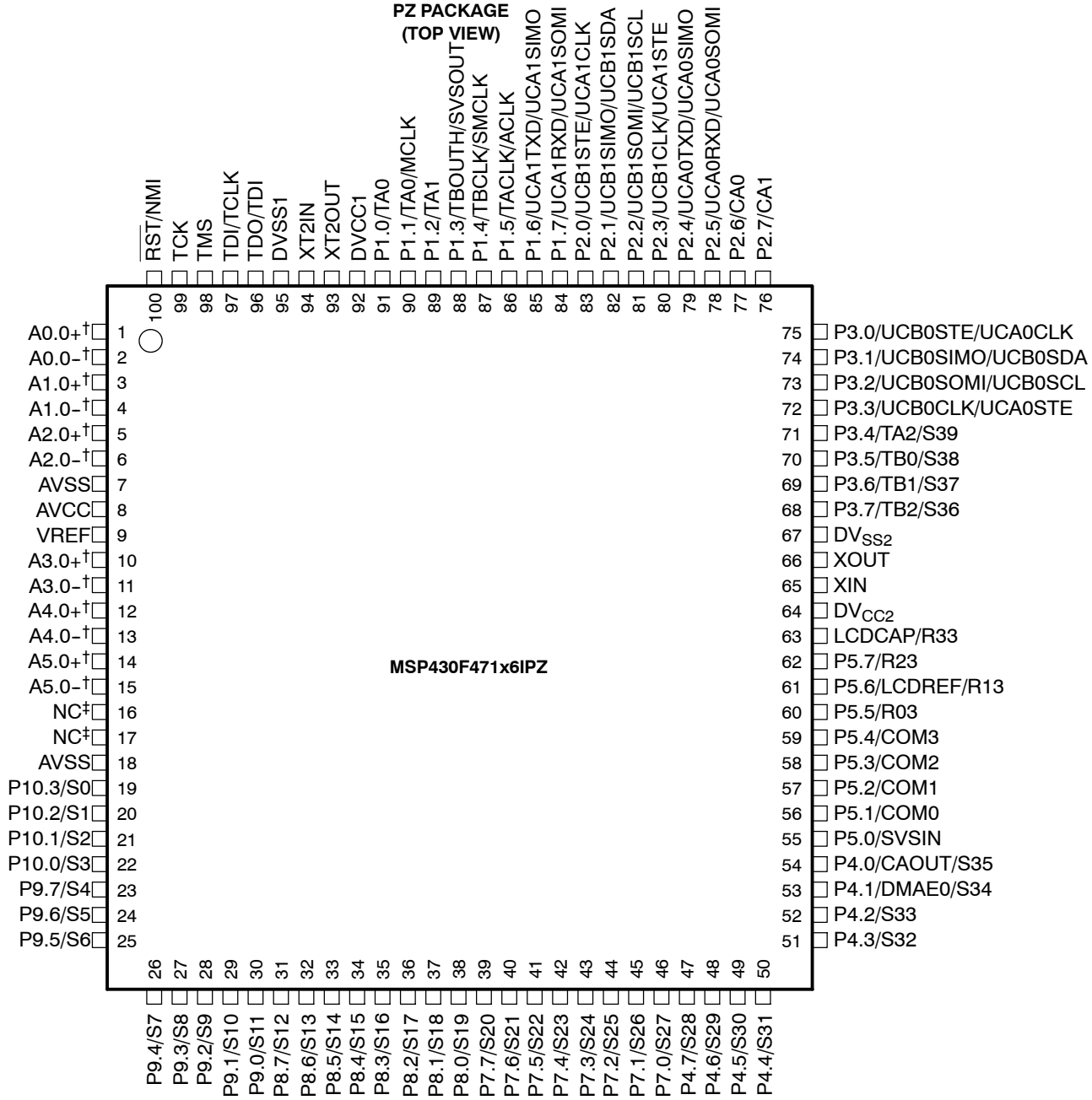


## pin designation, MSP430F471x7IPZ



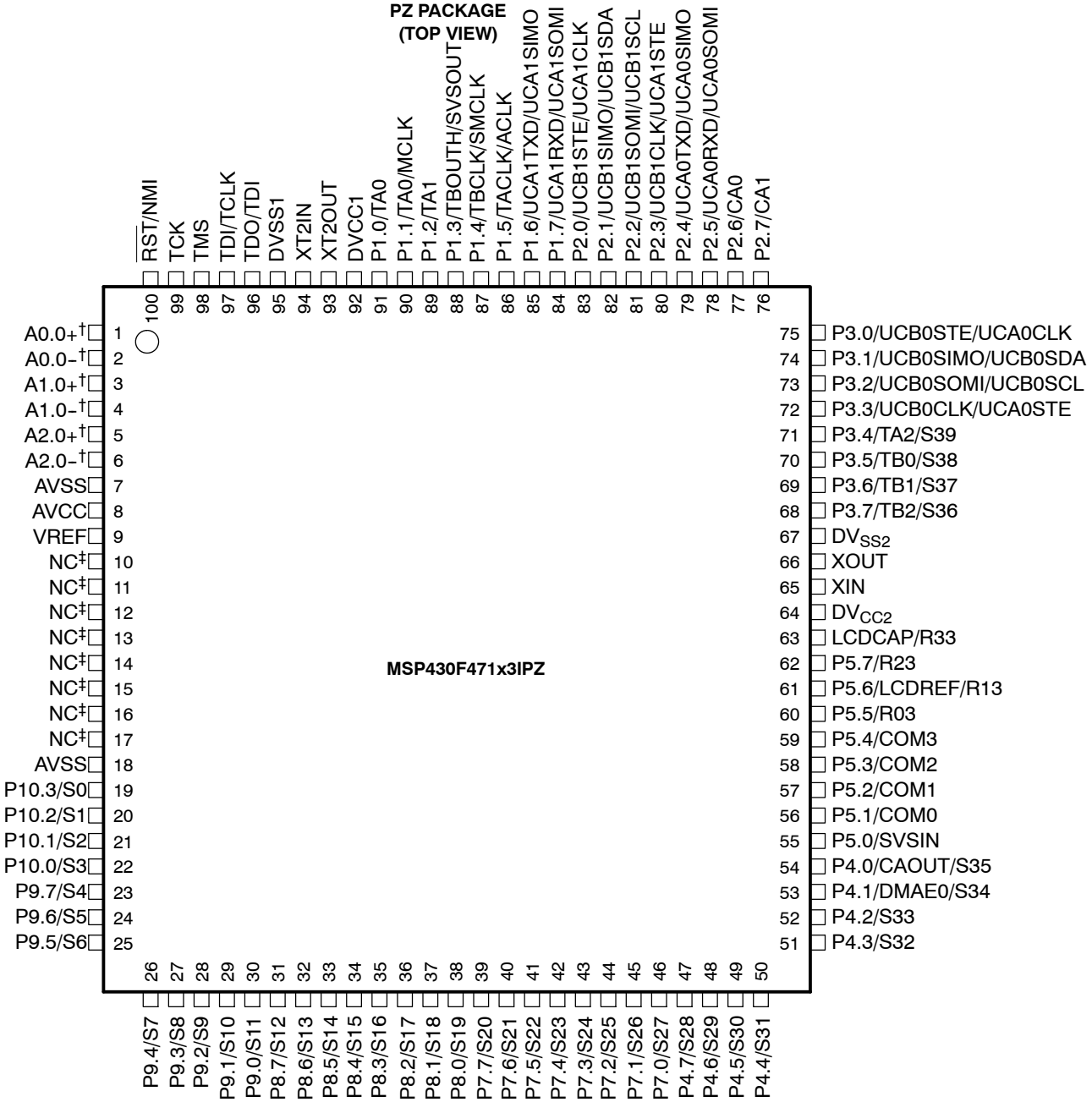

† It is recommended to short unused analog input pairs and connect them to analog ground (AVSS).

## pin designation, MSP430F471x6IPZ




† It is recommended to short unused analog input pairs and connect them to analog ground (AVSS).
‡ Connect pin to analog ground (AVSS).

## pin designation, MSP430F471x3IPZ




† It is recommended to short unused analog input pairs and connect them to analog ground (AVSS).
‡ Connect pin to analog ground (AVSS).

## Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| A0.0+ | 1 | I | SD16_A positive analog input A0.0 (see Note 1) |
| A0.0– | 2 | I | SD16_A negative analog input A0.0 (see Note 1) |
| A1.0+ | 3 | I | SD16_A positive analog input A1.0 (see Note 1) |
| A1.0– | 4 | I | SD16_A negative analog input A1.0 (see Note 1) |
| A2.0+ | 5 | I | SD16_A positive analog input A2.0 (see Note 1) |
| A2.0– | 6 | I | SD16_A negative analog input A2.0 (see Note 1) |
| $AV_{SS}$ | 7 | | Analog supply voltage, negative terminal. |
| $AV_{CC}$ | 8 | | Analog supply voltage, positive terminal. Must not power up prior to $DV_{CC1}/DV_{CC2}$. |
| $V_{REF}$ | 9 | I/O | Input for an external reference voltage / internal reference voltage output (can be used as mid-voltage) |
| A3.0+ (MSP430F471x6/7 only) | 10 | I | SD16_A positive analog input A3.0 (see Note 1) – Not connected in MSP430F471x3, connect pin to analog ground (AVSS). |
| A3.0– (MSP430F471x6/7 only) | 11 | I | SD16_A negative analog input A3.0 (see Note 1) – Not connected in MSP430F471x3, connect pin to analog ground (AVSS). |
| A4.0+ (MSP430F471x6/7 only) | 12 | I | SD16_A positive analog input A4.0 (see Note 1) – Not connected in MSP430F471x3, connect pin to analog ground (AVSS). |
| A4.0– (MSP430F471x6/7 only) | 13 | I | SD16_A negative analog input A4.0 (see Note 1) – Not connected in MSP430F471x3, connect pin to analog ground (AVSS). |
| A5.0+ (MSP430F471x6/7 only) | 14 | I | SD16_A positive analog input A5.0 (see Note 1) – Not connected in MSP430F471x3, connect pin to analog ground (AVSS). |
| A5.0– (MSP430F471x6/7 only) | 15 | I | SD16_A negative analog input A5.0 (see Note 1) – Not connected in MSP430F471x3, connect pin to analog ground (AVSS). |
| A6.0+ (MSP430F471x7 only) | 16 | I | SD16_A positive analog input A6.0 (see Note 1) – Not connected in MSP430F471x6, connect pin to analog ground (AVSS). |
| A6.0– (MSP430F471x7 only) | 17 | I | SD16_A negative analog input A6.0 (see Note 1) – Not connected in MSP430F471x6, connect pin to analog ground (AVSS). |
| $AV_{SS}$ | 18 | | Analog supply voltage, negative terminal. |
| P10.3/S0 | 19 | I/O | General-purpose digital I/O / LCD segment output 0 |
| P10.2/S1 | 20 | I/O | General-purpose digital I/O / LCD segment output 1 |
| P10.1/S2 | 21 | I/O | General-purpose digital I/O / LCD segment output 2 |
| P10.0/S3 | 22 | I/O | General-purpose digital I/O / LCD segment output 3 |
| P9.7/S4 | 23 | I/O | General-purpose digital I/O / LCD segment output 4 |
| P9.6/S5 | 24 | I/O | General-purpose digital I/O / LCD segment output 5 |
| P9.5/S6 | 25 | I/O | General-purpose digital I/O / LCD segment output 6 |
| P9.4/S7 | 26 | I/O | General-purpose digital I/O / LCD segment output 7 |
| P9.3/S8 | 27 | I/O | General-purpose digital I/O / LCD segment output 8 |
| P9.2/S9 | 28 | I/O | General-purpose digital I/O / LCD segment output 9 |
| P9.1/S10 | 29 | I/O | General-purpose digital I/O / LCD segment output 10 |
| P9.0/S11 | 30 | I/O | General-purpose digital I/O / LCD segment output 11 |
| P8.7/S12 | 31 | I/O | General-purpose digital I/O / LCD segment output 12 |
| P8.6/S13 | 32 | I/O | General-purpose digital I/O / LCD segment output 13 |
| P8.5/S14 | 33 | I/O | General-purpose digital I/O / LCD segment output 14 |
| P8.4/S15 | 34 | I/O | General-purpose digital I/O / LCD segment output 15 |
| P8.3/S16 | 35 | I/O | General-purpose digital I/O / LCD segment output 16 |
| P8.2/S17 | 36 | I/O | General-purpose digital I/O / LCD segment output 17 |
| P8.1/S18 | 37 | I/O | General-purpose digital I/O / LCD segment output 18 |

NOTES: 1. It is recommended to short unused analog input pairs and connect them to analog ground.

## Terminal Functions (continued)

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| P8.0/S19 | 38 | I/O | General-purpose digital I/O / LCD segment output 19 |
| P7.7/S20 | 39 | I/O | General-purpose digital I/O / LCD segment output 20 |
| P7.6/S21 | 40 | I/O | General-purpose digital I/O / LCD segment output 21 |
| P7.5/S22 | 41 | I/O | General-purpose digital I/O / LCD segment output 22 |
| P7.4/S23 | 42 | I/O | General-purpose digital I/O / LCD segment output 23 |
| P7.3/S24 | 43 | I/O | General-purpose digital I/O / LCD segment output 24 |
| P7.2/S25 | 44 | I/O | General-purpose digital I/O / LCD segment output 25 |
| P7.1/S26 | 45 | I/O | General-purpose digital I/O / LCD segment output 26 |
| P7.0/S27 | 46 | I/O | General-purpose digital I/O / LCD segment output 27 |
| P4.7/S28 | 47 | I/O | General-purpose digital I/O / LCD segment output 28 |
| P4.6/S29 | 48 | I/O | General-purpose digital I/O / LCD segment output 29 |
| P4.5/S30 | 49 | I/O | General-purpose digital I/O / LCD segment output 30 |
| P4.4/S31 | 50 | I/O | General-purpose digital I/O / LCD segment output 31 |
| P4.3/S32 | 51 | I/O | General-purpose digital I/O / LCD segment output 32 |
| P4.2/S33 | 52 | I/O | General-purpose digital I/O / LCD segment output 33 |
| P4.1/DMAE0/S34 | 53 | I/O | General-purpose digital I/O / DMA Channel 0 external trigger / LCD segment output 34 |
| P4.0/CAOUT/S35 | 54 | I/O | General-purpose digital I/O / Comparator_A output / LCD segment output 35 |
| P5.0/SVSIN | 55 | I/O | General-purpose digital I/O / analog input to supply voltage supervisor |
| P5.1/COM0 | 56 | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes. |
| P5.2/COM1 | 57 | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes. |
| P5.3/COM2 | 58 | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes. |
| P5.4/COM3 | 59 | I/O | General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes. |
| P5.5/R03 | 60 | I/O | General-purpose digital I/O / Input port of lowest analog LCD level (V5) |
| P5.6/LCDREF/R13 | 61 | I/O | General-purpose digital I/O / External reference voltage input for regulated LCD voltage / Input port of third most positive analog LCD level (V4 or V3) |
| P5.7/R23 | 62 | I/O | General-purpose digital I/O / Input port of second most positive analog LCD level (V2) |
| LCDCAP/R33 | 63 | I | LCD Capacitor connection / Input/output port of most positive analog LCD level (V1) |
| $DV_{CC2}$ | 64 | | Digital supply voltage, positive terminal. |
| XIN | 65 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 66 | O | Output terminal of crystal oscillator XT1 |
| $DV_{SS2}$ | 67 | | Digital supply voltage, negative terminal. |
| P3.7/TB2/S36 | 68 | I/O | General-purpose digital I/O / Timer_B3 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output / LCD segment output 36 |
| P3.6/TB1/S37 | 69 | I/O | General-purpose digital I/O / Timer_B3 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output / LCD segment output 37 |
| P3.5/TB0/S38 | 70 | I/O | General-purpose digital I/O / Timer_B3 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output / LCD segment output 38 |
| P3.4/TA2/S39 | 71 | I/O | General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output / LCD segment output 39 |
| P3.3/ UCB0CLK/UCA0STE | 72 | I/O | General-purpose digital I/O / USCI_B0 clock input/output / USCI_A0 slave transmit enable |
| P3.2/ UCB0SOMI/UCB0SCL | 73 | I/O | General-purpose digital I/O / USCI_B0 slave out/master in in SPI mode, SCL $I^2C$ clock in $I^2C$ mode |
| P3.1/ UCB0SIMO/UCB0SDA | 74 | I/O | General-purpose digital I/O / USCI_B0 slave in/master out in SPI mode, SDA $I^2C$ data in $I^2C$ mode |

## Terminal Functions (continued)

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| P3.0/ UCB0STE/UCA0CLK | 75 | I/O | General-purpose digital I/O / USCI_B0 slave transmit enable / USCI_A0 clock input/output |
| P2.7/CA1 | 76 | I/O | General-purpose digital I/O / Comparator_A input |
| P2.6/CA0 | 77 | I/O | General-purpose digital I/O / Comparator_A input |
| P2.5/ UCA0RXD/UCA0SOMI | 78 | I/O | General-purpose digital I/O / USCI_A0 receive data input in UART mode, slave out/master in in SPI mode |
| P2.4/ UCA0TXD/UCA0SIMO | 79 | I/O | General-purpose digital I/O / USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode |
| P2.3/ UCB1CLK/UCA1STE | 80 | I/O | General-purpose digital I/O / USCI_B1 clock input/output / USCI_A1 slave transmit enable |
| P2.2/ UCB1SOMI/UCB1SCL | 81 | I/O | General-purpose digital I/O / USCI_B1 slave out/master in in SPI mode, SCL $I^2C$ clock in $I^2C$ mode |
| P2.1/ UCB1SIMO/UCB1SDA | 82 | I/O | General-purpose digital I/O / USCI_B1 slave in/master out in SPI mode, SDA $I^2C$ data in $I^2C$ mode |
| P2.0/ UCB1STE/UCA1CLK | 83 | I/O | General-purpose digital I/O / USCI_B1 slave transmit enable / USCI_A1 clock input/output |
| P1.7/ UCA1RXD/UCA1SOMI | 84 | I/O | General-purpose digital I/O / USCI_A1 receive data input in UART mode, slave out/master in in SPI mode |
| P1.6/ UCA1TXD/UCA1SIMO | 85 | I/O | General-purpose digital I/O / USCI_A1 transmit data output in UART mode, slave in/master out in SPI mode |
| P1.5/TACLK/ACLK | 86 | I/O | General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8) |
| P1.4/TBCLK/SMCLK | 87 | I/O | General-purpose digital I/O / input clock TBCLK—Timer_B3 / submain system clock SMCLK output |
| P1.3/TBOUTH/SVSOUT | 88 | I/O | General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B3 TB0 to TB2 / SVS: output of SVS comparator |
| P1.2/TA1 | 89 | I/O | General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output |
| P1.1/TA0/MCLK | 90 | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output. Note: TA0 is only an input on this pin / BSL receive |
| P1.0/TA0 | 91 | I/O | General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit |
| $DV_{CC1}$ | 92 | | Digital supply voltage, positive terminal. |
| XT2OUT | 93 | O | Output terminal of crystal oscillator XT2 |
| XT2IN | 94 | I | Input port for crystal oscillator XT2. Only standard crystals can be connected. |
| $DV_{SS1}$ | 95 | | Digital supply voltage, negative terminal. |
| TDO/TDI | 96 | I/O | Test data output port. TDO/TDI data output or programming data input terminal |
| TDI/TCLK | 97 | I | Test data input or test clock input. The device protection fuse is connected to TDI/TCLK. |
| TMS | 98 | I | Test mode select. TMS is used as an input port for device programming and test. |
| TCK | 99 | I | Test clock. TCK is the clock input port for device programming and test. |
| $\overline{RST}$/NMI | 100 | I | Reset input or nonmaskable interrupt input port |

## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

### instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

**Table 1. Instruction Word Formats**

| | | |
|---|---|---|
| Dual operands, source-destination | e.g., ADD R4,R5 | R4 + R5 ---> R5 |
| Single operands, destination only | e.g., CALL R8 | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional | e.g., JNE | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE | S | D | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | ● | ● | MOV Rs,Rd | MOV R10,R11 | R10 --> R11 |
| Indexed | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5)--> M(6+R6) |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI | | M(EDE) --> M(TONI) |
| Absolute | ● | ● | MOV &MEM,&TCDAT | | M(MEM) --> M(TCDAT) |
| Indirect | ● | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) --> M(Tab+R6) |
| Indirect autoincrement | ● | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) --> R11<br>R10 + 2--> R10 |
| Immediate | ● | | MOV #X,TONI | MOV #45,TONI | #45 --> M(TONI) |

NOTE: S = source, D = destination

### operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled.
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL+ loop control is disabled
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL+ loop control and DCOCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

### interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. If the reset vector (at 0FFFEh) contains 0FFFFh (e.g., flash is not programmed) the CPU enters LPM4 after power-up.

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| Power-Up<br>External Reset<br>Watchdog<br>Flash Memory<br>PC Out-of-Range (see Note 4) | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV<br>(see Note 1) | Reset | 0FFFEh | 31, highest |
| NMI<br>Oscillator Fault<br>Flash Memory Access Violation | NMIIFG (see Notes 1 and 3)<br>OFIFG (see Notes 1 and 3)<br>ACCVIFG (see Notes 1 and 3) | (Non)maskable<br>(Non)maskable<br>(Non)maskable | 0FFFCh | 30 |
| Timer_B3 | TBCCR0 CCIFG (see Note 2) | Maskable | 0FFFAh | 29 |
| Timer_B3 | TBCCR1 to TBCCR2 CCIFGs<br>TBIFG (see Notes 1 and 2) | Maskable | 0FFF8h | 28 |
| Comparator_A | CAIFG | Maskable | 0FFF6h | 27 |
| Watchdog Timer | WDTIFG | Maskable | 0FFF4h | 26 |
| USCI_A0/B0 Receive<br>USCI_B0 I2C Status | UCA0RXIFG, UCB0RXIFG<br>(see Notes 1 and 5) | Maskable | 0FFF2h | 25 |
| USCI_A0/B0 Transmit<br>USCI_B0 I2C Receive/Transmit | UCA0TXIFG, UCB0TXIFG<br>(see Notes 1 and 6) | Maskable | 0FFF0h | 24 |
| SD16_A | SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG<br>(see Notes 1 and 2) | Maskable | 0FFEEh | 23 |
| Timer_A3 | TACCR0 CCIFG (see Note 2) | Maskable | 0FFECh | 22 |
| Timer_A3 | TACCR1 and TACCR2 CCIFGs,<br>TAIFG (see Notes 1 and 2) | Maskable | 0FFEAh | 21 |
| I/O Port P1 (Eight Flags) | P1IFG.0 to P1IFG.7 (see Notes 1 and 2) | Maskable | 0FFE8h | 20 |
| USCI_A1/B1 Receive<br>USCI_B1 I2C Status | UCA1RXIFG, UCB1RXIFG<br>(see Notes 1 and 5) | Maskable | 0FFE6h | 19 |
| USCI_A1/B1 Transmit<br>USCI_B1 I2C Receive/Transmit | UCA1TXIFG, UCB1TXIFG<br>(see Notes 1 and 6) | Maskable | 0FFE4h | 18 |
| I/O Port P2 (Eight Flags) | P2IFG.0 to P2IFG.7 (see Notes 1 and 2) | Maskable | 0FFE2h | 17 |
| Basic Timer1/RTC | BTIFG | Maskable | 0FFE0h | 16 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG<br>(see Notes 1 and 2) | Maskable | 0FFDEh | 15 |
| Reserved | Reserved (see Note 8) | | 0FFDCh to<br>0FFC0h | 14 to<br>0, lowest |

NOTES:
1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.
4. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
5. USCI_B in SPI mode: UCBxRXIFG. USCI_B in I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG
6. USCI_B in SPI mode: UCBxTXIFG. USCI_B in I2C mode: UCBxRXIFG, UCBxTXIFG
7. The address 0x0FFBE is used as bootstrap loader security key (BSLSKEY).
   A 0x0AA55 at this location disables the BSL completely.
   A zero disables the erasure of the flash if an invalid password is supplied.
8. The interrupt vectors at addresses 0FFDCh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

## special function registers

The MSP430 special function registers (SFR) are located in the lowest address space and are organized as byte mode registers. SFRs should be accessed with byte instructions.

### interrupt enable 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 00h | | | ACCVIE | NMIIE | | | OFIE | WDTIE |
| | | | rw-0 | rw-0 | | | rw-0 | rw-0 |

WDTIE Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE Oscillator fault enable

NMIIE (Non)maskable interrupt enable

ACCVIE Flash access violation interrupt enable

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 01h | BTIE | | | | UCB0TXIE | UCB0RXIE | UCA0TXIE | UCA0RXIE |
| | rw-0 | | | | rw-0 | rw-0 | rw-0 | rw-0 |

UCA0RXIE USCI_A0 receive interrupt enable

UCA0TXIE USCI_A0 transmit interrupt enable

UCB0RXIE USCI_B0 receive interrupt enable

UCB0TXIE USCI_B0 transmit interrupt enable

BTIE Basic timer interrupt enable

**interrupt flag register 1 and 2**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 02h | | | | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
| | | | | rw-0 | rw-(0) | rw-(1) | rw-1 | rw-(0) |

WDTIFG Set on watchdog timer overflow or security key violation.
Reset on $V_{CC}$ power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on $V_{CC}$ power-up

PORIFG Power-on interrupt flag. Set on $V_{CC}$ power-up.

NMIIFG Set via $\overline{RST}$/NMI-pin

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 03h | BTIFG | | | | UCB0 TXIFG | UCB0 RXIFG | UCA0 TXIFG | UCA0 RXIFG |
| | rw-0 | | | | rw-1 | rw-0 | rw-1 | rw-0 |

UCA0RXIFG USCI_A0 receive interrupt flag

UCA0TXIFG USCI_A0 transmit interrupt flag

UCB0RXIFG USCI_B0 receive interrupt flag

UCB0TXIFG USCI_B0 transmit interrupt flag

BTIFG Basic Timer1 interrupt flag

| Legend | | |
|---|---|---|
| | **rw:** | Bit can be read and written. |
| | **rw-0,1:** | Bit can be read and written. It is Reset or Set by PUC. |
| | **rw-(0,1):** | Bit can be read and written. It is Reset or Set by POR. |
| | | SFR bit is not present in device |

## memory organization

| | | MSP430F47126/ MSP430F47127 | MSP430F47163/ MSP430F47166/ MSP430F47167 | MSP430F47173/ MSP430F47176/ MSP430F47177 | MSP430F47183/ MSP430F47186/ MSP430F47187 | MSP430F47193/ MSP430F47196/ MSP430F47197 |
|---|---|---|---|---|---|---|
| Memory<br>Main: interrupt vector<br>Main: code memory | Size<br>Flash<br>Flash | 56KB<br>0FFFFh – 0FFC0h<br>0FFFFh–002100h | 92KB<br>0FFFFh – 0FFC0h<br>018FFFh–002100h | 92KB<br>0FFFFh – 0FFC0h<br>019FFFh–003100h | 116KB<br>0FFFFh – 0FFC0h<br>01FFFFh–003100h | 120KB<br>0FFFFh – 0FFC0h<br>01FFFFh–002100h |
| RAM (Total) | Size | 4KB<br>020FFh–01100h | 4KB<br>020FFh–01100h | 8KB<br>030FFh–01100h | 8KB<br>030FFh–01100h | 4KB<br>020FFh–01100h |
| Extended | Size | 2KB<br>020FFh–01900h | 2KB<br>020FFh–01900h | 6KB<br>030FFh–01900h | 6KB<br>030FFh–01900h | 2KB<br>020FFh–01900h |
| Mirrored | Size | 2KB<br>018FFh–01100h | 2KB<br>018FFh–01100h | 2KB<br>018FFh–01100h | 2KB<br>018FFh–01100h | 2KB<br>018FFh–01100h |
| Information memory | Size<br>Flash | 256 Byte<br>010FFh–01000h | 256 Byte<br>010FFh–01000h | 256 Byte<br>010FFh–01000h | 256 Byte<br>010FFh–01000h | 256 Byte<br>010FFh–01000h |
| Boot memory | Size<br>ROM | 1KB<br>0FFFh–0C00h | 1KB<br>0FFFh–0C00h | 1KB<br>0FFFh – 0C00h | 1KB<br>0FFFh–0C00h | 1KB<br>0FFFh–0C00h |
| RAM<br>(mirrored at<br>018FFh – 01100h) | Size | 2KB<br>09FFh–0200h | 2KB<br>09FFh–0200h | 2KB<br>09FFh–0200h | 2KB<br>09FFh–0200h | 2KB<br>09FFh–0200h |
| Peripherals | 16-bit<br>8-bit<br>8-bit SFR | 01FFh–0100h<br>0FFh–010h<br>0Fh–00h | 01FFh–0100h<br>0FFh–010h<br>0Fh–00h | 01FFh–0100h<br>0FFh–010h<br>0Fh–00h | 01FFh–0100h<br>0FFh–010h<br>0Fh–00h | 01FFh–0100h<br>0FFh–010h<br>0Fh–00h |

## bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide,* literature number SLAU265.

| BSL FUNCTION | PZ PACKAGE PINS |
|---|---|
| Data Transmit | 91 - P1.0 |
| Data Receive | 90 - P1.1 |

## flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory.*
- Segment A might contain calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.
- Flash content integrity check with marginal read modes.

### peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*, literature number SLAU056.

### oscillator and system clock

The clock system is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and an 8-MHz high-frequency crystal oscillator (XT1) plus a 16-MHz high-frequency crystal oscillator (XT2). The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

### brownout, supply voltage supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, $V_{CC}$ may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until $V_{CC}$ reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when $V_{CC}$ reaches $V_{CC(min)}$.

### digital I/O

There are nine 8-bit I/O ports implemented—ports P1 through P5 and P7 through P10.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports P7/P8 and P9/P10 can be accessed word-wise as ports PA and PB respectively.
- Each I/O has an individually programmable pullup/pulldown resistor.

**Note:** Only four bits of port P10 (P10.0 to P10.3) are available on external pins, but all control and data bits for port P10 are implemented.

### DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from a USCI module to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

| DMA TRIGGER SELECT DMAXTSELX | DESCRIPTION |
|---|---|
| 0000 | DMAREQ bit (software trigger) |
| 0001 | TACCR2 CCIFG bit |
| 0010 | TBCCR2 CCIFG bit |
| 0011 | UCA0RXIFG bit |
| 0100 | UCA0TXIFG bit |
| 0101 | N/A |
| 0110 | SD16IFG bit |
| 0111 | TACCR0 CCIFG bit |
| 1000 | TBCCR0 CCIFG bit |
| 1001 | UCA1RXIFG bit |
| 1010 | UCA1TXIFG bit |
| 1011 | Multiplier ready |
| 1100 | UCB0RXIFG bit |
| 1101 | UCB0TXIFG bit |
| 1110 | DMA0IFG bit triggers DMA channel 1<br>DMA1IFG bit triggers DMA channel 2<br>DMA2IFG bit triggers DMA channel 0 |
| 1111 | External trigger DMAE0 |

### hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

### watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

### Basic Timer1 and Real-Time Clock (RTC)

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for months with less than 31 days and includes leap year correction.

### universal serial communication interfaces (USCIs) (USCI_A0, USCI_B0, USCI_A1, USCI_B1)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I2C and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 and USCI_A1 provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

USCI_B0 and USCI_B1 provides support for SPI (3-pin or 4-pin) and I2C.

### Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_A3 SIGNAL CONNECTIONS | | | | | |
|---|---|---|---|---|---|
| **INPUT PIN NUMBER** | **DEVICE INPUT SIGNAL** | **MODULE INPUT NAME** | **MODULE BLOCK** | **MODULE OUTPUT SIGNAL** | **OUTPUT PIN NUMBER** |
| 86 - P1.5 | TACLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 86 - P1.5 | $\overline{\text{TACLK}}$ | INCLK | | | |
| 91 - P1.0 | TA0 | CCI0A | CCR0 | TA0 | 91 - P1.0 |
| 90 - P1.1 | TA0 | CCI0B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |
| 89 - P1.2 | TA1 | CCI1A | CCR1 | TA1 | 89 - P1.2 |
| | CAOUT (internal) | CCI1B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |
| 71 - P3.4 | TA2 | CCI2A | CCR2 | TA2 | 71 - P3.4 |
| | ACLK (internal) | CCI2B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |

### Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_B3 SIGNAL CONNECTIONS | | | | | |
|---|---|---|---|---|---|
| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
| 87 - P1.4 | TBCLK | TBCLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 87 - P1.4 | $\overline{\text{TBCLK}}$ | INCLK | | | |
| 70 – P3.5 | TB0 | CCI0A | CCR0 | TB0 | 70 - P3.5 |
| 70 – P3.5 | TB0 | CCI0B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |
| 69 - P3.6 | TB1 | CCI1A | CCR1 | TB1 | 69 - P3.6 |
| 69 - P3.6 | TB1 | CCI1B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |
| 68 - P3.7 | TB2 | CCI2A | CCR2 | TB2 | 68 - P3.7 |
| 68 - P3.7 | TB2 | CCI2B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |

### Comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

### SD16_A

The SD16_A module integrates three (MSP430F471x3), six (MSP430F471x6) or seven (MSP430F471x7) independent 16-bit sigma-delta A/D converters. Each channel is designed with a fully differential analog input pair and programmable gain amplifier input stage. In addition to external analog inputs, an internal $V_{CC}$ sense and temperature sensor are also available.

### LCD driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and thus contrast in software.

### embedded emulation module (EEM)

All MSP430F471x3, MSP430F471x6, and MSP430F471x7 devices have an EEM that supports real-time in-system debugging. The implemented L version of the EEM has the following features:

- Eight hardware triggers on memory address or data bus
- Two hardware triggers on write accesses to CPU register
- Eight combinational triggers to combine any of the 10 above hardware triggers
- Trigger sequencer
- CPU break reaction on combinational triggers for breakpoints
- State storage to trace internal buses
- Clock control on module level

## peripheral file map

| PERIPHERALS WITH WORD ACCESS | | | |
|---|---|---|---|
| **Watchdog** | Watchdog timer control | WDTCTL | 0120h |
| **Flash_A** | Flash control 4 | FCTL4 | 01BEh |
| | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |
| **Timer_B3** | Capture/compare register 2 | TBCCR2 | 0196h |
| | Capture/compare register 1 | TBCCR1 | 0194h |
| | Capture/compare register 0 | TBCCR0 | 0192h |
| | Timer_B register | TBR | 0190h |
| | Capture/compare control 2 | TBCCTL2 | 0186h |
| | Capture/compare control 1 | TBCCTL1 | 0184h |
| | Capture/compare control 0 | TBCCTL0 | 0182h |
| | Timer_B control | TBCTL | 0180h |
| | Timer_B interrupt vector | TBIV | 011Eh |
| **Timer_A3** | Capture/compare register 2 | TACCR2 | 0176h |
| | Capture/compare register 1 | TACCR1 | 0174h |
| | Capture/compare register 0 | TACCR0 | 0172h |
| | Timer_A register | TAR | 0170h |
| | Capture/compare control 2 | TACCTL2 | 0166h |
| | Capture/compare control 1 | TACCTL1 | 0164h |
| | Capture/compare control 0 | TACCTL0 | 0162h |
| | Timer_A control | TACTL | 0160h |
| | Timer_A interrupt vector | TAIV | 012Eh |
| **32-bit Hardware Multiplier** | MPY32 control 0 | MPY32CTL0 | 015Ch |
| | 64-bit result 3 – most significant word | RES3 | 015Ah |
| | 64-bit result 2 | RES2 | 0158h |
| | 64-bit result 1 | RES1 | 0156h |
| | 64-bit result 0 – least significant word | RES0 | 0154h |
| | Second 32-bit operand, high word | OP2H | 0152h |
| | Second 32-bit operand, low word | OP2L | 0150h |
| | Multiply signed + accumulate/ 32-bit operand1, high word | MACS32H | 014Eh |
| | Multiply signed + accumulate/ 32-bit operand1, low word | MACS32L | 014Ch |
| | Multiply + accumulate/ 32-bit operand1, high word | MAC32H | 014Ah |
| | Multiply + accumulate/ 32-bit operand1, low word | MAC32L | 0148h |
| | Multiply signed/32-bit operand1, high word | MPYS32H | 0146h |
| | Multiply signed/32-bit operand1, low word | MPYS32L | 0144h |
| | Multiply unsigned/32-bit operand1, high word | MPY32H | 0142h |
| | Multiply unsigned/32-bit operand1, low word | MPY32L | 0140h |

## peripheral file map (continued)

| PERIPHERALS WITH WORD ACCESS (CONTINUED) | | | |
|---|---|---|---|
| **32-bit Hardware Multiplier** | Sum extend | SUMEXT | 013Eh |
| | Result high word | RESHI | 013Ch |
| | Result low word | RESLO | 013Ah |
| | Second operand | OP2 | 0138h |
| | Multiply signed + accumulate/operand1 | MACS | 0136h |
| | Multiply + accumulate/operand1 | MAC | 0134h |
| | Multiply signed/operand1 | MPYS | 0132h |
| | Multiply unsigned/operand1 | MPY | 0130h |
| **USCI_B0 (see also: Peripherals with Byte Access)** | USCI_B0 I2C own address | UCB0I2COA | 016Ch |
| | USCI_B0 I2C slave address | UCB0I2CSA | 016Eh |
| **USCI_B1 (see also: Peripherals with Byte Access)** | USCI_B1 I2C own address | UCB1I2COA | 017Ch |
| | USCI_B1 I2C slave address | UCB1I2CSA | 017Eh |
| **SD16_A (see also: Peripherals with Byte Access)** | General Control | SD16CTL | 0100h |
| | Channel 0 Control | SD16CCTL0 | 0102h |
| | Channel 1 Control | SD16CCTL1 | 0104h |
| | Channel 2 Control | SD16CCTL2 | 0106h |
| | Channel 3 Control | SD16CCTL3 | 0108h |
| | Channel 4 Control | SD16CCTL4 | 010Ah |
| | Channel 5 Control | SD16CCTL5 | 010Ch |
| | Channel 6 Control | SD16CCTL6 | 010Eh |
| | Channel 0 conversion memory | SD16MEM0 | 0110h |
| | Channel 1 conversion memory | SD16MEM1 | 0112h |
| | Channel 2 conversion memory | SD16MEM2 | 0114h |
| | Channel 3 conversion memory | SD16MEM3 | 0116h |
| | Channel 4 conversion memory | SD16MEM4 | 0118h |
| | Channel 5 conversion memory | SD16MEM5 | 011Ah |
| | Channel 6 conversion memory | SD16MEM6 | 011Ch |
| | SD16 Interrupt vector word register | SD16IV | 01AEh |
| **Port PA** | Port PA resistor enable | PAREN | 014h |
| | Port PA selection | PASEL | 03Eh |
| | Port PA direction | PADIR | 03Ch |
| | Port PA output | PAOUT | 03Ah |
| | Port PA input | PAIN | 038h |
| **Port PB** | Port PB resistor enable | PBREN | 016h |
| | Port PB selection | PBSEL | 00Eh |
| | Port PB direction | PBDIR | 00Ch |
| | Port PB output | PBOUT | 00Ah |
| | Port PB input | PBIN | 008h |

## peripheral file map (continued)

| PERIPHERALS WITH WORD ACCESS (CONTINUED) | | | |
|---|---|---|---|
| **DMA** | DMA module control 0 | DMACTL0 | 0122h |
| | DMA module control 1 | DMACTL1 | 0124h |
| | DMA interrupt vector | DMAIV | 0126h |
| **DMA Channel 0** | DMA channel 0 control | DMA0CTL | 01D0h |
| | DMA channel 0 source address | DMA0SA | 01D2h |
| | DMA channel 0 destination address | DMA0DA | 01D6h |
| | DMA channel 0 transfer size | DMA0SZ | 01DAh |
| **DMA Channel 1** | DMA channel 1 control | DMA1CTL | 01DCh |
| | DMA channel 1 source address | DMA1SA | 01DEh |
| | DMA channel 1 destination address | DMA1DA | 01E2h |
| | DMA channel 1 transfer size | DMA1SZ | 01E6h |
| **DMA Channel 2** | DMA channel 2 control | DMA2CTL | 01E8h |
| | DMA channel 2 source address | DMA2SA | 01EAh |
| | DMA channel 2 destination address | DMA2DA | 01EEh |
| | DMA channel 2 transfer size | DMA2SZ | 01F2h |

## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS | | | |
|---|---|---|---|
| **SD16_A (see also: Peripherals with Word Access)** | Channel 0 Input Control | SD16INCTL0 | 0B0h |
| | Channel 1 Input Control | SD16INCTL1 | 0B1h |
| | Channel 2 Input Control | SD16INCTL2 | 0B2h |
| | Channel 3 Input Control | SD16INCTL3 | 0B3h |
| | Channel 4 Input Control | SD16INCTL4 | 0B4h |
| | Channel 5 Input Control | SD16INCTL5 | 0B5h |
| | Channel 6 Input Control | SD16INCTL6 | 0B6h |
| | Reserved | | 0B7h |
| | Channel 0 preload | SD16PRE0 | 0B8h |
| | Channel 1 preload | SD16PRE1 | 0B9h |
| | Channel 2 preload | SD16PRE2 | 0BAh |
| | Channel 3 preload | SD16PRE3 | 0BBh |
| | Channel 4 preload | SD16PRE4 | 0BCh |
| | Channel 5 preload | SD16PRE5 | 0BDh |
| | Channel 6 preload | SD16PRE6 | 0BEh |
| | Reserved | SD16CONF1 | 0BFh |
| **LCD_A** | LCD Voltage Control 1 | LCDAVCTL1 | 0AFh |
| | LCD Voltage Control 0 | LCDAVCTL0 | 0AEh |
| | LCD Voltage Port Control 1 | LCDAPCTL1 | 0ADh |
| | LCD Voltage Port Control 0 | LCDAPCTL0 | 0ACh |
| | LCD memory 20 | LCDM20 | 0A4h |
| | : | : | : |
| | LCD memory 16 | LCDM16 | 0A0h |
| | LCD memory 15 | LCDM15 | 09Fh |
| | : | : | : |
| | LCD memory 1 | LCDM1 | 091h |
| | LCD control and mode | LCDACTL | 090h |

## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) | | | |
|---|---|---|---|
| **USCI_A0** | USCI_A0 transmit buffer | UCA0TXBUF | 067h |
| | USCI_A0 receive buffer | UCA0RXBUF | 066h |
| | USCI_A0 status | UCA0STAT | 065h |
| | USCI_A0 modulation control | UCA0MCTL | 064h |
| | USCI_A0 baud rate control 1 | UCA0BR1 | 063h |
| | USCI_A0 baud rate control 0 | UCA0BR0 | 062h |
| | USCI_A0 control 1 | UCA0CTL1 | 061h |
| | USCI_A0 control 0 | UCA0CTL0 | 060h |
| | USCI_A0 IrDA receive control | UCA0IRRCTL | 05Fh |
| | USCI_A0 IrDA transmit control | UCA0IRTCTL | 05Eh |
| | USCI_A0 auto baud rate control | UCA0ABCTL | 05Dh |
| **USCI_B0** | USCI_B0 transmit buffer | UCB0TXBUF | 06Fh |
| | USCI_B0 receive buffer | UCB0RXBUF | 06Eh |
| | USCI_B0 status | UCB0STAT | 06Dh |
| | USCI_B1 I2C interrupt enable | UCB0I2CIE | 06Ch |
| | USCI_B0 bit rate control 1 | UCB0BR1 | 06Bh |
| | USCI_B0 bit rate control 0 | UCB0BR0 | 06Ah |
| | USCI_B0 control 1 | UCB0CTL1 | 069h |
| | USCI_B0 control 0 | UCB0CTL0 | 068h |
| **USCI_A1** | USCI_A1 transmit buffer | UCA1TXBUF | 0D7h |
| | USCI_A1 receive buffer | UCA1RXBUF | 0D6h |
| | USCI_A1 status | UCA1STAT | 0D5h |
| | USCI_A1 modulation control | UCA1MCTL | 0D4h |
| | USCI_A1 baud rate control 1 | UCA1BR1 | 0D3h |
| | USCI_A1 baud rate control 0 | UCA1BR0 | 0D2h |
| | USCI_A1 control 1 | UCA1CTL1 | 0D1h |
| | USCI_A1 control 0 | UCA1CTL0 | 0D0h |
| | USCI_A1 IrDA receive control | UCA1IRRCTL | 0CFh |
| | USCI_A1 IrDA transmit control | UCA1IRTCTL | 0CEh |
| | USCI_A1 auto baud rate control | UCA1ABCTL | 0CDh |
| | USCI_A1 interrupt flag | UC1IFG | 007h |
| | USCI_A1 interrupt enable | UC1IE | 006h |
| **USCI_B1** | USCI_B1 transmit buffer | UCB1TXBUF | 0DFh |
| | USCI_B1 receive buffer | UCB1RXBUF | 0DEh |
| | USCI_B1 status | UCB1STAT | 0DDh |
| | USCI_B1 I2C interrupt enable | UCB1I2CIE | 0DCh |
| | USCI_B1 bit rate control 1 | UCB1BR1 | 0DBh |
| | USCI_B1 bit rate control 0 | UCB1BR0 | 0DAh |
| | USCI_B1 control 1 | UCB1CTL1 | 0D9h |
| | USCI_B1 control 0 | UCB1CTL0 | 0D8h |
| | USCI_A1 interrupt flag | UC1IFG | 007h |
| | USCI_A1 interrupt enable | UC1IE | 006h |
| **Comparator_A** | Comparator_A port disable | CAPD | 05Bh |
| | Comparator_A control2 | CACTL2 | 05Ah |
| | Comparator_A control1 | CACTL1 | 059h |
| **BrownOUT, SVS** | SVS control register (Reset by brownout signal) | SVSCTL | 056h |

## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) | | | |
|---|---|---|---|
| **FLL+ Clock** | FLL+ Control2 | FLL_CTL2 | 055h |
| | FLL+ Control1 | FLL_CTL1 | 054h |
| | FLL+ Control0 | FLL_CTL0 | 053h |
| | System clock frequency control | SCFQCTL | 052h |
| | System clock frequency integrator | SCFI1 | 051h |
| | System clock frequency integrator | SCFI0 | 050h |
| **RTC (Basic Timer 1)** | Real Time Clock Year High Byte | RTCYEARH | 04Fh |
| | Real Time Clock Year Low Byte | RTCYEARL | 04Eh |
| | Real Time Clock Month | RTCMON | 04Dh |
| | Real Time Clock Day of Month | RTCDAY | 04Ch |
| | Basic Timer1 Counter 2 | BTCNT2 | 047h |
| | Basic Timer1 Counter 1 | BTCNT1 | 046h |
| | Real Time Counter 4 | RTCNT4 | 045h |
| | (Real Time Clock Day of Week) | (RTCDOW) | |
| | Real Time Counter 3 | RTCNT3 | 044h |
| | (Real Time Clock Hour) | (RTCHOUR) | |
| | Real Time Counter 2 | RTCNT2 | 043h |
| | (Real Time Clock Minute) | (RTCMIN) | |
| | Real Time Counter 1 | RTCNT1 | 042h |
| | (Real Time Clock Second) | (RTCSEC) | |
| | Real Time Clock Control | RTCCTL | 041h |
| | Basic Timer1 Control | BTCTL | 040h |
| **Port P10** | Port P10 resistor enable | P10REN | 017h |
| | Port P10 selection | P10SEL | 00Fh |
| | Port P10 direction | P10DIR | 00Dh |
| | Port P10 output | P10OUT | 00Bh |
| | Port P10 input | P10IN | 009h |
| **Port P9** | Port P9 resistor enable | P9REN | 016h |
| | Port P9 selection | P9SEL | 00Eh |
| | Port P9 direction | P9DIR | 00Ch |
| | Port P9 output | P9OUT | 00Ah |
| | Port P9 input | P9IN | 008h |
| **Port P8** | Port P8 resistor enable | P8REN | 015h |
| | Port P8 selection | P8SEL | 03Fh |
| | Port P8 direction | P8DIR | 03Dh |
| | Port P8 output | P8OUT | 03Bh |
| | Port P8 input | P8IN | 039h |
| **Port P7** | Port P7 resistor enable | P7REN | 014h |
| | Port P7 selection | P7SEL | 03Eh |
| | Port P7 direction | P7DIR | 03Ch |
| | Port P7 output | P7OUT | 03Ah |
| | Port P7 input | P7IN | 038h |

## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) | | | |
|---|---|---|---|
| **Port P5** | Port P5 resistor enable | P5REN | 012h |
| | Port P5 selection | P5SEL | 033h |
| | Port P5 direction | P5DIR | 032h |
| | Port P5 output | P5OUT | 031h |
| | Port P5 input | P5IN | 030h |
| **Port P4** | Port P4 resistor enable | P4REN | 011h |
| | Port P4 selection | P4SEL | 01Fh |
| | Port P4 direction | P4DIR | 01Eh |
| | Port P4 output | P4OUT | 01Dh |
| | Port P4 input | P4IN | 01Ch |
| **Port P3** | Port P3 resistor enable | P3REN | 010h |
| | Port P3 selection | P3SEL | 01Bh |
| | Port P3 direction | P3DIR | 01Ah |
| | Port P3 output | P3OUT | 019h |
| | Port P3 input | P3IN | 018h |
| **Port P2** | Port P2 resistor enable | P2REN | 02Fh |
| | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt-edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |
| **Port P1** | Port P1 resistor enable | P1REN | 027h |
| | Port P1 selection | P1SEL | 026h |
| | Port P1 interrupt enable | P1IE | 025h |
| | Port P1 interrupt-edge select | P1IES | 024h |
| | Port P1 interrupt flag | P1IFG | 023h |
| | Port P1 direction | P1DIR | 022h |
| | Port P1 output | P1OUT | 021h |
| | Port P1 input | P1IN | 020h |
| **Special Functions** | SFR interrupt flag2 | IFG2 | 003h |
| | SFR interrupt flag1 | IFG1 | 002h |
| | SFR interrupt enable2 | IE2 | 001h |
| | SFR interrupt enable1 | IE1 | 000h |

### absolute maximum ratings (see Note 1)

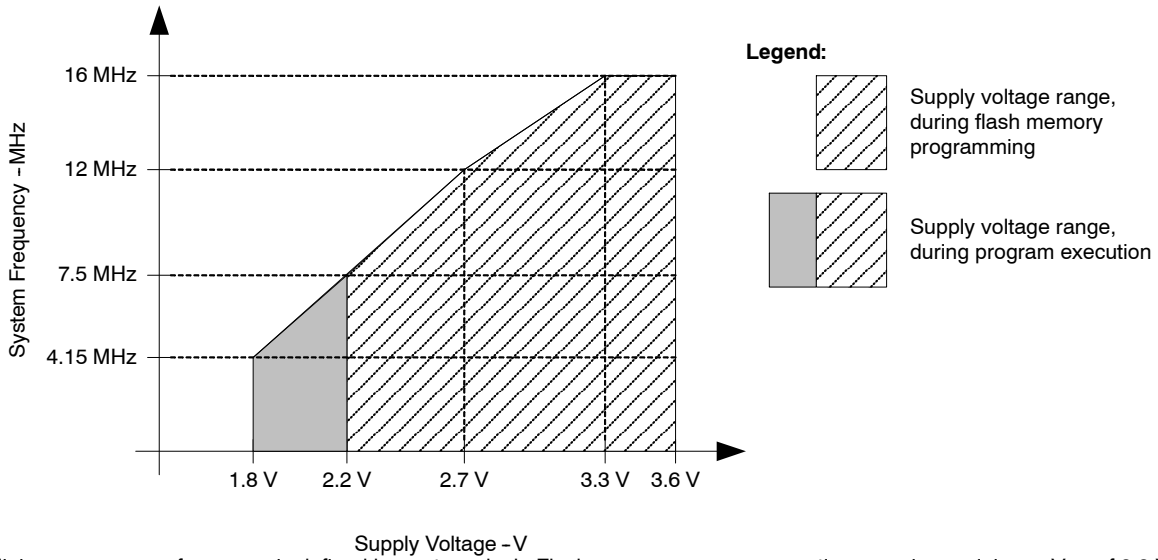
Voltage applied at $V_{CC}$ to $V_{SS}$ . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) . . . . . –0.3 V to $V_{CC}$ + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, $T_{stg}$: Unprogrammed device (see Note 3) . . . . . –55°C to 150°C
Programmed device (see Note 3) . . . . . –40°C to 85°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to $V_{SS}$. The JTAG fuse-blow voltage, $V_{FB}$, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage during program execution, $V_{CC}$ ($AV_{CC}$ = $DV_{CC}$ = $V_{CC}$) (see Note 1) | | 1.8 | | 3.6 | V |
| Supply voltage during program execution, SVS enabled, PORON = 1, $V_{CC}$ ($AV_{CC}$ = $DV_{CC}$ = $V_{CC}$) (see Notes 1, 2) | | 2.0 | | 3.6 | V |
| Supply voltage during program/erase flash memory, $V_{CC}$ ($AV_{CC}$ = $DV_{CC}$ = $V_{CC}$) (see Note 1) | | 2.2 | | 3.6 | V |
| Supply voltage, $V_{SS}$ | | | 0 | | V |
| Operating free-air temperature range, $T_A$ | | –40 | | 85 | °C |
| Processor frequency $f_{SYSTEM}$ (Maximum MCLK frequency) (see Notes 3, 4 and Figure 1) | $V_{CC}$ = 1.8 V, Duty cycle = 50% ±10% | dc | | 4.15 | MHz |
| | $V_{CC}$ = 2.2 V, Duty cycle = 50% ±10% | dc | | 7.5 | MHz |
| | $V_{CC}$ = 2.7 V, Duty cycle = 50% ±10% | dc | | 12 | MHz |
| | $V_{CC}$ ≥ 3.3 V, Duty cycle = 50% ±10% | dc | | 16 | |

NOTES: 1. It is recommended to power $AV_{CC}$ and $DV_{CC}$ from the same source. A maximum difference of 0.3 V between $AV_{CC}$ and $DV_{CC}$ can be tolerated during power up and operation.
2. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised above minimum supply voltage plus the hysteresis of the SVS circuitry.
3. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
4. Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.




NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum $V_{CC}$ of 2.2 V.

**Figure 1. Operating Area**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

### supply current into $AV_{CC}$ + $DV_{CC}$ excluding external current

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{(AM)}$ | Active mode, (see Note 1)<br>$f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz,<br>$f_{(ACLK)}$ = 32768 Hz<br>XTS = 0, SELM = (0,1)<br>(Program executes from flash) | $T_A$ = –40°C to 85°C | 2.2 V | | 350 | 400 | µA |
| | | | 3 V | | 500 | 560 | |
| $I_{(LPM0)}$ | Low-power mode, (LPM0)<br>(see Notes 1, 4) | $T_A$ = –40°C to 85°C | 2.2 V | | 45 | 70 | µA |
| | | | 3 V | | 75 | 110 | |
| $I_{(LPM2)}$ | Low-power mode, (LPM2),<br>f(MCLK) = f (SMCLK) = 0 MHz,<br>f(ACLK) = 32768 Hz, SCG0 = 0 (see Notes 2, 4) | $T_A$ = –40°C to 85°C | 2.2 V | | 11 | 14 | µA |
| | | | 3 V | | 17 | 22 | |
| $I_{(LPM3)}$ | Low-power mode, (LPM3)<br>$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz,<br>$f_{(ACLK)}$ = 32768 Hz, SCG0 = 1<br>Basic Timer1 and RTC enabled , ACLK selected<br>LCD_A enabled, LCDCPEN = 0:<br>(static mode , $f_{LCD} = f_{(ACLK)}/32$)<br>(see Notes 2, 3, and 4) | $T_A$ = –40°C | 2.2 V | | 0.7 | 2.0 | µA |
| | | $T_A$ = 25°C | | | 0.8 | 2.0 | |
| | | $T_A$ = 60°C | | | 2.0 | 3.5 | |
| | | $T_A$ = 85°C | | | 5.0 | 9.5 | |
| | | $T_A$ = –40°C | 3 V | | 1.1 | 3.0 | µA |
| | | $T_A$ = 25°C | | | 1.2 | 3.0 | |
| | | $T_A$ = 60°C | | | 2.5 | 4.0 | |
| | | $T_A$ = 85°C | | | 6.0 | 10.0 | |
| $I_{(LPM3)}$ | Low-power mode, (LPM3)<br>$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz,<br>$f_{(ACLK)}$ = 32768 Hz, SCG0 = 1<br>Basic Timer1 and RTC enabled , ACLK selected<br>LCD_A enabled, LCDCPEN = 0:<br>(4-mux mode, $f_{LCD} = f_{(ACLK)}/32$)<br>(see Notes 2, 3, and 4) | $T_A$ = –40°C | 2.2 V | | 3.5 | 5.5 | µA |
| | | $T_A$ = 25°C | | | 3.5 | 5.5 | |
| | | $T_A$ = 60°C | | | 5.5 | 7.0 | |
| | | $T_A$ = 85°C | | | 11.0 | 17.0 | |
| | | $T_A$ = –40°C | 3 V | | 4.0 | 6.5 | µA |
| | | $T_A$ = 25°C | | | 4.0 | 6.5 | |
| | | $T_A$ = 60°C | | | 6.0 | 8.0 | |
| | | $T_A$ = 85°C | | | 13.0 | 20.0 | |
| $I_{(LPM4)}$ | Low-power mode, (LPM4)<br>$f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz,<br>$f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Notes 2 and 4) | $T_A$ = –40°C | 2.2 V | | 0.1 | 1.0 | µA |
| | | $T_A$ = 25°C | | | 0.2 | 1.0 | |
| | | $T_A$ = 60°C | | | 1.0 | 2.5 | |
| | | $T_A$ = 85°C | | | 4.5 | 8.5 | |
| | | $T_A$ = –40°C | 3 V | | 0.1 | 2.0 | µA |
| | | $T_A$ = 25°C | | | 0.2 | 2.0 | |
| | | $T_A$ = 60°C | | | 1.5 | 3.0 | |
| | | $T_A$ = 85°C | | | 5.0 | 9.0 | |

NOTES: 1. Timer_A is clocked by $f_{(DCOCLK)} = f_{(DCO)}$ = 1 MHz. All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
3. The LPM3 currents are characterized with a Micro Crystal CC4V–T1A (9 pF) crystal and OSCCAPx = 01h.
4. Current for brownout included.

### typical characteristics – active mode supply current (into $V_{CC}$)

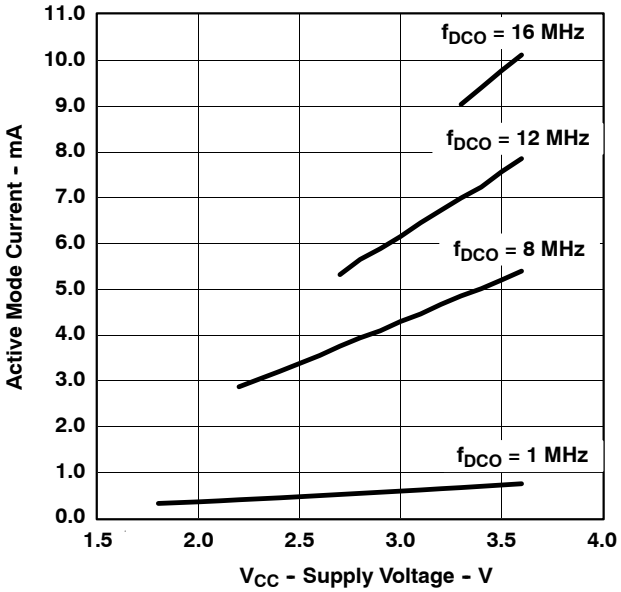



**Figure 2. Active Mode Current vs $V_{CC}$, $T_A$ = 25°C**

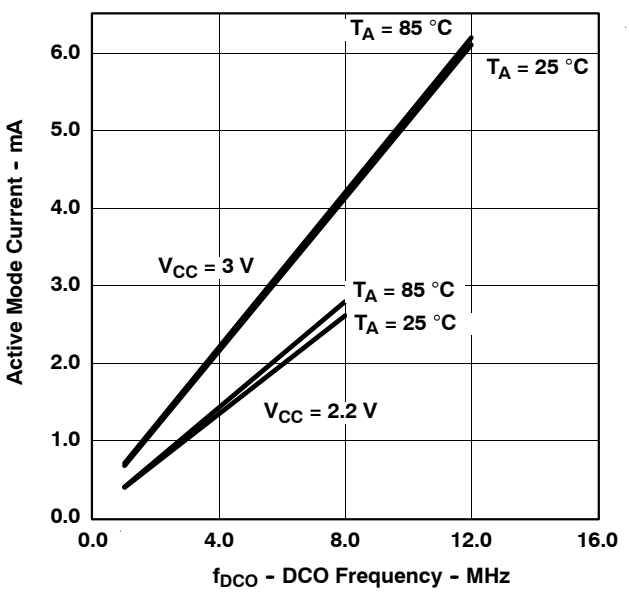



**Figure 3. Active Mode Current vs DCO Frequency**

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### Schmitt-trigger inputs – Ports P1 to P5, P7 to P10, RST/NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | | 0.45 | | 0.75 | $V_{CC}$ |
| | | | 2.2 V | 1.00 | | 1.65 | V |
| | | | 3 V | 1.35 | | 2.25 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | | 0.25 | | 0.55 | $V_{CC}$ |
| | | | 2.2 V | 0.55 | | 1.20 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+}$ - $V_{IT-}$) | | 2.2 V | 0.2 | | 1.0 | V |
| | | | 3 V | 0.3 | | 1.0 | |
| $R_{Pull}$ | Pullup/pulldown resistor (not RST/NMI and JTAG pins) | For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

### inputs – Ports P1, P2

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing | Port P1, P2: P1.x to P2.x, external trigger puls width to set interrupt flag (see Note 1) | 2.2 V/3 V | 20 | | ns |

NOTES: 1. An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

### leakage current – Ports P1 to P5, P7 to P10

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.x)}$ | High-impedance leakage current | See Notes 1 and 2 | 2.2 V/3 V | | ±50 | nA |

NOTES: 1. The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### outputs – Ports P1 to P5, P7 to P10

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1.5 mA (see Note 1) | 2.2 V | $V_{CC}$–0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –6 mA (see Note 2) | 2.2 V | $V_{CC}$–0.6 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –1.5 mA (see Note 1) | 3 V | $V_{CC}$–0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA (see Note 2) | 3 V | $V_{CC}$–0.6 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1.5 mA (see Note 1) | 2.2 V | $V_{SS}$ | $V_{SS}$+0.25 | V |
| | | $I_{(OLmax)}$ = 6 mA (see Note 2) | 2.2 V | $V_{SS}$ | $V_{SS}$+0.6 | |
| | | $I_{(OLmax)}$ = 1.5 mA (see Note 1) | 3 V | $V_{SS}$ | $V_{SS}$+0.25 | |
| | | $I_{(OLmax)}$ = 6 mA (see Note 2) | 3 V | $V_{SS}$ | $V_{SS}$+0.6 | |

NOTES: 1. The maximum total current, $I_{OHmax}$ and $I_{OLmax}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, $I_{OHmax}$ and $I_{OLmax}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

### output frequency – Ports P1 to P5, P7 to P10

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | P1.4/TBCLK/SMCLK, $C_L$ = 20 pF, $R_L$ = 1 kΩ against $V_{CC}$/2 (see Notes 1 and 2) | 2.2 V | | 10 | MHz |
| | | | 3 V | | 12 | MHz |
| $f_{Port_CLK}$ | Clock output frequency | P1.1/TA0/MCLK, P1.5/TACLK/ACLK, P1.4/TBCLK/SMCLK, $C_L$ = 20 pF (see Note 2) | 2.2 V | | 12 | MHz |
| | | | 3 V | | 16 | MHz |

NOTES: 1. Alternatively a resistive divider with 2 times 2 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**typical characteristics – outputs**

**TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

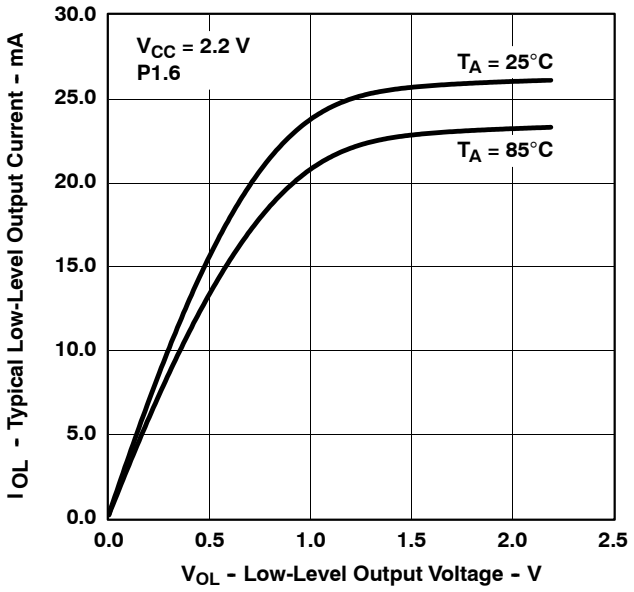



**Figure 4**

**TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

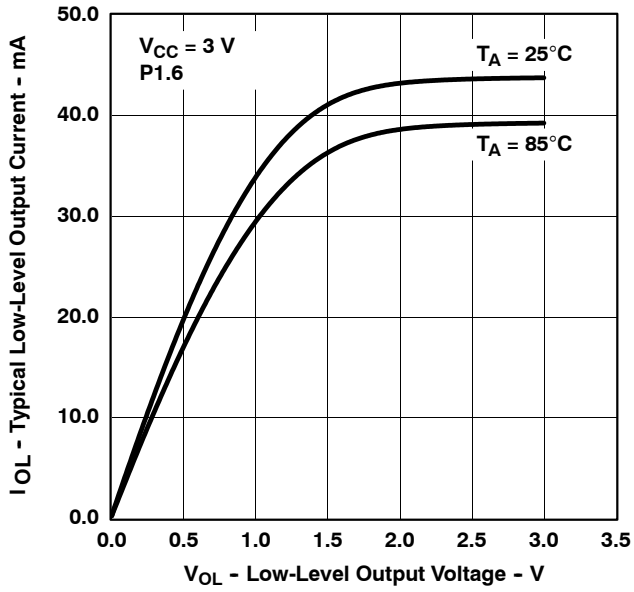



**Figure 5**

**TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

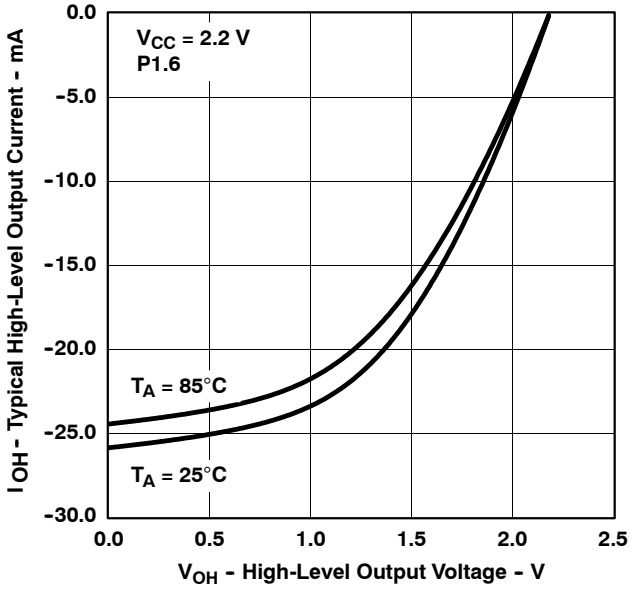



**Figure 6**

**TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

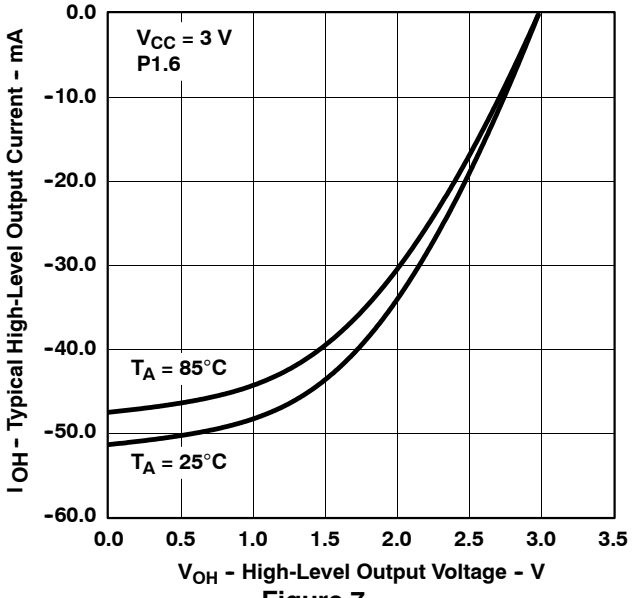



**Figure 7**

NOTE: One output loaded at a time.

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### POR/brownout reset (BOR) (see Notes 1 and 2)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(start)}$ | (See Figure 8) | $dV_{CC}/dt \le 3$ V/s | | | $0.7 \times V_{(B_IT-)}$ | | V |
| $V_{(B_IT-)}$ | (See Figure 8 through Figure 10) | $dV_{CC}/dt \le 3$ V/s | | | | 1.71 | V |
| $V_{hys(B_IT-)}$ | (See Figure 8) | $dV_{CC}/dt \le 3$ V/s | | 70 | 130 | 180 | mV |
| $t_{d(BOR)}$ | (See Figure 8) | | | | | 2000 | μs |
| $t_{(reset)}$ | Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally | | 2.2 V/3 V | 2 | | | μs |

NOTES: 1. The current consumption of the brownout module is already included in the $I_{CC}$ current consumption data. The voltage level $V_{(B_IT-)} + V_{hys(B_IT-)}$ is ≤ 1.8 V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide (SLAU056)* for more information on the brownout/SVS circuit.

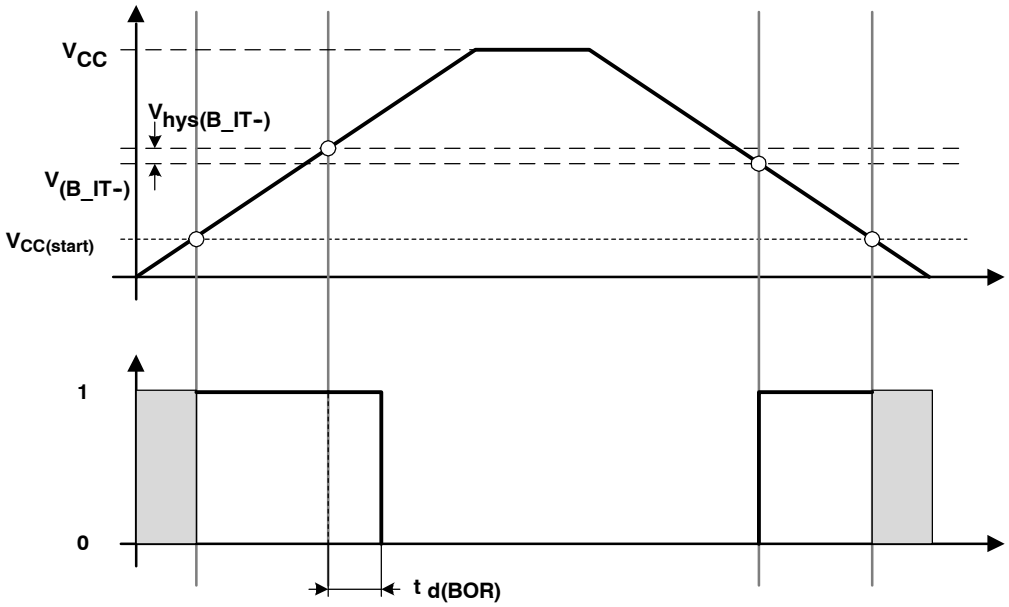



**Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**typical characteristics – POR/brownout reset (BOR)**

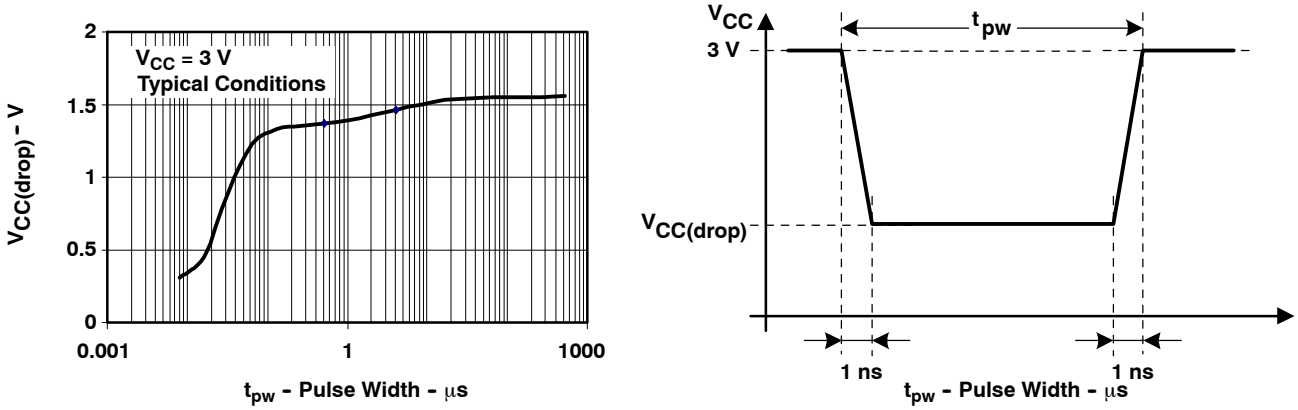



**Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal**

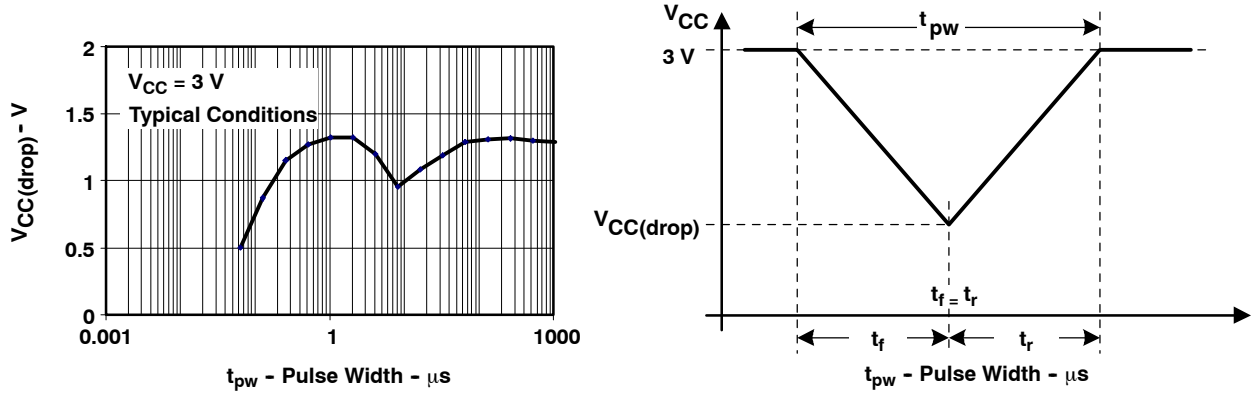



**Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal**

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### SVS (supply voltage supervisor/monitor) (see Note 1)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(SVSR)}$ | $dV_{CC}/dt$ > 30 V/ms (see Figure 11) | | 5 | | 150 | µs |
| | $dV_{CC}/dt$ ≤ 30 V/ms | | | | 2000 | µs |
| $t_{d(SVSon)}$ | SVSon, switch from VLD = 0 to VLD ≠ 0, $V_{CC}$ = 3 V | | | 150 | 300 | µs |
| $t_{settle}$ | VLD ≠ 0 (see Note 2) | | | | 12 | µs |
| $V_{(SVSstart)}$ | VLD ≠ 0, $V_{CC}/dt$ ≤ 3 V/s (see Figure 11) | | | 1.55 | 1.7 | V |
| $V_{hys(SVS_IT-)}$ | $V_{CC}/dt$ ≤ 3 V/s (see Figure 11) | VLD = 1 | 70 | 120 | 155 | mV |
| | | VLD = 2 to 14 | $V_{(SVS_IT-)}$ × 0.001 | | $V_{(SVS_IT-)}$ × 0.016 | |
| | $V_{CC}/dt$ ≤ 3 V/s (see Figure 11), External voltage applied on A7 | VLD = 15 | 4.4 | | 10.4 | mV |
| $V_{(SVS_IT-)}$ | $V_{CC}/dt$ ≤ 3 V/s (see Figure 11) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | 1.94 | 2.1 | 2.25 | |
| | | VLD = 3 | 2.05 | 2.2 | 2.37 | |
| | | VLD = 4 | 2.14 | 2.3 | 2.48 | |
| | | VLD = 5 | 2.24 | 2.4 | 2.6 | |
| | | VLD = 6 | 2.33 | 2.5 | 2.71 | |
| | | VLD = 7 | 2.46 | 2.65 | 2.86 | |
| | | VLD = 8 | 2.58 | 2.8 | 3 | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | 2.83 | 3.05 | 3.29 | |
| | | VLD = 11 | 2.94 | 3.2 | 3.42 | |
| | | VLD = 12 | 3.11 | 3.35 | 3.61† | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76† | |
| | | VLD = 14 | 3.43 | 3.7† | 3.99† | |
| | $V_{CC}/dt$ ≤ 3 V/s (see Figure 11), External voltage applied on A7 | VLD = 15 | 1.1 | 1.2 | 1.3 | |
| $I_{CC(SVS)}$ (see Note 1) | VLD ≠ 0, $V_{CC}$ = 2.2 V/3 V | | | 10 | 15 | µA |

† The recommended operating voltage range is limited to 3.6 V.

NOTES: 1. The current consumption of the SVS module is not included in the $I_{CC}$ current consumption data.
2. $t_{settle}$ is the settling time that the comparator output needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

## typical characteristics

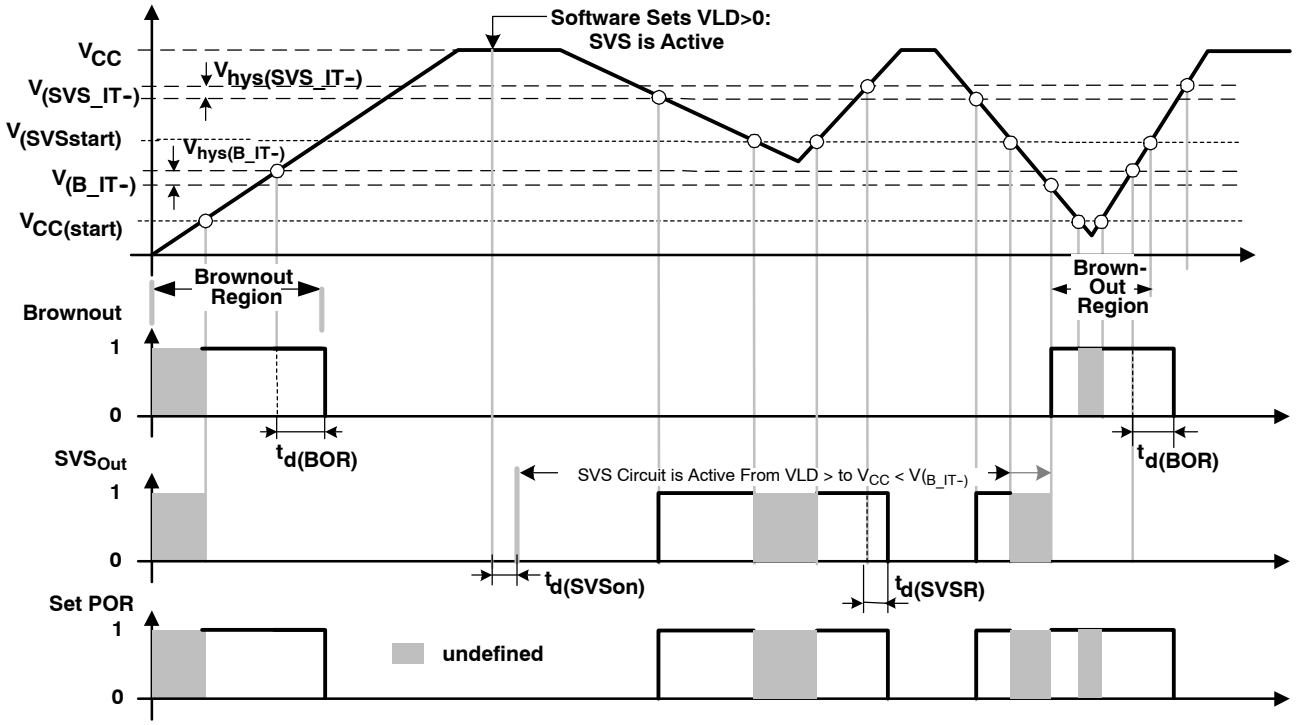



**Figure 11. SVS Reset (SVSR) vs Supply Voltage**

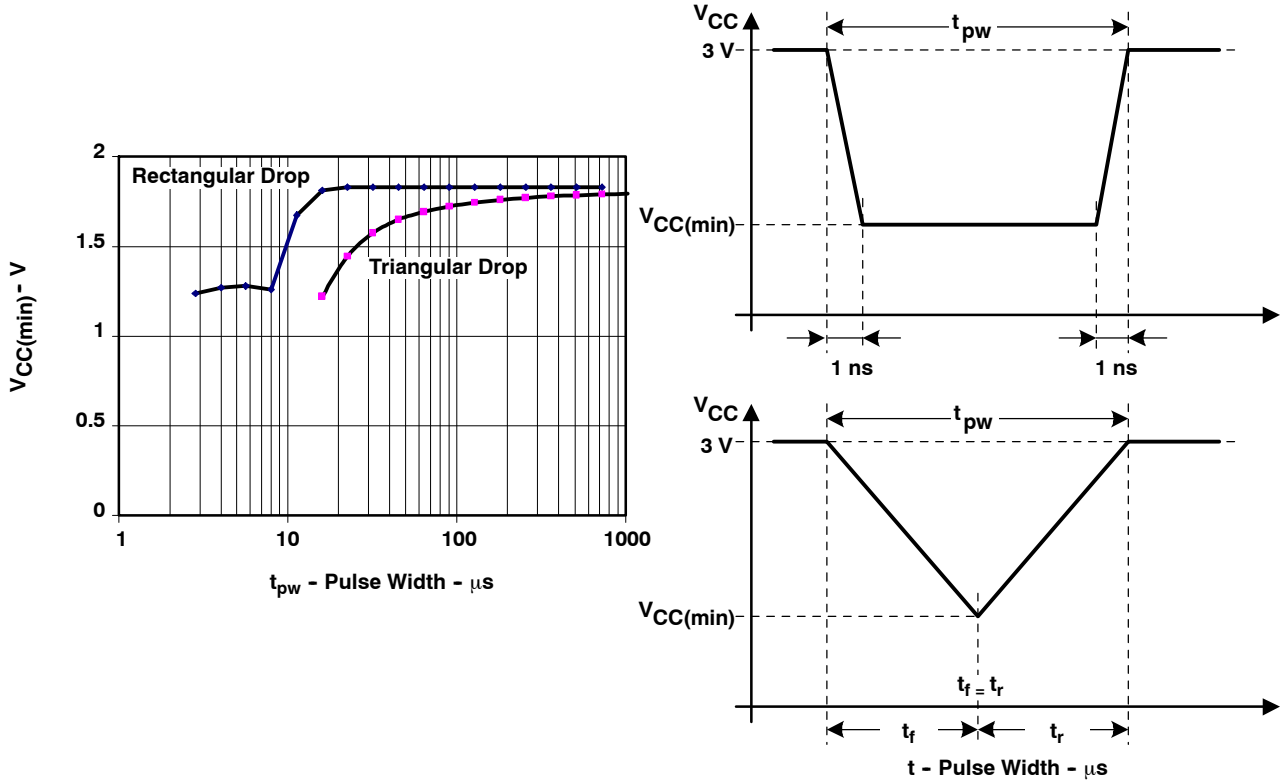



**Figure 12. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

### DCO

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(DCOCLK)}$ | $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0 | $V_{CC}$ = 2.2 V/3 V | | 1 | | MHz |
| $f_{(DCO = 2)}$ | FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 0.3 | 0.65 | 1.25 | MHz |
| | | $V_{CC}$ = 3 V | 0.3 | 0.7 | 1.3 | |
| $f_{(DCO = 27)}$ | FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 2.5 | 5.6 | 10.5 | MHz |
| | | $V_{CC}$ = 3 V | 2.7 | 6.1 | 11.3 | |
| $f_{(DCO = 2)}$ | FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 0.7 | 1.3 | 2.3 | MHz |
| | | $V_{CC}$ = 3 V | 0.8 | 1.5 | 2.5 | |
| $f_{(DCO = 27)}$ | FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DOPLUS = 1 | $V_{CC}$ = 2.2 V | 5.7 | 10.8 | 18 | MHz |
| | | $V_{CC}$ = 3 V | 6.5 | 12.1 | 20 | |
| $f_{(DCO = 2)}$ | FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 1.2 | 2 | 3 | MHz |
| | | $V_{CC}$ = 3 V | 1.3 | 2.2 | 3.5 | |
| $f_{(DCO = 27)}$ | FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 9 | 15.5 | 25 | MHz |
| | | $V_{CC}$ = 3 V | 10.3 | 17.9 | 28.5 | |
| $f_{(DCO = 2)}$ | FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 1.8 | 2.8 | 4.2 | MHz |
| | | $V_{CC}$ = 3 V | 2.1 | 3.4 | 5.2 | |
| $f_{(DCO = 27)}$ | FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 13.5 | 21.5 | 33 | MHz |
| | | $V_{CC}$ = 3 V | 16 | 26.6 | 41 | |
| $f_{(DCO = 2)}$ | FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 2.8 | 4.2 | 6.2 | MHz |
| | | $V_{CC}$ = 3 V | 4.2 | 6.3 | 9.2 | |
| $f_{(DCO = 27)}$ | FN_8 = 1,FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1 | $V_{CC}$ = 2.2 V | 21 | 32 | 46 | MHz |
| | | $V_{CC}$ = 3 V | 30 | 46 | 70 | |
| $S_n$ | Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$, (see Figure 14 for taps 21 to 27) | 1 < TAP ≤ 20 | 1.06 | | 1.11 | |
| | | TAP = 27 | 1.07 | | 1.17 | |
| $D_t$ | Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0 D = 2, DCOPLUS = 0 | $V_{CC}$ = 2.2 V | –0.2 | –0.4 | –0.6 | %/°C |
| | | $V_{CC}$ = 3 V | –0.2 | –0.4 | –0.6 | |
| $D_V$ | Drift with $V_{CC}$ variation, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0 | $V_{CC}$ = 2.2 V/3 V | 0 | 5 | 15 | %/V |

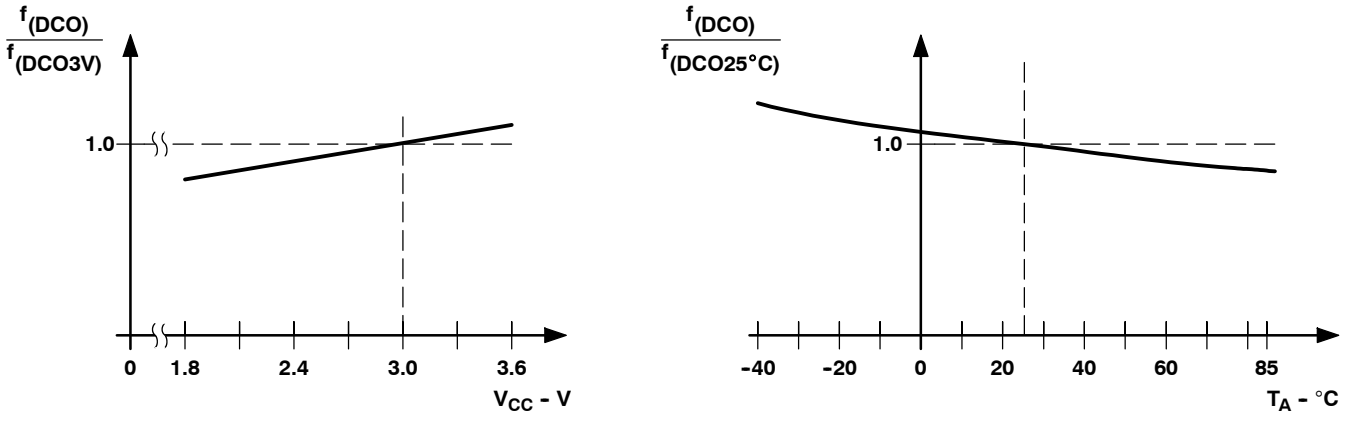



**Figure 13. DCO Frequency vs Supply Voltage $V_{CC}$ and vs Ambient Temperature**

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

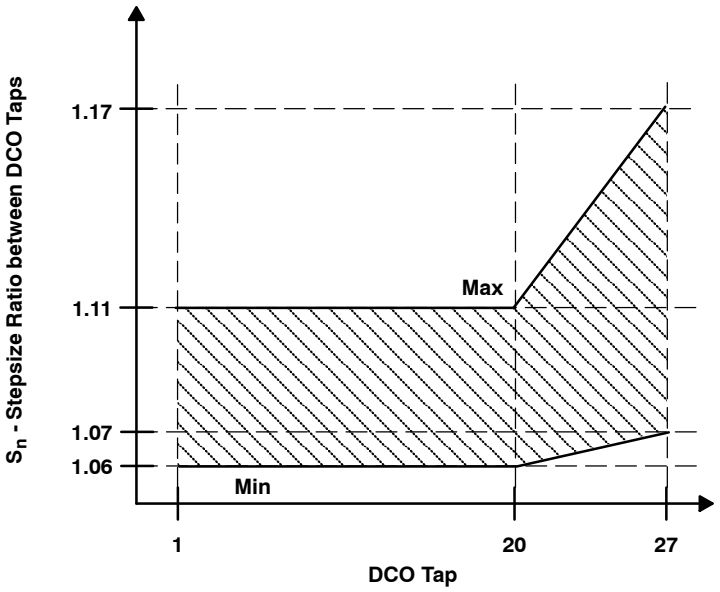



**Figure 14. DCO Tap Step Size**

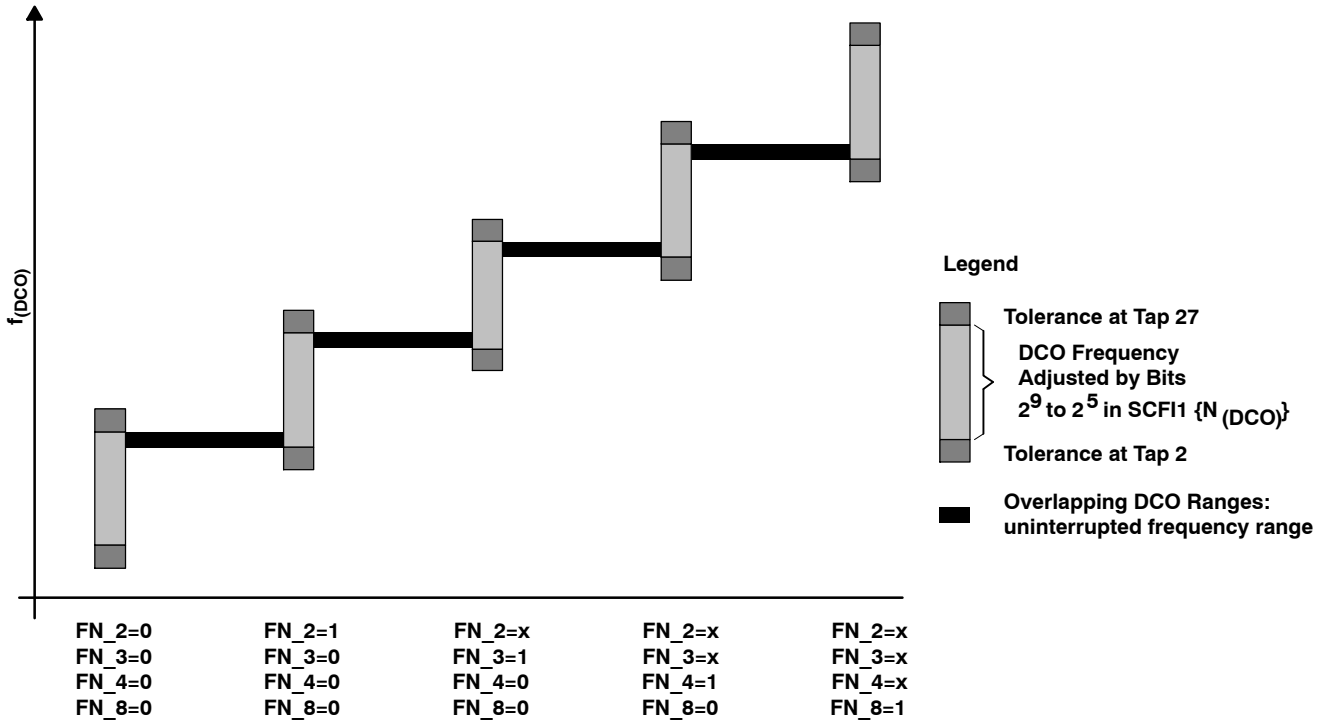



**Figure 15. Five Overlapping DCO Ranges Controlled by FN_x Bits**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### crystal oscillator, LFXT1, low-frequency mode (see Note 4)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{LFXT1,LF}$ | LFXT1 oscillator crystal frequency, LF mode | XTS = 0 | 1.8 V to 3.6 V | | 32768 | | Hz |
| $OA_{LF}$ | Oscillation allowance for LF crystals | XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 500 | | kΩ |
| | | XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | | 200 | | kΩ |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode (see Note 1) | XTS = 0, XCAPxPF = 0 | | | 1 | | pF |
| | | XTS = 0, XCAPxPF = 1 | | | 5.5 | | pF |
| | | XTS = 0, XCAPxPF = 2 | | | 8.5 | | pF |
| | | XTS = 0, XCAPxPF = 3 | | | 11 | | pF |
| Duty Cycle | LF mode | XTS = 0, $f_{LFXT1,LF}$ = 32768 Hz Measured at P1.5/TACLK/ACLK | 2.2 V/3 V | 30 | 50 | 70 | % |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode (see Note 3) | XTS = 0 (see Note 2) | 2.2 V/3 V | 10 | | 10,000 | Hz |

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

### crystal oscillator, LFXT1, high-frequency mode

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{XT1}$ | XT1 oscillator crystal frequency | XTS = 1, Ceramic resonator | 1.8 V to 3.6 V | 0.45 | | 6 | MHz |
| $f_{XT1}$ | XT1 oscillator crystal frequency | XTS = 1, Crystal | 1.8 V to 3.6 V | 1 | | 6 | MHz |
| $C_{L,eff}$ | Integrated effective load capacitance (see Note 1) | (see Note 2) | | | 1 | | pF |
| Duty Cycle | | Measured at P1.5/TACLK/ACLK | 2.2 V/3 V | 40 | 50 | 60 | % |

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### crystal oscillator, XT2 oscillator (see Note 5)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{XT2,0}$ | XT2 oscillator crystal frequency, mode 0 | XT2Sx = 0 | 1.8 V to 3.6 V | 0.4 | | 1 | MHz |
| $f_{XT2,1}$ | XT2 oscillator crystal frequency, mode 1 | XT2Sx = 1 | 1.8 V to 3.6 V | 1 | | 4 | MHz |
| $f_{XT2,2}$ | XT2 oscillator crystal frequency, mode 2 | XT2Sx = 2 | 1.8 V to 3.6 V | 2 | | 10 | MHz |
| | | | 2.2 V to 3.6 V | 2 | | 12 | MHz |
| | | | 3.0 V to 3.6 V | 2 | | 16 | MHz |
| $f_{XT2,logic}$ | XT2 oscillator logic level square wave input frequency | XT2Sx = 3 | 1.8 V to 3.6 V | 0.4 | | 10 | MHz |
| | | | 2.2 V to 3.6 V | 0.4 | | 12 | MHz |
| | | | 3.0 V to 3.6 V | 0.4 | | 16 | MHz |
| $OA_{XT2}$ | Oscillation allowance for HF crystals (see Figure 16) | XT2Sx = 0, $f_{XT2}$ = 1 MHz, $C_{L,eff}$ = 15 pF | | | 2700 | | Ω |
| | | XT2Sx = 1 $f_{XT2}$ = 4 MHz, $C_{L,eff}$ = 15 pF | | | 800 | | Ω |
| | | XT2Sx = 2 $f_{XT2}$ = 16 MHz, $C_{L,eff}$ = 15 pF | | | 300 | | Ω |
| $C_{L,eff}$ | Integrated effective load capacitance (see Note 1) | (see Note 2) | | | 1 | | pF |
| Duty cycle | | Measured at P1.5/TACLK/ACLK, $f_{XT2}$ = 10 MHz | 2.2 V/3 V | 40 | 50 | 60 | % |
| | | Measured at P1.5/TACLK/ACLK, $f_{XT2}$ = 16 MHz | 2.2 V/3 V | 40 | 50 | 60 | % |
| $f_{Fault,XT2}$ | Oscillator fault frequency (see Note 4) | XT2Sx = 3 (see Notes 3) | 2.2 V/3 V | 30 | | 300 | kHz |

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
5. To improve EMI on the XT2 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
   - Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**typical characteristics – XT2 oscillator**

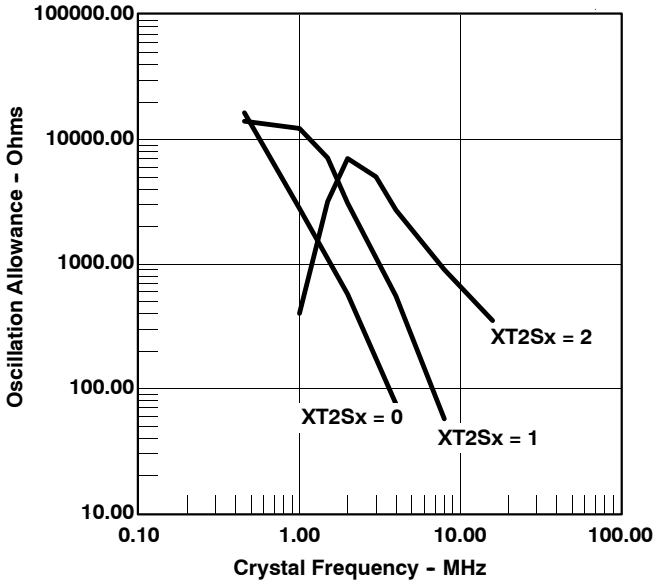



**Figure 16. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, $T_A$ = 25°C**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### wake-up LPM3

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(LPM3)}$ | Delay time | f = 1 MHz | 2.2 V/3 V | | 6 | µs |
| | | f = 2 MHz | | | 6 | |
| | | f = 3 MHz | | | 6 | |

### LCD_A

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(LCD)}$ | Supply voltage range | Charge pump enabled (LCDCPEN = 1, VLCDx > 0000) | | 2.2 | | 3.6 | V |
| $C_{LCD}$ | Capacitor on LCDCAP (see Note 1) | Charge pump enabled (LCDCPEN = 1, VLCDx > 0000) | | 4.7 | | | µF |
| $I_{CC(LCD)}$ | Supply current | $V_{LCD(typ)}$ = 3 V, LCDCPEN = 1, VLCDx = 1000, all segments on, $f_{LCD} = f_{ACLK}/32$ no LCD connected (see Note 2), $T_A$ = 25°C | 2.2 V | | 3.8 | | µA |
| $f_{LCD}$ | LCD frequency | | | | | 1.1 | kHz |
| $V_{LCD}$ | LCD voltage | VLCDx = 0000 | | | $V_{CC}$ | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 0001 | | | 2.60 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 0010 | | | 2.66 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 0011 | | | 2.72 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 0100 | | | 2.78 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 0101 | | | 2.84 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 0110 | | | 2.90 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 0111 | | | 2.96 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1000 | | | 3.02 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1001 | | | 3.08 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1010 | | | 3.14 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1011 | | | 3.20 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1100 | | | 3.26 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1101 | | | 3.32 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1110 | | | 3.38 | | V |
| $V_{LCD}$ | LCD voltage | VLCDx = 1111 | | | 3.44 | 3.60 | V |
| $R_{LCD}$ | LCD driver output impedance | $V_{LCD}$ = 3 V, LCDCPEN = 1, VLCDx = 1000, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |

NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Connecting an actual display will increase the current consumption depending on the size of the LCD.

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### Comparator_A (see Note 1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{(CC)}$ | | CAON = 1, CARSEL = 0, CAREF = 0 | 2.2 V | | 25 | 40 | μA |
| | | | 3 V | | 45 | 60 | |
| $I_{(Refladder/RefDiode)}$ | | CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P2.6/CA0 and P2.7/CA1 | 2.2 V | | 30 | 50 | μA |
| | | | 3 V | | 45 | 80 | |
| $V_{(Ref025)}$ | $\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$ | PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.6/CA0 and P2.7/CA1 | 2.2 V / 3 V | 0.23 | 0.24 | 0.25 | |
| $V_{(Ref050)}$ | $\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$ | PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.6/CA0 and P2.7/CA1 | 2.2V / 3 V | 0.47 | 0.48 | 0.5 | |
| $V_{(RefVT)}$ | See Figure 17 and Figure 18 | PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.6/CA0 and P2.7/CA1, $T_{A\ =}$ 85°C | 2.2 V | 390 | 480 | 540 | mV |
| | | | 3 V | 400 | 490 | 550 | |
| $V_{IC}$ | Common-mode input voltage range | CAON = 1 | 2.2 V / 3 V | 0 | | $V_{CC}$–1 | V |
| $V_p$–$V_S$ | Offset voltage | See Note 2 | 2.2 V / 3 V | –30 | | 30 | mV |
| $V_{hys}$ | Input hysteresis | CAON = 1 | 2.2 V / 3 V | 0 | 0.7 | 1.4 | mV |
| $t_{(response\ LH\ and\ HL)}$ (See Note 3) | | $T_A$ = 25°C, Overdrive 10 mV, without filter: CAF = 0 | 2.2 V | 80 | 165 | 300 | ns |
| | | | 3 V | 70 | 120 | 240 | |
| | | $T_A$ = 25°C Overdrive 10 mV, with filter: CAF = 1 | 2.2 V | 1.4 | 1.9 | 2.8 | μs |
| | | | 3 V | 0.9 | 1.5 | 2.2 | |

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.
3. The response time is measured at P2.6/CA0 with an input voltage step and the Comparator_A already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**typical characteristics**

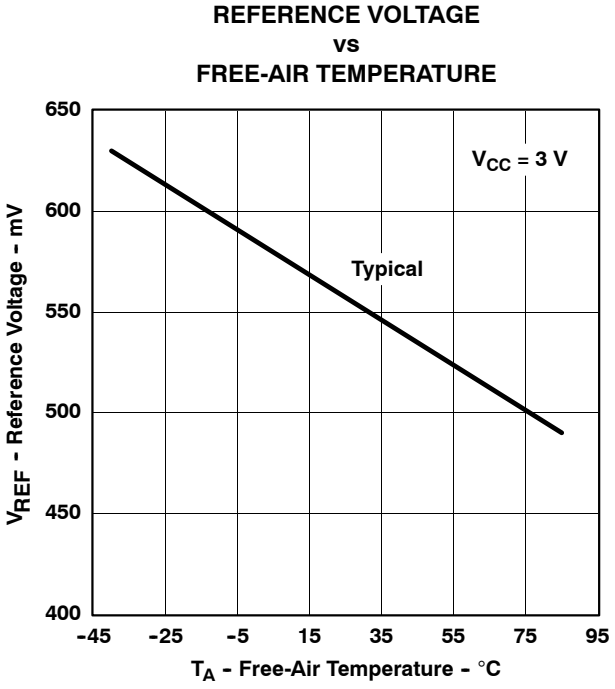



**Figure 17. $V_{(RefVT)}$ vs Temperature**

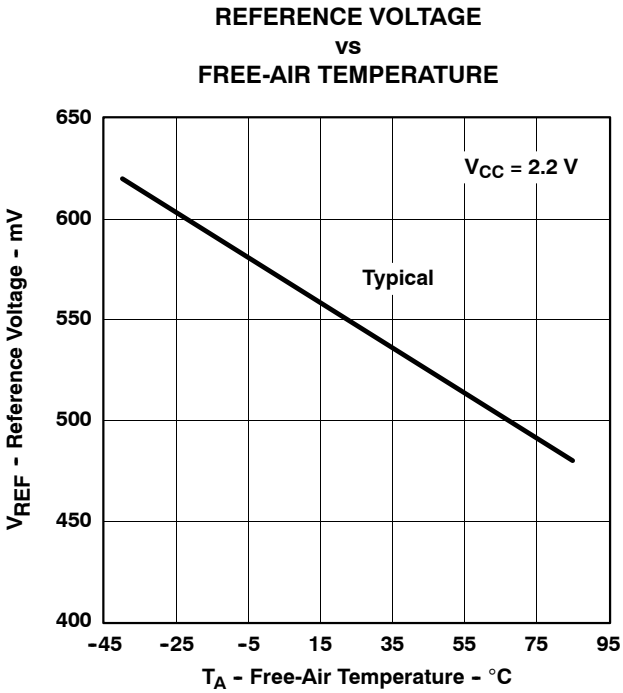



**Figure 18. $V_{(RefVT)}$ vs Temperature**

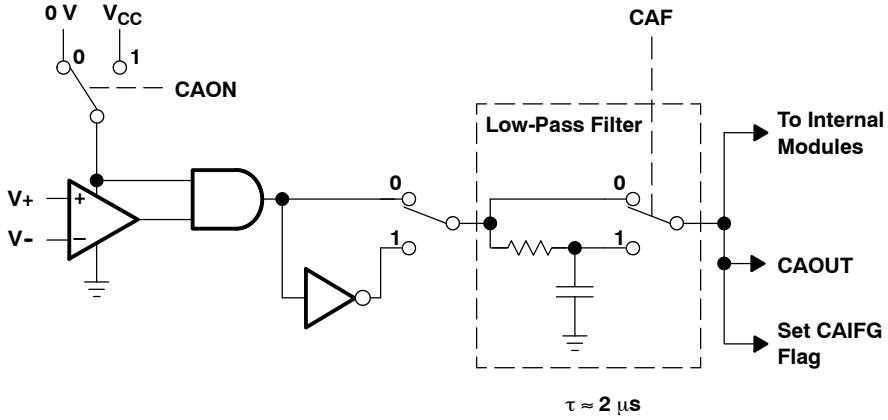



**Figure 19. Block Diagram of Comparator_A Module**

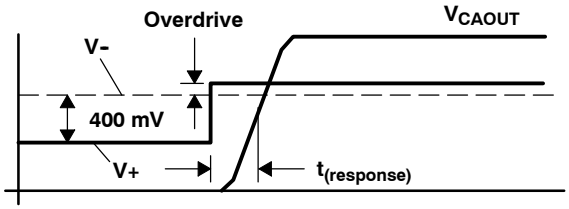



**Figure 20. Overdrive Definition**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

### Timer_A

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A clock frequency | Internal: SMCLK, ACLK,<br>External: TACLK, INCLK,<br>Duty cycle = 50% ±10% | 2.2 V | | 10 | MHz |
| | | | 3 V | | 16 | |
| $t_{TA,cap}$ | Timer_A, capture timing | TA0, TA1, TA2 | 2.2 V/3 V | 20 | | ns |

### Timer_B

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TB}$ | Timer_B clock frequency | Internal: SMCLK, ACLK,<br>External: TBCLK,<br>Duty cycle = 50% ±10% | 2.2 V | | 10 | MHz |
| | | | 3 V | | 16 | |
| $t_{TB,cap}$ | Timer_B, capture timing | TB0, TB1, TB2 | 2.2 V/3 V | 20 | | ns |

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### USCI (UART mode) – recommended operating conditions

| PARAMETER | | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% | | $f_{SYSTEM}$ | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency<br>(equals baud rate in MBaud) | | | 1 | MHz |

### USCI (UART mode)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_\tau$ | UART receive deglitch time<br>(see Note 1) | | 2.2 V | 50 | 150 | 600 | ns |
| | | | 3 V | 50 | 100 | 600 | ns |

NOTES: 1. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

### USCI (SPI master mode) – recommended operating conditions

| PARAMETER | | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | SMCLK, ACLK<br>Duty cycle = 50% ± 10% | | $f_{SYSTEM}$ | MHz |

### USCI (SPI master mode) (see Note 1, Figure 21, and Figure 22)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | SMCLK, ACLK<br>Duty cycle = 50% ± 10% | | | $f_{SYSTEM}$ | MHz |
| $t_{SU,MI}$ | SOMI input data setup time | | 2.2 V | 110 | | ns |
| | | | 3 V | 75 | | ns |
| $t_{HD,MI}$ | SOMI input data hold time | | 2.2 V | 0 | | ns |
| | | | 3 V | 0 | | ns |
| $t_{VALID,MO}$ | SIMO output data valid time (Note 2) | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF | 2.2 V | | 30 | ns |
| | | | 3 V | | 20 | ns |
| $t_{HD,MO}$ | SIMO output data hold time (Note 3) | $C_L$ = 20 pF | 2.2 V | 0 | | ns |
| | | | 3 V | 0 | | ns |

NOTES: 1. $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.
2. Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 21 and Figure 22.
3. Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 21 and Figure 22.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

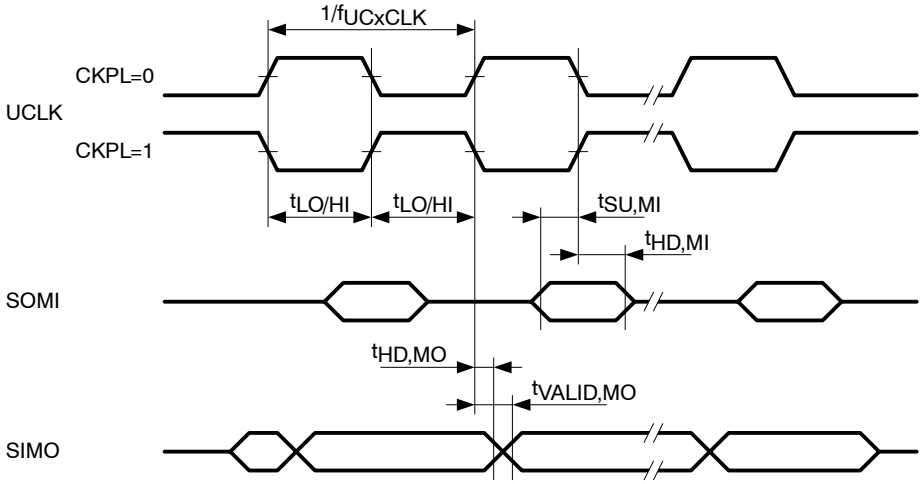



**Figure 21. SPI Master Mode, CKPH = 0**

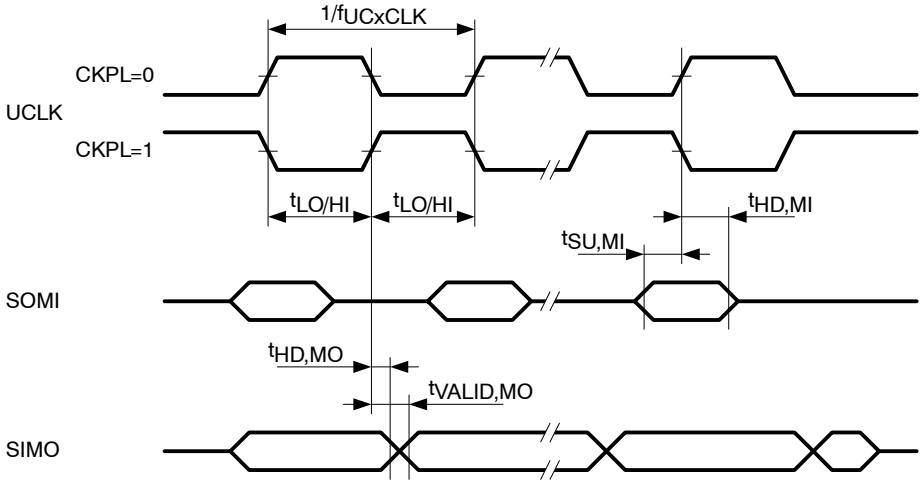



**Figure 22. SPI Master Mode, CKPH = 1**

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### USCI (SPI slave mode) (see Note 1, Figure 23, and Figure 24)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time<br>STE low to clock | | 2.2 V/3 V | | 50 | | ns |
| $t_{STE,LAG}$ | STE lag time<br>Last clock to STE high | | 2.2 V/3 V | 10 | | | ns |
| $t_{STE,ACC}$ | STE access time<br>STE low to SOMI data out | | 2.2 V/3 V | | 50 | | ns |
| $t_{STE,DIS}$ | STE disable time<br>STE high to SOMI high impedance | | 2.2 V/3 V | | 50 | | ns |
| $t_{SU,SI}$ | SIMO input data setup time | | 2.2 V | 20 | | | ns |
| | | | 3 V | 15 | | | ns |
| $t_{HD,SI}$ | SIMO input data hold time | | 2.2 V | 10 | | | ns |
| | | | 3 V | 10 | | | ns |
| $t_{VALID,SO}$ | SOMI output data valid time (Note 2) | UCLK edge to SOMI valid,<br>$C_L$ = 20 pF | 2.2 V | | 75 | 110 | ns |
| | | | 3 V | | 50 | 75 | ns |
| $t_{HD,MO}$ | SOMI output data hold time (Note 3) | $C_L$ = 20 pF | 2.2 V | 0 | | | ns |
| | | | 3 V | 0 | | | ns |

NOTES: 1. $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached master.
2. Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 23 and Figure 24.
3. Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SOMI output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 23 and Figure 24.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

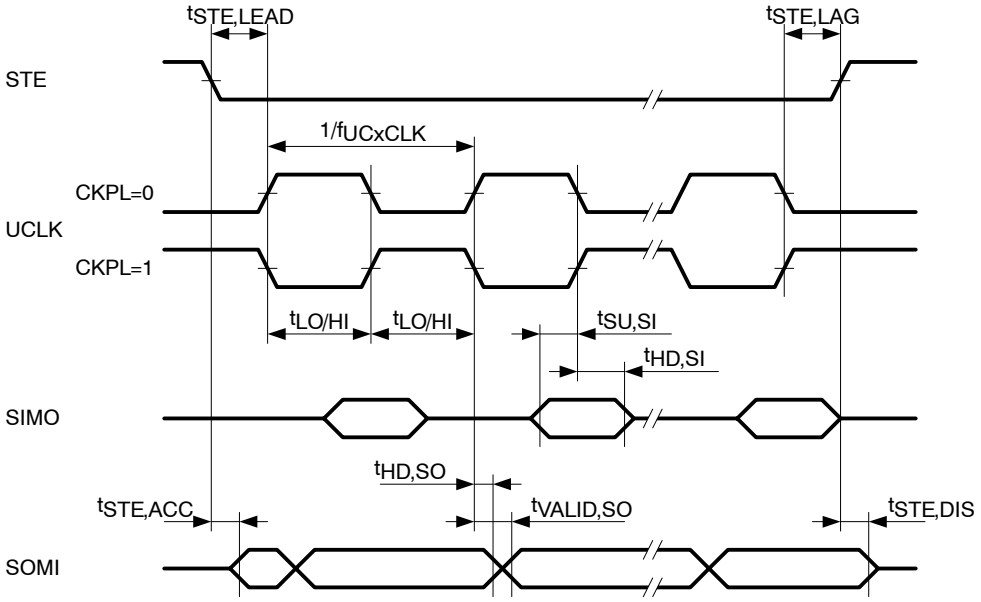



**Figure 23. SPI Slave Mode, CKPH = 0**

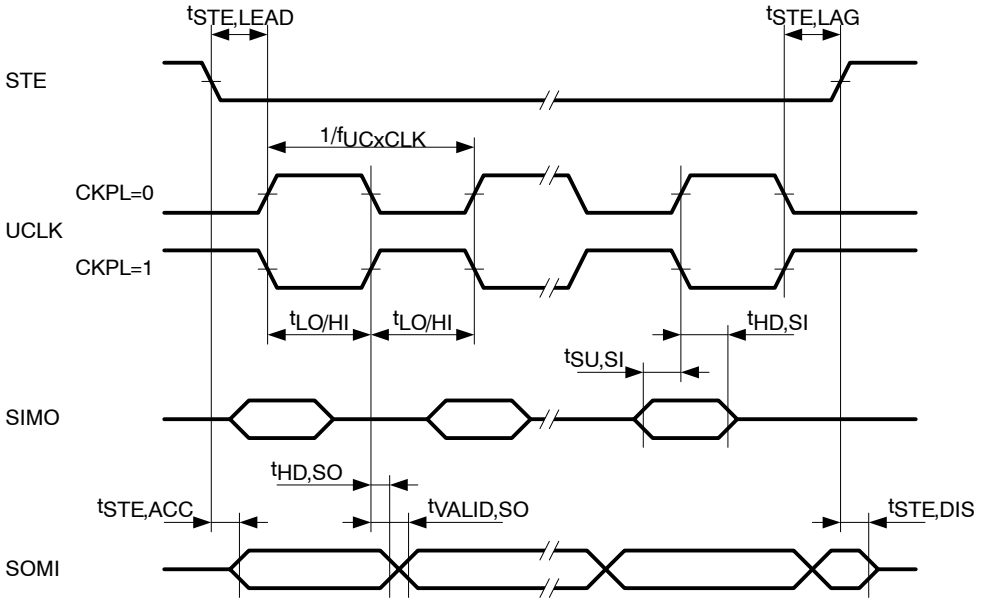



**Figure 24. SPI Slave Mode, CKPH = 1**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**USCI (I2C mode) (see Figure 25)**

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{USCI}$ | USCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2.2 V/3 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ ≤ 100kHz (standard mode) | 2.2 V/3 V | 4.0 | | | μs |
| | | $f_{SCL}$ > 100kHz (fast mode) | 2.2 V/3 V | 0.6 | | | μs |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ ≤ 100kHz (standard mode) | 2.2 V/3 V | 4.7 | | | μs |
| | | $f_{SCL}$ > 100kHz (fast mode) | 2.2 V/3 V | 0.6 | | | μs |
| $t_{HD,DAT}$ | Data hold time | | 2.2 V/3 V | 0 | | | ns |
| $t_{SU,DAT}$ | Data setup time | | 2.2 V/3 V | 250 | | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ ≤ 100kHz (standard mode) | 2.2 V/3 V | 4.0 | | | μs |
| | | $f_{SCL}$ > 100kHz (fast mode) | 2.2 V/3 V | 0.6 | | | μs |
| $t_{SP}$ | Pulse width of spikes suppressed by input filter | | 2.2 V | 50 | 150 | 600 | ns |
| | | | 3 V | 50 | 100 | 600 | ns |

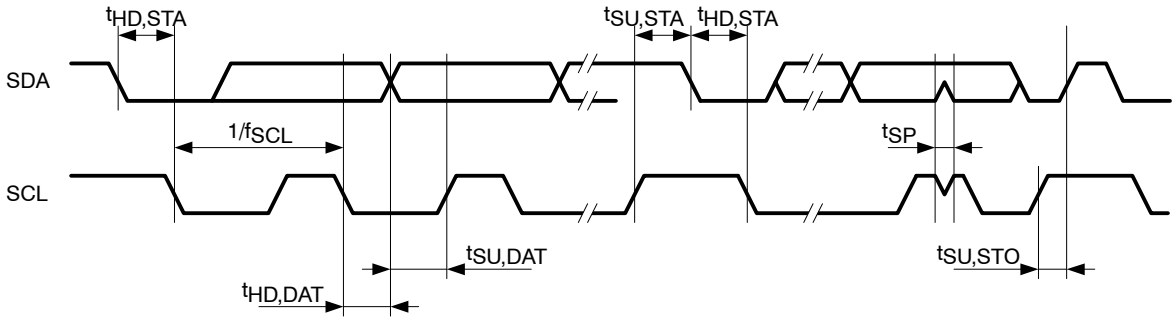



**Figure 25. I2C Mode Timing**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### SD16_A, power supply and recommended operating conditions

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC} = DV_{CC}$<br>$AV_{SS} = DV_{SS} = 0V$ | | | 2.5 | | 3.6 | V |
| $I_{SD16}$ | Analog supply current: 1 active SD16_A channel including internal reference | SD16LP = 0,<br>$f_{SD16}$ = 1 MHz,<br>SD16OSR = 256 | GAIN: 1,2 | 3 V | | 800 | 1100 | µA |
| | | | GAIN: 4,8,16 | 3 V | | 900 | 1200 | |
| | | | GAIN: 32 | 3 V | | 1200 | 1700 | |
| | | SD16LP = 1,<br>$f_{SD16}$ = 0.5 MHz,<br>SD16OSR = 256 | GAIN: 1 | 3 V | | 800 | 1100 | |
| | | | GAIN: 32 | 3 V | | 900 | 1200 | |
| $f_{SD16}$ | Analog front-end input clock frequency | SD16LP = 0 (low-power mode disabled) | | 3 V | 0.03 | 1 | 1.1 | MHz |
| | | SD16LP = 1 (low-power mode enabled) | | 3 V | 0.03 | 0.5 | | |

### SD16_A, input range (see Note 1)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{ID,FSR}$ | Differential full scale input voltage range | Bipolar mode, SD16UNI = 0 | | | $-V_{REF}/2GAIN$ | | $+V_{REF}/2GAIN$ | mV |
| | | Unipolar mode, SD16UNI = 1 | | | 0 | | $+V_{REF}/2GAIN$ | mV |
| $V_{ID}$ | Differential input voltage range for specified performance (see Note 2) | SD16REFON = 1 | SD16GAINx = 1 | | | ±500 | | mV |
| | | | SD16GAINx = 2 | | | ±250 | | |
| | | | SD16GAINx = 4 | | | ±125 | | |
| | | | SD16GAINx = 8 | | | ±62 | | |
| | | | SD16GAINx = 16 | | | ±31 | | |
| | | | SD16GAINx = 32 | | | ±15 | | |
| $Z_I$ | Input impedance (one input pin to $AV_{SS}$) | $f_{SD16}$ = 1 MHz | SD16GAINx = 1 | 3 V | | 200 | | kΩ |
| | | | SD16GAINx = 32 | 3 V | | 75 | | |
| $Z_{ID}$ | Differential input impedance (IN+ to IN–) | $f_{SD16}$ = 1 MHz | SD16GAINx = 1 | 3 V | 300 | 400 | | kΩ |
| | | | SD16GAINx = 32 | 3 V | 100 | 150 | | |
| $V_I$ | Absolute input voltage range | | | | $AV_{SS}$ -1V | | $AV_{CC}$ | V |
| $V_{IC}$ | Common-mode input voltage range | | | | $AV_{SS}$ -1V | | $AV_{CC}$ | V |

NOTES: 1. All parameters pertain to each SD16_A channel.
2. The full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR-} = -(V_{REF}/2)/GAIN$.
If $V_{REF}$ is sourced externally, the analog input range should not exceed 80% of $V_{FSR+}$ or $V_{FSR-}$; i.e., $V_{ID}$ = 0.8 $V_{FSR-}$ to 0.8 $V_{FSR+}$.
If $V_{REF}$ is sourced internally, the given $V_{ID}$ ranges apply.

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### SD16_A, performance ($f_{SD16}$ = 1 MHz, SD16OSRx = 256, SD16REFON = 1)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD16GAINx = 1, Signal amplitude $V_{PP}$ = 500 mV | $f_{IN}$ = 50 Hz, 100 Hz (see Note 1) | 3 V | 83 | 85 | | dB |
| | | SD16GAINx = 2, Signal amplitude $V_{PP}$ = 250 mV | | 3 V | 81 | 84 | | |
| | | SD16GAINx = 4, Signal amplitude $V_{PP}$ = 125 mV | | 3 V | 76 | 79 | | |
| | | SD16GAINx = 8, Signal amplitude $V_{PP}$ = 62 mV | | 3 V | 73 | 76 | | |
| | | SD16GAINx = 16, Signal amplitude $V_{PP}$ = 31 mV | | 3 V | 69 | 73 | | |
| | | SD16GAINx = 32, Signal amplitude $V_{PP}$ = 15 mV | | 3 V | 62 | 69 | | |
| G | Nominal gain | SD16GAINx = 1 | | 3 V | 0.97 | 1.00 | 1.02 | |
| | | SD16GAINx = 2 | | 3 V | 1.90 | 1.96 | 2.02 | |
| | | SD16GAINx = 4 | | 3 V | 3.76 | 3.86 | 3.96 | |
| | | SD16GAINx = 8 | | 3 V | 7.36 | 7.62 | 7.84 | |
| | | SD16GAINx = 16 | | 3 V | 14.56 | 15.04 | 15.52 | |
| | | SD16GAINx = 32 | | 3 V | 27.20 | 28.35 | 29.76 | |
| $E_{OS}$ | Offset error | SD16GAINx = 1 | | 3 V | | | ±0.2 | %FSR |
| | | SD16GAINx = 32 | | 3 V | | | ±1.5 | |
| $dE_{OS}/dT$ | Offset error temperature coefficient | SD16GAINx = 1 | | 3 V | | ±4 | ±20 | ppm FSR/°C |
| | | SD16GAINx = 32 | | 3 V | | ±20 | ±100 | |
| CMRR | Common-mode rejection ratio | SD16GAINx = 1, Common-mode input signal: $V_{ID}$ = 500 mV, $f_{IN}$ = 50 Hz, 100 Hz | | 3 V | | >90 | | dB |
| | | SD16GAINx = 32, Common-mode input signal: $V_{ID}$ = 16 mV, $f_{IN}$ = 50 Hz, 100 Hz | | 3 V | | >75 | | |
| AC PSRR | AC power supply rejection ratio | SD16GAINx = 1, $V_{CC}$ = 3 V ± 100 mV, $f_{VCC}$ = 50 Hz | | 3 V | | >80 | | dB |
| $X_T$ | Crosstalk | SD16GAINx = 1, $V_{ID}$ = 500 mV, $f_{IN}$ = 50 Hz, 100 Hz | | 3 V | | <–100 | | dB |

NOTE 1: The following voltages were applied to the SD16_A inputs:
$V_{IN,A+}(t) = 0V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{IN,A-}(t) = 0V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{diff} = V_{IN,A+}(t) - V_{IN,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### typical characteristics – SD16_A SINAD performance over OSR

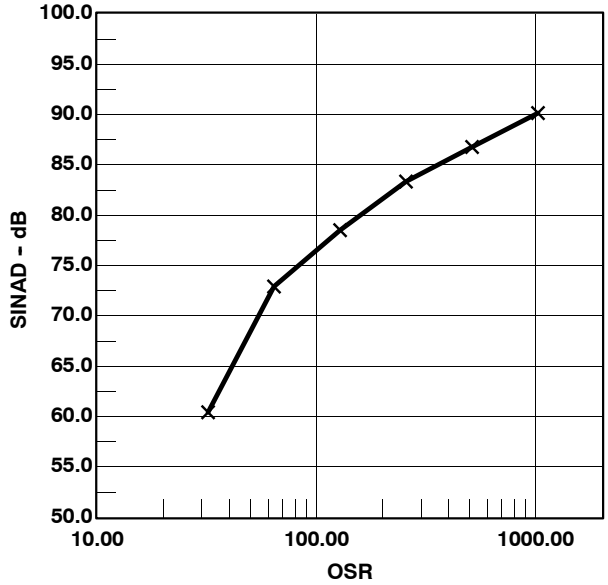



**Figure 26. SINAD performance over OSR, $f_{SD16}$ = 1 MHz, SD16REFON = 1, SD16GAINx = 1**

### SD16_A, temperature sensor and built-in $V_{CC}$ sense

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $TC_{Sensor}$ | Sensor temperature coefficient | | | 1.18 | 1.32 | 1.46 | mV/K |
| $V_{Offset,sensor}$ | Sensor offset voltage | | | –100 | | 100 | mV |
| $V_{Sensor}$ | Sensor output voltage (see Note 2) | Temperature sensor voltage at $T_A$ = 85°C | 3 V | 435 | 475 | 515 | mV |
| | | Temperature sensor voltage at $T_A$ = 25°C | 3 V | 355 | 395 | 435 | |
| | | Temperature sensor voltage at $T_A$ = 0°C | 3 V | 320 | 360 | 400 | |
| $V_{CC,Sense}$ | $V_{CC}$ divider at input 5 | $f_{SD16}$ = 1 MHz, SD16OSRx = 256, SD16REFON = 1 | | 0.08 | 1/11 | 0.1 | $V_{CC}$ |
| $R_{Source,VCC}$ | Source resistance of $V_{CC}$ divider at input 5 | | | | 20 | | kΩ |

NOTES: 1. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ ( 273 + T [°C] ) + $V_{Offset,sensor}$ [mV]
2. Results based on characterization and/or production test, not $TC_{Sensor}$ or $V_{Offset,sensor}$. Measured with $f_{SD16}$ = 1 MHz, SD16OSRx = 256, SD16REFON = 1.

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### SD16_A, built-in voltage reference

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF}$ | Internal reference voltage | SD16REFON = 1, SD16VMIDON = 0 | 3 V | 1.14 | 1.20 | 1.26 | V |
| $I_{REF}$ | Reference supply current | SD16REFON = 1, SD16VMIDON = 0 | 3 V | | 175 | 260 | μA |
| TC | Temperature coefficient | SD16REFON = 1, SD16VMIDON = 0 (see Note 1) | 3 V | | 18 | 50 | ppm/°C |
| $C_{REF}$ | $V_{REF}$ load capacitance | SD16REFON = 1, SD16VMIDON = 0 (see Note 2) | | | 100 | | nF |
| $I_{LOAD}$ | $V_{REF(I)}$ maximum load current | SD16REFON = 1, SD16VMIDON = 0 | 3 V | | | ±200 | nA |
| $t_{ON}$ | Turn-on time | SD16REFON = 0->1, SD16VMIDON = 0, $C_{REF}$ = 100nF | 3 V | | 5 | | ms |
| DC PSR | DC power supply rejection $\Delta V_{REF}/\Delta V_{CC}$ | SD16REFON = 1, SD16VMIDON = 0, $V_{CC}$ = 2.5 V to 3.6 V | | | 100 | | uV/V |

NOTES: 1. Calculated using the box method: (MAX(-40...85°C) – MIN(-40...85°C)) / MIN(–40...85°C) / (85°C – (-40°C))
2. There is no capacitance required on $V_{REF}$. However, a capacitance of at least 100 nF is recommended to reduce any reference voltage noise.

### SD16_A, reference output buffer

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF,BUF}$ | Reference buffer output voltage | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | 1.2 | | V |
| $I_{REF,BUF}$ | Reference supply + reference output buffer quiescent current | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | 385 | 600 | μA |
| $C_{REF(O)}$ | Required load capacitance on $V_{REF}$ | SD16REFON = 1, SD16VMIDON = 1 | | 470 | | | nF |
| $I_{LOAD,Max}$ | Maximum load current on $V_{REF}$ | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | | ±1 | mA |
| | Maximum voltage variation vs load current | $\|I_{LOAD}\|$ = 0 to 1mA | 3 V | –15 | | +15 | mV |
| $t_{ON}$ | Turn-on time | SD16REFON = 0->1, SD16VMIDON = 0->1, $C_{REF}$ = 470nF | 3 V | | 100 | | μs |

### SD16_A, external reference input

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF(I)}$ | Input voltage range | SD16REFON = 0 | 3 V | 1.0 | 1.25 | 1.5 | V |
| $I_{REF(I)}$ | Input current | SD16REFON = 0 | 3 V | | | 50 | nA |

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

### flash memory

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | | 2.2 | | 3.6 | V |
| $f_{FTG}$ | Flash timing generator frequency | | | 257 | | 476 | kHz |
| $I_{PGM}$ | Supply current from $V_{CC}$ during program | | 2.2 V/3.6 V | | 3 | 5 | mA |
| $I_{ERASE}$ | Supply current from $V_{CC}$ during erase | | 2.2 V/3.6 V | | 3 | 7 | mA |
| $t_{CPT}$ | Cumulative program time (see Note 1) | | 2.2 V/3.6 V | | | 10 | ms |
| $t_{CMErase}$ | Cumulative mass erase time | | 2.2 V/3.6 V | 20 | | | ms |
| | Program/Erase endurance | | | $10^4$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | | 100 | | | years |
| $t_{Word}$ | Word or byte program time | see Note 2 | | | 30 | | $t_{FTG}$ |
| $t_{Block, 0}$ | Block program time for 1st byte or word | | | | 25 | | $t_{FTG}$ |
| $t_{Block, 1-63}$ | Block program time for each additional byte or word | | | | 18 | | $t_{FTG}$ |
| $t_{Block, End}$ | Block program end-sequence wait time | | | | 6 | | $t_{FTG}$ |
| $t_{Mass Erase}$ | Mass erase time | | | | 10593 | | $t_{FTG}$ |
| $t_{Seg Erase}$ | Segment erase time | | | | 4819 | | $t_{FTG}$ |
| $f_{MCLK,MGR}$ | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | | 0 | | 1 | MHz |

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

### RAM

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{(RAMh)}$ | RAM retention supply voltage (see Note 1) | CPU halted | 1.6 | | V |

NOTE 1: This parameter defines the minimum supply voltage $V_{CC}$ when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

### JTAG interface

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TCK}$ | TCK input frequency | See Note 1 | 2.2 V | 0 | | 5 | MHz |
| | | | 3 V | 0 | | 10 | MHz |
| $R_{Internal}$ | Internal pullup resistance on TMS, TCK, TDI/TCLK | See Note 2 | 2.2 V/ 3 V | 25 | 40 | 90 | kΩ |

NOTES: 1. $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

### JTAG fuse (see Note 1)

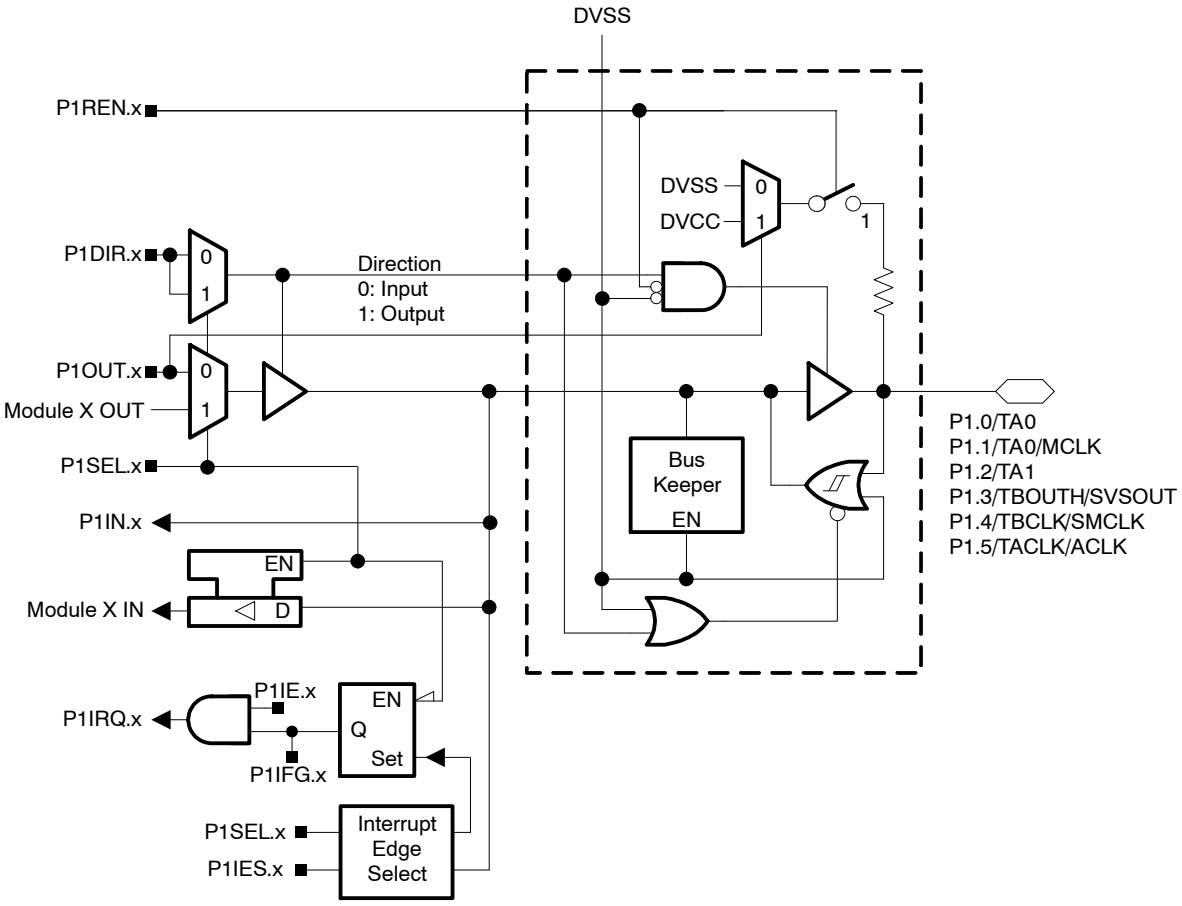
| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(FB)}$ | Supply voltage during fuse-blow condition | $T_A$ = 25°C | | 2.5 | | | V |
| $V_{FB}$ | Voltage level on TDI/TCLK for fuse-blow: F versions | | | 6 | | 7 | V |
| $I_{FB}$ | Supply current into TDI/TCLK during fuse blow | | | | | 100 | mA |
| $t_{FB}$ | Time to blow fuse | | | | | 1 | ms |

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/test and emulation features is possible. The JTAG block is switched to bypass mode.

## APPLICATION INFORMATION

### input/output schematics

#### Port P1, P1.0 to P1.5, input/output with Schmitt trigger

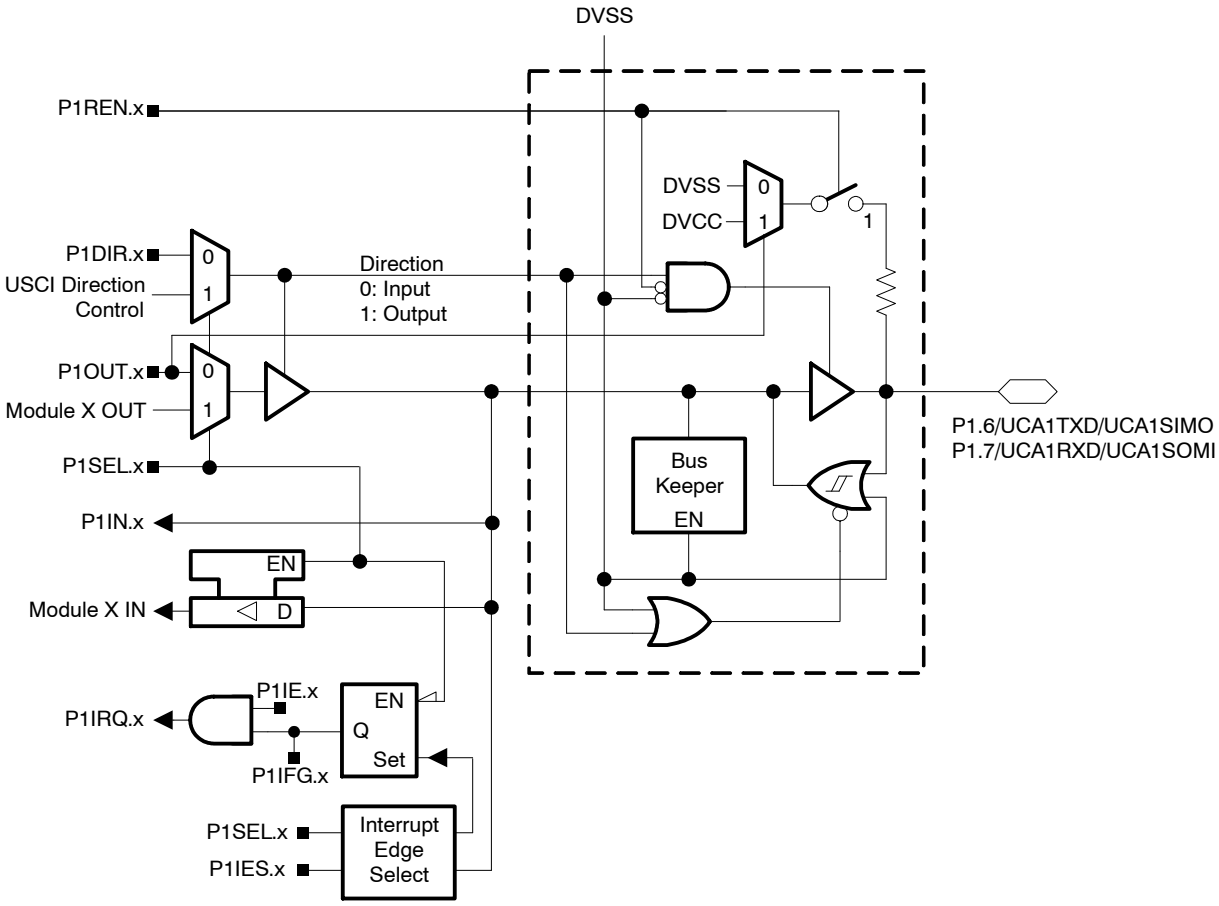


### Port P1 (P1.0 to P1.5) pin functions

| PIN NAME (P1.X) | X | FUNCTION | CONTROL BITS / SIGNALS | |
|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x |
| P1.0/TA0 | 0 | P1.0 (I/O) | I: 0, O: 1 | 0 |
| | | Timer_A3.CCI0A | 0 | 1 |
| | | Timer_A3.TA0 | 1 | 1 |
| P1.1/TA0/MCLK | 1 | P1.1 (I/O) | I: 0, O: 1 | 0 |
| | | Timer_A3.CCI0B | 0 | 1 |
| | | MCLK | 1 | 1 |
| P1.2/TA1 | 2 | P1.2 (I/O) | I: 0, O: 1 | 0 |
| | | Timer_A3.CCI1A | 0 | 1 |
| | | Timer_A3.TA1 | 1 | 1 |
| P1.3/ TBOUTH/SVSOUT | 3 | P1.3 (I/O) | I: 0, O: 1 | 0 |
| | | Timer_B7.TBOUTH | 0 | 1 |
| | | SVSOUT | 1 | 1 |
| P1.4/TBCLK/SMCLK | 4 | P1.4 (I/O) | I: 0, O: 1 | 0 |
| | | Timer_B7.TBCLK | 0 | 1 |
| | | SMCLK | 1 | 1 |
| P1.5/TACLK/ACLK | 5 | P1.5 (I/O) | I: 0, O: 1 | 0 |
| | | Timer_A3.TACLK | 0 | 1 |
| | | ACLK | 1 | 1 |

NOTES: 1. X: Don’t care

### Port P1, P1.6 and P1.7, input/output with Schmitt trigger

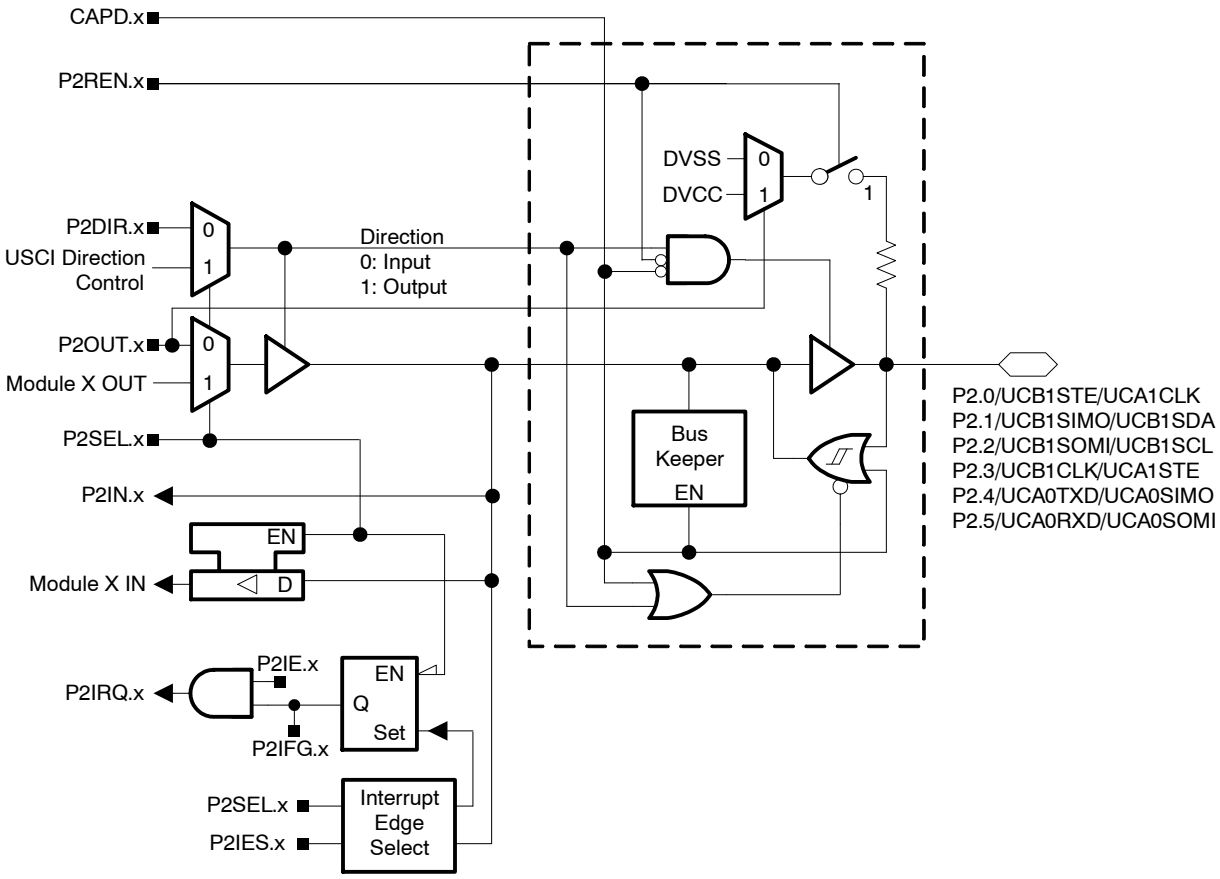



### Port P1 (P1.6 and P1.7) pin functions

| PIN NAME (P1.X) | X | FUNCTION | CONTROL BITS / SIGNALS | |
|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x |
| P1.6/ UCA1TXD/UCA1SIMO | 4 | P1.6 (I/O) | I: 0, O: 1 | 0 |
| | | UCA1TXD/UCA1SIMO (see Note 1, 2) | X | 1 |
| P1.7/ UCA1RXD/UCA1SOMI | 5 | P1.7 (I/O) | I: 0, O: 1 | 0 |
| | | UCA1RXD/UCA1SOMI (see Note 1, 2) | X | 1 |

NOTES: 1. X: Don't care
2. The pin direction is controlled by the USCI module.

### Port P2, P2.0 to P2.5, input/output with Schmitt trigger

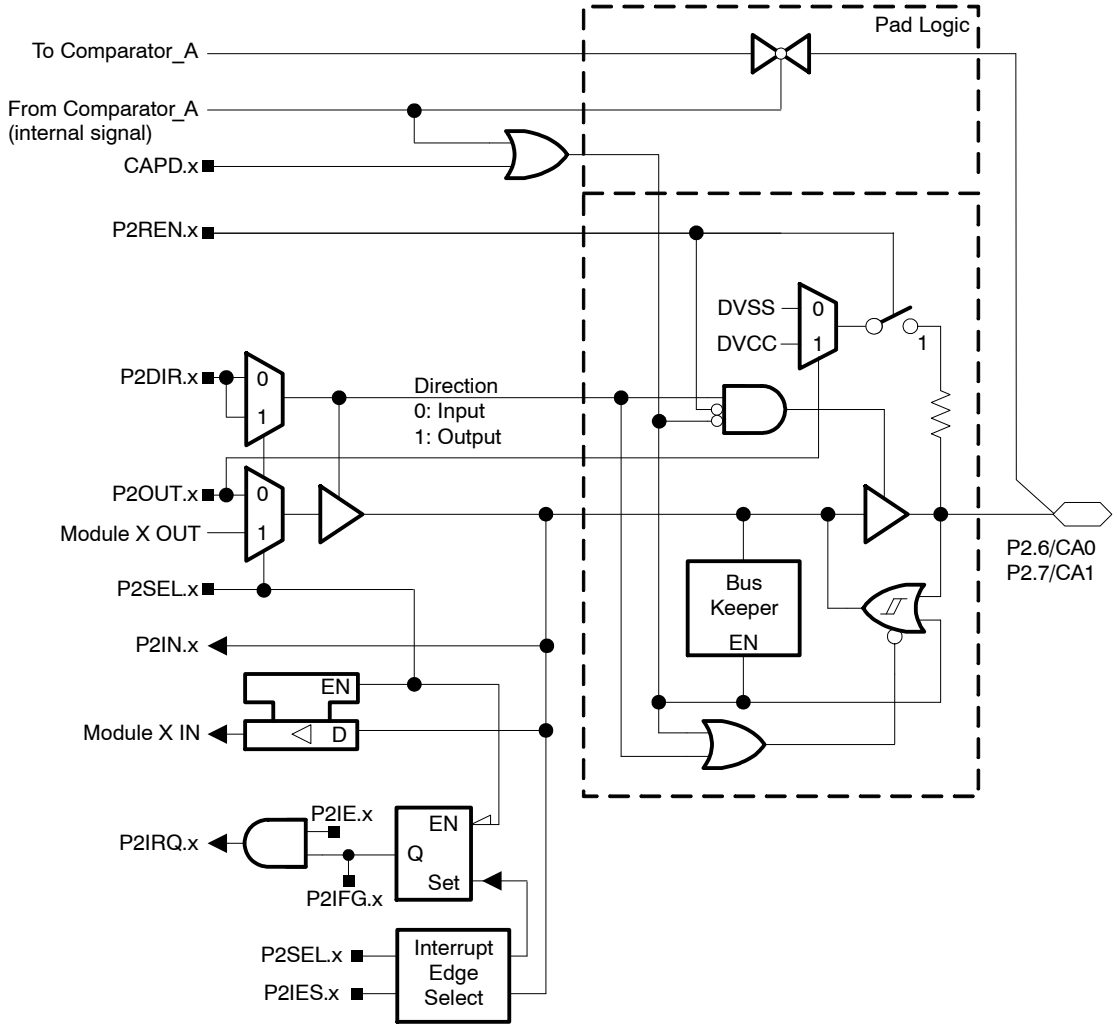


### Port P2 (P2.0 to P2.5) pin functions

| PIN NAME (P2.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | CAPD.x |
| P2.0/ UCB1STE/UCA1CLK | 4 | P2.0 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | UCB1STE/UCA1CLK (see Note 1, 2, 3) | X | 1 | 0 |
| | | Input buffer disabled (see Note 6) | X | X | 1 |
| P2.1/ UCB1SIMO/UCB1SDA | 4 | P2.1 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | UCB1SIMO/UCB1SDA (see Note 1, 2, 4) | X | 1 | 0 |
| | | Input buffer disabled (see Note 6) | X | X | 1 |
| P2.2/ UCB1SOMI/UCB1SCL | 4 | P2.2 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | UCB1SOMI/UCB1SCL (see Note 1, 2, 4) | X | 1 | 0 |
| | | Input buffer disabled (see Note 6) | X | X | 1 |
| P2.3/ UCB1CLK/UCA1STE | 4 | P2.3 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | UCB1CLK/UCA1STE (see Note 1, 2, 5) | X | 1 | 0 |
| | | Input buffer disabled (see Note 6) | X | X | 1 |
| P2.4/ UCA0TXD/UCA0SIMO | 4 | P2.4 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | UCA0TXD/UCA0SIMO (see Note 1, 2) | X | 1 | 0 |
| | | Input buffer disabled (see Note 6) | X | X | 1 |
| P2.5/ UCA0RXD/UCA0SOMI | 5 | P2.5 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | UCA0RXD/UCA0SOMI (see Note 1, 2) | X | 1 | 0 |
| | | Input buffer disabled (see Note 6) | X | X | 1 |

NOTES:
1. X: Don't care
2. The pin direction is controlled by the USCI module.
3. UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output USCI_B1 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.
4. In case the I2C functionality is selected the output drives only the logical 0 to $V_{SS}$ level.
5. UCB1CLK function takes precedence over UCA1STE function. If the pin is required as UCB1CLK input or output USCI_A1 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.
6. Setting the CAPD.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

### Port P2, P2.6 and P2.7, input/output with Schmitt trigger

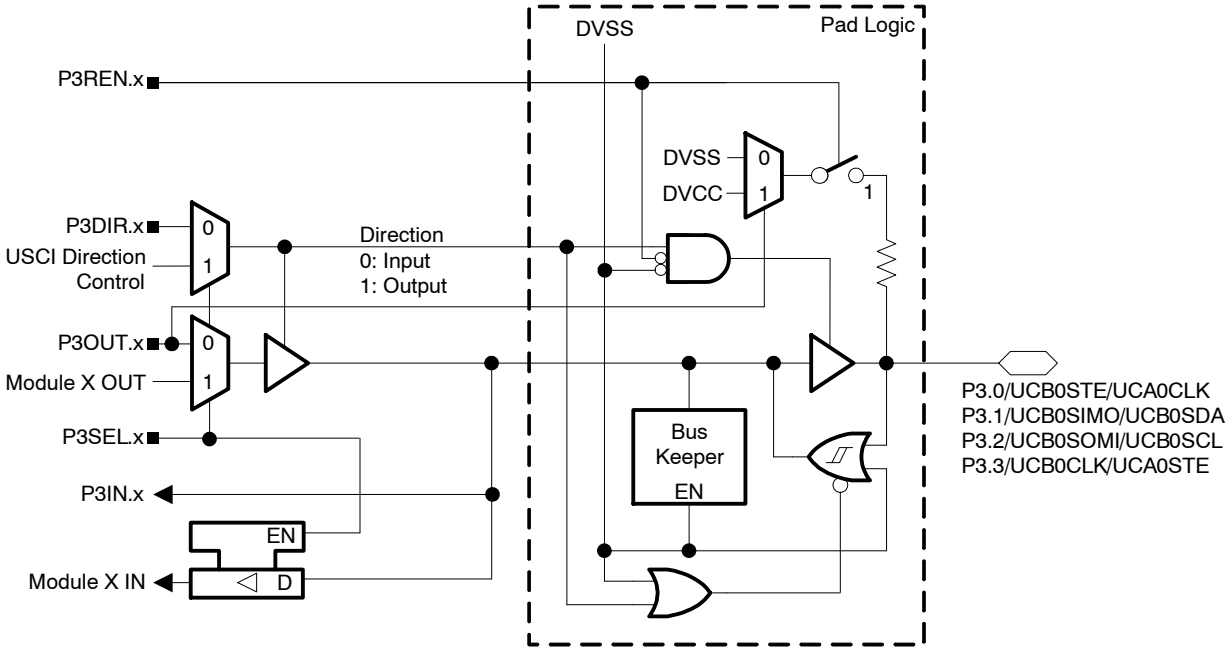



### Port P2 (P2.6 and P2.7) pin functions

| PIN NAME (P2.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | CAPD.x |
| P2.6/CA0 | 6 | P2.6 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | CA0 (see Note 3) | X | X | 1 |
| P2.7/CA1 | 7 | P2.7 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | CA1 (see Note 3) | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.
3. Setting the CAPD.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

### Port P3, P3.0 to P3.3, input/output with Schmitt trigger

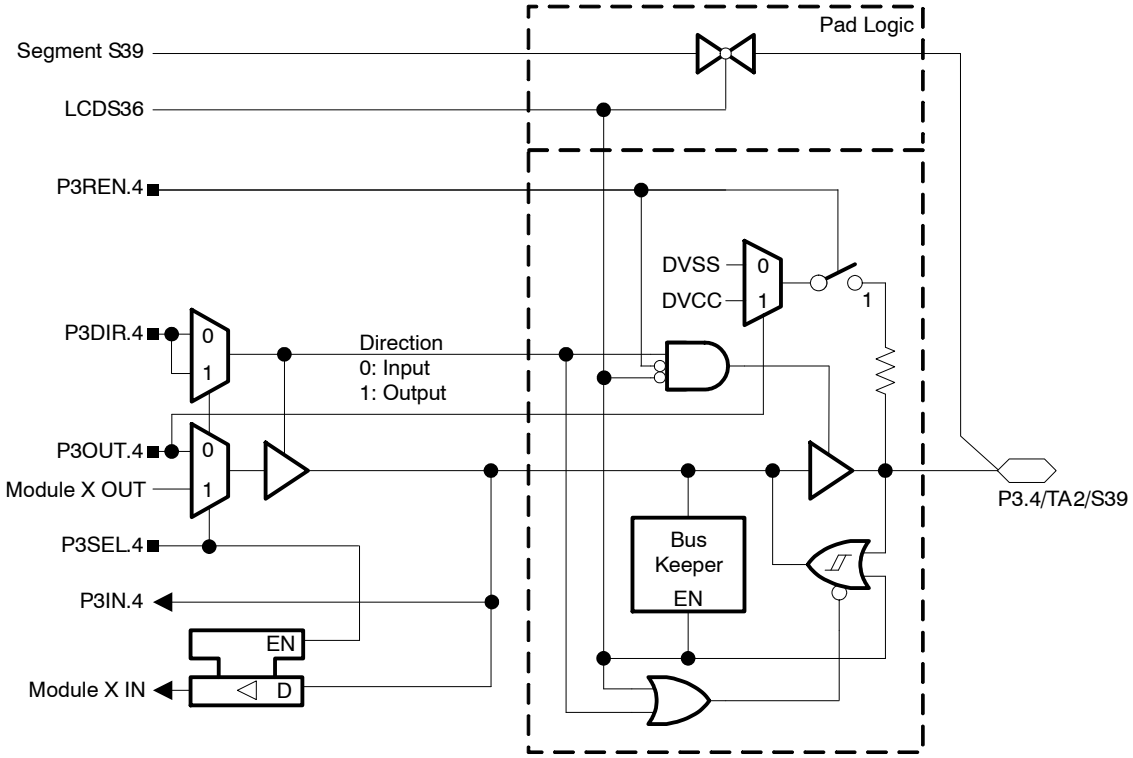



### Port P3 (P3.0 to P3.3) pin functions

| PIN NAME (P3.X) | X | FUNCTION | CONTROL BITS / SIGNALS | |
|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x |
| P3.0/ UCA0CLK/UCB0STE | 0 | P3.0 (I/O) | I: 0, O: 1 | 0 |
| | | UCA0CLK/UCB0STE (see Notes 1, 2, 3) | X | 1 |
| P3.1/ UCB0SIMO/ UCB0SDA | 1 | P3.1 (I/O) | I: 0, O: 1 | 0 |
| | | UCB0SIMO/UCB0SDA (see Notes 1, 2, 4) | X | 1 |
| P3.2/ UCB0SOMI/ UCB0SCL | 2 | P3.2 (I/O) | I: 0, O: 1 | 0 |
| | | UCB0SOMI/UCB0SCL (see Notes 1, 2, 4) | X | 1 |
| P3.3/ UCB0CLK/UCA0STE | 3 | P3.3 (I/O) | I: 0, O: 1 | 0 |
| | | UCB0CLK/UCA0STE (see Notes 1, 2, 5) | X | 1 |

NOTES: 1. X: Don't care
2. The pin direction is controlled by the USCI module.
3. UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output USCI_B0 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.
4. In case the I2C functionality is selected the output drives only the logical 0 to $V_{SS}$ level.
5. UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output USCI_A0 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

### Port P3, P3.4, input/output with Schmitt trigger

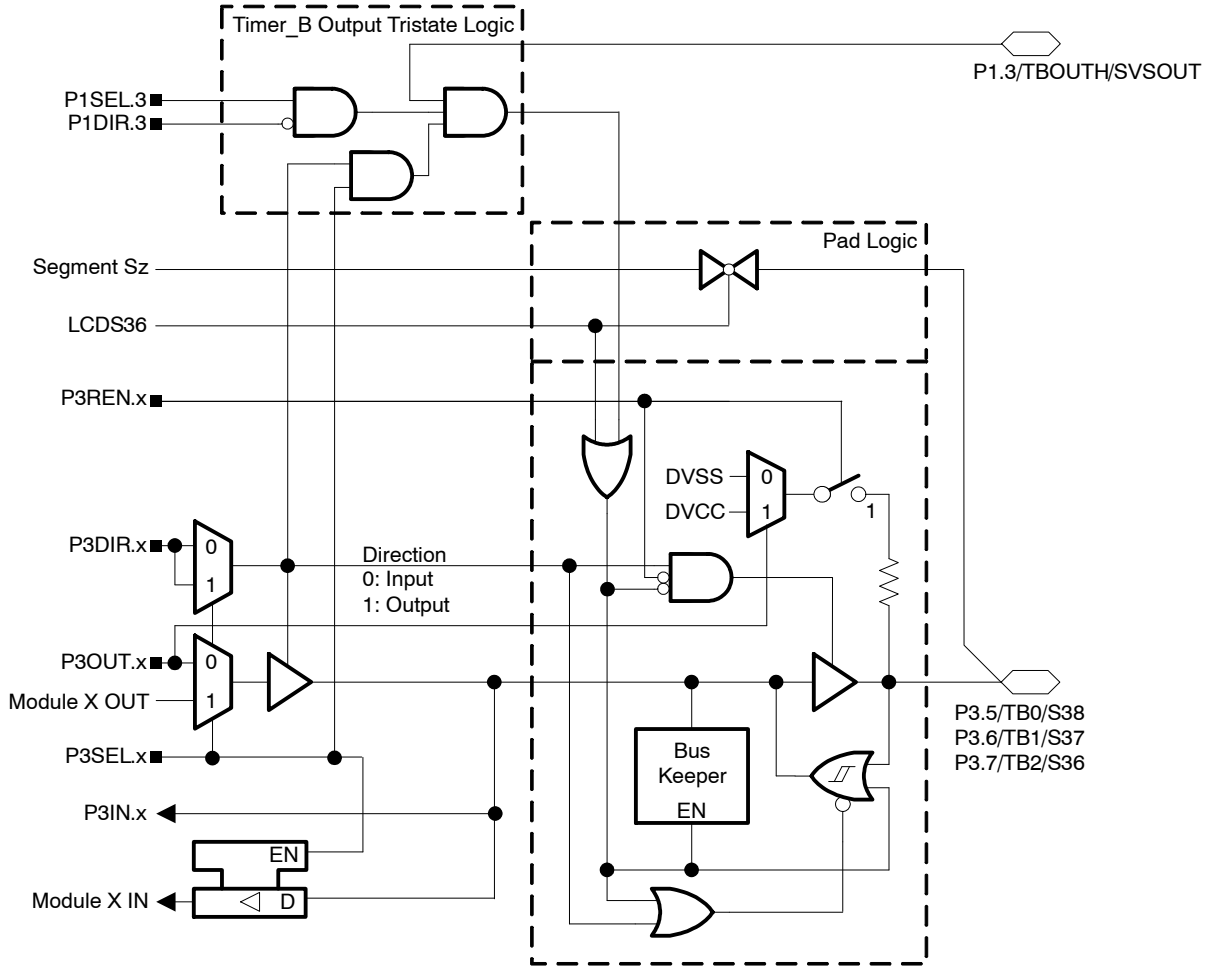



### Port P3 (P3.4) pin functions

| PIN NAME (P3.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x | LCDS36 |
| P3.4/TA2/S39 | 4 | P3.4 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | Timer_A3.CCI2A | 0 | 1 | 0 |
| | | Timer_A3.TA2 | 1 | 1 | 0 |
| | | S39 | X | X | 1 |

NOTES: 1. X: Don't care

### Port P3, P3.5 to P3.7, input/output with Schmitt trigger

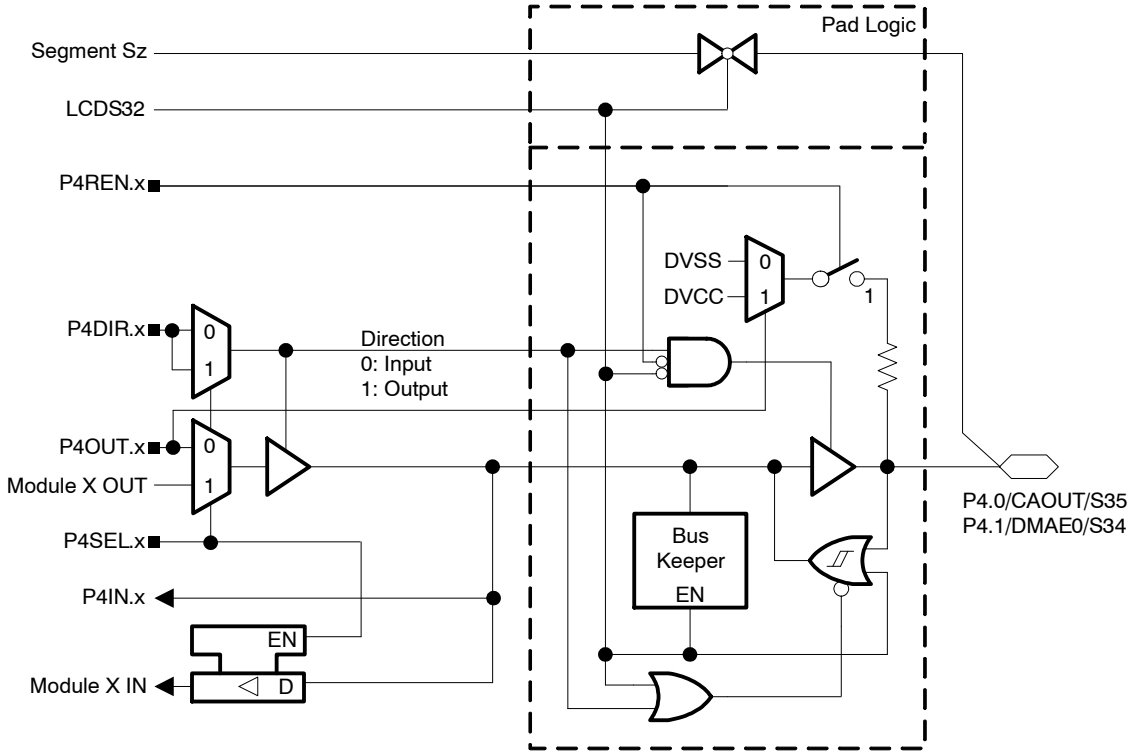



### Port P3 (P3.5 to P3.7) pin functions

| PIN NAME (P3.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x | LCDS36 |
| P3.5/TB0/S38 | 5 | P3.5 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | Timer_B3.CCI0A and Timer_B3.CCI0B | 0 | 1 | 0 |
| | | Timer_B3.TB0 (see Note 2) | 1 | 1 | 0 |
| | | S38 | X | X | 1 |
| P3.6/TB1/S37 | 6 | P3.6 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | Timer_B3.CCI1A and Timer_B3.CCI1B | 0 | 1 | 0 |
| | | Timer_B3.TB1 (see Note 2) | 1 | 1 | 0 |
| | | S37 | X | X | 1 |
| P3.7/TB2/S36 | 7 | P3.7 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | Timer_B3.CCI2A and Timer_B3.CCI2B | 0 | 1 | 0 |
| | | Timer_B3.TB3 (see Note 2) | 1 | 1 | 0 |
| | | S36 | X | X | 1 |

NOTES: 1. X: Don't care
2. Setting TBOUTH causes all Timer_B outputs to be set to high impedance.

### Port P4, P4.0 and P4.1, input/output with Schmitt trigger

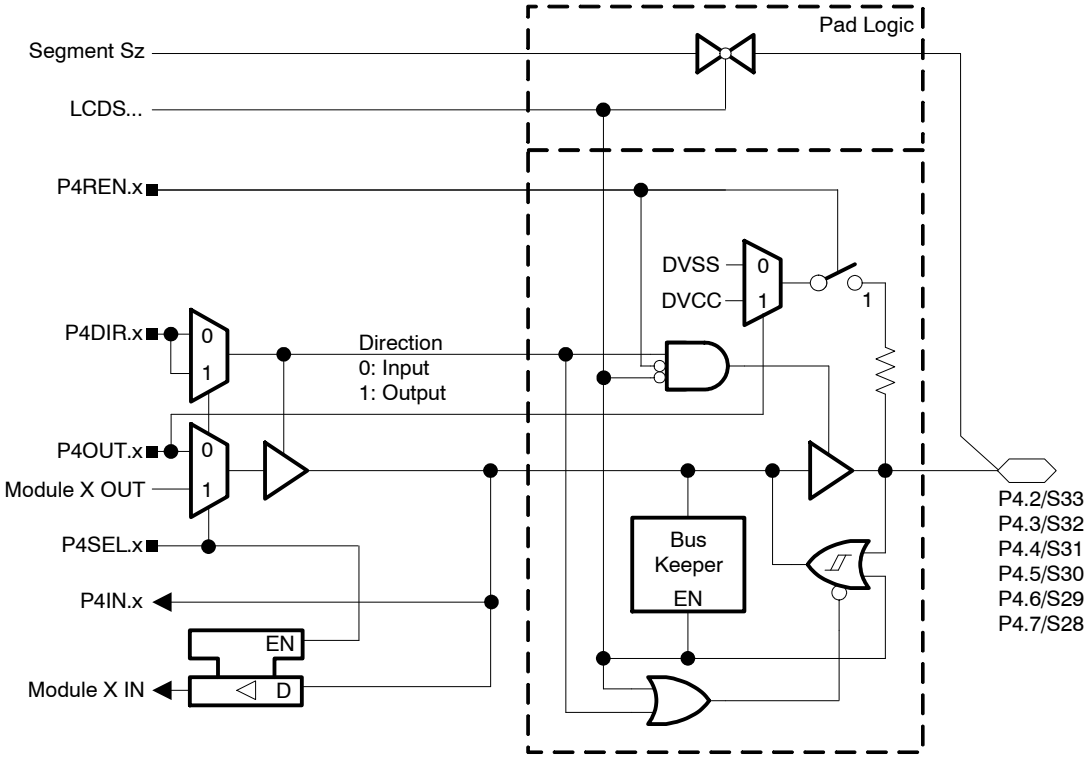



### Port P4 (P4.0 and P4.1) pin functions

| PIN NAME (P4.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL.x | LCDS32 |
| P4.0/CAOUT/S35 | 0 | P4.0 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | CAOUT | 1 | 1 | 0 |
| | | S35 | X | X | 1 |
| P4.1/DMAE0/S34 | 1 | P4.1 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | DMAE0 | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S34 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

**Port P4, P4.2 to P4.7, input/output with Schmitt trigger**



### Port P4 (P4.2 and P4.3) pin functions

| PIN NAME (P4.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL.x | LCDS32 |
| P4.2/S33 | 2 | P4.2 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S33 | X | X | 1 |
| P4.3/S32 | 3 | P4.3 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S32 | X | X | 1 |

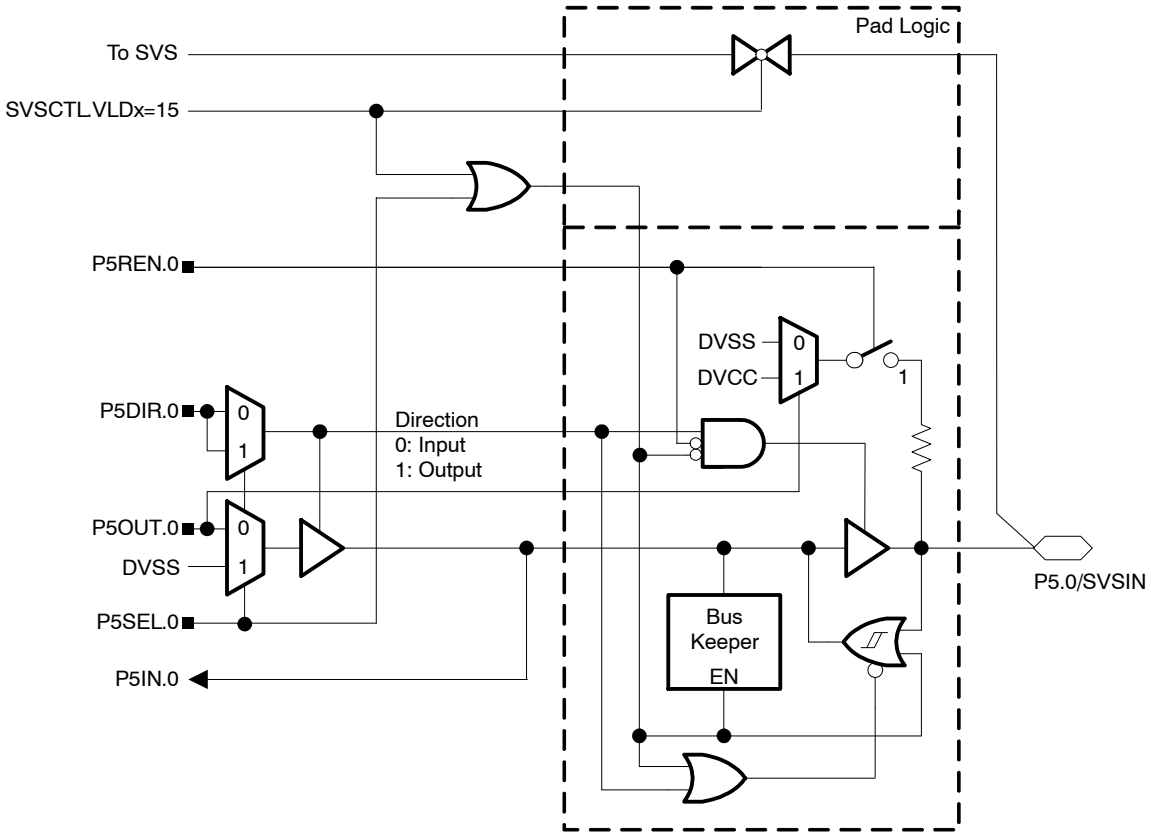
NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P4 (P4.4 to P4.7) pin functions

| PIN NAME (P4.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL.x | LCDS28 |
| P4.4/S31 | 4 | P4.4 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S31 | X | X | 1 |
| P4.5/S30 | 5 | P4.5 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S30 | X | X | 1 |
| P4.6/S29 | 5 | P4.6 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S29 | X | X | 1 |
| P4.7/S28 | 5 | P4.7 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S28 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P5, P5.0, input/output with Schmitt trigger

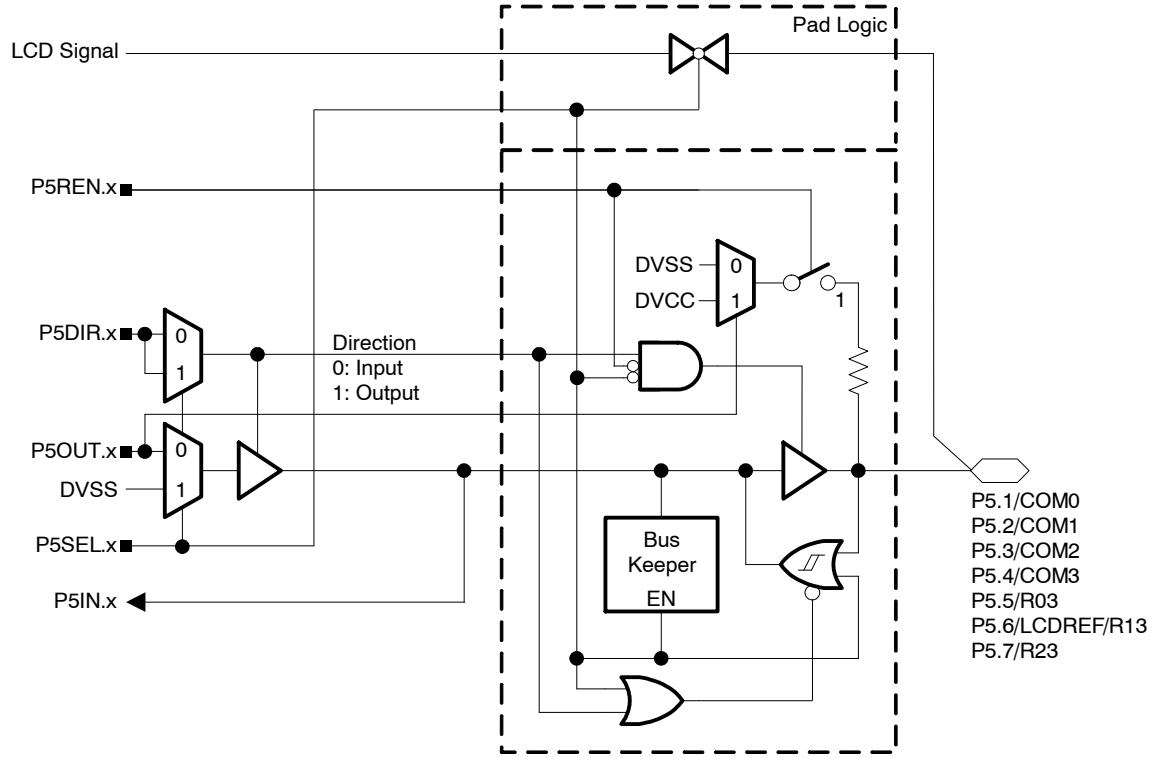



### Port P5 (P5.0) pin functions

| PIN NAME (P5.X) | X | FUNCTION | CONTROL BITS / SIGNALS | |
|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x |
| P5.0/SVSIN | 0 | P5.0 (I/O) (see Note 1) | I: 0, O: 1 | 0 |
| | | SVSIN (see Notes 1 and 3) | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.
3. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. To enable the SVSIN function the SVS input also needs to be selected in the SVS module by setting the VLDx bits to 15.

### Port P5, P5.1 to P5.7, input/output with Schmitt trigger

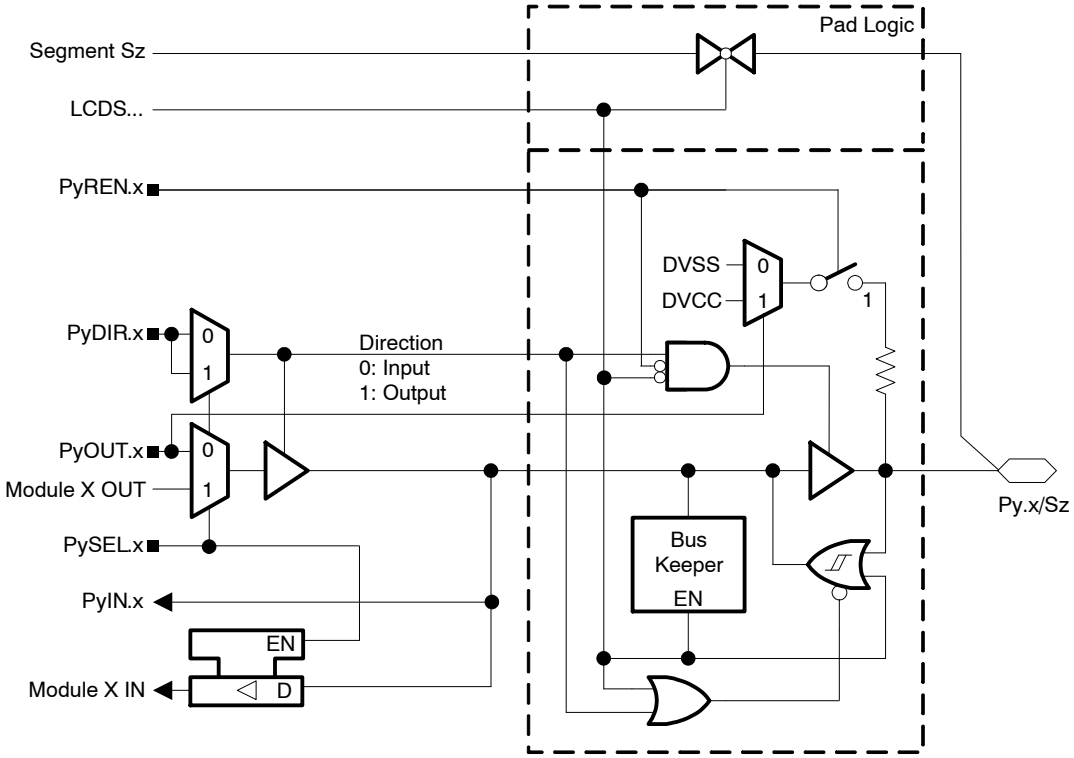



### Port P5 (P5.1 to P5.7) pin functions

| PIN NAME (P5.X) | X | FUNCTION | CONTROL BITS / SIGNALS | |
|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x |
| P5.1/COM0 | 2 | P5.1 (I/O) | I: 0, O: 1 | 0 |
| | | COM0 (see Note 2) | X | 1 |
| P5.2/COM1 | 2 | P5.2 (I/O) | I: 0, O: 1 | 0 |
| | | COM1 (see Note 2) | X | 1 |
| P5.3/COM2 | 3 | P5.3 (I/O) | I: 0, O: 1 | 0 |
| | | COM2 (see Note 2) | X | 1 |
| P5.4/COM3 | 4 | P5.4 (I/O) | I: 0, O: 1 | 0 |
| | | COM3 (see Note 2) | X | 1 |
| P5.5/R03 | 5 | P5.5 (I/O) | I: 0, O: 1 | 0 |
| | | R03 (see Note 2) | X | 1 |
| P5.6/LCDREF/R13 | 6 | P5.6 (I/O) | I: 0, O: 1 | 0 |
| | | R13 or LCDREF (see Notes 2 and 3) | X | 1 |
| P5.7/R23 | 7 | P5.7 (I/O) | I: 0, O: 1 | 0 |
| | | R23 (see Note 2) | X | 1 |

NOTES: 1. X: Don't care
2. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
3. External reference for the LCD_A charge pump is applied when VLCDREFx = 01. Otherwise R13 is selected.

**Port P7 to port P10, input/output with Schmitt trigger**



### Port P7 (P7.0 to P7.3) pin functions

| PIN NAME (P7.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL.x | LCDS24 |
| P7.0/S27 | 0 | P7.0 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S27 | X | X | 1 |
| P7.1/S26 | 1 | P7.1 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S26 | X | X | 1 |
| P7.2/S25 | 2 | P7.2 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S25 | X | X | 1 |
| P7.3/S24 | 3 | P7.3 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S24 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P7 (P7.4 to P7.7) pin functions

| PIN NAME (P7.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL.x | LCDS20 |
| P7.4/S23 | 4 | P7.4 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P7.5/S22 | 5 | P7.5 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P7.6/S21 | 6 | P7.6 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P7.7/S20 | 7 | P7.7 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S20 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P8 (P8.0 to P8.3) pin functions

| PIN NAME (P8.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL.x | LCDS16 |
| P8.0/S19 | 0 | P8.0 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P8.1/S18 | 1 | P8.0 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P8.2/S17 | 2 | P8.2 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S17 | X | X | 1 |
| P8.3/S16 | 3 | P8.3 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P8 (P8.4 to P8.7) pin functions

| PIN NAME (P8.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL.x | LCDS12 |
| P8.4/S15 | 4 | P8.4 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P8.5/S14 | 5 | P8.5 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P8.6/S13 | 6 | P8.6 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P8.7/S12 | 7 | P8.7 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P9 (P9.0 to P9.3) pin functions

| PIN NAME (P9.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL.x | LCDS8 |
| P9.0/S11 | 0 | P9.0 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P9.1/S10 | 1 | P9.1 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P9.2/S9 | 2 | P9.2 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |
| P9.3/S8 | 3 | P9.3 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P9 (P9.4 to P9.7) pin functions

| PIN NAME (P9.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL.x | LCDS4 |
| P9.4/S7 | 4 | P9.4 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P9.5/S6 | 5 | P9.5 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P9.6/S5 | 6 | P9.6 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P9.7/S4 | 7 | P9.7 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |

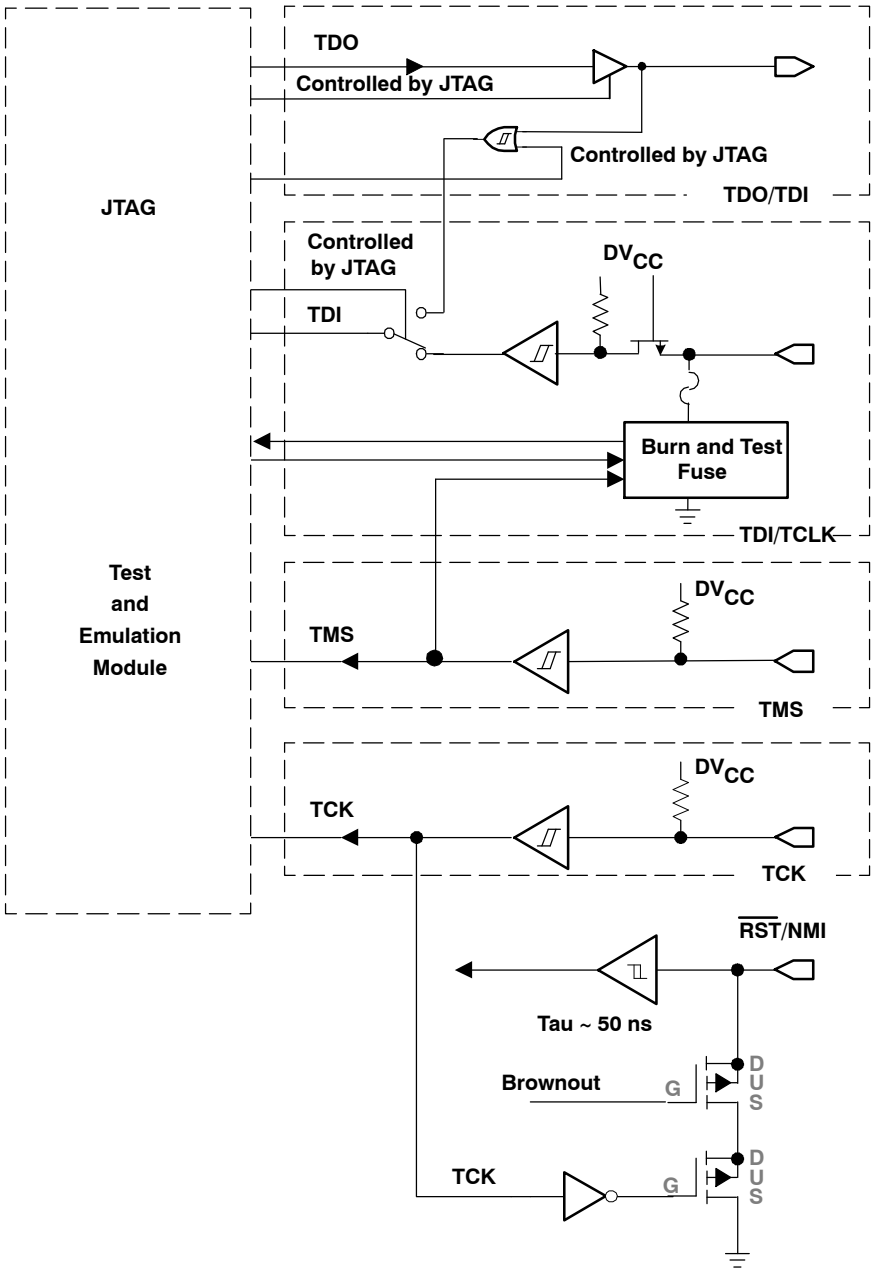
NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### Port P10 (P10.0 to P10.3) pin functions

| PIN NAME (P10.X) | X | FUNCTION | CONTROL BITS / SIGNALS | | |
|---|---|---|---|---|---|
| | | | P10DIR.x | P10SEL.x | LCDS0 |
| P10.0/S3 | 0 | P10.0 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P10.1/S2 | 1 | P10.1 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P10.2/S1 | 2 | P10.2 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |
| P10.3/S0 | 3 | P10.3 (I/O) | I: 0, O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.

### JTAG pins (TMS, TCK, TDI/TCLK, TDO/TDI), input/output with Schmitt trigger or output



### JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 27). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

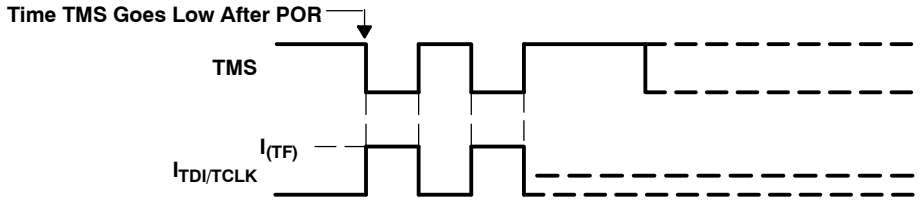



**Figure 27. Fuse Check Mode Current MSP430F471x3/6/7**

## Data Sheet Revision History

| LITERATURE NUMBER | SUMMARY |
|---|---|
| SLAS626 | Product Preview release |
| SLAS626A | Production Data release |
| SLAS626B | Added MSP430F471x3, MSP430F47126, and MSP430F47127 devices |
| SLAS626C | Corrected pin numbers in BSL function table (page 16)<br>Changed limits on $t_{d(SVSon)}$ parameter (page 38) |

NOTE: Page and figure numbers refer to the respective document revision and may differ in other revisions.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F47126IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47126 | Samples |
| MSP430F47126IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47126 | Samples |
| MSP430F47127IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47127 | Samples |
| MSP430F47127IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47127 | Samples |
| MSP430F47163IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47163 | Samples |
| MSP430F47163IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47163 | Samples |
| MSP430F47166IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47166 REV # | Samples |
| MSP430F47166IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47166 REV # | Samples |
| MSP430F47167IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47167 REV # | Samples |
| MSP430F47167IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47167 REV # | Samples |
| MSP430F47173IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47173 | Samples |
| MSP430F47173IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47173 | Samples |
| MSP430F47176IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47176 REV # | Samples |
| MSP430F47176IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47176 REV # | Samples |
| MSP430F47177IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47177 REV # | Samples |
| MSP430F47177IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47177 REV # | Samples |
| MSP430F47183IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47183 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F47183IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47183 | Samples |
| MSP430F47186IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47186 REV # | Samples |
| MSP430F47186IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47186 REV # | Samples |
| MSP430F47187IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47187 REV # | Samples |
| MSP430F47187IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47187 REV # | Samples |
| MSP430F47193IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47193 | Samples |
| MSP430F47193IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47193 | Samples |
| MSP430F47196IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47196 REV # | Samples |
| MSP430F47196IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47196 REV # | Samples |
| MSP430F47197IPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47197 REV # | Samples |
| MSP430F47197IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F47197 REV # | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

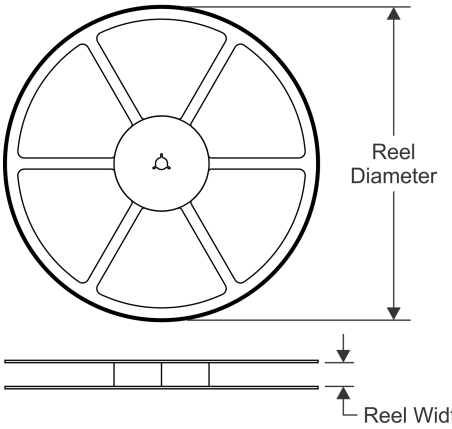
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

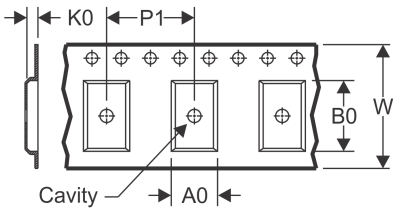
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

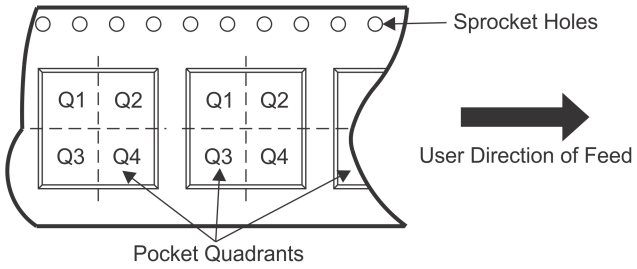



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

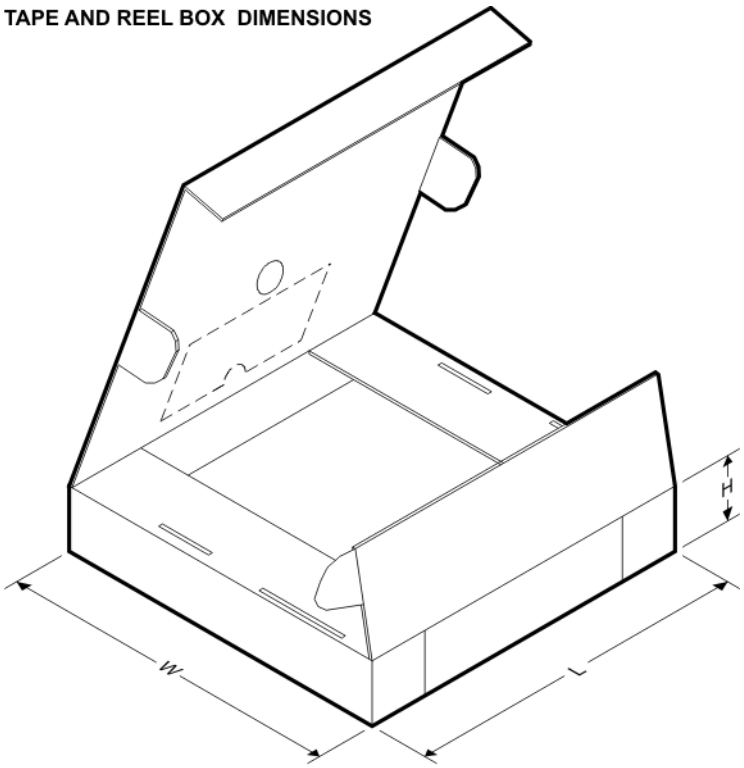
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F47163IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F47173IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F47183IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F47193IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

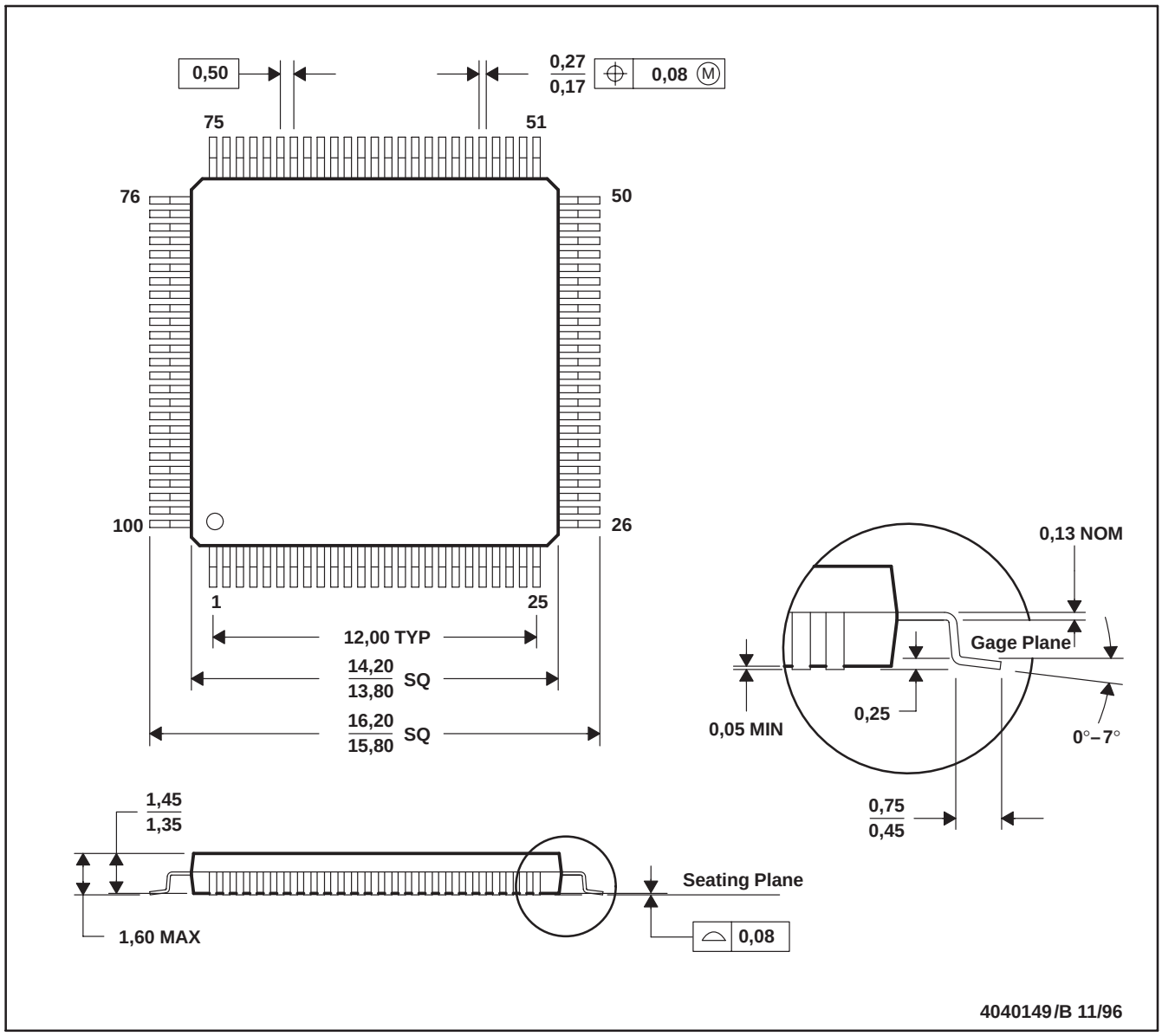



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430F47163IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F47173IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F47183IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F47193IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |

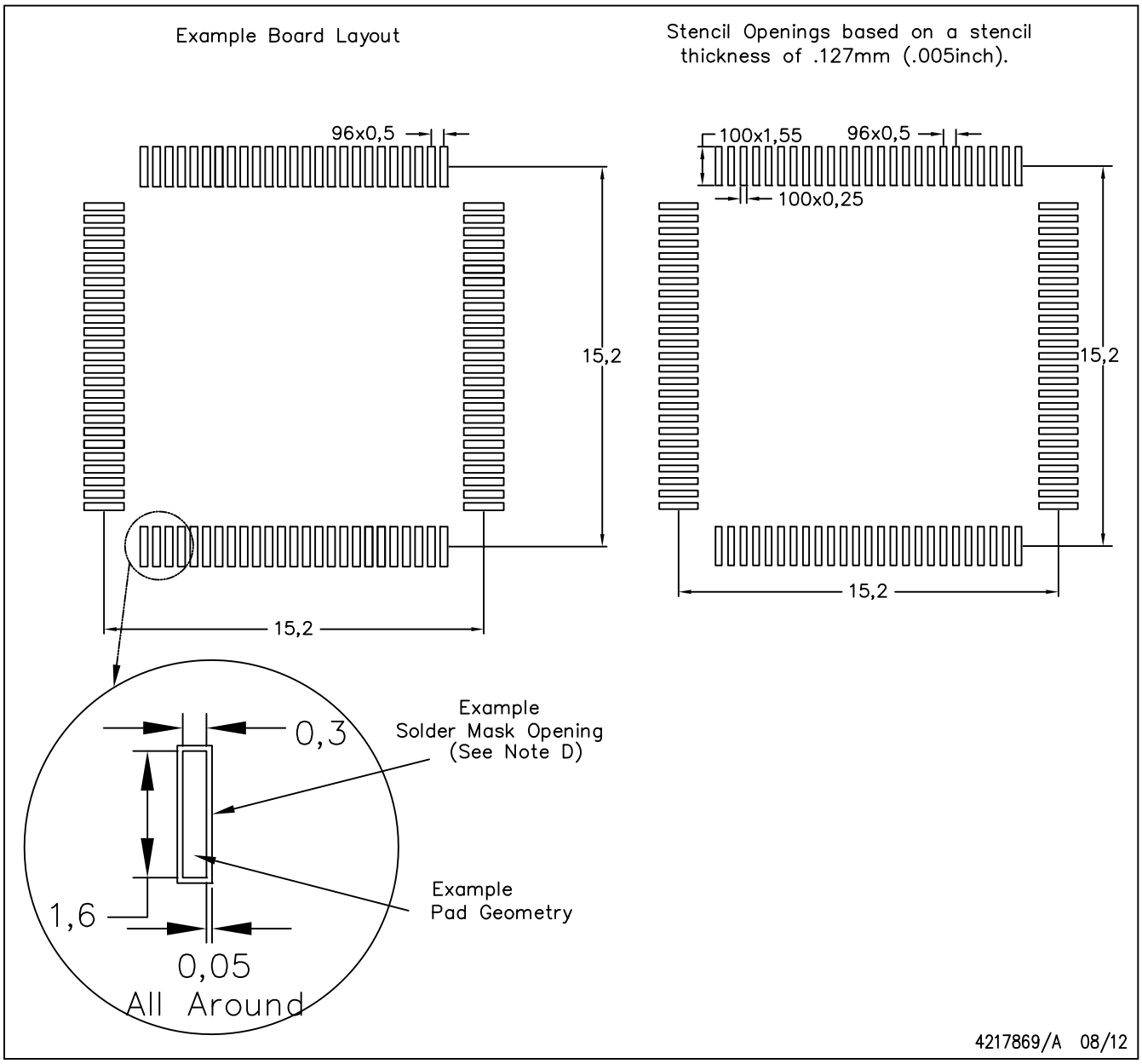
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

**PZ (S-PQFP-G100)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK




NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MSP430F47193IPZR on WIN SOURCE
- Texas Instruments Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management