THE DATASHEET OF

MT47H64M16HR-25E:G

www.win-source.net 0086-755-83957316

DDR2 SDRAM

MT47H256M4 – 32 Meg x 4 x 8 banks
MT47H128M8 – 16 Meg x 8 x 8 banks
MT47H64M16 – 8 Meg x 16 x 8 banks

Features

- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Selectable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Automotive temperature (AT) option
- RoHS-compliant
- Supports JEDEC clock jitter specification

Options[1]	Marking
• Configuration	
– 256 Meg x 4 (32 Meg x 4 x 8 banks)	256M4
– 128 Meg x 8 (16 Meg x 8 x 8 banks)	128M8
– 64 Meg x 16 (8 Meg x 16 x 8 banks)	64M16
• FBGA package (Pb-free) – x16	
– 84-ball FBGA (8mm x 12.5mm) Die Rev :H	HR
– 84-ball FBGA (8mm x 12.5mm) Die Rev :M	NF
• FBGA package (Pb-free) – x4, x8	
– 60-ball FBGA (8mm x 10mm) Die Rev :H	CF
– 60-ball FBGA (8mm x 10mm) Die Rev :M	SH
• FBGA package (lead solder) – x16	
– 84-ball FBGA (8mm x 12.5mm) Die Rev :H	HW
• FBGA package (lead solder) – x4, x8	
– 60-ball FBGA (8mm x 10mm) Die Rev :H	JN
• Timing – cycle time	
– 1.875ns @ CL = 7 (DDR2-1066)	-187E
– 2.5ns @ CL = 5 (DDR2-800)	-25E
– 3.0ns @ CL = 5 (DDR2-667)	-3
• Self refresh	
– Standard	None
– Low-power	L
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +85°C)[2]	None
– Industrial (–40°C ≤ T_C ≤ +95°C; –40°C ≤ T_A ≤ +85°C)	IT
• Revision	:H / :M

Notes:
1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.
2. For extended CT operating temperature see IDD Table 11 (page 32) Note 7.

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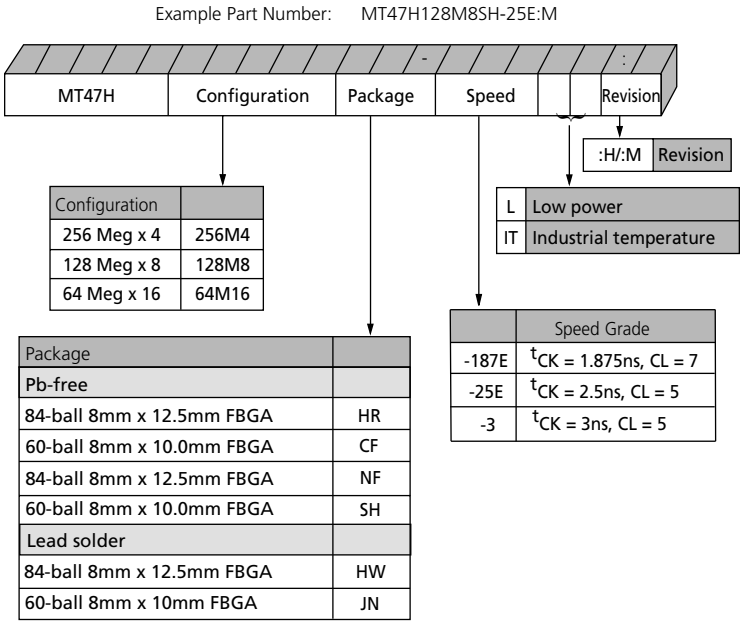
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)					tRC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	CL = 7	
-187E	400	533	800	800	1066	54
-25E	400	533	800	800	n/a	55
-3	400	533	667	n/a	n/a	55

Table 2: Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	A[13:0] (16K)	A[13:0] (16K)	A[12:0] (8K)
Bank address	BA[2:0] (8)	BA[2:0] (8)	BA[2:0] (8)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)	A[9:0] (1K)

Figure 1: 1Gb DDR2 Part Numbers



Note: 1. Not all speeds and configurations are available in all packages.

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

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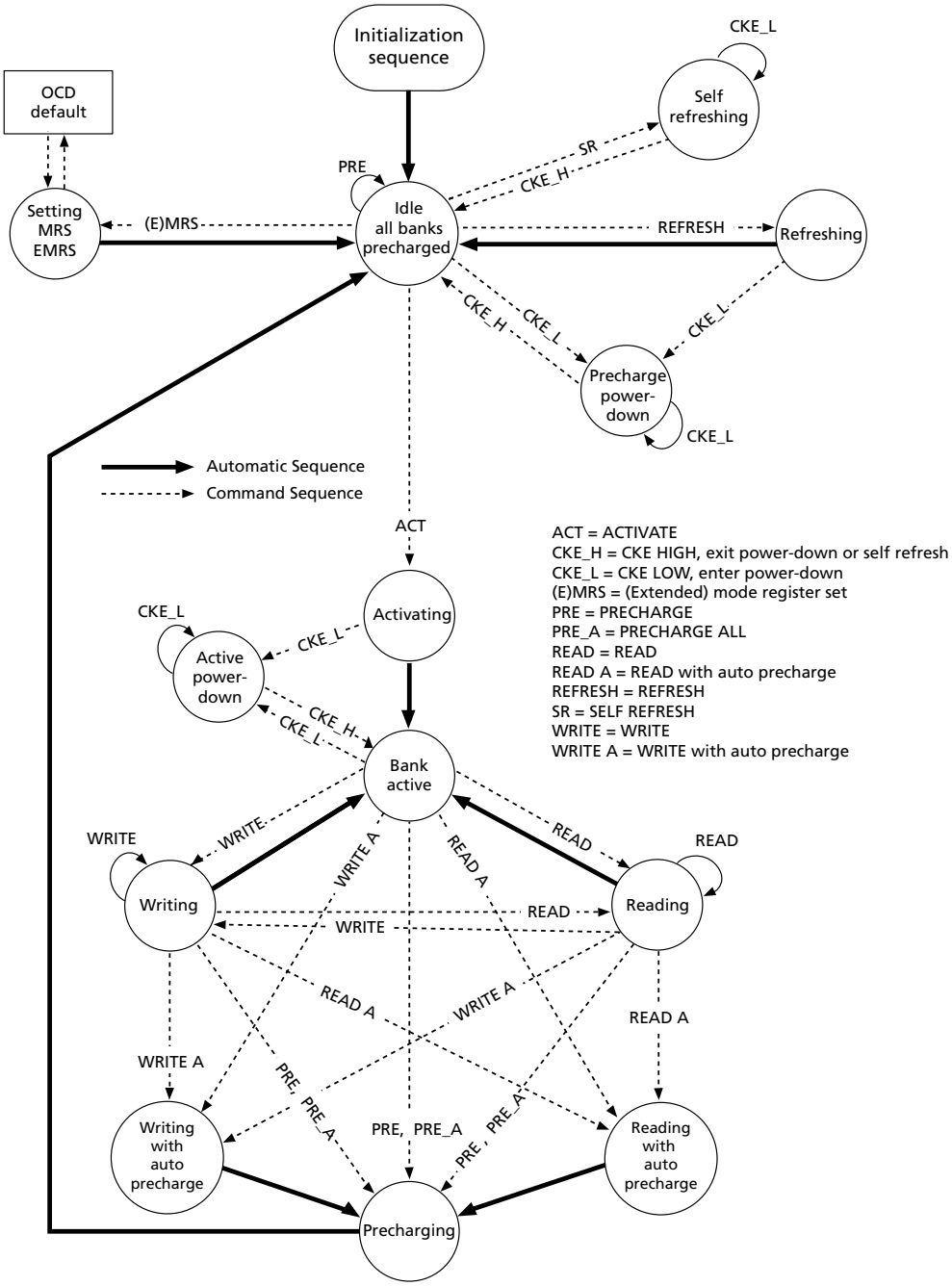
State Diagram

Figure 2: Simplified State Diagram



Note: 1. This diagram provides the basic command flow. It is not comprehensive and does not identify all timing requirements or possible command restrictions such as multibank interaction, power down, entry/exit, etc.

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Functional Description

The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single READ or WRITE operation for the DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, two-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR2 SDRAM enables concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Industrial Temperature

The industrial temperature (IT) option, if offered, has two simultaneous requirements: ambient temperature surrounding the device cannot be less than –40°C or greater than 85°C, and the case temperature cannot be less than –40°C or greater than 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, input/output impedance and I_{DD} values must be derated when T_C is < 0°C or > 85°C.

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General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
  - Connect UDQS to ground via 1kΩ* resistor
  - Connect UDQS# to V_{DD} via 1kΩ* resistor
  - Connect UDM to V_{DD} via 1kΩ* resistor
  - Connect DQ[15:8] individually to either V_{SS} or V_{DD} via 1kΩ* resistors, or float DQ[15:8].

  *If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.
- Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

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Functional Block Diagrams

The DDR2 SDRAM is a high-speed CMOS, dynamic random access memory. It is internally configured as a multibank DRAM.

Figure 3: 256 Meg x 4 Functional Block Diagram

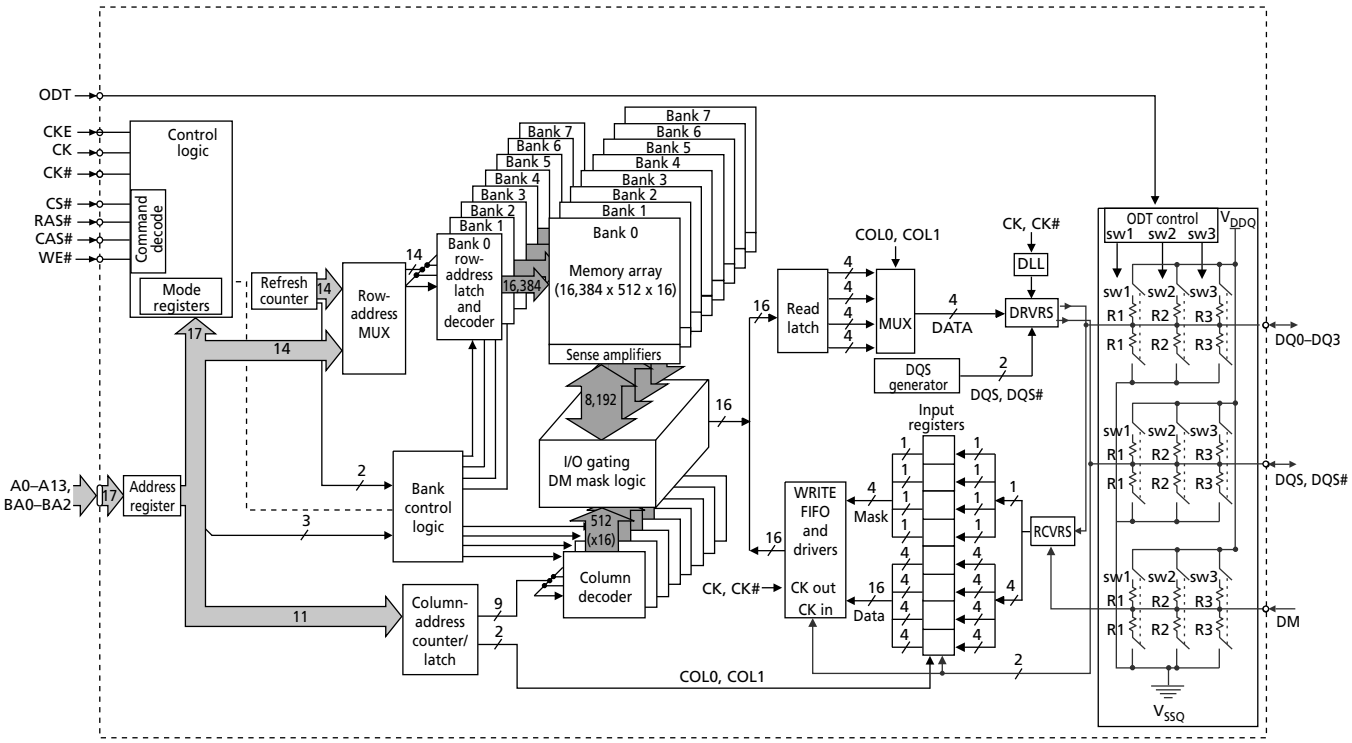

Figure 4: 128 Meg x 8 Functional Block Diagram

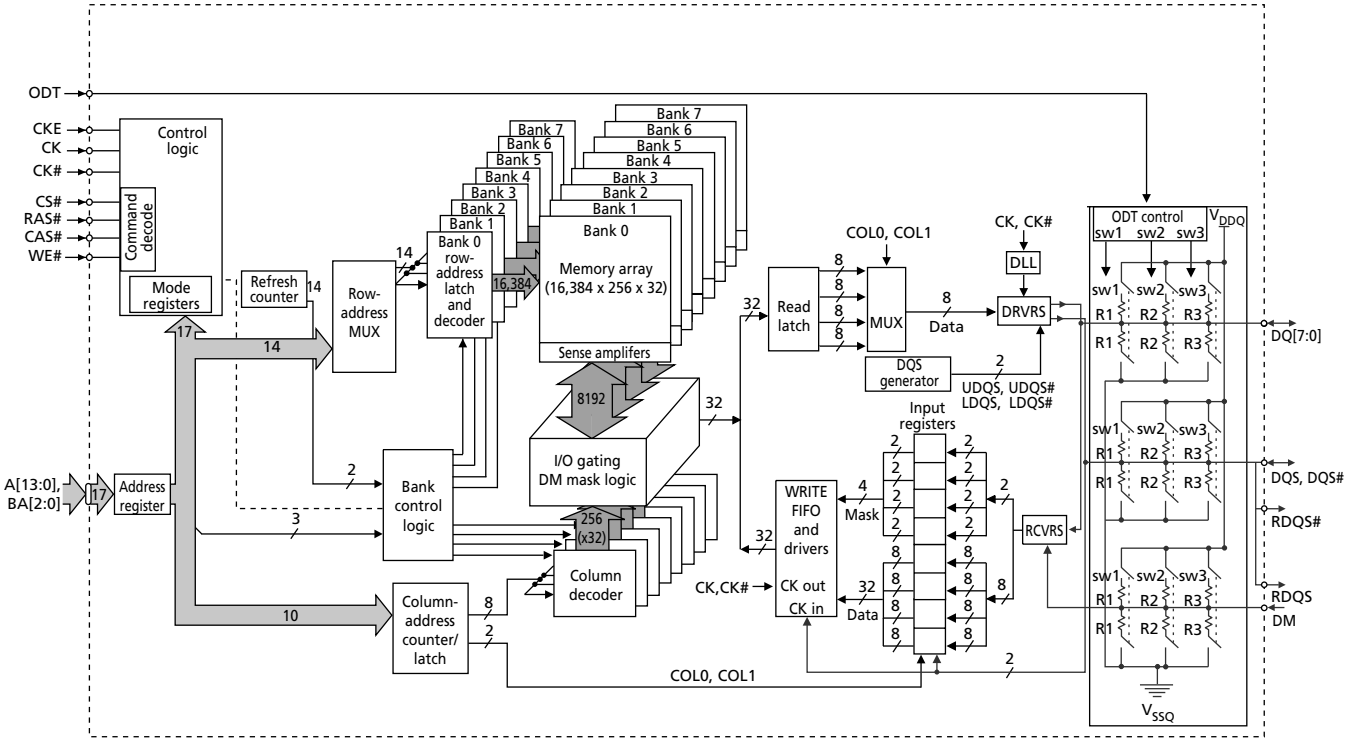

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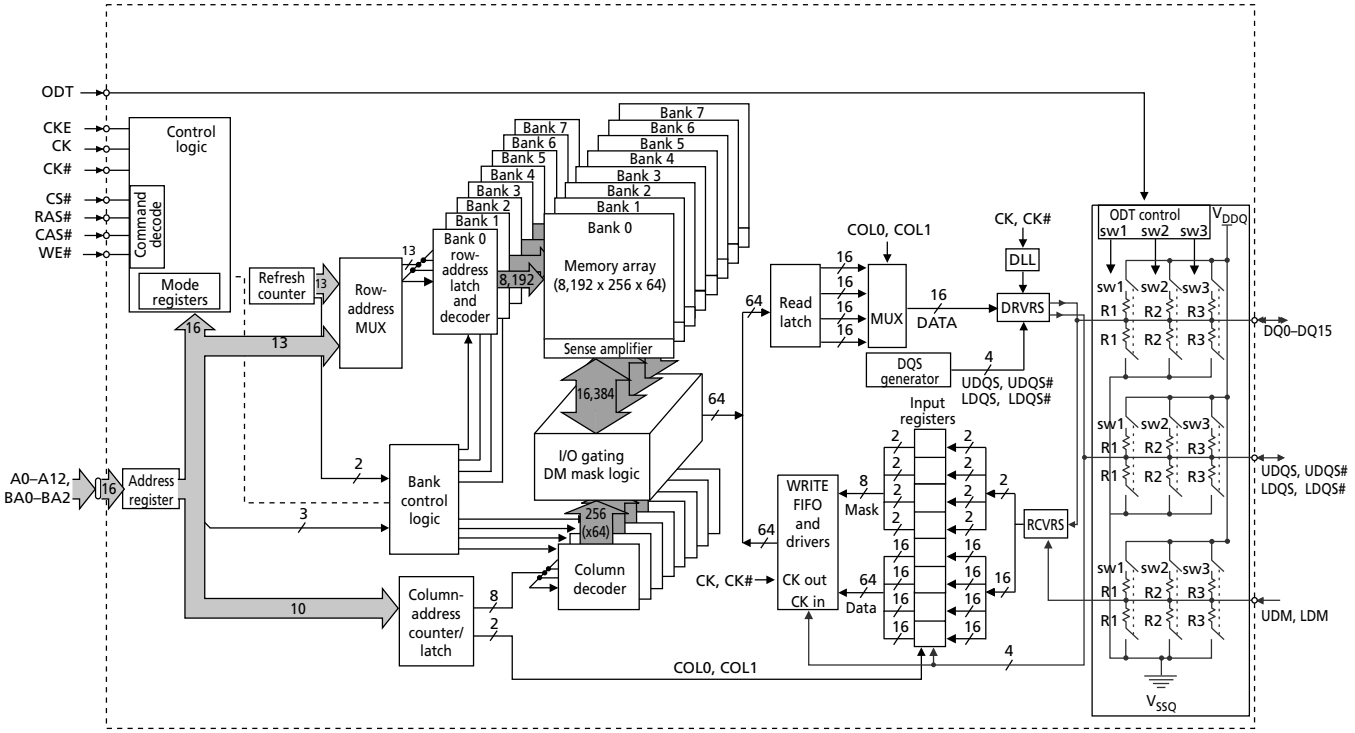
Figure 5: 64 Meg x 16 Functional Block Diagram



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Ball Assignments and Descriptions

Figure 6: 60-Ball FBGA – x4, x8 Ball Assignments (Top View)

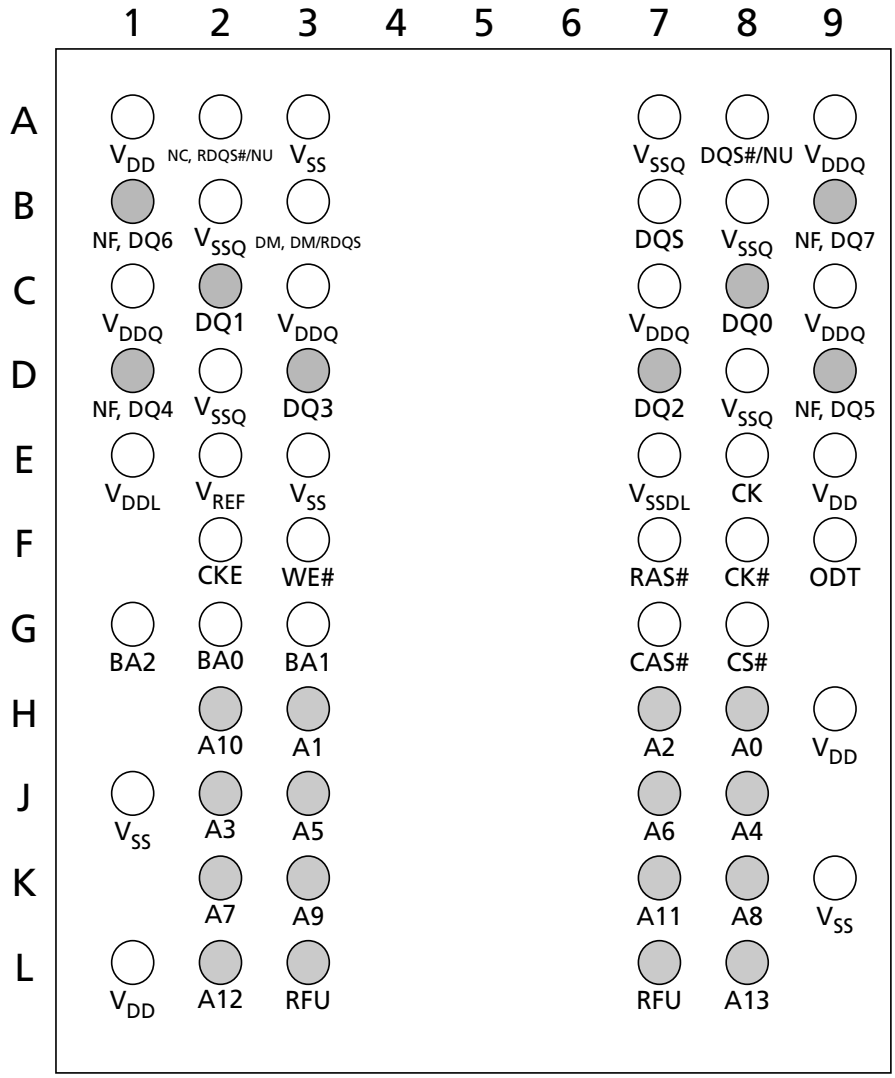

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Figure 7: 84-Ball FBGA – x16 Ball Assignments (Top View)

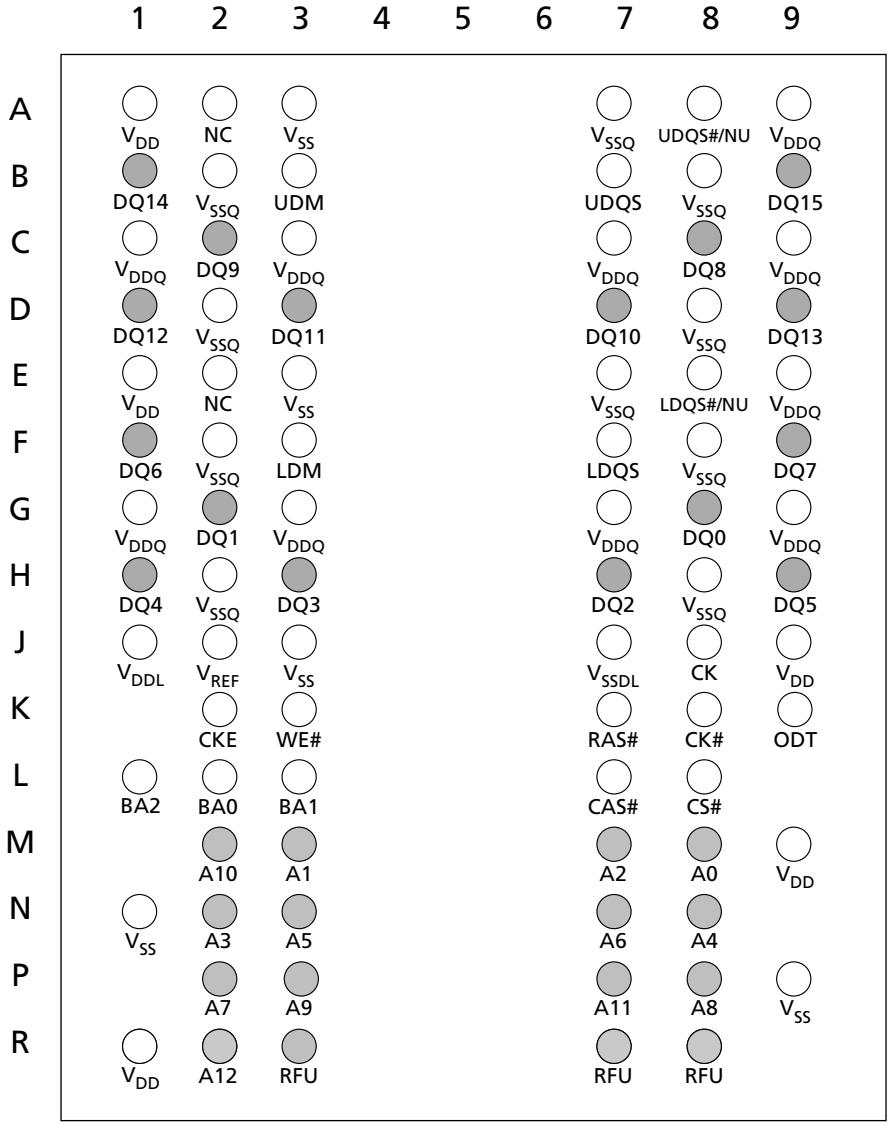

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Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions

Symbol	Type	Description
A[12:0] (x16), A[13:0] (x4, x8)	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0] or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define to which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down and SELF REFRESH operations (all banks idle), or ACTIVATE power-down (row active in any bank). CKE is synchronous for power-down entry, power-down exit, output disable, and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level after V_{DD} is applied during first power-up. After V_{REF} has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF REFRESH operation, V_{REF} must be maintained.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered high. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
LDM, UDM, DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ[7:0] and UDM is DM for upper byte DQ[15:8].
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ[15:0], LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ[7:0], DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs**: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
DQ[15:0] (x16) DQ[3:0] (x4) DQ[7:0] (x8)	I/O	**Data input/output:** Bidirectional data bus for 64 Meg x 16. Bidirectional data bus for 256 Meg x 4. Bidirectional data bus for 128 Meg x 8.

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Table 3: FBGA 84-Ball – x16 and 60-Ball – x4, x8 Descriptions (Continued)

Symbol	Type	Description
DQS, DQS#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
LDQS, LDQS#	I/O	**Data strobe for lower byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
UDQS, UDQS#	I/O	**Data strobe for upper byte:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
RDQS, RDQS#	Output	**Redundant data strobe:** For x8 only. RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled *and* differential data strobe mode is enabled.
V_{DD}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDQ}	Supply	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
V_{DDL}	Supply	**DLL power supply:** 1.8V ±0.1V.
V_{REF}	Supply	SSTL_18 reference voltage (V_{DDQ}/2).
V_{SS}	Supply	Ground.
V_{SSDL}	Supply	**DLL ground:** Isolated on the device from V_{SS} and V_{SSQ}.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NC	–	**No connect:** These balls should be left unconnected.
NF	–	**No function:** x8: these balls are used as DQ[7:4]; x4: they are no function.
NU	–	**Not used:** For x16 only. If EMR(E10) = 0, A8 and E8 are UDQS# and LDQS#. If EMR(E10) = 1, then A8 and E8 are not used.
NU	–	**Not used:** For x8 only. If EMR(E10) = 0, A2 and E8 are RDQS# and DQS#. If EMR(E10) = 1, then A2 and E8 are not used.
RFU	–	**Reserved for future use:** Row address bits A13 (x16 only), A14, and A15.

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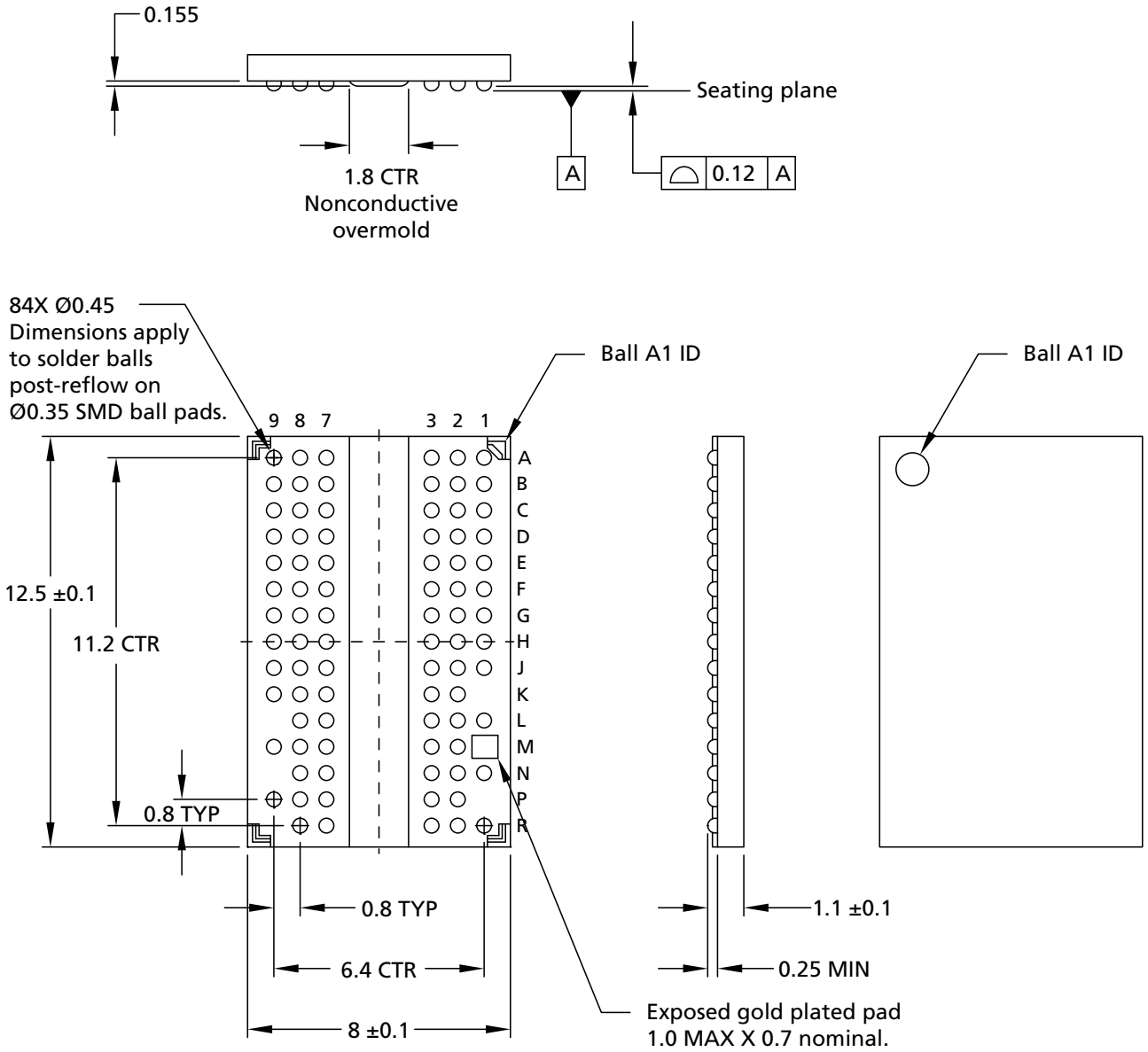
Packaging

Package Dimensions

Figure 8: 84-Ball FBGA Package (8mm x 12.5mm) – x16 Die Rev :H



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu) or leaded Eutectic (62% Sn, 36%Pb, 2% Ag).

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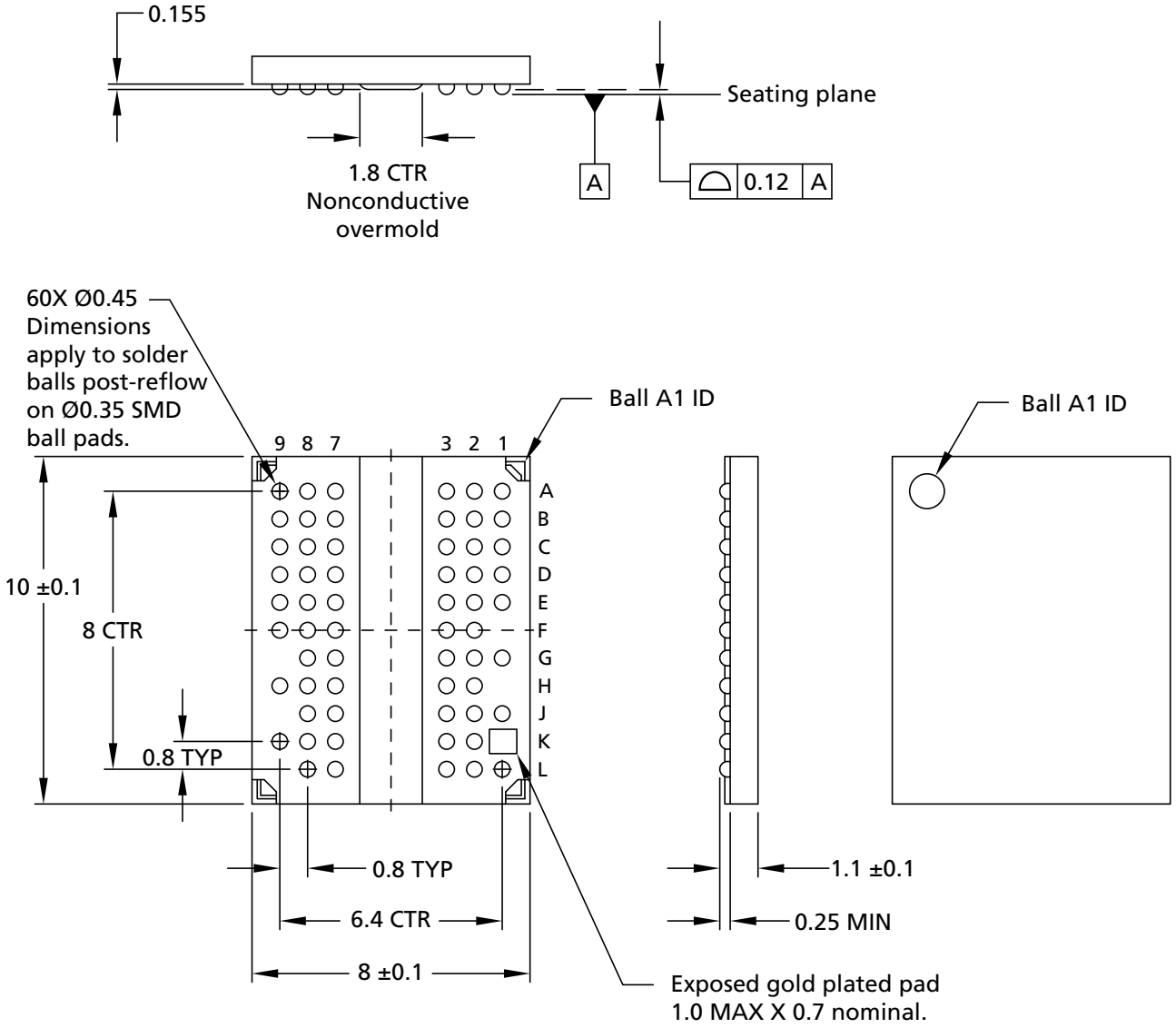
Figure 9: 60-Ball FBGA (8mm x 10mm) – x4, x8 Die Rev :H



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu) or leaded Eutectic (62% Sn, 36%Pb, 2% Ag).

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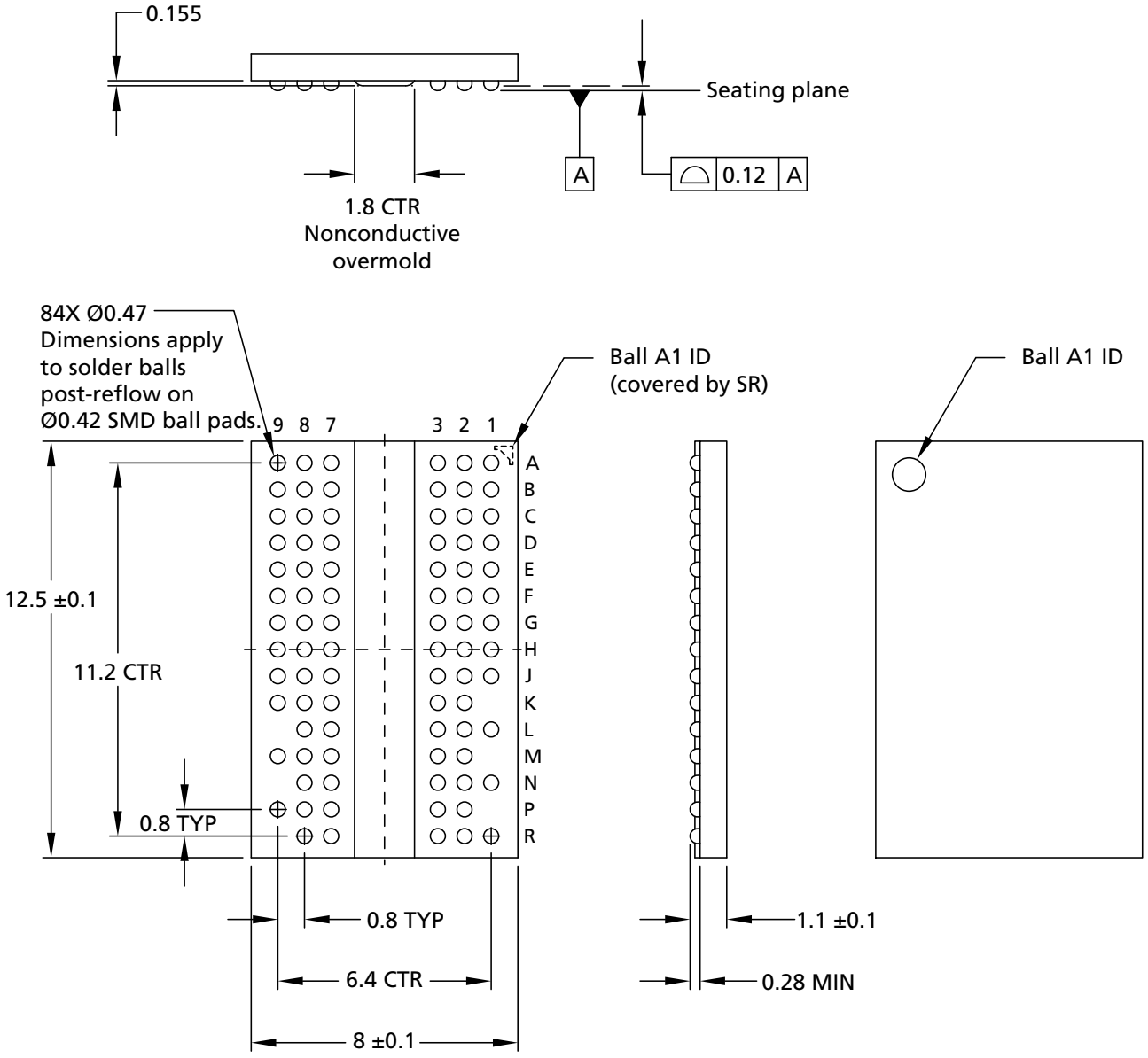
Figure 10: 84-Ball FBGA Package (8mm x 12.5mm) – x16; "NF" Die Rev :M



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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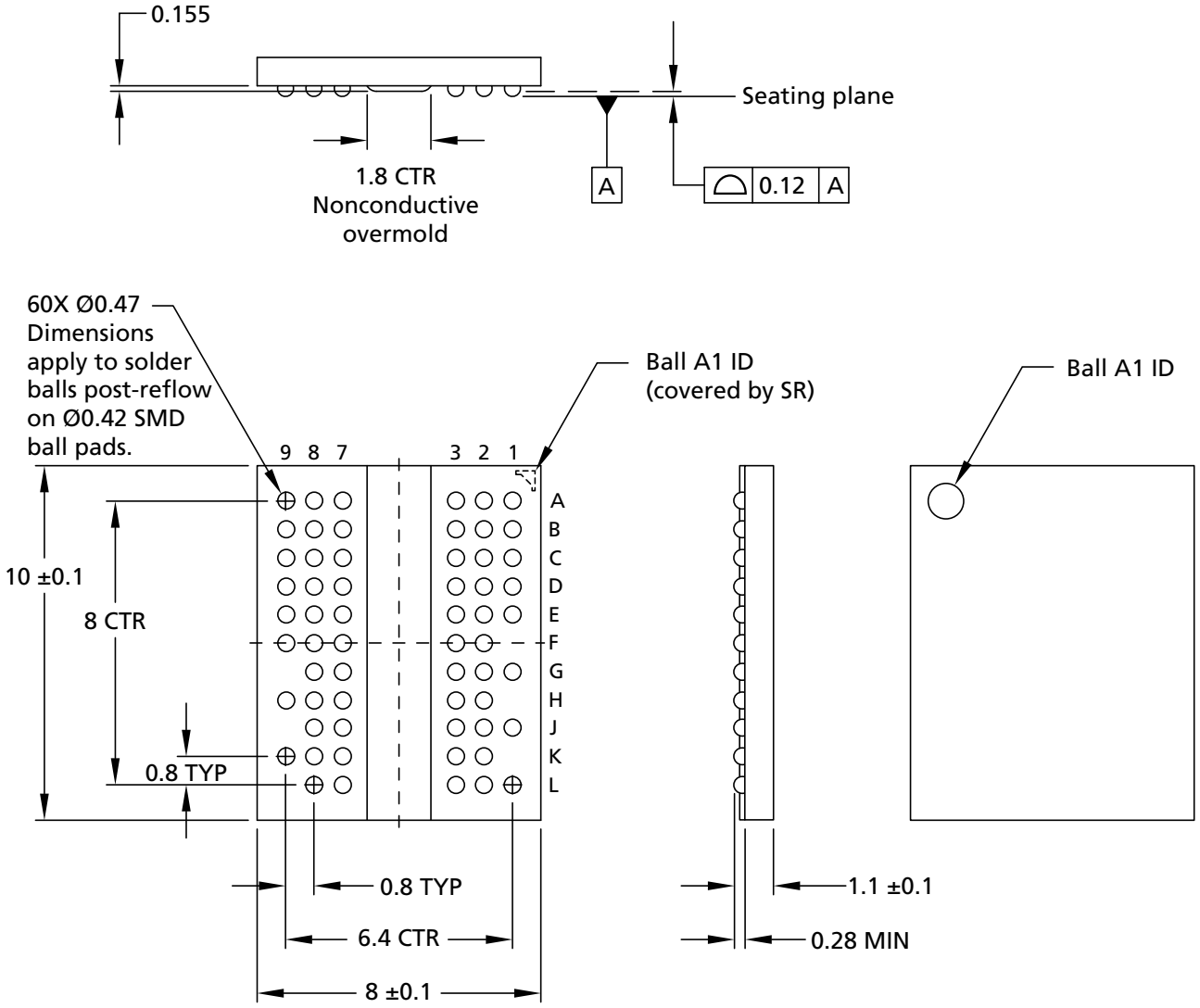
Figure 11: 60-Ball FBGA (8mm x 10mm) – x4, x8; "SH" Die Rev :M



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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FBGA Package Capacitance

Table 4: Input Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance: CK, CK#	C_{CK}	1.0	2.0	pF	1
Delta input capacitance: CK, CK#	C_{DCK}	–	0.25	pF	2, 3
Input capacitance: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, ODT	C_{I}	1.0	2.0	pF	1, 4
Delta input capacitance: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, ODT	C_{DI}	–	0.25	pF	2, 3
Input/output capacitance: DQ, DQS, DM, NF	C_{IO}	2.5	4.0	pF	1, 5
Delta input/output capacitance: DQ, DQS, DM, NF	C_{DIO}	–	0.5	pF	2, 3

Notes:
1. This parameter is sampled. V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V, V_{REF} = V_{SS}, *f* = 100 MHz, T_C = 25°C, $V_{OUT(DC)}$ = V_{DDQ}/2, V_{OUT} (peak-to-peak) = 0.1V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
2. The capacitance per ball group will not differ by more than this maximum amount for any given device.
3. ΔC are not pass/fail parameters; they are targets.
4. Reduce MAX limit by 0.25pF for -25, -25E, and -187E speed devices.
5. Reduce MAX limit by 0.5pF for -3, -3E, -25, -25E, and -187E speed devices.

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Electrical Specifications – Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD} supply voltage relative to V_{SS}	V_{DD}	–1.0	2.3	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	–0.5	2.3	V	1, 2
V_{DDL} supply voltage relative to V_{SSL}	V_{DDL}	–0.5	2.3	V	1
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	2.3	V	3
Input leakage current; any input 0V ≤ V_{IN} ≤ V_{DD}; all other balls not under test = 0V	I_I	–5	5	µA	
Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT disabled	I_{OZ}	–5	5	µA	
V_{REF} leakage current; V_{REF} = Valid V_{REF} level	I_{VREF}	–2	2	µA	

Notes:
1. V_{DD}, V_{DDQ}, and V_{DDL} must be within 300mV of each other at all times; this is not required when power is ramping down.
2. V_{REF} ≤ 0.6 × V_{DDQ}; however, V_{REF} may be ≥ V_{DDQ} provided that V_{REF} ≤ 300mV.
3. Voltage on any I/O may not exceed voltage on V_{DDQ}.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in Table 6 (page 25), be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 7 (page 27) for the applicable and available die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" (see www.micron.com/products/support/technical-notes), prior to using the thermal impedances listed in Table 7. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

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Table 6: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T_{STG}	–55	150	°C	1
Operating temperature: commercial	T_C	0	85	°C	2, 3
Operating temperature: industrial	T_C	–40	95	°C	2, 3, 4
	T_A	–40	85	°C	4, 5
Operating temperature: automotive	T_C	–40	105	°C	2, 3, 4
	T_A	–40	105	°C	4, 5

Notes:
1. MAX storage case temperature T_{STG} is measured in the center of the package, as shown in Figure 12. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in Micron technical note TN-00-15, "Recommended Soldering Parameters."
2. MAX operating case temperature T_C is measured in the center of the package, as shown in Figure 12.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. Both temperature specifications must be satisfied.
5. Operating ambient temperature surrounding the package.

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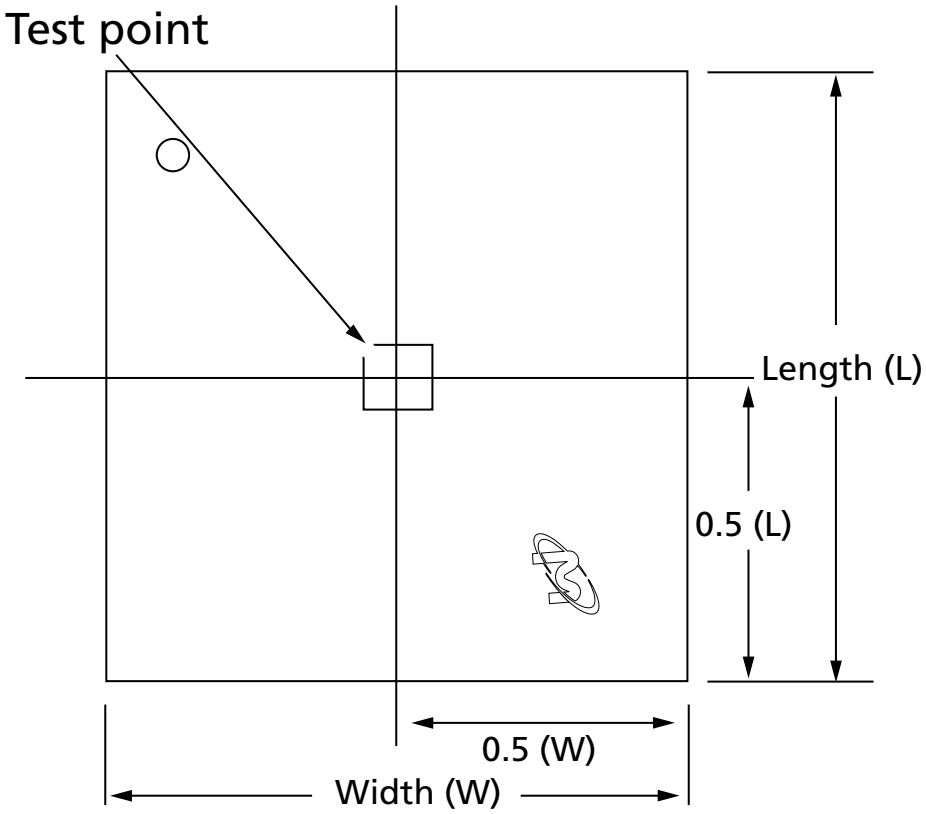
Figure 12: Example Temperature Test Point Location



Lmm x Wmm FBGA

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Table 7: Thermal Impedance

Die Revision	Package	Substrate (pcb)	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)
H [1]	60-ball	2-layer	72.5	55.5	49.5	35.6	5.7
		4-layer	54.5	45.7	42.3	35.2	
	84-ball	2-layer	68.8	52.0	46.5	32.5	5.6
		4-layer	51.3	42.7	39.6	32.3	
M [1]	60-ball	Low Conductivity	85.4	70.6	64.5	42.8	11.7
		High Conductivity	63.2	56.1	52.8		
	84-ball	Low Conductivity	80.8	67.0	61.6	44.7	11.7
		High Conductivity	59.7	53.3	50.7		

Note: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

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Electrical Specifications – I_{DD} Parameters

I_{DD} Specifications and Conditions

Table 8: General I_{DD} Parameters

I_{DD} Parameters	-187E	-25E	-25	-3E	-3	-37E	Units
CL (I_{DD})	7	5	6	4	5	4	^{t}CK
^{t}RCD (I_{DD})	13.125	12.5	15	12	15	15	ns
^{t}RC (I_{DD})	58.125	57.5	60	57	60	60	ns
^{t}RRD (I_{DD}) - x4/x8 (1KB)	7.5	7.5	7.5	7.5	7.5	7.5	ns
^{t}RRD (I_{DD}) - x16 (2KB)	10	10	10	10	10	10	ns
^{t}CK (I_{DD})	1.875	2.5	2.5	3	3	3.75	ns
^{t}RAS MIN (I_{DD})	45	45	45	45	45	45	ns
^{t}RAS MAX (I_{DD})	70,000	70,000	70,000	70,000	70,000	70,000	ns
^{t}RP (I_{DD})	13.125	12.5	15	12	15	15	ns
^{t}RFC (I_{DD} - 256Mb)	75	75	75	75	75	75	ns
^{t}RFC (I_{DD} - 512Mb)	105	105	105	105	105	105	ns
^{t}RFC (I_{DD} - 1Gb)	127.5	127.5	127.5	127.5	127.5	127.5	ns
^{t}RFC (I_{DD} - 2Gb)	197.5	197.5	197.5	197.5	197.5	197.5	ns
^{t}FAW (I_{DD}) - x4/x8 (1KB)	Defined by pattern in Table 9 (page 28)						ns
^{t}FAW (I_{DD}) - x16 (2KB)	Defined by pattern in Table 9 (page 28)						ns

I_{DD7} Conditions

The detailed timings are shown below for I_{DD7}. Where general I_{DD} parameters in Table 8 (page 28) conflict with pattern requirements of Table 9, then Table 9 requirements take precedence.

Table 9: I_{DD7} Timing Patterns (8-Bank Interleave READ Operation)

Speed Grade	I_{DD7} Timing Patterns
Timing patterns for 8-bank x4/x8 devices	
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 A4 RA4 A5 RA5 A6 RA6 A7 RA7
-37E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D
-3	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D
-3E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D
-25	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-25E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-187E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D
Timing patterns for 8-bank x16 devices	
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D A4 RA4 A5 RA5 A6 RA6 A7 RA7 D D

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Table 9: I_{DD7} Timing Patterns (8-Bank Interleave READ Operation) (Continued)

Speed Grade	I_{DD7} Timing Patterns
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
-3	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D
-3E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D
-25	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D
-25E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D
-187E	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D

Notes:
1. A = active; RA = read auto precharge; D = deselect.
2. All banks are being interleaved at ^{t}RC (I_{DD}) without violating ^{t}RRD (I_{DD}) using a BL = 4.
3. Control and address bus inputs are stable during deselects.

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Table 10: DDR2 I_{DD} Specifications and Conditions (Die Revision H)

Notes: 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-187E	-25E	-3	Units
Operating one bank active-precharge current: tCK = tCK (I_{DD}), tRC = tRC (I_{DD}), tRAS = tRAS MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD0}	x4, x8	75	65	60	mA
		x16	90	80	75	
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; tCK = tCK (I_{DD}), tRC = tRC (I_{DD}), tRAS = tRAS MIN (I_{DD}), tRCD = tRCD (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}	I_{DD1}	x4, x8	85	75	70	mA
		x16	100	95	90	
Precharge power-down current: All banks idle; tCK = tCK (I_{DD}); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}	x4, x8, x16	7	7	7	mA
Precharge quiet standby current: All banks idle; tCK = tCK (I_{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}	x4, x8	28	24	24	mA
		x16	30	26	26	
Precharge standby current: All banks idle; tCK = tCK (I_{DD}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}	x4, x8	34	28	24	mA
		x16	36	30	26	
Active power-down current: All banks open; tCK = tCK (I_{DD}); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3Pf}	Fast exit MR12 = 0	23	20	15	mA
	I_{DD3Ps}	Slow exit MR12 = 1	10	10	10	
Active standby current: All banks open; tCK = tCK (I_{DD}), tRAS = tRAS MAX (I_{DD}), tRP = tRP (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}	x4, x8	40	33	30	mA
		x16	42	35	32	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; tCK = tCK (I_{DD}), tRAS = tRAS MAX (I_{DD}), tRP = tRP (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4W}	x4 ,x8	145	125	115	mA
		x16	185	160	135	
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; tCK = tCK (I_{DD}), tRAS = tRAS MAX (I_{DD}), tRP = tRP (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4R}	x4, x8	140	120	110	mA
		x16	180	150	125	

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Table 10: DDR2 I_{DD} Specifications and Conditions (Die Revision H) (Continued)

Notes: 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-187E	-25E	-3	Units
Burst refresh current: $^{t}CK = {}^{t}CK (I_{DD})$; REFRESH command at every $^{t}RFC (I_{DD})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD5}	x4, x8	155	145	140	mA
		x16	160	150	145	
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{DD6}	x4, x8, x16	7	7	7	mA
	I_{DD6L}		5	5	5	
Operating bank interleave read current: All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^{t}RCD (I_{DD})$ - 1 × $^{t}CK (I_{DD})$; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RRD = {}^{t}RRD (I_{DD})$, $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions (page 28) for details	I_{DD7}	x4, x8	220	210	185	mA
		x16	270	260	230	

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +85°C.
2. V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V, V_{DDL} = +1.8V ±0.1V, $V_{REF} = V_{DDQ}/2$.
3. I_{DD} parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. I_{DD} values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for I_{DD} conditions:

   LOW $V_{IN} \le V_{IL(AC)max}$

   HIGH $V_{IN} \ge V_{IH(AC)min}$

   Stable Inputs stable at a HIGH or LOW level

   Floating Inputs at $V_{REF} = V_{DDQ}/2$

   Switching Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals

   Switching Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes
6. I_{DD1}, I_{DD4R}, and I_{DD7} require A12 in EMR to be enabled during testing.
7. The following I_{DD} values must be derated (I_{DD} limits increase) on IT-option and AT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:

   When T_C ≤ 0°C I_{DD2P} and $I_{DD3P(SLOW)}$ must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%

   When T_C ≥ 85°C I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2Q}, I_{DD3N}, $I_{DD3P(FAST)}$, I_{DD4R}, I_{DD4W}, and I_{DD5} must be derated by 2%; I_{DD2P} must be derated by 20%; $I_{DD3P(SLOW)}$ must be derated by 30%; and I_{DD6} must be derated by 80% (I_{DD6} will increase by this amount if T_C < 85°C and the 2X refresh option is still enabled)

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Table 11: DDR2 I_{DD} Specifications and Conditions (Die Revision M)

Notes: 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-187E	-25E	-3	Units
Operating one bank active-precharge current: $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD0}	x4, x8	75	65	60	mA
		x16	90	80	75	
Operating one bank active-read-precharge current: I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRC = ^tRC (I_{DD})$, $^tRAS = ^tRAS$ MIN (I_{DD}), $^tRCD = ^tRCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I_{DD4W}	I_{DD1}	x4, x8	85	75	70	mA
		x16	100	95	90	
Precharge power-down current: All banks idle; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}	x4, x8, x16	10	10	10	mA
Precharge quiet standby current: All banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}	x4, x8	28	24	24	mA
		x16	30	26	26	
Precharge standby current: All banks idle; $^tCK = ^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}	x4, x8	34	28	24	mA
		x16	36	30	26	
Active power-down current: All banks open; $^tCK = ^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3Pf}	Fast exit MR12 = 0	32	30	28	mA
	I_{DD3Ps}	Slow exit MR12 = 1	20	20	20	
Active standby current: All banks open; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}	x4, x8	40	33	30	mA
		x16	43	38	36	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4W}	x4 ,x8	145	125	115	mA
		x16	185	160	135	
Operating burst read current: All banks open, continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = ^tCK (I_{DD})$, $^tRAS = ^tRAS$ MAX (I_{DD}), $^tRP = ^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4R}	x4, x8	140	120	110	mA
		x16	180	150	125	

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Table 11: DDR2 I_{DD} Specifications and Conditions (Die Revision M) (Continued)

Notes: 1–7 apply to the entire table

Parameter/Condition	Symbol	Configuration	-187E	-25E	-3	Units
Burst refresh current: $^{t}CK = {}^{t}CK (I_{DD})$; REFRESH command at every $^{t}RFC (I_{DD})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD5}	x4, x8	165	155	150	mA
		x16	170	160	155	
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{DD6}	x4, x8, x16	7	7	7	mA
Operating bank interleave read current: All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = $^{t}RCD (I_{DD})$ - 1 × $^{t}CK (I_{DD})$; $^{t}CK = {}^{t}CK (I_{DD})$, $^{t}RC = {}^{t}RC (I_{DD})$, $^{t}RRD = {}^{t}RRD (I_{DD})$, $^{t}RCD = {}^{t}RCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 Conditions (page 28) for details	I_{DD7}	x4, x8	220	210	185	mA
		x16	270	260	230	

Notes:
1. I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +85°C.
2. V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V, V_{DDL} = +1.8V ±0.1V, $V_{REF} = V_{DDQ}/2$.
3. I_{DD} parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. I_{DD} values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for I_{DD} conditions:

   LOW $V_{IN} \le V_{IL(AC)max}$

   HIGH $V_{IN} \ge V_{IH(AC)min}$

   Stable Inputs stable at a HIGH or LOW level

   Floating Inputs at $V_{REF} = V_{DDQ}/2$

   Switching Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals

   Switching Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes
6. I_{DD1}, I_{DD4R}, and I_{DD7} require A12 in EMR to be enabled during testing.
7. The following I_{DD} values must be derated (I_{DD} limits increase) on IT-option and AT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:

   When T_C ≤ 0°C (IT) I_{DD2P} and $I_{DD3P(SLOW)}$ must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%

   When 85°C ≥ T_C ≤ 95°C (CT) (Extended CT Temperature) I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2Q}, I_{DD3N}, $I_{DD3P(FAST)}$, I_{DD4R}, I_{DD4W}, and I_{DD5} must be derated by 2%; I_{DD2P} must be derated by 20%; $I_{DD3P(SLOW)}$ must be derated by 30%; and I_{DD6} must be derated by 80% (I_{DD6} will increase by this amount if T_C < 85°C and the 2X refresh option is still enabled)

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AC Timing Operating Specifications

Table 12: AC Operating Specifications and Conditions

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th

V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics				-187E		-25E		-25		-3E		-3		-37E		-5E	
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	
Clock	Clock cycle time	CL = 7	tCK (avg)	1.875	8.0	–	–	–	–	–	–	–	–	–	–	–	
		CL = 6	tCK (avg)	2.5	8.0	2.5	8.0	2.5	8.0	–	–	–	–	–	–	–	
		CL = 5	tCK (avg)	2.5	8.0	2.5	8.0	3.0	8.0	3.0	8.0	3.0	8.0	–	–	–	
		CL = 4	tCK (avg)	3.75	8.0	3.75	8.0	3.75	8.0	3.0	8.0	3.75	8.0	3.75	8.0	5.0	
		CL = 3	tCK (avg)	5.0	8.0	5.0	8.0	5.0	8.0	5.0	8.0	5.0	8.0	5.0	8.0	5.0	
	CK high-level width		tCH (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	
	CK low-level width		tCL (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	
	Half clock period		tHP	MIN = lesser of tCH and tCL MAX = n/a													
	Absolute tCK		tCK (abs)	MIN = tCK (AVG) MIN + tJITper (MIN) MAX = tCK (AVG) MAX + tJITper (MAX)													
	Absolute CK high-level width		tCH (abs)	MIN = tCK (AVG) MIN × tCH (AVG) MIN + tJITdty (MIN) MAX = tCK (AVG) MAX × tCH (AVG) MAX + tJITdty (MAX)													
	Absolute CK low-level width		tCL (abs)	MIN = tCK (AVG) MIN × tCL (AVG) MIN + tJITdty (MIN) MAX = tCK (AVG) MAX × tCL (AVG) MAX + tJITdty (MAX)													

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E	
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	
Clock Jitter	Period jitter	^{t}JITper	–90	90	–100	100	–100	100	–125	125	–125	125	–125	125	–125	
	Half period	^{t}JITdty	–75	75	–100	100	–100	100	–125	125	–125	125	–125	125	–150	
	Cycle to cycle	^{t}JITcc	180		200		200		250		250		250		250	
	Cumulative error, 2 cycles	$^{t}ERR_{2per}$	–132	132	–150	150	–150	150	–175	175	–175	175	–175	175	–175	
	Cumulative error, 3 cycles	$^{t}ERR_{3per}$	–157	157	–175	175	–175	175	–225	225	–225	225	–225	225	–225	
	Cumulative error, 4 cycles	$^{t}ERR_{4per}$	–175	175	–200	200	–200	200	–250	250	–250	250	–250	250	–250	
	Cumulative error, 5 cycles	$^{t}ERR_{5per}$	–188	188	–200	200	–200	200	–250	250	–250	250	–250	250	–250	
	Cumulative error, 6–10 cycles	$^{t}ERR_{6–10per}$	–250	250	–300	300	–300	300	–350	350	–350	350	–350	350	–350	
	Cumulative error, 11–50 cycles	$^{t}ERR_{11–50per}$	–425	425	–450	450	–450	450	–450	450	–450	450	–450	450	–450	
Data Strobe-Out	DQS output access time from CK/CK#	^{t}DQSCK	–300	300	–350	350	–350	350	–400	400	–400	400	–450	450	–500	
	DQS read preamble	^{t}RPRE	MIN = 0.9 × ^{t}CK MAX = 1.1 × ^{t}CK													
	DQS read postamble	^{t}RPST	MIN = 0.4 × ^{t}CK MAX = 0.6 × ^{t}CK													
	CK/CK# to DQS Low-Z	$^{t}LZ_{1}$	MIN = ^{t}AC (MIN) MAX = ^{t}AC (MAX)													

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E	
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	
Data Strobe-In	DQS rising edge to CK rising edge	^{t}DQSS	MIN = –0.25 × ^{t}CK MAX = 0.25 × ^{t}CK													
	DQS input-high pulse width	^{t}DQSH	MIN = 0.35 × ^{t}CK MAX = n/a													
	DQS input-low pulse width	^{t}DQSL	MIN = 0.35 × ^{t}CK MAX = n/a													
	DQS falling to CK rising: setup time	^{t}DSS	MIN = 0.2 × ^{t}CK MAX = n/a													
	DQS falling from CK rising: hold time	^{t}DSH	MIN = 0.2 × ^{t}CK MAX = n/a													
	Write preamble setup time	^{t}WPRES	MIN = 0 MAX = n/a													
	DQS write preamble	^{t}WPRE	MIN = 0.35 × ^{t}CK MAX = n/a													
	DQS write postamble	^{t}WPST	MIN = 0.4 × ^{t}CK MAX = 0.6 × ^{t}CK													
	WRITE command to first DQS transition	–	MIN = WL - ^{t}DQSS MAX = WL + ^{t}DQSS													

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E	
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	
Data-Out	DQ output access time from CK/CK#	^{t}AC	–350	350	–400	400	–400	400	–450	450	–450	450	–500	500	–600	
	DQS–DQ skew, DQS to last DQ valid, per group, per access	^{t}DQSQ	–	175	–	200	–	200	–	240	–	240	–	300	–	
	DQ hold from next DQS strobe	^{t}QHS	–	250	–	300	–	300	–	340	–	340	–	400	–	
	DQ–DQS hold, DQS to first DQ not valid	^{t}QH	MIN = ^{t}HP - ^{t}QHS MAX = n/a													
	CK/CK# to DQ, DQS High-Z	^{t}HZ	MIN = n/a MAX = ^{t}AC (MAX)													
	CK/CK# to DQ Low-Z	^{t}LZ$_2$	MIN = 2 × ^{t}AC (MIN) MAX = ^{t}AC (MAX)													
	Data valid output window	DVW	MIN = ^{t}QH - ^{t}DQSQ MAX = n/a													
Data-In	DQ and DM input setup time to DQS	^{t}DSb	0	–	50	–	50	–	100	–	100	–	100	–	150	
	DQ and DM input hold time to DQS	^{t}DHb	75	–	125	–	125	–	175	–	175	–	225	–	275	
	DQ and DM input setup time to DQS	^{t}DSa	200	–	250	–	250	–	300	–	300	–	350	–	400	
	DQ and DM input hold time to DQS	^{t}DHa	200	–	250	–	250	–	300	–	300	–	350	–	400	
	DQ and DM input pulse width	^{t}DIPW	MIN = 0.35 × ^{t}CK MAX = n/a													

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics				-187E		-25E		-25		-3E		-3		-37E		-5E
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
Command and Address	Input setup time		tISb	125	–	175	–	175	–	200	–	200	–	250	–	350
	Input hold time		tIHb	200	–	250	–	250	–	275	–	275	–	375	–	475
	Input setup time		tISa	325	–	375	–	375	–	400	–	400	–	500	–	600
	Input hold time		tIHa	325	–	375	–	375	–	400	–	400	–	500	–	600
	Input pulse width		tIPW	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	0.6	–	0.6
	ACTIVATE-to-ACTIVATE delay, same bank		tRC	54	–	55	–	55	–	54	–	55	–	55	–	55
	ACTIVATE-to-READ or WRITE delay		tRCD	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15
	ACTIVATE-to-PRECHARGE delay		tRAS	40	70K	40	70K	40	70K	40	70K	40	70K	40	70K	40
	PRECHARGE period		tRP	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15
	PRE-CHARGE ALL period	<1Gb	tRPA	13.125	–	12.5	–	15	–	12	–	15	–	15	–	15
		≥1Gb	tRPA	15	–	15	–	17.5		15		18		18.75		20
	ACTIVATE-to-ACTIVATE delay different bank	x4, x8	tRRD	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5
		x16	tRRD	10	–	10	–	10	–	10	–	10	–	10	–	10
	4-bank activate period (≥1Gb)	x4, x8	tFAW	35	–	35	–	35	–	37.5	–	37.5	–	37.5	–	37.5
		x16	tFAW	45	–	45	–	45	–	50	–	50	–	50	–	50

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics				-187E		-25E		-25		-3E		-3		-37E		-5E
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
Command and Address	Internal READ-to-PRECHARGE delay		^{t}RTP	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5
	CAS#-to-CAS# delay		^{t}CCD	2	–	2	–	2	–	2	–	2	–	2	–	2
	Write recovery time		^{t}WR	15	–	15	–	15	–	15	–	15	–	15	–	15
	Write AP recovery + precharge time		^{t}DAL	^{t}WR + ^{t}RP	–	^{t}WR + ^{t}RP	–	^{t}WR + ^{t}RP	–	^{t}WR + ^{t}RP	–	^{t}WR + ^{t}RP	–	^{t}WR + ^{t}RP	–	^{t}WR + ^{t}RP
	Internal WRITE-to-READ delay		^{t}WTR	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	10
	LOAD MODE cycle time		^{t}MRD	2	–	2	–	2	–	2	–	2	–	2	–	2
Refresh	REFRESH-to-ACTIVATE or to -REFRESH interval	256Mb	^{t}RFC	75	–	75	–	75	–	75	–	75	–	75	–	75
		512Mb		105	–	105	–	105	–	105	–	105	–	105	–	105
		1Gb		127.5	–	127.5	–	127.5	–	127.5	–	127.5	–	127.5	–	127.5
		2Gb		195	–	195	–	195	–	195	–	195	–	195	–	195
	Average periodic refresh (commercial)		^{t}REFI	–	7.8	–	7.8	–	7.8	–	7.8	–	7.8	–	7.8	–
	Average periodic refresh (industrial)		^{t}REFI$_{IT}$	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–
	Average periodic refresh (automotive)		^{t}REFI$_{AT}$	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–	3.9	–
	CKE LOW to CK, CK# uncertainty		^{t}DELAY	MIN limit = ^{t}IS + ^{t}CK + ^{t}IH MAX limit = n/a												

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics				-187E		-25E		-25		-3E		-3		-37E		-5E	
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	
Self Refresh	Exit SELF REFRESH to nonREAD command		tXSNR	MIN limit = tRFC (MIN) + 10 MAX limit = n/a													
	Exit SELF REFRESH to READ command		tXSRD	MIN limit = 200 MAX limit = n/a													
	Exit SELF REFRESH timing reference		tISXR	MIN limit = tIS MAX limit = n/a													
Power-Down	Exit active power-down to READ command	MR12 = 0	tXARD	3	–	2	–	2	–	2	–	2	–	2	–	2	
		MR12 = 1		10 - AL	–	8 - AL	–	8 - AL	–	7 - AL	–	7 - AL	–	6 - AL	–	6 - AL	
	Exit precharge power-down and active power-down to any nonREAD command		tXP	3	–	2	–	2	–	2	–	2	–	2	–	2	
	CKE MIN HIGH/LOW time		tCKE	MIN = 3 MAX = n/a													

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Table 12: AC Operating Specifications and Conditions (Continued)

Not all speed grades listed may be supported for this device; refer to the title page for speeds supported; Notes: 1–5 apply to th
V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V

AC Characteristics			-187E		-25E		-25		-3E		-3		-37E		-5E
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
ODT	ODT to power-down entry latency	tANPD	4	–	3	–	3	–	3	–	3	–	3	–	3
	ODT power-down exit latency	tAXPD	11	–	8	–	8	–	8	–	8	–	8	–	8
	ODT turn-on delay	tAOND	2												
	ODT turn-off delay	tAOFD	2.5												
	ODT turn-on	tAON	tAC (MIN)	tAC (MAX) + 2575	MIN = tAC (MIN) MAX = tAC (MAX) + 600				MIN = tAC (MIN) MAX = tAC (MAX) + 700				MIN = tAC (MIN) MAX = tAC (MAX) + 1		
	ODT turn-off	tAOF	MIN = tAC (MIN) MAX = tAC (MAX) + 600												
	ODT turn-on (power-down mode)	tAONPD	tAC (MIN) + 2000	2 × tCK + tAC (MAX) + 1000	MIN = tAC (MIN) + 2000 MAX = 2 × tCK + tAC (MAX) + 1000										
	ODT turn-off (power-down mode)	tAOFPD	MIN = tAC (MIN) + 2000 MAX = 2.5 × tCK + tAC (MAX) + 1000												
	ODT enable from MRS command	tMOD	MIN = 12 MAX = n/a												

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Notes:
1. All voltages are referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nomina voltage levels, but the related specifications and the operation of the device are warranted fo range specified. ODT is disabled for all measurements that are not ODT-specific.
3. Outputs measured with equivalent load (see Figure 16 (page 52)).
4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment, and tions are guaranteed for the specified AC input levels under normal use conditions. The slew signals used to test the device is 1.0 V/ns for signals in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$. S 1.0 V/ns may require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (that is, the re ly switch as a result of the signal crossing the AC input level and will remain in that state as lo does not ring back above [below] the DC input LOW [HIGH] level).
6. CK and CK# input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
7. Operating frequency is only allowed to change during self refresh mode (see Figure 79 (page power-down mode, or system reset condition (see Reset (page 132)). SSC allows for small devi frequency, provided the SSC guidelines are satisfied.
8. The clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK (AVG) MIN rate allowed (except for a deviation due to allowed clock jitter). Input clock jitter is allowed p exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.
9. Spread spectrum is not included in the jitter specification values. However, the input clock car spread spectrum at a sweep rate in the range 8–60 kHz with an additional one percent ^{t}CK (A spread spectrum may not use a clock rate below ^{t}CK (AVG) MIN or above ^{t}CK (AVG) MAX.
10. MIN (^{t}CL, ^{t}CH) refers to the smaller of the actual clock LOW time and the actual clock HIGH tir device. The clock's half period must also be of a Gaussian distribution; ^{t}CH (AVG) and ^{t}CL (AVG or without clock jitter and with or without duty cycle jitter. ^{t}CH (AVG) and ^{t}CL (AVG) are the a consecutive CK falling edges. ^{t}CH limits may be exceeded if the duty cycle jitter is small enoug half period limits (^{t}CH [ABS], ^{t}CL [ABS]) are not violated.
11. ^{t}HP (MIN) is the lesser of ^{t}CL and ^{t}CH actually applied to the device CK and CK# inputs; thus, ^{t}H of ^{t}CL (ABS) MIN and ^{t}CH (ABS) MIN.
12. The period jitter (^{t}JITper) is the maximum deviation in the clock period from the average or n in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL l DLL lock time, the jitter values should be 20 percent less those than noted in the table (DLL lo
13. The half-period jitter (^{t}JITdty) applies to either the high pulse of clock or the low pulse of cloc cumulatively can not exceed ^{t}JITper.
14. The cycle-to-cycle jitter (^{t}JITcc) is the amount the clock period can deviate from one cycle to th fies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values sho less than those noted in the table (DLL locked).
15. The cumulative jitter error ($^{t}ERR_{nper}$), where *n* is 2, 3, 4, 5, 6–10, or 11–50 is the amount of cloc consecutively accumulate away from the average clock over any number of clock cycles.
16. JEDEC specifies using $^{t}ERR_{6–10per}$ when derating clock-related output timing (see notes 19 and less derating by allowing $^{t}ERR_{5per}$ to be used.
17. This parameter is not referenced to a specific voltage level but is specified when the device ou driving (^{t}RPST) or beginning to drive (^{t}RPRE).

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18. The inputs to the DRAM must be aligned to the associated clock, that is, the actual clock that er, the input timing (in ns) references to the ^{t}CK (AVG) when determining the required numbe lowing input parameters are determined by taking the specified percentage times the ^{t}CK (AV ^{t}IPW, ^{t}DIPW, ^{t}DQSS, ^{t}DQSH, ^{t}DQSL, ^{t}DSS, ^{t}DSH, ^{t}WPST, and ^{t}WPRE.
19. The DRAM output timing is aligned to the nominal or average clock. Most output parameters the actual jitter error when input clock jitter is present; this will result in each parameter beco following parameters are required to be derated by subtracting $^{t}ERR_{5per}$ (MAX): ^{t}AC (MIN), ^{t}D (MIN), $^{t}LZ_{DQ}$ (MIN), ^{t}AON (MIN); while the following parameters are required to be derated by $^{t}ERR_{5per}$ (MIN): ^{t}AC (MAX), ^{t}DQSCK (MAX), ^{t}HZ (MAX), $^{t}LZ_{DQS}$ (MAX), $^{t}LZ_{DQ}$ (MAX), ^{t}AON (MAX ^{t}RPRE (MIN) is derated by subtracting ^{t}JITper (MAX), while ^{t}RPRE (MAX), is derated by subtrac The parameter ^{t}RPST (MIN) is derated by subtracting ^{t}JITdty (MAX), while ^{t}RPST (MAX), is dera ^{t}JITdty (MIN). Output timings that require $^{t}ERR_{5per}$ derating can be observed to have offsets re however, the total window will not degrade.
20. When DQS is used single-ended, the minimum limit is reduced by 100ps.
21. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These referenced to a specific voltage level, but specify when the device output is no longer driving ing (^{t}LZ).
22. ^{t}LZ (MIN) will prevail over a ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
23. This is not a device limit. The device will operate with a negative value, but system performan ded due to bus turnaround.
24. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The c ing from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bu WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
25. The intent of the "Don't Care" state after completion of the postamble is that the DQS-driver be HIGH, LOW, or High-Z, and that any signal transition within the input switching region mu requirements. That is, if DQS transitions HIGH (above $V_{IH[DC]min}$), then it must not transition LO prior to ^{t}DQSH (MIN).
26. Referenced to each output group: x4 = DQS with DQ[3:0]; x8 = DQS with DQ[7:0]; x16 = LDQS UDQS with DQ[15:8].
27. The data valid window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}Q The data valid window derates in direct proportion to the clock duty cycle and a practical dat be derived.
28. ^{t}QH = ^{t}HP - ^{t}QHS; the worst case ^{t}QH would be the lesser of ^{t}CL (ABS) MAX or ^{t}CH (ABS) MAX - ^{t}QHS. Minimizing the amount of ^{t}CH (AVG) offset and value of ^{t}JITdty will provide a larger ^{t} will provide a larger valid data out window.
29. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQ (MAX) condition.
30. The values listed are for the differential DQS strobe (DQS and DQS#) with a differential slew r for each signal). There are two sets of values listed: $^{t}DS_a$, $^{t}DH_a$ and $^{t}DS_b$, $^{t}DH_b$. The $^{t}DS_a$, $^{t}DH_a$ v only) are equivalent to the baseline values of $^{t}DS_b$, $^{t}DH_b$ at V_{REF} when the slew rate is 2 V/ns, c baseline values, $^{t}DS_b$, $^{t}DH_b$, are the JEDEC-defined values, referenced from the logic trip point from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while $^{t}DH_b$ is referenced from V_{IL} nal and $V_{IH(DC)}$ for a falling signal. If the differential DQS slew rate is not equal to 2 V/ns, then must be derated by adding the values from Table 31 (page 65) and Table 32 (page 67). If the D

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strobe feature is not enabled, then the DQS strobe is single-ended and the baseline values mu
Table 33 (page 68). Single-ended DQS data timing is referenced at DQS crossing V_{REF}. The corr
for a single-ended DQS strobe are listed in Table 34 (page 68)–Table 36 (page 69) on Table 34
Table 35 (page 69), and Table 36 (page 69); listed values are already derated for slew rate vari
verted from baseline values to V_{REF} values.

31. V_{IL}/V_{IH} DDR2 overshoot/undershoot. See AC Overshoot/Undershoot Specification (page 58).
32. For each input signal—not the group collectively.
33. There are two sets of values listed for command/address: $^{t}IS_a$, $^{t}IH_a$ and $^{t}IS_b$, $^{t}IH_b$. The $^{t}IS_a$, $^{t}IH_a$ v
only) are equivalent to the baseline values of $^{t}IS_b$, $^{t}IH_b$ at V_{REF} when the slew rate is 1 V/ns. Th
$^{t}IS_b$, $^{t}IH_b$, are the JEDEC-defined values, referenced from the logic trip points. $^{t}IS_b$ is referenced
rising signal and $V_{IL(AC)}$ for a falling signal, while $^{t}IH_b$ is referenced from $V_{IL(DC)}$ for a rising sign
falling signal. If the command/address slew rate is not equal to 1 V/ns, then the baseline value
by adding the values from Table 29 (page 61) and Table 30 (page 62).
34. This is applicable to READ cycles only. WRITE cycles generally require additional time due to ^{t}V
charge.
35. READs and WRITEs with auto precharge *are* allowed to be issued before ^{t}RAS (MIN) is satisfied
out feature is supported in DDR2 SDRAM.
36. When a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA timing applies w
CHARGE (ALL) command is issued, regardless of the number of banks open. For 8-bank device
= ^{t}RP (MIN) + ^{t}CK (AVG) (Table 12 (page 34) lists ^{t}RP [MIN] + ^{t}CK [AVG] MIN).
37. This parameter has a two clock minimum requirement at any ^{t}CK.
38. The ^{t}FAW (MIN) parameter applies to all 8-bank DDR2 devices. No more than four bank-ACTIV
be issued in a given ^{t}FAW (MIN) period. ^{t}RRD (MIN) restriction still applies.
39. The minimum internal READ-to-PRECHARGE time. This is the time from which the last 4-bit pr
when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command i
READ so that data will output CL later. This parameter is only applicable when $^{t}RTP/(2 \times {}^{t}CK) >$
cies faster than 533 MHz when ^{t}RTP = 7.5ns. If $^{t}RTP/(2 \times {}^{t}CK) \leq 1$, then equation AL + BL/2 app
to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE co
(MIN) has been satisfied.
40. ^{t}DAL = (*n*WR) + (^{t}RP/^{t}CK). Each of these terms, if not already an integer, should be rounded up
^{t}CK refers to the application clock period; *n*WR refers to the ^{t}WR parameter stored in the MRS
ple, -37E at ^{t}CK = 3.75ns with ^{t}WR programmed to four clocks would have ^{t}DAL = 4 + (15ns/3.7
clocks = 8 clocks.
41. The refresh period is 64ms (commercial) or 32ms (industrial and automotive). This equates to a
rate of 7.8125µs (commercial) or 3.9607µs (industrial and automotive). To ensure all rows of a
refreshed, 8192 REFRESH commands must be issued every 64ms (commercial) or 32ms (industr
The JEDEC ^{t}RFC MAX of 70,000ns is not required as bursting of AUTO REFRESH commands is a
42. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to C
moved in a system RESET condition (see Reset (page 132)).
43. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit, as shown in Figure
44. ^{t}CKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock e
main at the valid input level the entire time it takes to achieve the three clocks of registration
CKE transition, CKE may not transition from its valid level during the time period of $^{t}IS + 2 \times {}^{t}$

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45. The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must b amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD w 0.03, or 2.47, for ^{t}AOF (MIN) and 2.5 + 0.03, or 2.53, for ^{t}AOF (MAX).
46. ODT turn-on time ^{t}AON (MIN) is when the device leaves High-Z and ODT resistance begins to on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
47. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn o is when the bus is in High-Z. Both are measured from ^{t}AOFD.
48. Half-clock output parameters must be derated by the actual $^{t}ERR_{5per}$ and ^{t}JITdty when input c this will result in each parameter becoming larger. The parameter ^{t}AOF (MIN) is required to b tracting both $^{t}ERR_{5per}$ (MAX) and ^{t}JITdty (MAX). The parameter ^{t}AOF (MAX) is required to be ing both $^{t}ERR_{5per}$ (MIN) and ^{t}JITdty (MIN).
49. The -187E maximum limit is 2 × ^{t}CK + ^{t}AC (MAX) + 1000 but it will likely be 3 x ^{t}CK + ^{t}AC (MA future.
50. Should use 8 ^{t}CK for backward compatibility.
51. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to dress may result in reduction of the product lifetime.

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AC and DC Operating Conditions

Table 13: Recommended DC Operating Conditions (SSTL_18)

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.8	1.9	V	1, 2
V_{DDL} supply voltage	V_{DDL}	1.7	1.8	1.9	V	2, 3
I/O supply voltage	V_{DDQ}	1.7	1.8	1.9	V	2, 3
I/O reference voltage	$V_{REF(DC)}$	0.49 × V_{DDQ}	0.50 × V_{DDQ}	0.51 × V_{DDQ}	V	4
I/O termination voltage (system)	V_{TT}	$V_{REF(DC)}$ - 40	$V_{REF(DC)}$	$V_{REF(DC)}$ + 40	mV	5

Notes:
1. V_{DD} and V_{DDQ} must track each other. V_{DDQ} must be ≤ V_{DD}.
2. V_{SSQ} = V_{SSL} = V_{SS}.
3. V_{DDQ} tracks with V_{DD}; V_{DDL} tracks with V_{DD}.
4. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of $V_{REF(DC)}$. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
5. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

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ODT DC Electrical Characteristics

Table 14: ODT DC Electrical Characteristics

All voltages are referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
R_{TT} effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT1(EFF)}$	60	75	90	Ω	1, 2
R_{TT} effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT2(EFF)}$	120	150	180	Ω	1, 2
R_{TT} effective impedance value for 50Ω setting EMR (A6, A2) = 1, 1	$R_{TT3(EFF)}$	40	50	60	Ω	1, 2
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	–6	–	6	%	3

Notes:
1. $R_{TT1(EFF)}$ and $R_{TT2(EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(DC)}$ to the ball being tested, and then measuring current, $I(V_{IH[AC]})$, and $I(V_{IL[AC]})$, respectively.

$$R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

2. Minimum IT and AT device values are derated by six percent less when the devices operate between –40°C and 0°C (T_C).
3. Measure voltage (VM) at tested ball with no load.

$$\Delta VM = \left(\frac{2 \times VM}{V_{DD}Q} - 1\right) \times 100$$

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Input Electrical Characteristics and Operating Conditions

Table 15: Input DC Logic Levels

All voltages are referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input high (logic 1) voltage	$V_{IH(DC)}$	$V_{REF(DC)}$ + 125	V_{DDQ}[1]	mV
Input low (logic 0) voltage	$V_{IL(DC)}$	–300	$V_{REF(DC)}$ - 125	mV

Note: 1. V_{DDQ} + 300mV allowed provided 1.9V is not exceeded.

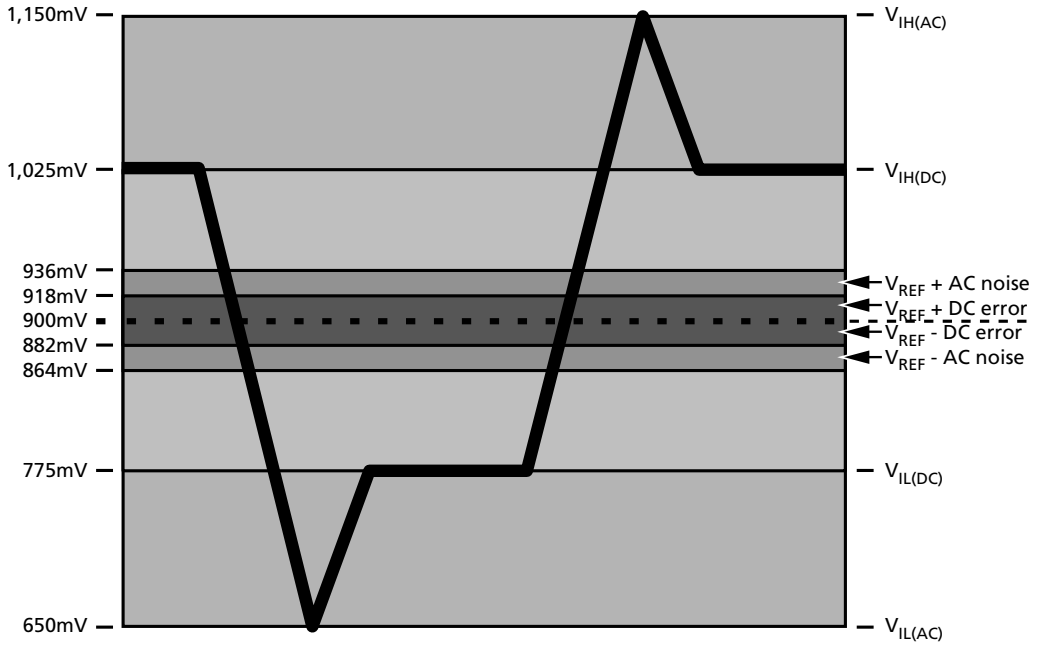
Table 16: Input AC Logic Levels

All voltages are referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input high (logic 1) voltage (-37E/-5E)	$V_{IH(AC)}$	$V_{REF(DC)}$ + 250	V_{DDQ}[1]	mV
Input high (logic 1) voltage (-187E/-25E/-25/-3E/-3)	$V_{IH(AC)}$	$V_{REF(DC)}$ + 200	V_{DDQ}[1]	mV
Input low (logic 0) voltage (-37E/-5E)	$V_{IL(AC)}$	–300	$V_{REF(DC)}$ - 250	mV
Input low (logic 0) voltage (-187E/-25E/-25/-3E/-3)	$V_{IL(AC)}$	–300	$V_{REF(DC)}$ - 200	mV

Note: 1. Refer to AC Overshoot/Undershoot Specification (page 58).

Figure 13: Single-Ended Input Signal Levels



Note: 1. Numbers in diagram reflect nominal DDR2-400/DDR2-533 values.

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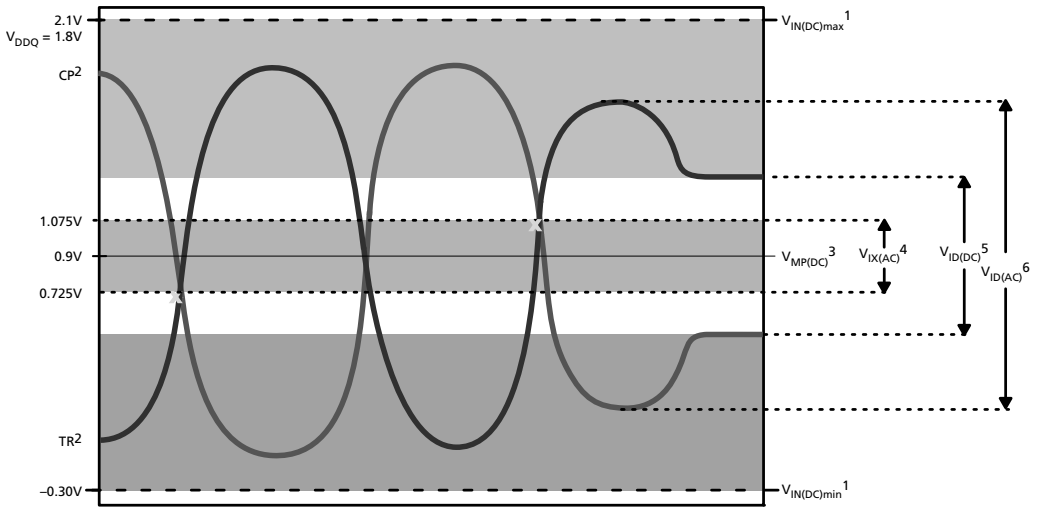
Table 17: Differential Input Logic Levels

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units	Notes
DC input signal voltage	$V_{IN(DC)}$	–300	V_{DDQ}	mV	1, 6
DC differential input voltage	$V_{ID(DC)}$	250	V_{DDQ}	mV	2, 6
AC differential input voltage	$V_{ID(AC)}$	500	V_{DDQ}	mV	3, 6
AC differential cross-point voltage	$V_{IX(AC)}$	0.50 × V_{DDQ} - 175	0.50 × V_{DDQ} + 175	mV	4
Input midpoint voltage	$V_{MP(DC)}$	850	950	mV	5

Notes:
1. $V_{IN(DC)}$ specifies the allowable DC execution of each input of differential pair such as CK, CK#, DQS, DQS#, LDQS, LDQS#, UDQS, UDQS#, and RDQS, RDQS#.
2. $V_{ID(DC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#) level. The minimum value is equal to $V_{IH(DC)} - V_{IL(DC)}$. Differential input signal levels are shown in Figure 14.
3. $V_{ID(AC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#) level. The minimum value is equal to $V_{IH(AC)} - V_{IL(AC)}$, as shown in Table 16 (page 48).
4. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DDQ} of the transmitting device and $V_{IX(AC)}$ is expected to track variations in V_{DDQ}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross, as shown in Figure 14.
5. $V_{MP(DC)}$ specifies the input differential common mode voltage $(V_{TR} + V_{CP})/2$ where V_{TR} is the true input (CK, DQS) level and V_{CP} is the complementary input (CK#, DQS#). $V_{MP(DC)}$ is expected to be approximately 0.5 × V_{DDQ}.
6. V_{DDQ} + 300mV allowed provided 1.9V is not exceeded.

Figure 14: Differential Input Signal Levels



Notes:
1. TR and CP may not be more positive than V_{DDQ} + 0.3V or more negative than V_{SS} - 0.3V.
2. TR represents the CK, DQS, RDQS, LDQS, and UDQS signals; CP represents CK#, DQS#, RDQS#, LDQS#, and UDQS# signals.
3. This provides a minimum of 850mV to a maximum of 950mV and is expected to be

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V_{DDQ}/2.

4. TR and CP must cross in this region.
5. TR and CP must meet at least $V_{ID(DC)min}$ when static and is centered around $V_{MP(DC)}$.
6. TR and CP must have a minimum 500mV peak-to-peak swing.
7. Numbers in diagram reflect nominal values (V_{DDQ} = 1.8V).

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Output Electrical Characteristics and Operating Conditions

Table 18: Differential AC Output Parameters

Parameter	Symbol	Min	Max	Units	Notes
AC differential cross-point voltage	$V_{OX(AC)}$	0.50 × V_{DDQ} - 125	0.50 × V_{DDQ} + 125	mV	1

Note: 1. The typical value of $V_{OX(AC)}$ is expected to be about 0.5 × V_{DDQ} of the transmitting device and $V_{OX(AC)}$ is expected to track variations in V_{DDQ}. $V_{OX(AC)}$ indicates the voltage at which differential output signals must cross.

Figure 15: Differential Output Signal Levels

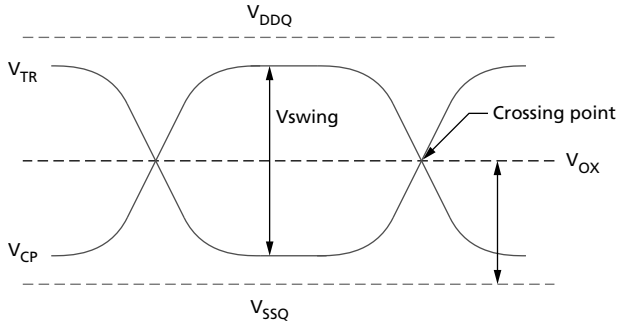

Table 19: Output DC Current Drive

Parameter	Symbol	Value	Units	Notes
Output MIN source DC current	I_{OH}	–13.4	mA	1, 2, 4
Output MIN sink DC current	I_{OL}	13.4	mA	2, 3, 4

Notes:
1. For $I_{OH(DC)}$; V_{DDQ} = 1.7V, V_{OUT} = 1,420mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV.
2. For $I_{OL(DC)}$; V_{DDQ} = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of $I_{OH(DC)}$ and $I_{OL(DC)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure $V_{IH,min}$ plus a noise margin and $V_{IL,max}$ minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see output IV curves) along a 21Ω load line to define a convenient driver current for measurement.

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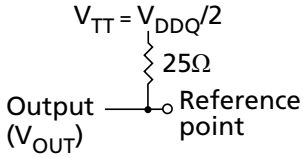
Table 20: Output Characteristics

Parameter	Min	Nom	Max	Units	Notes
Output impedance	See Output Driver Characteristics (page 53)			Ω	1, 2
Pull-up and pull-down mismatch	0	–	4	Ω	1, 2, 3
Output slew rate	1.5	–	5	V/ns	1, 4, 5, 6

Notes:
1. Absolute specifications: 0°C ≤ T_C ≤ +85°C; V_{DDQ} = 1.8V ±0.1V, V_{DD} = 1.8V ±0.1V.
2. Impedance measurement conditions for output source DC current: V_{DDQ} = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - V_{DDQ})/I_{OH} must be less than 23.4Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV. The impedance measurement condition for output sink DC current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is an absolute value between pull-up and pull-down; both are measured at the same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single-ended signals. For differential signals (DQS, DQS#), output slew rate is measured between DQS - DQS# = –500mV and DQS# - DQS = 500mV. Output slew rate is guaranteed by design but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from $V_{IL(DC)max}$ to $V_{IH(DC)min}$ is equal to or greater than the slew rate as measured from $V_{IL(AC)max}$ to $V_{IH(AC)min}$. This is guaranteed by design and characterization.
6. IT and AT devices require an additional 0.4 V/ns in the MAX limit when T_C is between –40°C and 0°C.

Figure 16: Output Slew Rate Load



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Output Driver Characteristics

Figure 17: Full Strength Pull-Down Characteristics

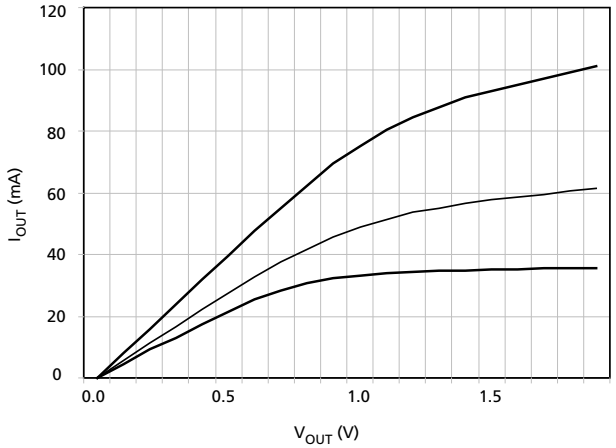

Table 21: Full Strength Pull-Down Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	4.30	5.63	7.95
0.2	8.60	11.30	15.90
0.3	12.90	16.52	23.85
0.4	16.90	22.19	31.80
0.5	20.40	27.59	39.75
0.6	23.28	32.39	47.70
0.7	25.44	36.45	55.55
0.8	26.79	40.38	62.95
0.9	27.67	44.01	69.55
1.0	28.38	47.01	75.35
1.1	28.96	49.63	80.35
1.2	29.46	51.71	84.55
1.3	29.90	53.32	87.95
1.4	30.29	54.9	90.70
1.5	30.65	56.03	93.00
1.6	30.98	57.07	95.05
1.7	31.31	58.16	97.05
1.8	31.64	59.27	99.05
1.9	31.96	60.35	101.05

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Figure 18: Full Strength Pull-Up Characteristics

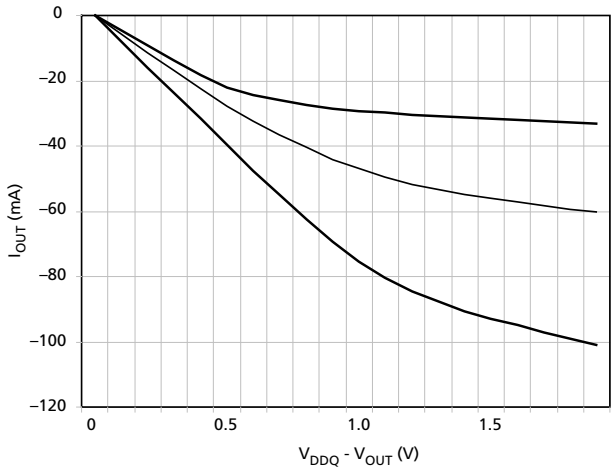

Table 22: Full Strength Pull-Up Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	–4.30	–5.63	–7.95
0.2	–8.60	–11.30	–15.90
0.3	–12.90	–16.52	–23.85
0.4	–16.90	–22.19	–31.80
0.5	–20.40	–27.59	–39.75
0.6	–23.28	–32.39	–47.70
0.7	–25.44	–36.45	–55.55
0.8	–26.79	–40.38	–62.95
0.9	–27.67	–44.01	–69.55
1.0	–28.38	–47.01	–75.35
1.1	–28.96	–49.63	–80.35
1.2	–29.46	–51.71	–84.55
1.3	–29.90	–53.32	–87.95
1.4	–30.29	–54.90	–90.70
1.5	–30.65	–56.03	–93.00
1.6	–30.98	–57.07	–95.05
1.7	–31.31	–58.16	–97.05
1.8	–31.64	–59.27	–99.05
1.9	–31.96	–60.35	–101.05

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Figure 19: Reduced Strength Pull-Down Characteristics

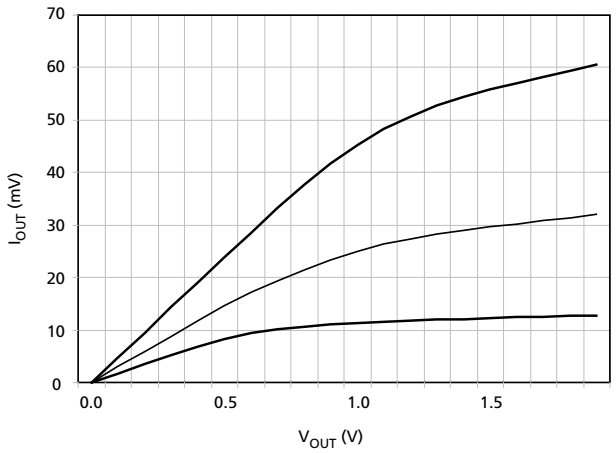

Table 23: Reduced Strength Pull-Down Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	1.72	2.98	4.77
0.2	3.44	5.99	9.54
0.3	5.16	8.75	14.31
0.4	6.76	11.76	19.08
0.5	8.16	14.62	23.85
0.6	9.31	17.17	28.62
0.7	10.18	19.32	33.33
0.8	10.72	21.40	37.77
0.9	11.07	23.32	41.73
1.0	11.35	24.92	45.21
1.1	11.58	26.30	48.21
1.2	11.78	27.41	50.73
1.3	11.96	28.26	52.77
1.4	12.12	29.10	54.42
1.5	12.26	29.70	55.80
1.6	12.39	30.25	57.03
1.7	12.52	30.82	58.23
1.8	12.66	31.41	59.43
1.9	12.78	31.98	60.63

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Figure 20: Reduced Strength Pull-Up Characteristics

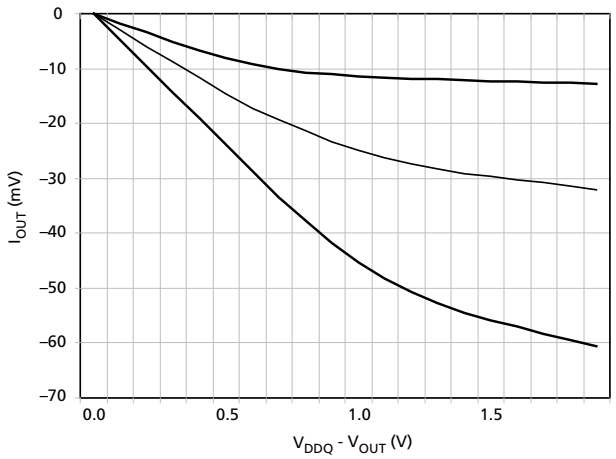

Table 24: Reduced Strength Pull-Up Current (mA)

Voltage (V)	Min	Nom	Max
0.0	0.00	0.00	0.00
0.1	–1.72	–2.98	–4.77
0.2	–3.44	–5.99	–9.54
0.3	–5.16	–8.75	–14.31
0.4	–6.76	–11.76	–19.08
0.5	–8.16	–14.62	–23.85
0.6	–9.31	–17.17	–28.62
0.7	–10.18	–19.32	–33.33
0.8	–10.72	–21.40	–37.77
0.9	–11.07	–23.32	–41.73
1.0	–11.35	–24.92	–45.21
1.1	–11.58	–26.30	–48.21
1.2	–11.78	–27.41	–50.73
1.3	–11.96	–28.26	–52.77
1.4	–12.12	–29.10	–54.42
1.5	–12.26	–29.69	–55.8
1.6	–12.39	–30.25	–57.03
1.7	–12.52	–30.82	–58.23
1.8	–12.66	–31.42	–59.43
1.9	–12.78	–31.98	–60.63

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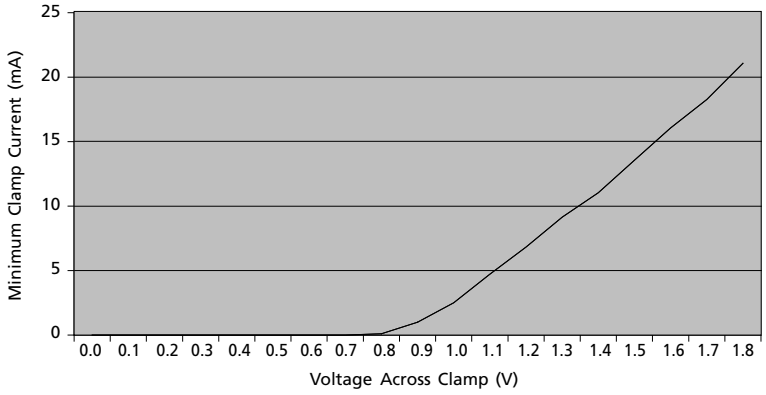
Power and Ground Clamp Characteristics

Power and ground clamps are provided on the following input-only balls: Address balls, bank address balls, CS#, RAS#, CAS#, WE#, ODT, and CKE.

Table 25: Input Clamp Characteristics

Voltage Across Clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Figure 21: Input Clamp Characteristics



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AC Overshoot/Undershoot Specification

Table 26: Address and Control Balls

Applies to address balls, bank address balls, CS#, RAS#, CAS#, WE#, CKE, and ODT

Parameter	Specification				
	-187E	-25/-25E	-3/-3E	-37E	-5E
Maximum peak amplitude allowed for overshoot area (see Figure 22)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum peak amplitude allowed for undershoot area (see Figure 23)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum overshoot area above V_{DD} (see Figure 22)	0.5 Vns	0.66 Vns	0.80 Vns	1.00 Vns	1.33 Vns
Maximum undershoot area below V_{SS} (see Figure 23)	0.5 Vns	0.66 Vns	0.80 Vns	1.00 Vns	1.33 Vns

Table 27: Clock, Data, Strobe, and Mask Balls

Applies to DQ, DQS, DQS#, RDQS, RDQS#, UDQS, UDQS#, LDQS, LDQS#, DM, UDM, and LDM

Parameter	Specification				
	-187E	-25/-25E	-3/-3E	-37E	-5E
Maximum peak amplitude allowed for overshoot area (see Figure 22)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum peak amplitude allowed for undershoot area (see Figure 23)	0.50V	0.50V	0.50V	0.50V	0.50V
Maximum overshoot area above V_{DDQ} (see Figure 22)	0.19 Vns	0.23 Vns	0.23 Vns	0.28 Vns	0.38 Vns
Maximum undershoot area below V_{SSQ} (see Figure 23)	0.19 Vns	0.23 Vns	0.23 Vns	0.28 Vns	0.38 Vns

Figure 22: Overshoot

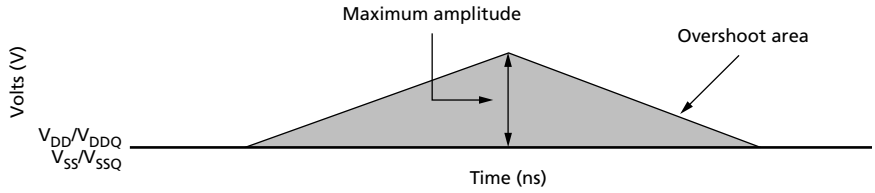

Figure 23: Undershoot

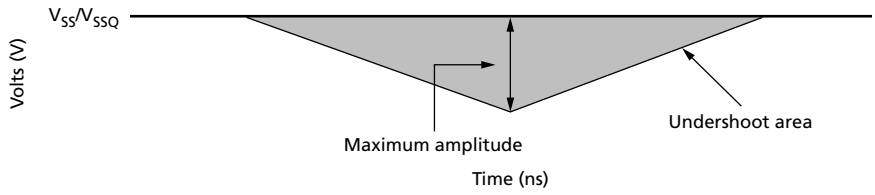

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Table 28: AC Input Test Conditions

Parameter	Symbol	Min	Max	Units	Notes
Input setup timing measurement reference level address balls, bank address balls, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	V_{RS}	See Note 2			1, 2, 3, 4
Input hold timing measurement reference level address balls, bank address balls, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	V_{RH}	See Note 5			1, 3, 4, 5
Input timing measurement reference level (single-ended) DQS for x4, x8; UDQS, LDQS for x16	$V_{REF(DC)}$	V_{DDQ} × 0.49	V_{DDQ} × 0.51	V	1, 3, 4, 6
Input timing measurement reference level (differential) CK, CK# for x4, x8, x16; DQS, DQS# for x4, x8; RDQS, RDQS# for x8; UDQS, UDQS#, LDQS, LDQS# for x16	V_{RD}	$V_{IX(AC)}$		V	1, 3, 7, 8, 9

Notes:
1. All voltages referenced to V_{SS}.
2. Input waveform setup timing ($^{t}IS_b$) is referenced from the input signal crossing at the $V_{IH(AC)}$ level for a rising signal and $V_{IL(AC)}$ for a falling signal applied to the device under test, as shown in Figure 32 (page 72).
3. See Input Slew Rate Derating (page 60).
4. The slew rate for single-ended inputs is measured from DC level to AC level, $V_{IL(DC)}$ to $V_{IH(AC)}$ on the rising edge and $V_{IL(AC)}$ to $V_{IH(DC)}$ on the falling edge. For signals referenced to V_{REF}, the valid intersection is where the "tangent" line intersects V_{REF}, as shown in Figure 25 (page 63), Figure 27 (page 64), Figure 29 (page 70), and Figure 31 (page 71).
5. Input waveform hold ($^{t}IH_b$) timing is referenced from the input signal crossing at the $V_{IL(DC)}$ level for a rising signal and $V_{IH(DC)}$ for a falling signal applied to the device under test, as shown in Figure 32 (page 72).
6. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) for single-ended data strobe is referenced from the crossing of DQS, UDQS, or LDQS through the Vref level applied to the device under test, as shown in Figure 34 (page 73).
7. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) when differential data strobe is enabled is referenced from the cross-point of DQS/DQS#, UDQS/UDQS#, or LDQS/LDQS#, as shown in Figure 33 (page 72).
8. Input waveform timing is referenced to the crossing point level (V_{IX}) of two input signals (V_{TR} and V_{CP}) applied to the device under test, where V_{TR} is the true input signal and V_{CP} is the complementary input signal, as shown in Figure 35 (page 73).
9. The slew rate for differentially ended inputs is measured from twice the DC level to twice the AC level: 2 × $V_{IL(DC)}$ to 2 × $V_{IH(AC)}$ on the rising edge and 2 × $V_{IL(AC)}$ to 2 × $V_{IH(DC)}$ on the falling edge. For example, the CK/CK# would be –250mV to 500mV for CK rising edge and would be 250mV to –500mV for CK falling edge.

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Input Slew Rate Derating

For all input signals, the total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the data sheet ^{t}IS (base) and ^{t}IH (base) value to the Δ^{t}IS and Δ^{t}IH derating value, respectively. Example: ^{t}IS (total setup time) = ^{t}IS (base) + Δ^{t}IS.

^{t}IS, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. Setup nominal slew rate (^{t}IS) for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$.

If the actual signal is always earlier than the nominal slew rate line between shaded "$V_{REF(DC)}$ to AC region," use the nominal slew rate for the derating value (Figure 24 (page 63)).

If the actual signal is later than the nominal slew rate line anywhere between the shaded "$V_{REF(DC)}$ to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for the derating value (see Figure 25 (page 63)).

^{t}IH, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. ^{t}IH, nominal slew rate for a falling signal, is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$.

If the actual signal is always later than the nominal slew rate line between shaded "DC to $V_{REF(DC)}$ region," use the nominal slew rate for the derating value (Figure 26 (page 64)).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to $V_{REF(DC)}$ region," the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (Figure 27 (page 64)).

Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH(AC)}/V_{IL(AC)}$.

For slew rates in between the values listed in Table 29 (page 61) and Table 30 (page 62), the derating values may obtained by linear interpolation.

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Table 29: DDR2-400/533 Setup and Hold Time Derating Values (^{t}IS and ^{t}IH)

Command/Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	
4.0	187	94	217	124	247	154	ps
3.5	179	89	209	119	239	149	ps
3.0	167	83	197	113	227	143	ps
2.5	150	75	180	105	210	135	ps
2.0	125	45	155	75	185	105	ps
1.5	83	21	113	51	143	81	ps
1.0	0	0	30	30	60	60	ps
0.9	–11	–14	19	16	49	46	ps
0.8	–25	–31	5	–1	35	29	ps
0.7	–43	–54	–13	–24	17	6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

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Table 30: DDR2-667/800/1066 Setup and Hold Time Derating Values (^{t}IS and ^{t}IH)

Command/ Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Units
4.0	150	94	180	124	210	154	ps
3.5	143	89	173	119	203	149	ps
3.0	133	83	163	113	193	143	ps
2.5	120	75	150	105	180	135	ps
2.0	100	45	160	75	160	105	ps
1.5	67	21	97	51	127	81	ps
1.0	0	0	30	30	60	60	ps
0.9	–5	–14	25	16	55	46	ps
0.8	–13	–31	17	–1	47	29	ps
0.7	–22	–54	8	–24	38	6	ps
0.6	–34	–83	–4	–53	36	–23	ps
0.5	–60	–125	–30	–95	0	–65	ps
0.4	–100	–188	–70	–158	–40	–128	ps
0.3	–168	–292	–138	–262	–108	–232	ps
0.25	–200	–375	–170	–345	–140	–315	ps
0.2	–325	–500	–295	–470	–265	–440	ps
0.15	–517	–708	–487	–678	–457	–648	ps
0.1	–1000	–1125	–970	–1095	–940	–1065	ps

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Figure 24: Nominal Slew Rate for ^{t}IS

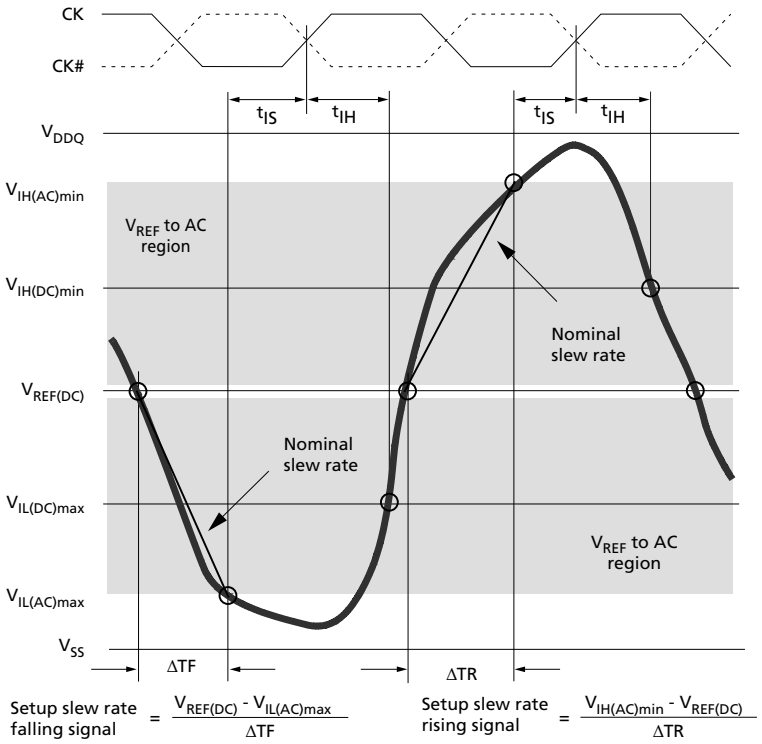

Figure 25: Tangent Line for ^{t}IS

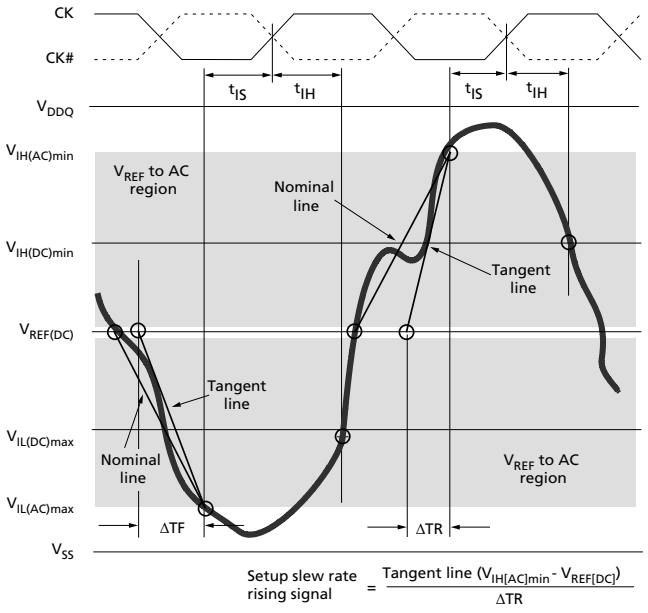

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Figure 26: Nominal Slew Rate for ^{t}IH

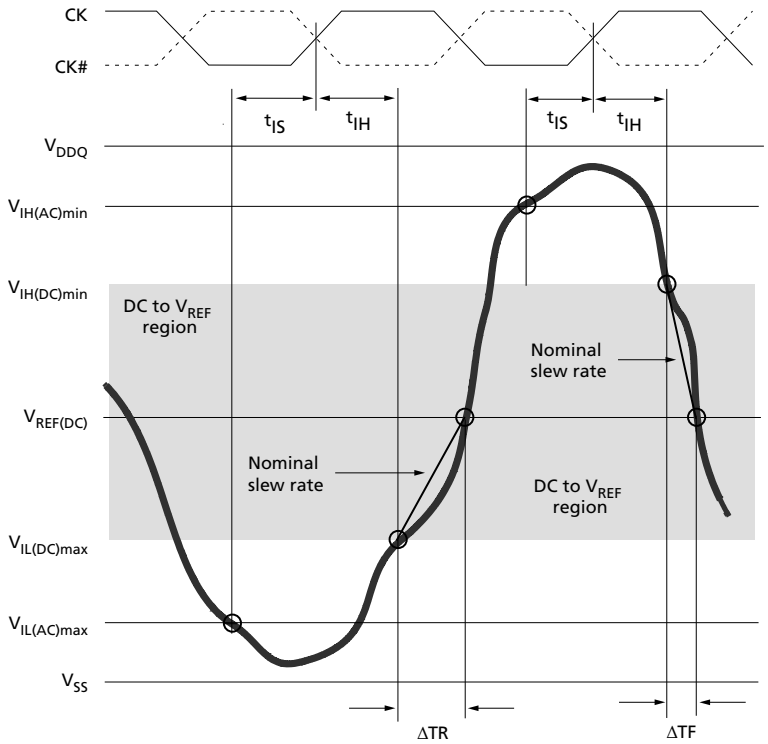
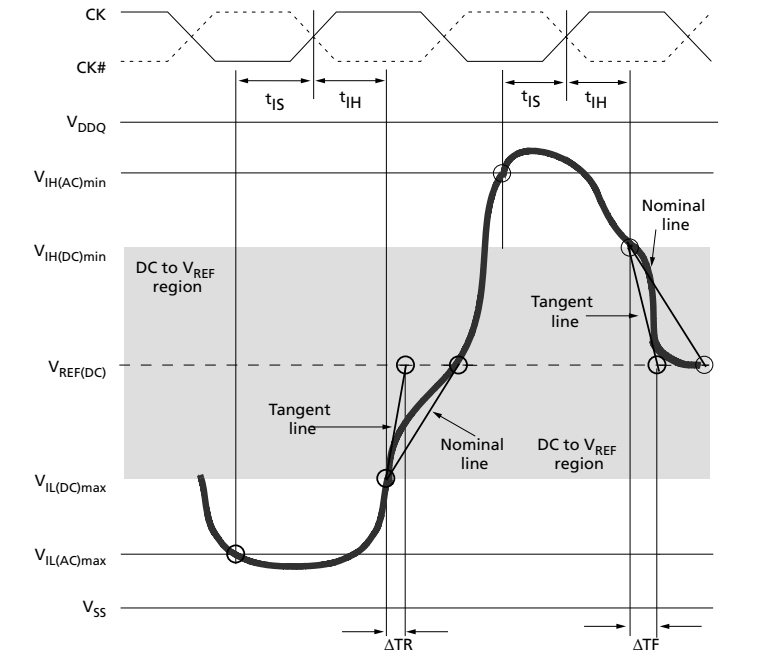


Figure 27: Tangent Line for ^{t}IH



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF[DC]} - V_{IL[DC]max})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH[DC]min} - V_{REF[DC]})}{\Delta TF}$$

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Table 31: DDR2-400/533 ^{t}DS, ^{t}DH Derating Values with Differential Strobe

All units are shown in picoseconds

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH
2.0	125	45	125	45	125	45	–	–	–	–	–	–	–	–	–	–	–	–
1.5	83	21	83	21	83	21	95	33	–	–	–	–	–	–	–	–	–	–
1.0	0	0	0	0	0	0	12	12	24	24	–	–	–	–	–	–	–	–
0.9	–	–	–11	–14	–11	–14	1	–2	13	10	25	22	–	–	–	–	–	–
0.8	–	–	–	–	–25	–31	–13	–19	–1	–7	11	5	23	17	–	–	–	–
0.7	–	–	–	–	–	–	–31	–42	–19	–30	–7	–18	5	–6	17	6	–	–
0.6	–	–	–	–	–	–	–	–	–43	–59	–31	–47	–19	–35	–7	–23	5	–11
0.5	–	–	–	–	–	–	–	–	–	–	–74	–89	–62	–77	–50	–65	–38	–53
0.4	–	–	–	–	–	–	–	–	–	–	–	–	–127	–140	–115	–128	–103	–116

Notes:
1. For all input signals, the total ^{t}DS and ^{t}DH required is calculated by adding the data sheet value to the derating value listed in Table 31.
2. ^{t}DS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. ^{t}DS nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded "$V_{REF(DC)}$ to AC region," use the nominal slew rate for the derating value (see Figure 28 (page 70)). If the actual signal is later than the nominal slew rate line anywhere between the shaded "$V_{REF(DC)}$ to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for the derating value (see Figure 29 (page 70)).
3. ^{t}DH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. ^{t}DH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded "DC level to $V_{REF(DC)}$ region," use the nominal slew rate for the derating value (see Figure 30 (page 71)). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to $V_{REF(DC)}$ region," the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see Figure 31 (page 71)).
4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH(AC)}/V_{IL(AC)}$.
5. For slew rates between the values listed in this table, the derating values may be obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.
7. Single-ended DQS requires special derating. The values in Table 33 (page 68) are the DQS single-ended slew rate derating with DQS referenced at V_{REF} and DQ referenced at the logic levels $^{t}DS_b$ and $^{t}DH_b$. Converting the derated base values from DQ referenced to the AC/DC trip points to DQ referenced to V_{REF} is listed in Table 35 (page 69) and Table 36 (page 69). Table 35 provides the V_{REF}-based fully derated values for the DQ

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($^{t}DS_a$ and $^{t}DH_a$) for DDR2-533. Table 36 provides the V_{REF}-based fully derated values for the DQ ($^{t}DS_a$ and $^{t}DH_a$) for DDR2-400.

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Table 32: DDR2-667/800/1066 ^{t}DS, ^{t}DH Derating Values with Differential Strobe

All units are shown in picoseconds

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	2.8 V/ns		2.4 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH	Δ ^{t}DS	Δ ^{t}DH
2.0	100	63	100	63	100	63	112	75	124	87	136	99	148	111	160	123	172	135
1.5	67	42	67	42	67	42	79	54	91	66	103	78	115	90	127	102	139	114
1.0	0	0	0	0	0	0	12	12	24	24	36	36	48	48	60	60	72	72
0.9	–5	–14	–5	–14	–5	–14	7	–2	19	10	31	22	43	34	55	46	67	58
0.8	–13	–31	–13	–31	–13	–31	–1	–19	11	–7	23	5	35	17	47	29	59	41
0.7	–22	–54	–22	–54	–22	–54	–10	–42	2	–30	14	–18	26	–6	38	6	50	18
0.6	–34	–83	–34	–83	–34	–83	–22	–71	–10	–59	2	–47	14	–35	26	–23	38	–11
0.5	–60	–125	–60	–125	–60	–125	–48	–113	–36	–101	–24	–89	–12	–77	0	–65	12	–53
0.4	–100	–188	–100	–188	–100	–188	–88	–176	–76	–164	–64	–152	–52	–140	–40	–128	–28	–116

Notes:
1. For all input signals the total ^{t}DS and ^{t}DH required is calculated by adding the data sheet value to the derating value listed in Table 32.
2. ^{t}DS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)min}$. ^{t}DS nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded "$V_{REF(DC)}$ to AC region," use the nominal slew rate for the derating value (see Figure 28 (page 70)). If the actual signal is later than the nominal slew rate line anywhere between shaded "$V_{REF(DC)}$ to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for the derating value (see Figure 29 (page 70)).
3. ^{t}DH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REF(DC)}$. ^{t}DH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between the shaded "DC level to $V_{REF(DC)}$ region," use the nominal slew rate for the derating value (see Figure 30 (page 71)). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded "DC to $V_{REF(DC)}$ region," the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for the derating value (see Figure 31 (page 71)).
4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached $V_{IH[AC]}/V_{IL[AC]}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH(AC)}/V_{IL(AC)}$.
5. For slew rates between the values listed in this table, the derating values may be obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.
7. Single-ended DQS requires special derating. The values in Table 33 (page 68) are the DQS single-ended slew rate derating with DQS referenced at V_{REF} and DQ referenced at the logic levels $^{t}DS_b$ and $^{t}DH_b$. Converting the derated base values from DQ referenced to the AC/DC trip points to DQ referenced to V_{REF} is listed in Table 34 (page 68). Table 34 provides the V_{REF}-based fully derated values for the DQ ($^{t}DS_a$ and $^{t}DH_a$) for

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DDR2-667. It is not advised to operate DDR2-800 and DDR2-1066 devices with single-ended DQS; however, Table 33 would be used with the base values.

Table 33: Single-Ended DQS Slew Rate Derating Values Using $^{t}DS_{b}$ and $^{t}DH_{b}$

Reference points indicated in bold; Derating values are to be used with base $^{t}DS_{b}$- and $^{t}DH_{b}$-specified values

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH
2.0	130	53	130	53	130	53	130	53	130	53	145	48	155	45	165	41	175	38
1.5	97	32	97	32	97	32	97	32	97	32	112	27	122	24	132	20	142	17
1.0	30	–10	30	–10	30	–10	30	–10	30	–10	**45**	**–15**	55	–18	65	–22	75	–25
0.9	25	–24	25	–24	25	–24	25	–24	25	–24	40	–29	50	–32	60	–36	70	–39
0.8	17	–41	17	–41	17	–41	17	–41	17	–41	32	–46	42	–49	52	–53	61	–56
0.7	5	–64	5	–64	5	–64	5	–64	5	–64	20	–69	30	–72	40	–75	50	–79
0.6	–7	–93	–7	–93	–7	–93	–7	–93	–7	–93	8	–98	18	–102	28	–105	38	–108
0.5	–28	–135	–28	–135	–28	–135	–28	–135	–28	–135	–13	–140	–3	–143	7	–147	17	–150
0.4	–78	–198	–78	–198	–78	–198	–78	–198	–78	–198	–63	–203	–53	–206	–43	–210	–33	–213

Table 34: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at V_{REF}) at DDR2-667

Reference points indicated in bold

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH
2.0	330	291	330	291	330	291	330	291	330	291	345	286	355	282	365	29	375	276
1.5	330	290	330	290	330	290	330	290	330	290	345	285	355	282	365	279	375	275
1.0	330	290	330	290	330	290	330	290	330	290	**345**	**285**	355	282	365	278	375	275
0.9	347	290	347	290	347	290	347	290	347	290	362	285	372	282	382	278	392	275
0.8	367	290	367	290	367	290	367	290	367	290	382	285	392	282	402	278	412	275
0.7	391	290	391	290	391	290	391	290	391	290	406	285	416	281	426	278	436	275
0.6	426	290	426	290	426	290	426	290	426	290	441	285	451	282	461	278	471	275
0.5	472	290	472	290	472	290	472	290	472	290	487	285	497	282	507	278	517	275
0.4	522	289	522	289	522	289	522	289	522	289	537	284	547	281	557	278	567	274

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Table 35: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at V_{REF}) at DDR2-533

Reference points indicated in bold

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH
2.0	355	341	355	341	355	341	355	341	355	341	370	336	380	332	390	329	400	326
1.5	364	340	364	340	364	340	364	340	364	340	379	335	389	332	399	329	409	325
1.0	380	340	380	340	380	340	380	340	380	340	**395**	**335**	405	332	415	328	425	325
0.9	402	340	402	340	402	340	402	340	402	340	417	335	427	332	437	328	447	325
0.8	429	340	429	340	429	340	429	340	429	340	444	335	454	332	464	328	474	325
0.7	463	340	463	340	463	340	463	340	463	340	478	335	488	331	498	328	508	325
0.6	510	340	510	340	510	340	510	340	510	340	525	335	535	332	545	328	555	325
0.5	572	340	572	340	572	340	572	340	572	340	587	335	597	332	607	328	617	325
0.4	647	339	647	339	647	339	647	339	647	339	662	334	672	331	682	328	692	324

Table 36: Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at V_{REF}) at DDR2-400

Reference points indicated in bold

	DQS Single-Ended Slew Rate Derated (at V_{REF})																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4 V/ns	
DQ (V/ns)	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH	^{t}DS	^{t}DH
2.0	405	391	405	391	405	391	405	391	405	391	420	386	430	382	440	379	450	376
1.5	414	390	414	390	414	390	414	390	414	390	429	385	439	382	449	379	459	375
1.0	430	390	430	390	430	390	430	390	430	390	**445**	**385**	455	382	465	378	475	375
0.9	452	390	452	390	452	390	452	390	452	390	467	385	477	382	487	378	497	375
0.8	479	390	479	390	479	390	479	390	479	390	494	385	504	382	514	378	524	375
0.7	513	390	513	390	513	390	513	390	513	390	528	385	538	381	548	378	558	375
0.6	560	390	560	390	560	390	560	390	560	390	575	385	585	382	595	378	605	375
0.5	622	390	622	390	622	390	622	390	622	390	637	385	647	382	657	378	667	375
0.4	697	389	697	389	697	389	697	389	697	389	712	384	722	381	732	378	742	374

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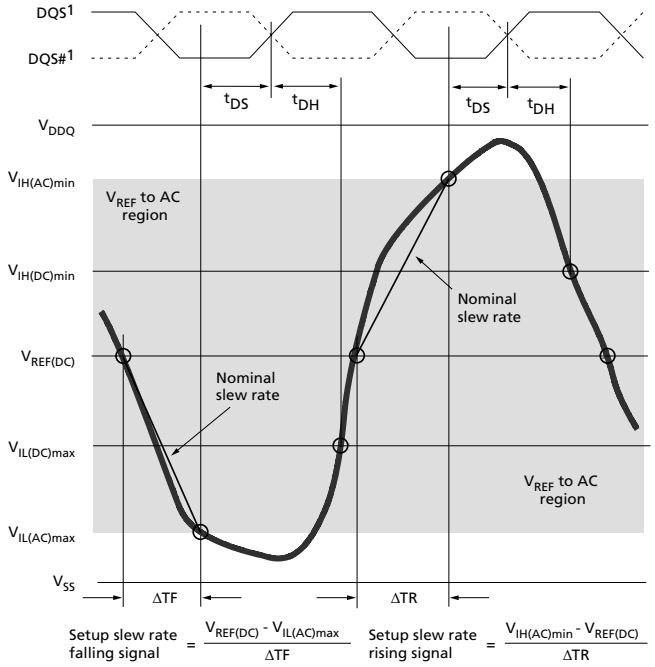
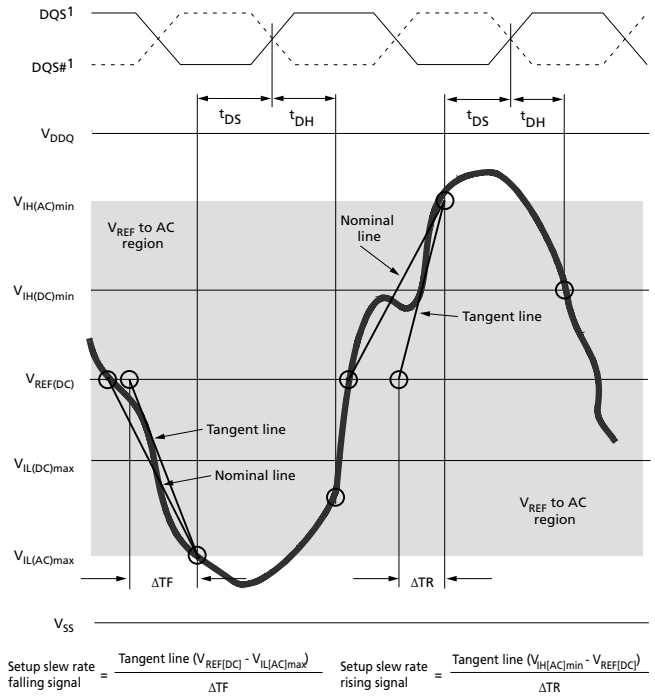
Figure 28: Nominal Slew Rate for ^{t}DS



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

Figure 29: Tangent Line for ^{t}DS



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

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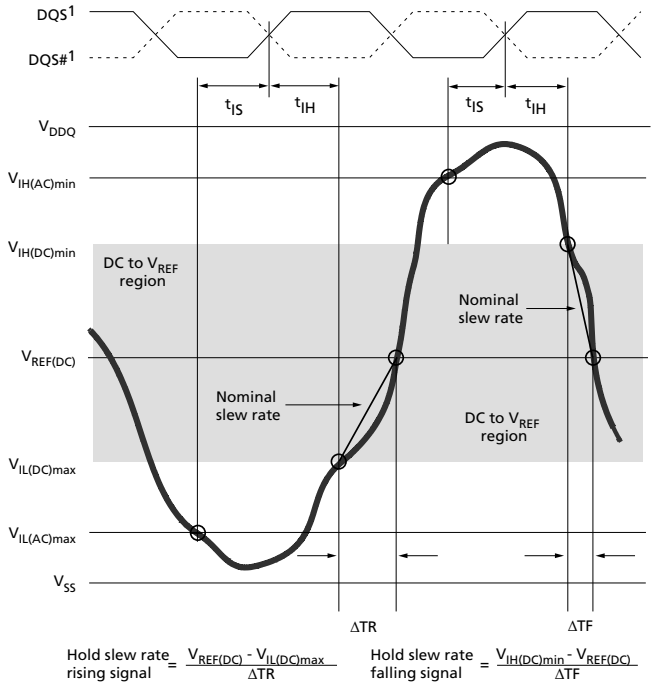
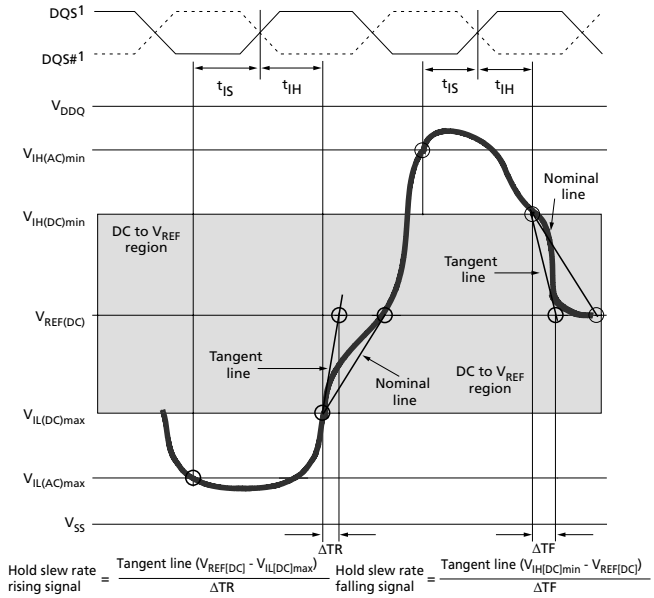
Figure 30: Nominal Slew Rate for ^{t}DH



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

Figure 31: Tangent Line for ^{t}DH



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

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Figure 32: AC Input Test Signal Waveform Command/Address Balls

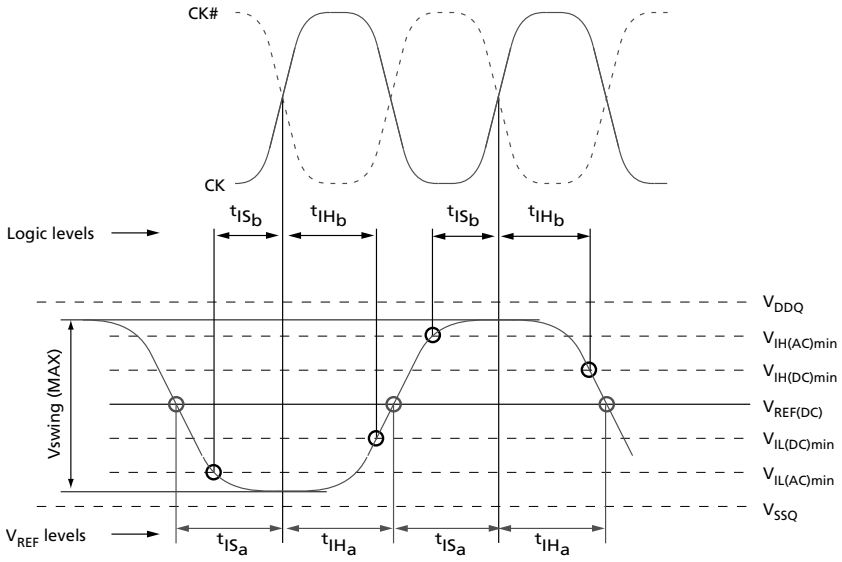

Figure 33: AC Input Test Signal Waveform for Data with DQS, DQS# (Differential)

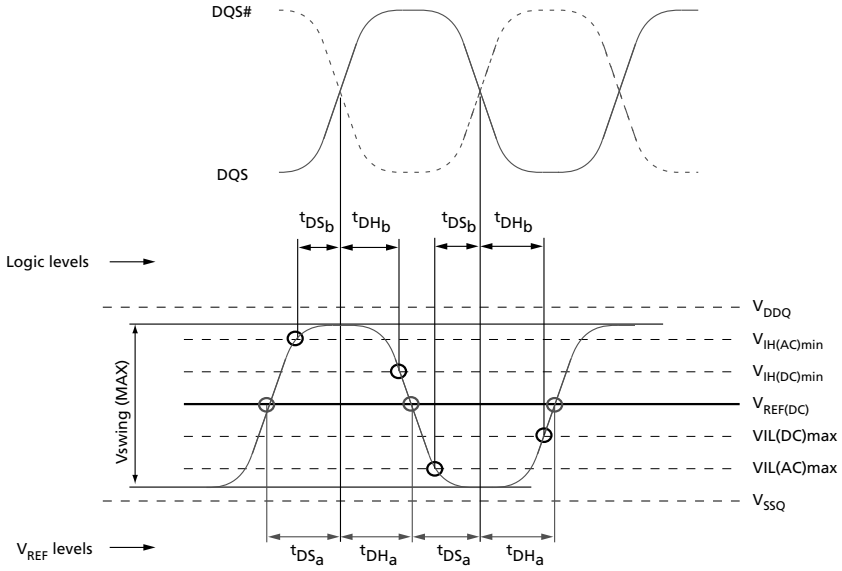

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Figure 34: AC Input Test Signal Waveform for Data with DQS (Single-Ended)

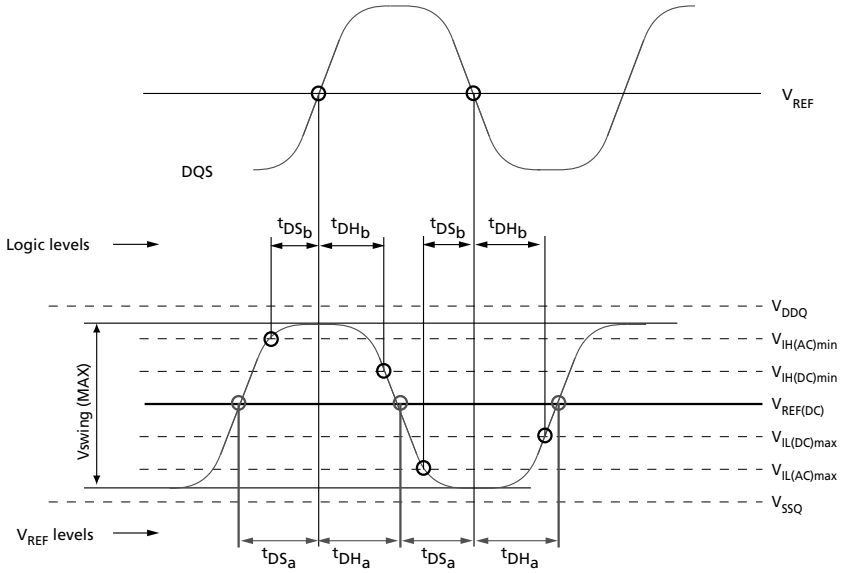
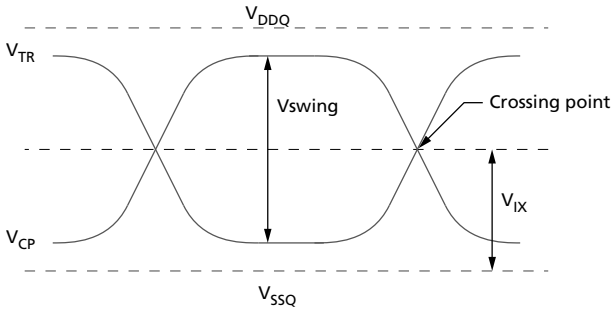


Figure 35: AC Input Test Signal Waveform (Differential)



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Commands

Truth Tables

The following tables provide a quick reference of available DDR2 SDRAM commands, including CKE power-down modes and bank-to-bank commands.

Table 37: Truth Table – DDR2 Commands

Notes: 1–3 apply to the entire table

Function	CKE		CS#	RAS#	CAS#	WE#	BA2–BA0	An–A11	A10	A9–A0	Notes
	Previous Cycle	Current Cycle									
LOAD MODE	H	H	L	L	L	L	BA	OP code			4, 6
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF REFRESH entry	H	L	L	L	L	H	X	X	X	X	
SELF REFRESH exit	L	H	H	X	X	X	X	X	X	X	4, 7
			L	H	H	H					
Single bank PRECHARGE	H	H	L	L	H	L	BA	X	L	X	6
All banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank ACTIVATE	H	H	L	L	H	H	BA	Row address			4
WRITE	H	H	L	H	L	L	BA	Column address	L	Column address	4, 5, 6, 8
WRITE with auto precharge	H	H	L	H	L	L	BA	Column address	H	Column address	4, 5, 6, 8
READ	H	H	L	H	L	H	BA	Column address	L	Column address	4, 5, 6, 8
READ with auto precharge	H	H	L	H	L	H	BA	Column address	H	Column address	4, 5, 6, 8
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
Power-down entry	H	L	H	X	X	X	X	X	X	X	9
			L	H	H	H					
Power-down exit	L	H	H	X	X	X	X	X	X	X	9
			L	H	H	H					

Notes:
1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See ODT Timing (page 134) for details.
3. "X" means "H or L" (but a defined logic level) for valid I_{DD} measurements.
4. BA2 is only applicable for densities ≥1Gb.
5. An *n* is the most significant address bit for a given density and configuration. Some larger address bits may be "Don't Care" during column addressing, depending on density and configuration.

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6. Bank addresses (BA) determine which bank is to be operated upon. BA during a LOAD MODE command selects which mode register is programmed.
7. SELF REFRESH exit is asynchronous.
8. Burst reads or writes at BL = 4 cannot be terminated or interrupted. See Figure 49 (page 101) and Figure 61 (page 113) for other restrictions and details.
9. The power-down mode does not perform any REFRESH operations. The duration of power-down is limited by the refresh requirements outlined in the AC parametric section.

Table 38: Truth Table – Current State Bank *n* – Command to Bank *n*

Notes: 1–6 apply to the entire table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVATE (select and activate row)	
	L	L	L	H	REFRESH	7
	L	L	L	L	LOAD MODE	7
Row active	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst)	8
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	9
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst)	8, 10
	L	L	H	L	PRECHARGE (start PRECHARGE)	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start new WRITE burst)	8
	L	L	H	L	PRECHARGE (start PRECHARGE)	9

Notes:
1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, ^{t}RP has been met, and any READ burst is complete.

   Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated.

   Write: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.
4. The following states must not be interrupted by a command issued to the same bank. Issue DESELECT or NOP commands, or allowable commands to the other bank, on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table, and according to Table 39 (page 77).

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Precharge:	Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. After ^{t}RP is met, the bank will be in the idle state.
Read with auto precharge enabled:	Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.
Row activate:	Starts with registration of an ACTIVATE command and ends when ^{t}RCD is met. After ^{t}RCD is met, the bank will be in the row active state.
Write with auto precharge enabled:	Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command (DESELECT or NOP commands must be applied on each positive clock edge during these states):

Refresh:	Starts with registration of a REFRESH command and ends when ^{t}RFC is met. After ^{t}RFC is met, the DDR2 SDRAM will be in the all banks idle state.
Accessing mode register:	Starts with registration of the LOAD MODE command and ends when ^{t}MRD has been met. After ^{t}MRD is met, the DDR2 SDRAM will be in the all banks idle state.
Precharge all:	Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and bursts are not in progress.
8. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
9. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
10. A WRITE command may be applied after the completion of the READ burst.

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Table 39: Truth Table – Current State Bank *n* – Command to Bank *m*

Notes: 1–6 apply to the entire table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank *m*	
Row active, active, or precharge	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 9, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVATE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	

Notes:
1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table describes an alternate bank operation, except where noted (the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

Idle:	The bank has been precharged, ^{t}RP has been met, and any READ burst is complete.
Row active:	A row in the bank has been activated and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated with auto precharge disabled and has not yet terminated.
Write:	A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.

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READ with auto precharge enabled/ WRITE with auto precharge enabled: The READ with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For READ with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For WRITE with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled, any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (contention between read data and write data must be avoided).

The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized in Table 40 (page 78).

4. REFRESH and LOAD MODE commands may only be issued when all banks are idle.
5. Not used.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. A WRITE command may be applied after the completion of the READ burst.
9. Requires appropriate DM.
10. The number of clock cycles required to meet ^{t}WTR is either two or ^{t}WTR/^{t}CK, whichever is greater.

Table 40: Minimum Delay with Auto Precharge Enabled

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (with Concurrent Auto Precharge)	Units
WRITE with auto precharge	READ or READ with auto precharge	(CL - 1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2)	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK
READ with auto precharge	READ or READ with auto precharge	(BL/2)	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2) + 2	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected. DESELECT is also referred to as COMMAND INHIBIT.

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NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE (LM)

The mode registers are loaded via bank address and address inputs. The bank address balls determine which mode register will be programmed. See Mode Register (MR) (page 81). The LM command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the bank address inputs determines the bank, and the address inputs select the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the bank address inputs determine the bank, and the address provided on address inputs A0–A*i* (where A*i* is the most significant column address bit for a given configuration) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the bank select inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given configuration) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location (see Figure 66 (page 118)).

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PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

REFRESH

REFRESH is used during normal operation of the DDR2 SDRAM and is analogous to CAS#-before-RAS# (CBR) REFRESH. All banks must be in the idle mode prior to issuing a REFRESH command. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during a REFRESH command.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including Vref) must be maintained at valid levels upon entry/exit *and* during SELF REFRESH operation.

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh.

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Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 36 (page 82). Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables must be programmed when the command is issued.

The MR is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVATE command. Violating either of these requirements will result in an unspecified operation.

Burst Length

Burst length is defined by bits M0–M2, as shown in Figure 36. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when BL = 4 and by A3–A*i* when BL = 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

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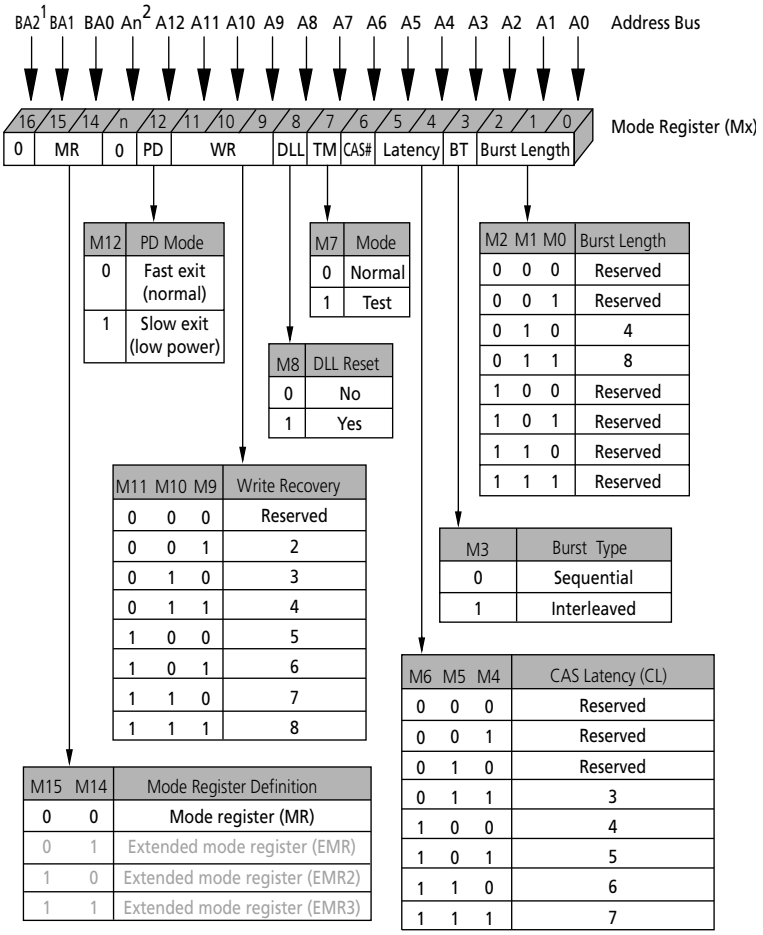
Figure 36: MR Definition



Notes:
1. M16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to "0."
2. Mode bits (M*n*) with corresponding address balls (A*n*) greater than M12 (A12) are reserved for future use and must be programmed to "0."
3. Not all listed WR and CL options are supported in any individual speed grade.

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Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 36. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 41. DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full interleaved address ordering is supported; however, sequential address ordering is nibble-based.

Table 41: Burst Definition

Burst Length	Starting Column Address (A2, A1, A0)	Order of Accesses Within a Burst	
		Burst Type = Sequential	Burst Type = Interleaved
4	0 0 0	0, 1, 2, 3	0, 1, 2, 3
	0 0 1	1, 2, 3, 0	1, 0, 3, 2
	0 1 0	2, 3, 0, 1	2, 3, 0, 1
	0 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Operating Mode

The normal operating mode is selected by issuing a command with bit M7 set to "0," and all other bits set to the desired values, as shown in Figure 36 (page 82). When bit M7 is "1," no other bits of the mode register are programmed. Programming bit M7 to "1" places the DDR2 SDRAM into a test mode that is only used by the manufacturer and should *not* be used. No operation or functionality is guaranteed if M7 bit is "1."

DLL RESET

DLL RESET is defined by bit M8, as shown in Figure 36. Programming bit M8 to "1" will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of "0" after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Write Recovery

Write recovery (WR) time is defined by bits M9–M11, as shown in Figure 36 (page 82). The WR register is used by the DDR2 SDRAM during WRITE with auto precharge operation. During WRITE with auto precharge operation, the DDR2 SDRAM delays the inter-

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nal auto precharge operation by WR clocks (programmed in bits M9–M11) from the last data burst. An example of WRITE with auto precharge is shown in Figure 65 (page 117).

WR values of 2, 3, 4, 5, 6, 7, or 8 clocks may be used for programming bits M9–M11. The user is required to program the value of WR, which is calculated by dividing ^{t}WR (in nanoseconds) by ^{t}CK (in nanoseconds) and rounding up a noninteger value to the next integer; WR (cycles) = ^{t}WR (ns)/^{t}CK (ns). Reserved states should not be used as an unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12, as shown in Figure 36. PD mode enables the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to precharge PD mode.

When bit M12 = 0, standard active PD mode, or "fast-exit" active PD mode, is enabled. The ^{t}XARD parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower-power active PD mode, or "slow-exit" active PD mode, is enabled. The ^{t}XARDS parameter is used for slow-exit active PD exit timing. The DLL can be enabled but "frozen" during active PD mode because the exit-to-READ command timing is relaxed. The power difference expected between I_{DD3P} normal and I_{DD3P} low-power mode is defined in the DDR2 I_{DD} Specifications and Conditions table.

CAS Latency (CL)

The CAS latency (CL) is defined by bits M4–M6, as shown in Figure 36 (page 82). CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, 5, 6, or 7 clocks, depending on the speed grade option being used.

DDR2 SDRAM does not support any half-clock latencies. Reserved states should not be used as an unknown operation otherwise incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD (MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks. The AL feature is described in further detail in Posted CAS Additive Latency (AL) (page 88).

Examples of CL = 3 and CL = 4 are shown in Figure 37; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CL is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m* (this assumes AL = 0).

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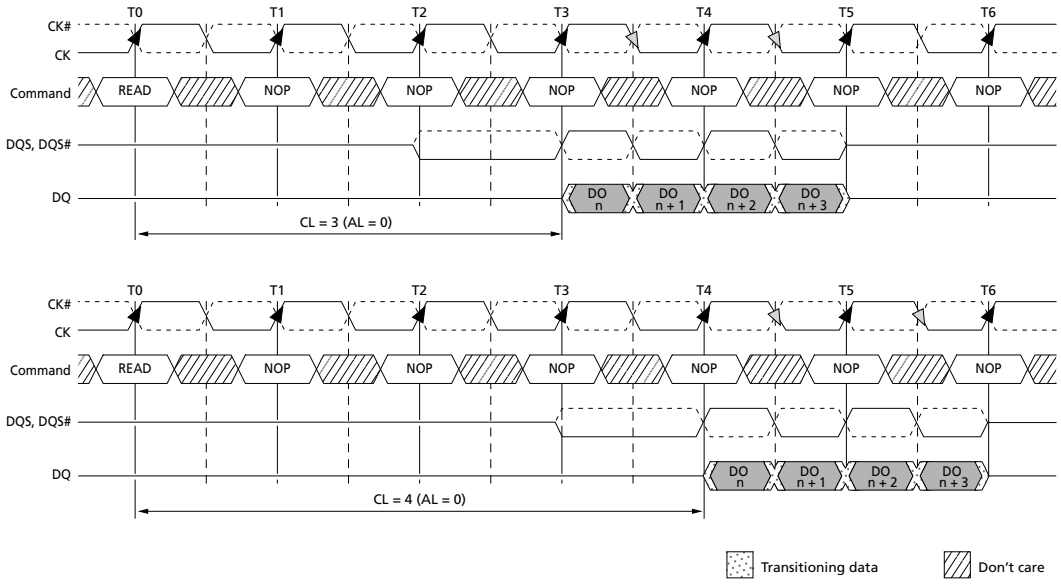
Figure 37: CL



Notes:
1. BL = 4.
2. Posted CAS# additive latency (AL) = 0.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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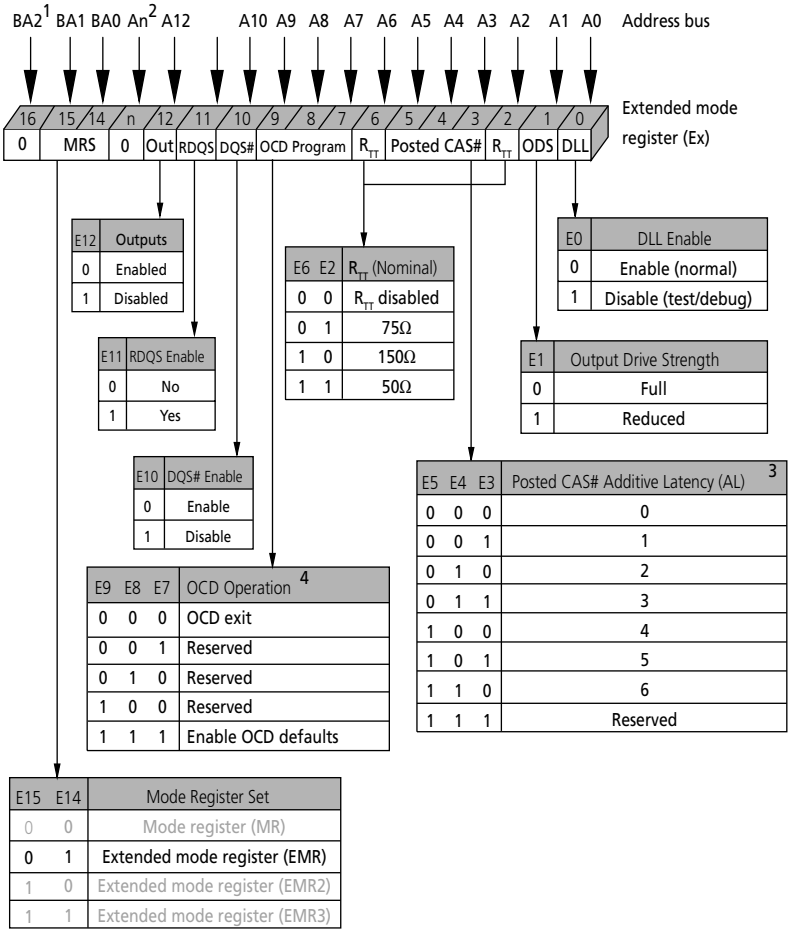
Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on-die termination (ODT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 38. The EMR is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 38: EMR Definition



Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to 0.
2. Mode bits (E*n*) with corresponding address balls (A*n*) greater than E12 (A12) are reserved for future use and must be programmed to 0.
3. Not all listed AL options are supported in any individual speed grade.

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4. As detailed in the Initialization section notes, during initialization of the OCD operation, all three bits must be set to 1 for the OCD default state, then set to 0 before initialization is finished.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LM command, as shown in Figure 38 (page 86). These specifications are applicable when the DLL is enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the LM command.

The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation.

Anytime the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Anytime the DLL is disabled and the device is operated below 25 MHz, any AUTO REFRESH command should be followed by a PRECHARGE ALL command.

Output Drive Strength

The output drive strength is defined by bit E1, as shown in Figure 38. The normal drive strength for all outputs is specified to be SSTL_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 45 to 60 percent of the SSTL_18 drive strength. This option is intended for the support of lighter load and/or point-to-point environments.

DQS# Enable/Disable

The DQS# ball is enabled by bit E10. When E10 = 0, DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (E10 = 1), DQS is used in a single-ended mode and the DQS# ball is disabled. When disabled, DQS# should be left floating; however, it may be tied to ground via a 20Ω to 10kΩ resistor. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

RDQS Enable/Disable

The RDQS ball is enabled by bit E11, as shown in Figure 38. This feature is only applicable to the x8 configuration. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM.

Output Enable/Disable

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 38. When enabled (E12 = 0), all outputs (DQ, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all outputs (DQ, DQS, DQS#, RDQS, RDQS#) are disabled, thus re-

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moving output buffer current. The output disable feature is intended to be used during I_{DD} characterization of read current.

On-Die Termination (ODT)

ODT effective resistance, $R_{TT(EFF)}$, is defined by bits E2 and E6 of the EMR, as shown in Figure 38 (page 86). The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. R_{TT} effective resistance values of 50Ω, 75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signal. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off sw1, sw2, or sw3. The ODT effective resistance value is selected by enabling switch sw1, which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω ($R_{TT2\ [EFF]}$ = R2/2). Similarly, if sw2 is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω ($R_{TT2[EFF]}$ = R2/2). Switch sw3 enables R1 values of 100Ω, enabling effective resistance of 50Ω. Reserved states should not be used, as an unknown operation or incompatibility with future versions may result.

The ODT control ball is used to determine when $R_{TT(EFF)}$ is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation.

ODT must be turned off prior to entering self refresh mode. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until the EMR command is issued. This will enable the ODT feature, at which point the ODT ball will determine the $R_{TT(EFF)}$ value. Anytime the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled (see Figure 81 (page 135) for ODT timing diagrams).

Off-Chip Driver (OCD) Impedance Calibration

The OFF-CHIP DRIVER function is an optional DDR2 JEDEC feature not supported by Micron and thereby must be set to the default state. Enabling OCD beyond the default settings will alter the I/O drive characteristics and the timing and output I/O specifications will no longer be valid (see Initialization section for proper setting of OCD defaults).

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL, as shown in Figure 38. Bits E3–E5 allow the user to program the DDR2 SDRAM with an AL of 0, 1, 2, 3, 4, 5, or 6 clocks. Reserved states should not be used as an unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD (MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 × ^{t}CK. The READ or WRITE command is held for the time of the AL before it is issued internally to the DDR2 SDRAM device. RL is controlled by the sum of AL and CL; RL = AL + CL. WRITE latency (WL) is equal to RL minus one clock; WL = AL + CL - 1 × ^{t}CK. An example of RL is shown in Figure 39 (page 89). An example of a WL is shown in Figure 40 (page 89).

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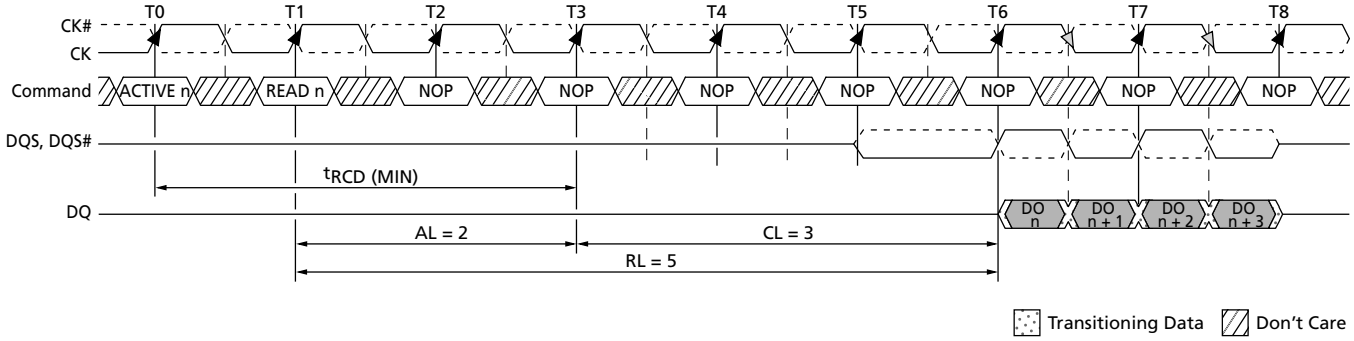
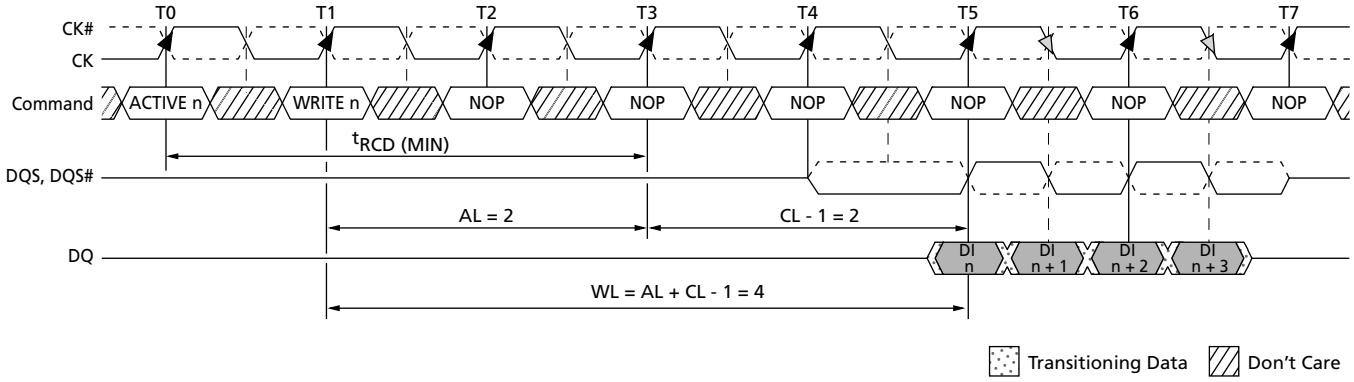
Figure 39: READ Latency



Notes:
1. BL = 4.
2. Shown with nominal tAC, tDQSCK, and tDQSQ.
3. RL = AL + CL = 5.

Figure 40: WRITE Latency



Notes:
1. BL = 4.
2. CL = 3.
3. WL = AL + CL - 1 = 4.

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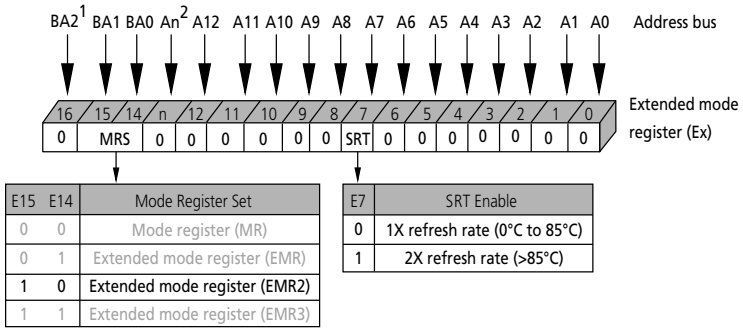
Extended Mode Register 2 (EMR2)

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved, except for E7, which is used in commercial or high-temperature operations, as shown in Figure 41. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

Bit E7 (A7) must be programmed as 1 to provide a faster refresh rate on IT and AT devices if T_C exceeds 85°C.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 41: EMR2 Definition



Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, reserved for future use, and must be programmed to 0.
2. Mode bits (E*n*) with corresponding address balls (A*n*) greater than E12 (A12) are reserved for future use and must be programmed to 0.

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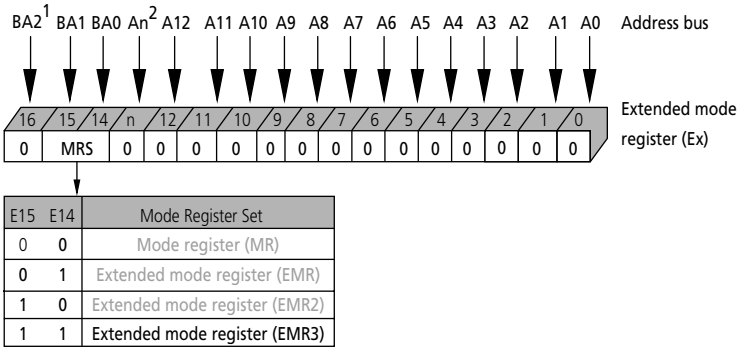
Extended Mode Register 3 (EMR3)

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently all bits in EMR3 are reserved, as shown in Figure 42. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

Figure 42: EMR3 Definition



E15	E14	Mode Register Set
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

Notes:
1. E16 (BA2) is only applicable for densities ≥1Gb, is reserved for future use, and must be programmed to 0.
2. Mode bits (E*n*) with corresponding address balls (A*n*) greater than E12 (A12) are reserved for future use and must be programmed to 0.

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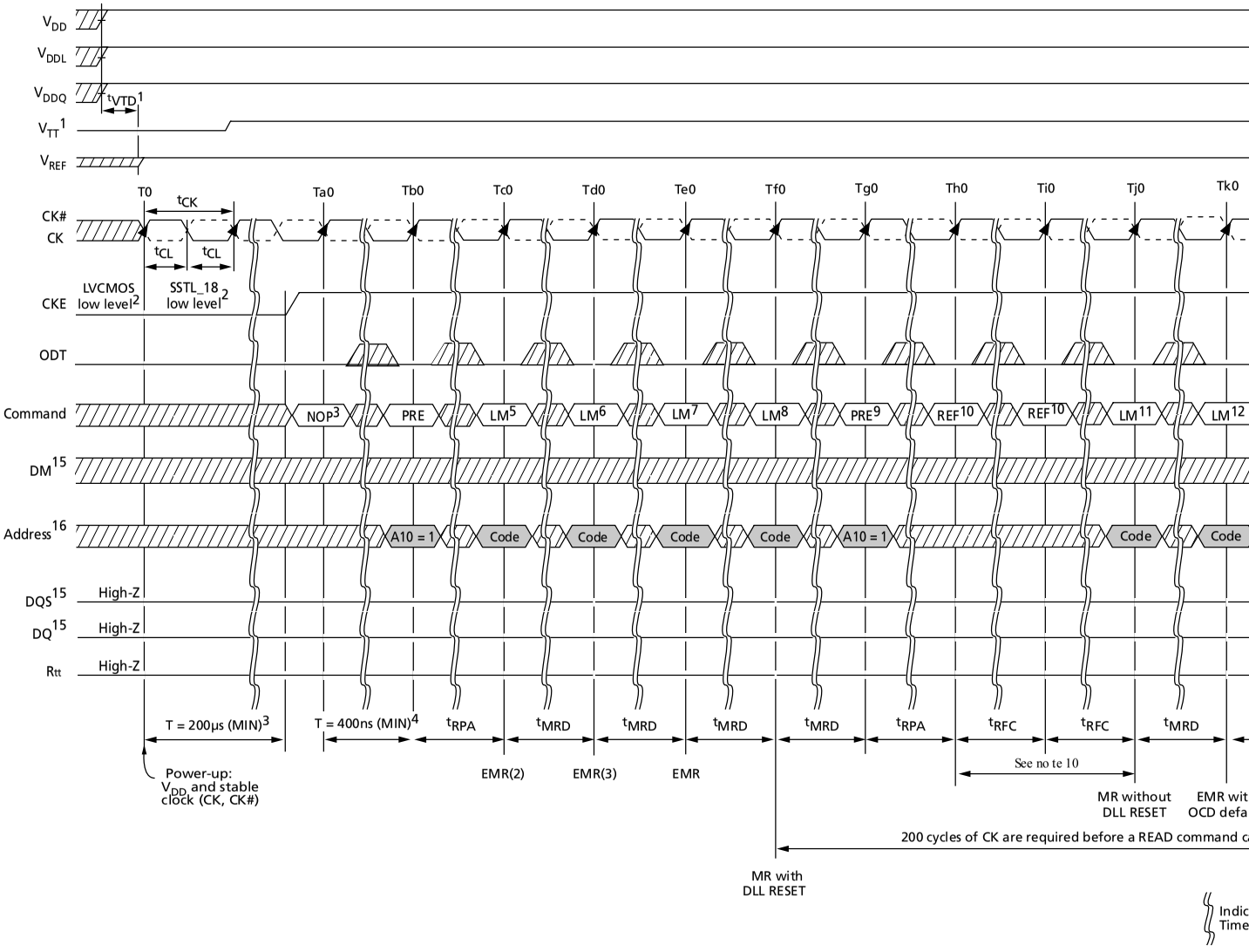
Initialization

Figure 43: DDR2 Power-Up and Initialization

DDR2 SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified m
fined operation. Figure 43 illustrates, and the notes outline, the sequence required for power-up and initialization.



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Notes:

1. Applying power; if CKE is maintained below 0.2 × V_{DDQ}, outputs remain disabled. To guarantee R_{TT} (ODT resistance) is off, V_{REF} must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined; I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DDR2 SDRAM device latch-up). V_{TT} is not applied directly to the device; however, ^{t}VTD should be ≥0 to avoid device latch-up. At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as V_{DD}, V_{DDL}, V_{DDQ}, V_{REF}, and V_{TT} are between their minimum and maximum values as stated in Table 13 (page 46)):

   A. Single power source: The V_{DD} voltage ramp from 300mV to $V_{DD,min}$ must take no longer than 200ms; during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3V$. Once supply voltage ramping is complete (when V_{DDQ} crosses $V_{DD,min}$), Table 13 specifications apply.

   - V_{DD}, V_{DDL}, and V_{DDQ} are driven from a single power converter output
   - V_{TT} is limited to 0.95V MAX
   - V_{REF} tracks $V_{DDQ}/2$; V_{REF} must be within ±0.3V with respect to $V_{DDQ}/2$ during supply ramp time; does not need to be satisfied when ramping power down
   - $V_{DDQ} \geq V_{REF}$ at all times

   B. Multiple power sources: $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (V_{DDQ} crosses $V_{DD,min}$). Once supply voltage ramping is complete, Table 13 specifications apply.

   - Apply V_{DD} and V_{DDL} before or at the same time as V_{DDQ}; V_{DD}/V_{DDL} voltage ramp time must be ≤ 200ms from when V_{DD} ramps from 300mV to $V_{DD,min}$
   - Apply V_{DDQ} before or at the same time as V_{TT}; the V_{DDQ} voltage ramp time from when $V_{DD,min}$ is achieved to when $V_{DDQ,min}$ is achieved must be ≤ 500ms; while V_{DD} is ramping, current can be supplied from V_{DD} through the device to V_{DDQ}
   - V_{REF} must track $V_{DDQ}/2$; V_{REF} must be within ±0.3V with respect to $V_{DDQ}/2$ during supply ramp time; $V_{DDQ} \geq V_{REF}$ must be met at all times; does not need to be satisfied when ramping power down
   - Apply V_{TT}; the V_{TT} voltage ramp time from when $V_{DDQ,min}$ is achieved to when $V_{TT,min}$ is achieved must be no greater than 500ms
2. CKE requires LVCMOS input levels prior to state T0 to ensure DQs are High-Z during device power-up prior to V_{REF} being stable. After state T0, CKE is required to have SSTL_18 input levels. Once CKE transitions to a high level, it must stay HIGH for the duration of the initialization sequence.
3. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH.
4. Wait a minimum of 400ns then issue a PRECHARGE ALL command.
5. Issue a LOAD MODE command to the EMR(2). To issue an EMR(2) command, provide LOW to BA0, and provide HIGH to BA1; set register E7 to "0" or "1" to select appropriate self refresh rate; remaining EMR(2) bits must be "0" (see Extended Mode Register 2 (EMR2) (page 90) for all EMR(2) requirements).
6. Issue a LOAD MODE command to the EMR(3). To issue an EMR(3) command, provide HIGH to BA0 and BA1; remaining EMR(3) bits must be "0." Extended Mode Register 3 (EMR3) for all EMR(3) requirements.
7. Issue a LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0; provide HIGH to BA0; bits E7, E8, and E9 can be set to "0" or "1;" Micron recommends setting them to "0;" remaining EMR bits must be "0." Extended Mode Register (EMR) (page 86) for all EMR requirements.
8. Issue a LOAD MODE command to the MR for DLL RESET. 200 cycles of clock input is required to lock the DLL. To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1 and BA0; CKE must be HIGH the entire time the DLL is resetting; remaining MR bits must be "0." Mode Register (MR) (page 81) for all MR requirements.

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9. Issue PRECHARGE ALL command.
10. Issue two or more REFRESH commands.
11. Issue a LOAD MODE command to the MR with LOW to A8 to initialize device operation (that is, to program operating parameters without resetting the DLL). To access the MR, set BA0 and BA1 LOW; remaining MR bits must be set to desired settings. Mode Register (MR) (page 81) for all MR requirements.
12. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters. To access the EMR, set BA0 HIGH and BA1 LOW (see Extended Mode Register (EMR) (page 86) for all EMR requirements.
13. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters. To access the extended mode registers, EMR, set BA0 HIGH and BA1 LOW for all EMR requirements.
14. The DDR2 SDRAM is now initialized and ready for normal operation 200 clock cycles after the DLL RESET at Tf0.
15. DM represents DM for the x4, x8 configurations and UDM, LDM for the x16 configuration; DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS# for the appropriate configuration (x4, x8, x16); DQ represents DQ[3:0] for x4, DQ[7:0] for x8 and DQ[15:0] for x16.
16. A10 = PRECHARGE ALL, CODE = desired values for mode registers (bank addresses are required to be decoded).

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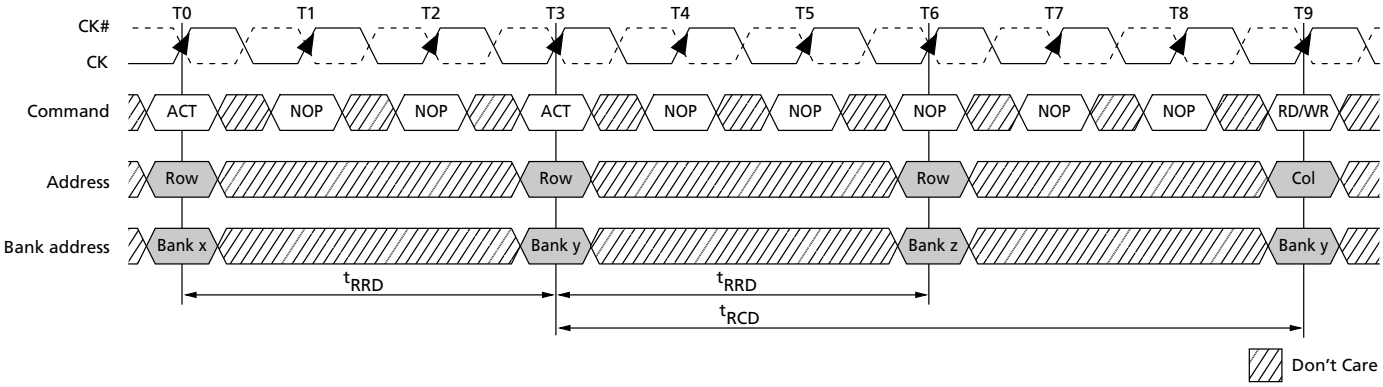
ACTIVATE

Before any READ or WRITE commands can be issued to a bank within the DDR2 SDRAM, a row in that bank must be opened (activated), even when additive latency is used. This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a ^{t}RCD (MIN) specification of 20ns with a 266 MHz clock (^{t}CK = 3.75ns) results in 5.3 clocks, rounded up to 6. This is shown in Figure 44, which covers any case where $5 < {}^{t}\text{RCD (MIN)} / {}^{t}\text{CK} \leq 6$. Figure 44 also shows the case for ^{t}RRD where $2 < {}^{t}\text{RRD (MIN)} / {}^{t}\text{CK} \leq 3$.

Figure 44: Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN)



A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by ^{t}RRD.

DDR2 devices with 8 banks (1Gb or larger) have an additional requirement: ^{t}FAW. This requires no more than four ACTIVATE commands may be issued in any given ^{t}FAW (MIN) period, as shown in Figure 45 (page 96).

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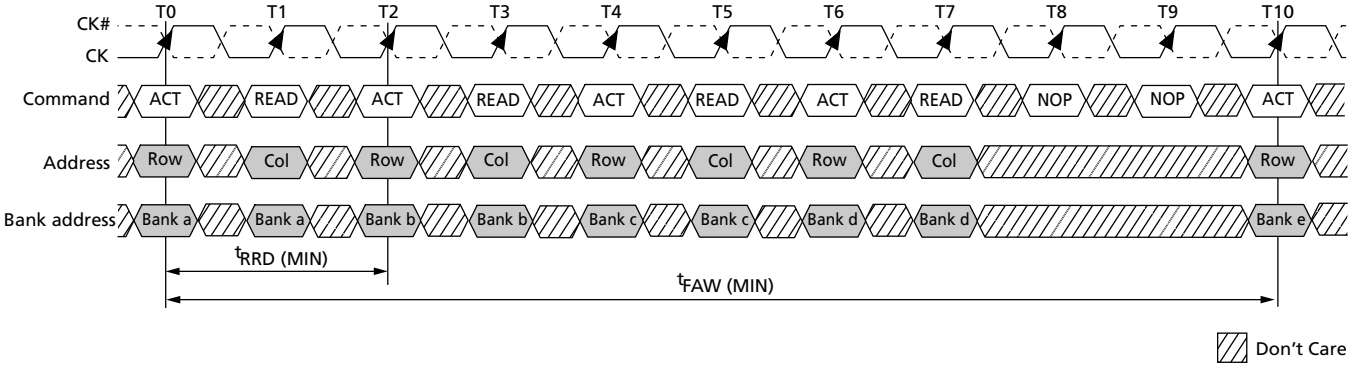
Figure 45: Multibank Activate Restriction



Note: 1. DDR2-533 (-37E, x4 or x8), ^{t}CK = 3.75ns, BL = 4, AL = 3, CL = 4, ^{t}RRD (MIN) = 7.5ns, ^{t}FAW (MIN) = 37.5ns.

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READ

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL: RL = AL + CL. The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (at the next crossing of CK and CK#). Figure 46 (page 98) shows examples of RL based on different AL and CL settings.

DQS/DQS# is driven by the DDR2 SDRAM along with output data. The initial LOW state on DQS and the HIGH state on DQS# are known as the read preamble (^{t}RPRE). The LOW state on DQS and the HIGH state on DQS# coincident with the last data-out element are known as the read postamble (^{t}RPST).

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), and the valid data window are depicted in Figure 55 (page 106) and Figure 56 (page 107). A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is shown in Figure 57 (page 108).

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued *x* cycles after the first READ command, where *x* equals BL/2 cycles (see Figure 47 (page 99)).

Nonconsecutive read data is illustrated in Figure 48 (page 100). Full-speed random read accesses within a page (or pages) can be performed. DDR2 SDRAM supports the use of concurrent auto precharge timing (see Table 42 (page 103)).

DDR2 SDRAM does not allow interrupting or truncating of any READ burst using BL = 4 operations. Once the BL = 4 READ command is registered, it must be allowed to complete the entire READ burst. However, a READ (with auto precharge disabled) using BL = 8 operation may be interrupted and truncated *only* by another READ burst as long as the interruption occurs on a 4-bit boundary due to the 4*n* prefetch architecture of DDR2 SDRAM. As shown in Figure 49 (page 101), READ burst BL = 8 operations may not be interrupted or truncated with any other command except another READ command.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst is shown in Figure 50 (page 101). The ^{t}DQSS (NOM) case is shown (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in Figure 58 (page 110)).

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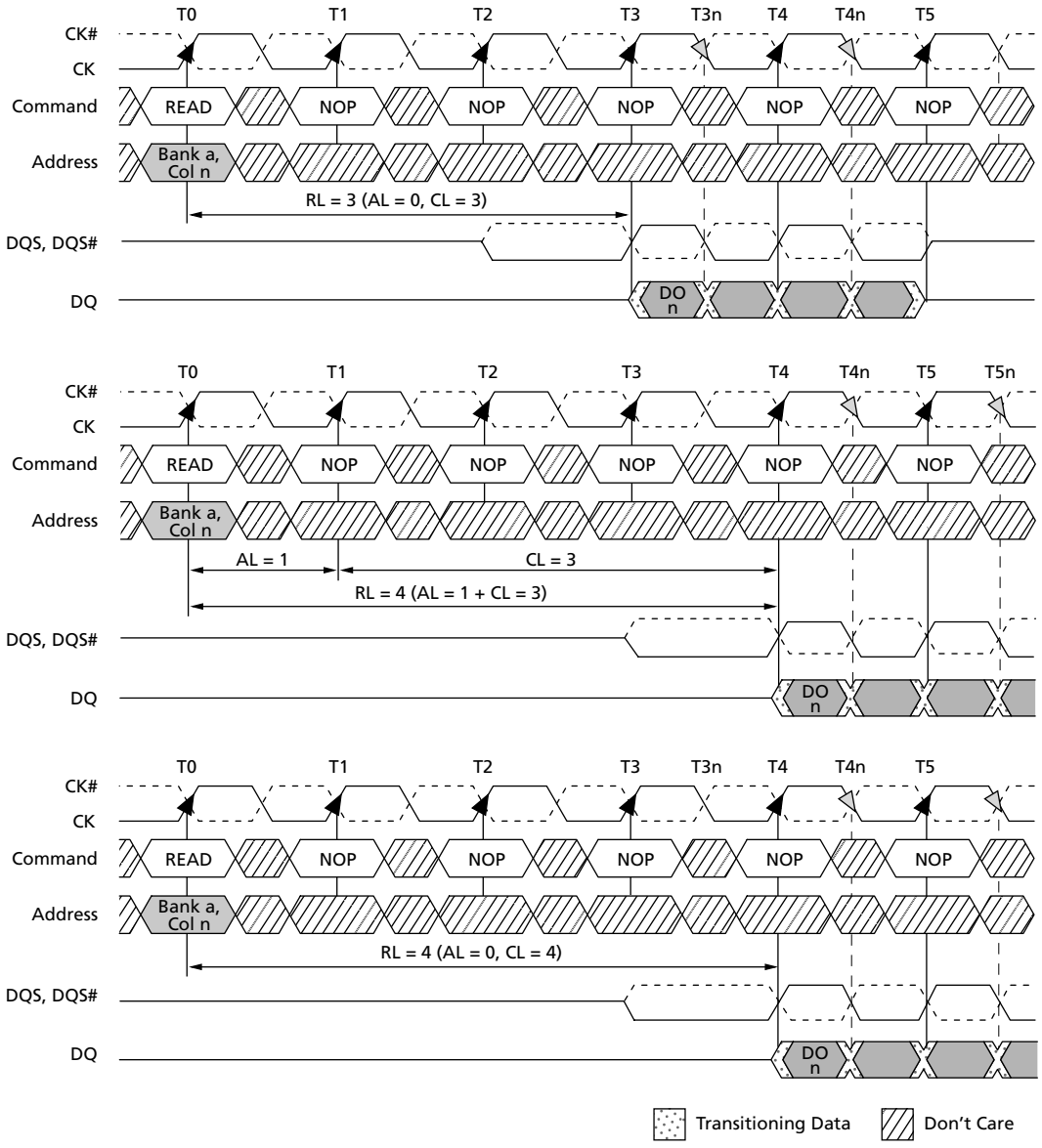
Figure 46: READ Latency



Notes:
1. DO *n* = data-out from column *n*.
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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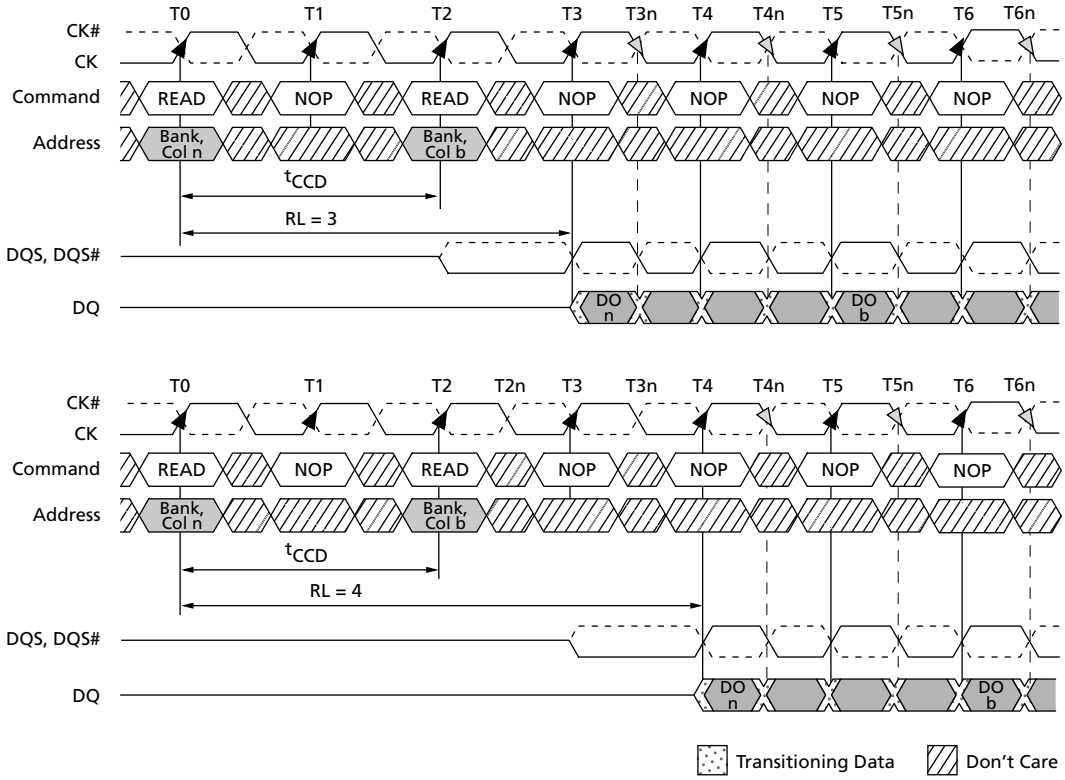
Figure 47: Consecutive READ Bursts



Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to same device.

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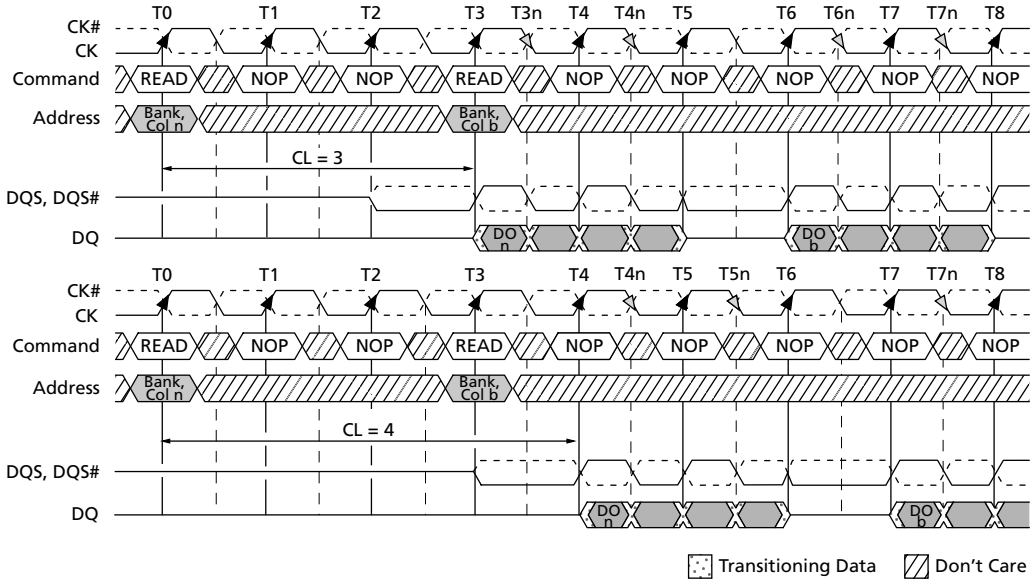
Figure 48: Nonconsecutive READ Bursts



Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.

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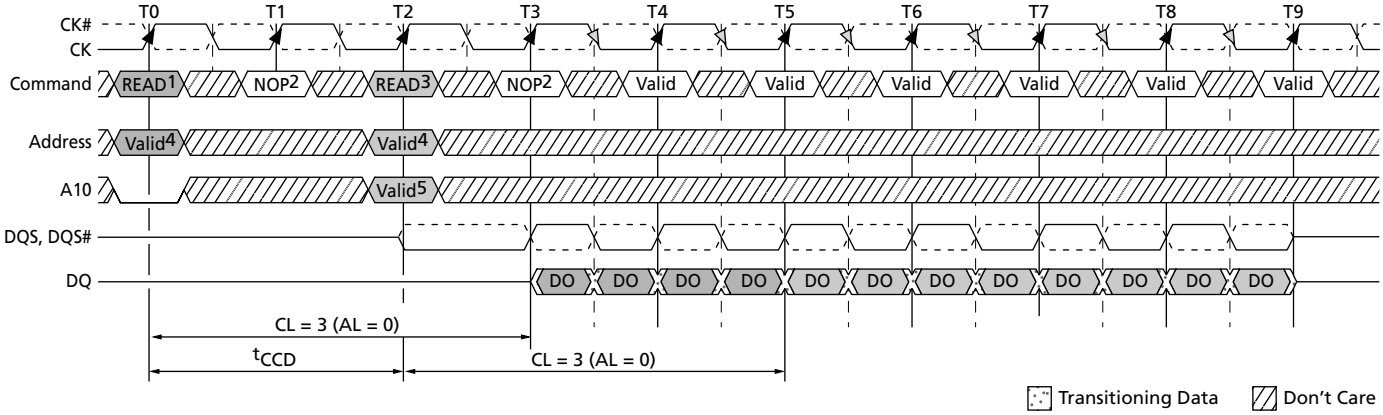
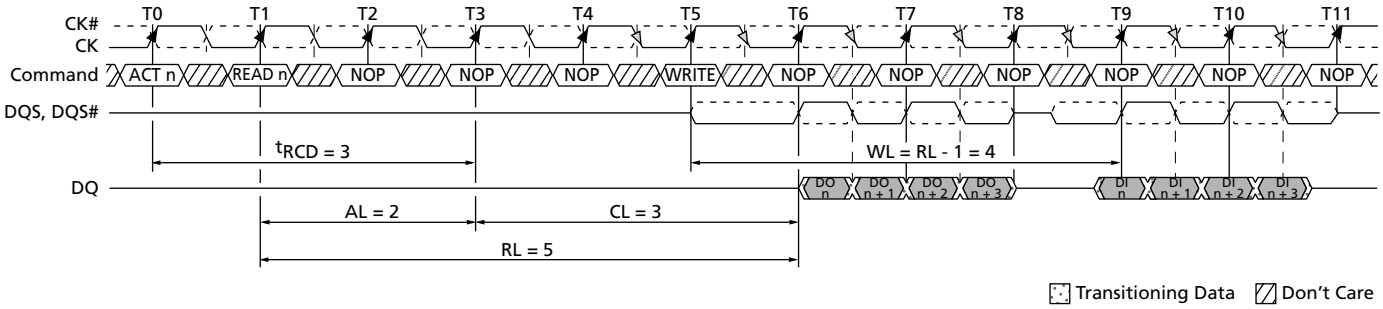
Figure 49: READ Interrupted by READ



Notes:
1. BL = 8 required; auto precharge must be disabled (A10 = LOW).
2. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for READs at T0 and T2.
3. Interrupting READ command must be issued exactly 2 × ^{t}CK from previous READ.
4. READ command can be issued to any valid bank and row address (READ command at T0 and T2 can be either same bank or different bank).
5. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting READ command.
6. Example shown uses AL = 0; CL = 3, BL = 8, shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 50: READ-to-WRITE



Notes:
1. BL = 4; CL = 3; AL = 2.
2. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

READ with Precharge

A READ burst may be followed by a PRECHARGE command to the same bank, provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank has two requirements that must be satisfied: AL + BL/2 clocks and ^{t}RTP. ^{t}RTP is the minimum time from the rising clock edge that initiates the last 4-bit prefetch of a READ command to the PRECHARGE command. For BL = 4, this is the time from the actual READ (AL after the READ command) to PRECHARGE command. For BL = 8, this is the time from AL + 2 × CK after the READ-to-PRECHARGE command. Follow-

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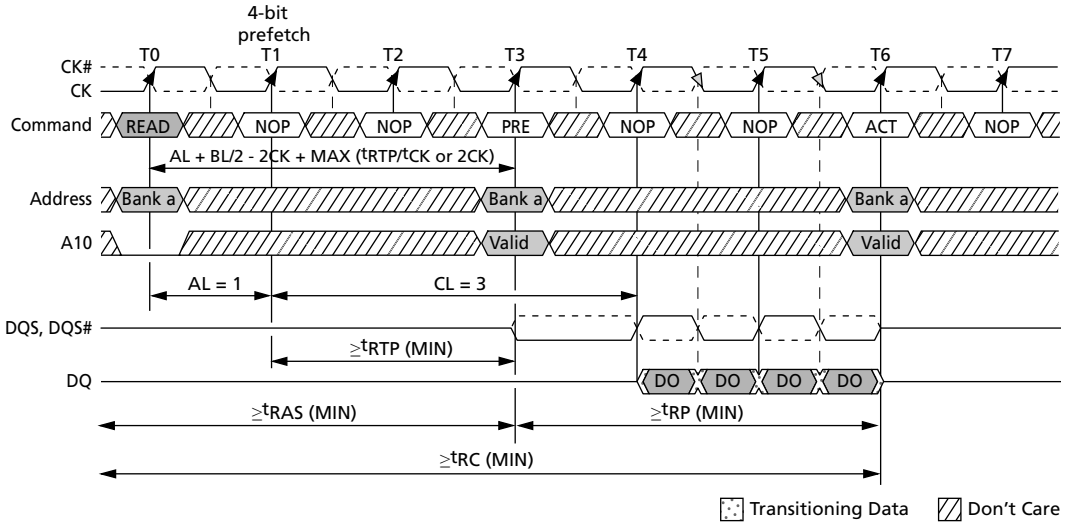
ing the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. However, part of the row precharge time is hidden during the access of the last data elements.

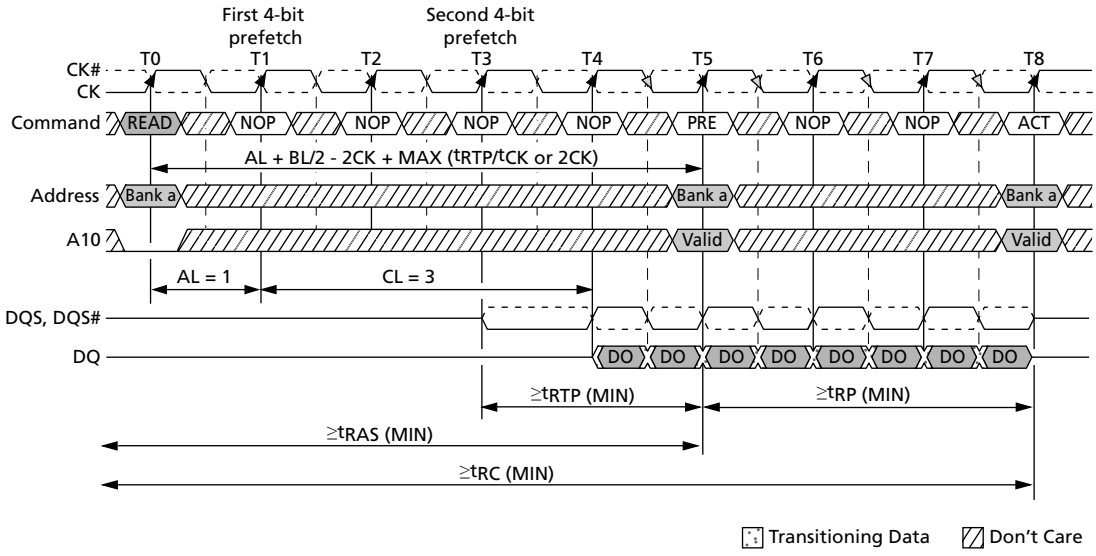
Examples of READ-to-PRECHARGE for BL = 4 are shown in Figure 51 and in Figure 52 for BL = 8. The delay from READ-to-PRECHARGE period to the same bank is AL + BL/2 - 2CK + MAX (^{t}RTP/^{t}CK or 2 × CK) where MAX means the larger of the two.

Figure 51: READ-to-PRECHARGE – BL = 4



Notes: 1. RL = 4 (AL = 1, CL = 3); BL = 4.
2. ^{t}RTP ≥ 2 clocks.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 52: READ-to-PRECHARGE – BL = 8



Notes: 1. RL = 4 (AL = 1, CL = 3); BL = 8.
2. ^{t}RTP ≥ 2 clocks.

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3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

READ with Auto Precharge

If A10 is high when a READ command is issued, the READ with auto precharge function is engaged. The DDR2 SDRAM starts an auto precharge operation on the rising clock edge that is AL + (BL/2) cycles later than the read with auto precharge command provided ^{t}RAS (MIN) and ^{t}RTP are satisfied. If ^{t}RAS (MIN) is not satisfied at this rising clock edge, the start point of the auto precharge operation will be delayed until ^{t}RAS (MIN) is satisfied. If ^{t}RTP (MIN) is not satisfied at this rising clock edge, the start point of the auto precharge operation will be delayed until ^{t}RTP (MIN) is satisfied. When the internal precharge is pushed out by ^{t}RTP, ^{t}RP starts at the point where the internal precharge happens (not at the next rising clock edge after this event).

When BL = 4, the minimum time from READ with auto precharge to the next ACTIVATE command is AL + (^{t}RTP + ^{t}RP)/^{t}CK. When BL = 8, the minimum time from READ with auto precharge to the next ACTIVATE command is AL + 2 clocks + (^{t}RTP + ^{t}RP)/^{t}CK. The term (^{t}RTP + ^{t}RP)/^{t}CK is always rounded up to the next integer. A general purpose equation can also be used: AL + BL/2 - 2CK + (^{t}RTP + ^{t}RP)/^{t}CK. In any event, the internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

READ with auto precharge command may be applied to one bank while another bank is operational. This is referred to as concurrent auto precharge operation, as noted in Table 42. Examples of READ with precharge and READ with auto precharge with applicable timing requirements are shown in Figure 53 (page 104) and Figure 54 (page 105), respectively.

Table 42: READ Using Concurrent Auto Precharge

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (with Concurrent Auto Precharge)	Units
READ with auto precharge	READ or READ with auto precharge	BL/2	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2) + 2	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK

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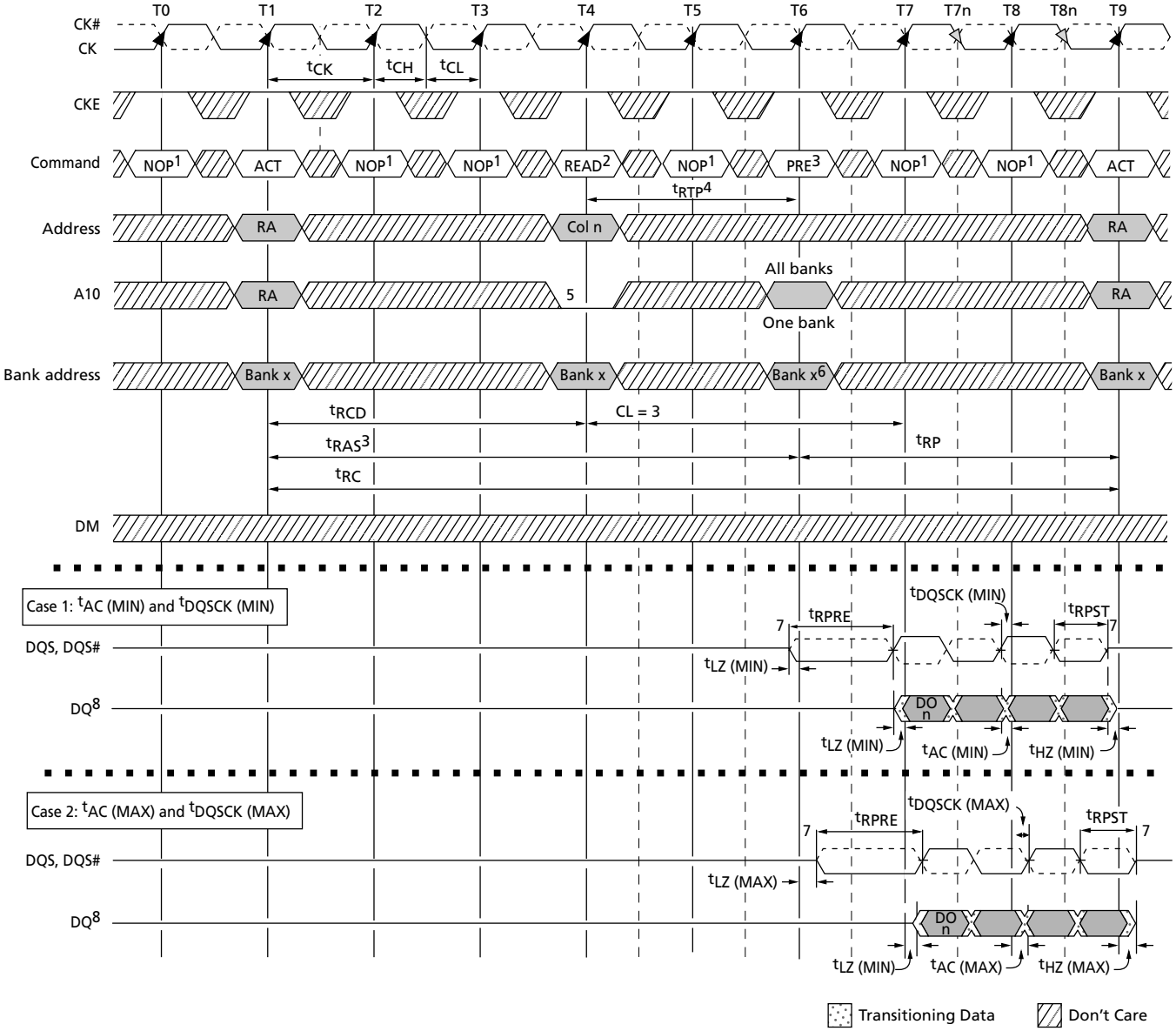
Figure 53: Bank Read – Without Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. The PRECHARGE command can only be applied at T6 if ^{t}RAS (MIN) is met.
4. READ-to-PRECHARGE = AL + BL/2 - 2CK + MAX (^{t}RTP/^{t}CK or 2CK).
5. Disable auto precharge.
6. "Don't Care" if A10 is HIGH at T5.
7. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
8. DO *n* = data-out from column *n*; subsequent elements are applied in the programmed order.

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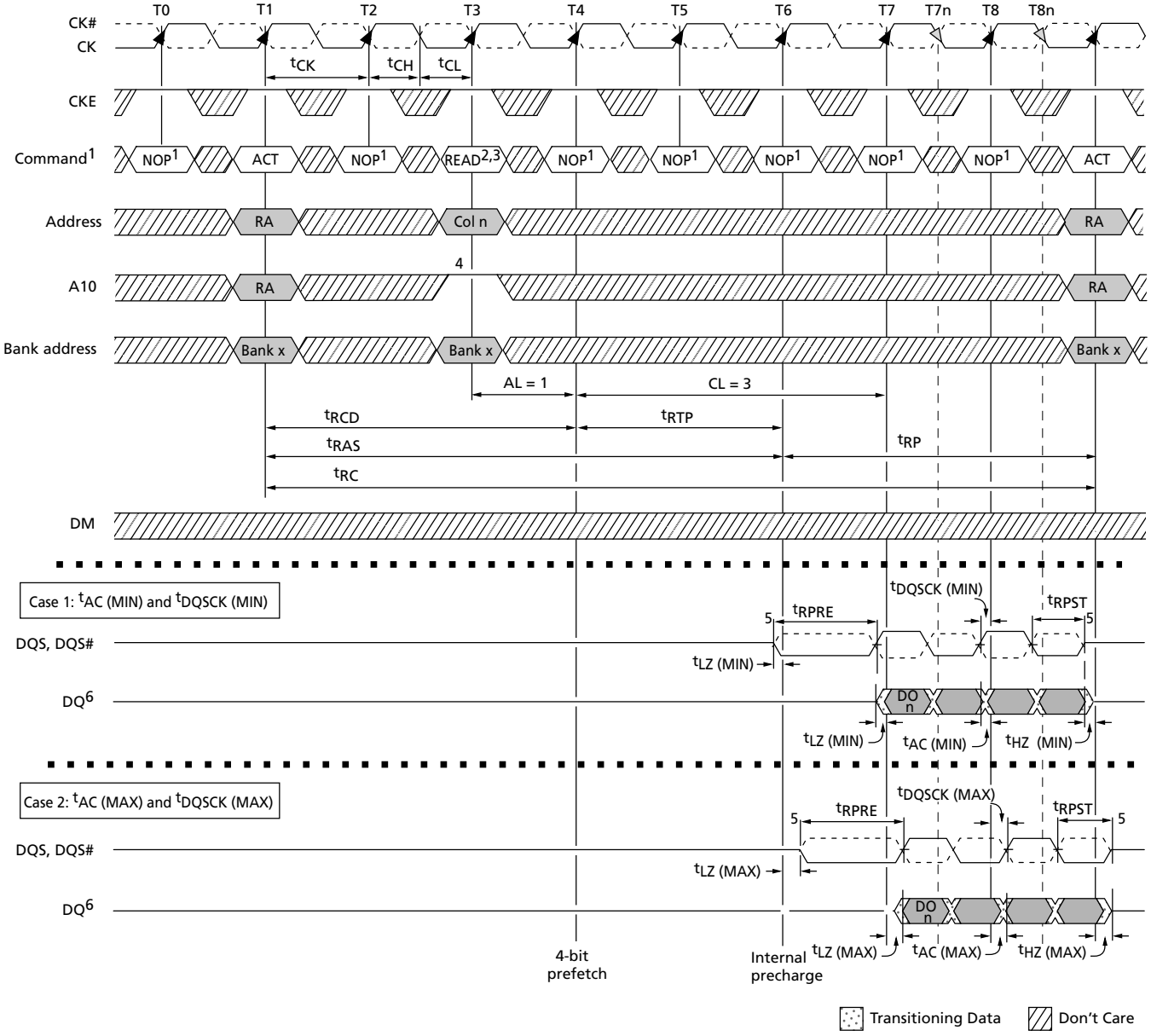
Figure 54: Bank Read – with Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4, RL = 4 (AL = 1, CL = 3) in the case shown.
3. The DDR2 SDRAM internally delays auto precharge until both ^{t}RAS (MIN) and ^{t}RTP (MIN) have been satisfied.
4. Enable auto precharge.
5. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
6. DO *n* = data-out from column *n*; subsequent elements are applied in the programmed order.

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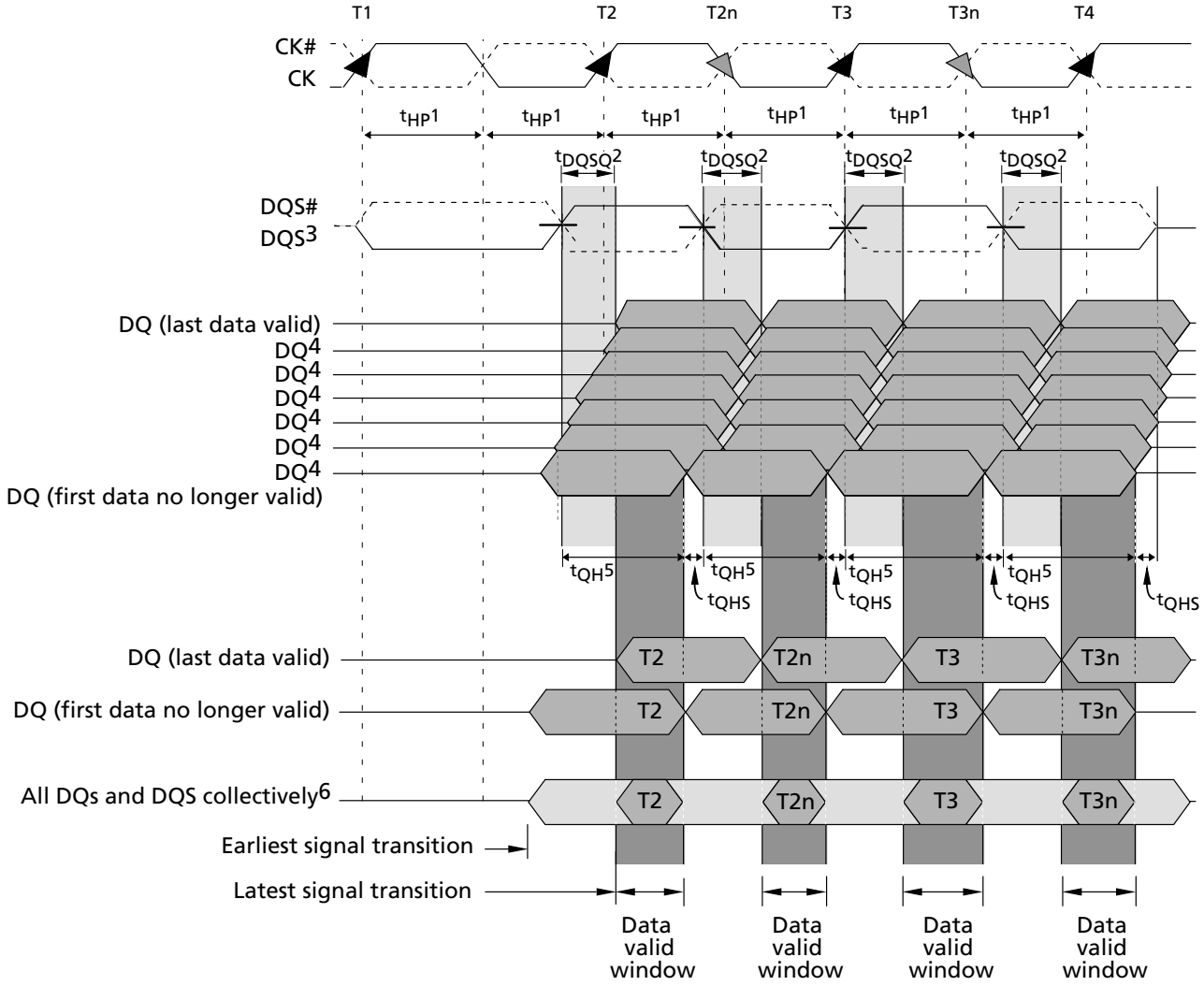
Figure 55: x4, x8 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



Notes:
1. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transitions collectively when a bank is active.
2. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
3. DQ transitioning after the DQS transition defines the ^{t}DQSQ window. DQS transitions at T2 and at T2n are "early DQS," at T3 are "nominal DQS," and at T3n are "late DQS."
4. DQ0, DQ1, DQ2, DQ3 for x4 or DQ[7:0] for x8.
5. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
6. The data valid window is derived for each DQS transition and is defined as ^{t}QH - ^{t}DQSQ.

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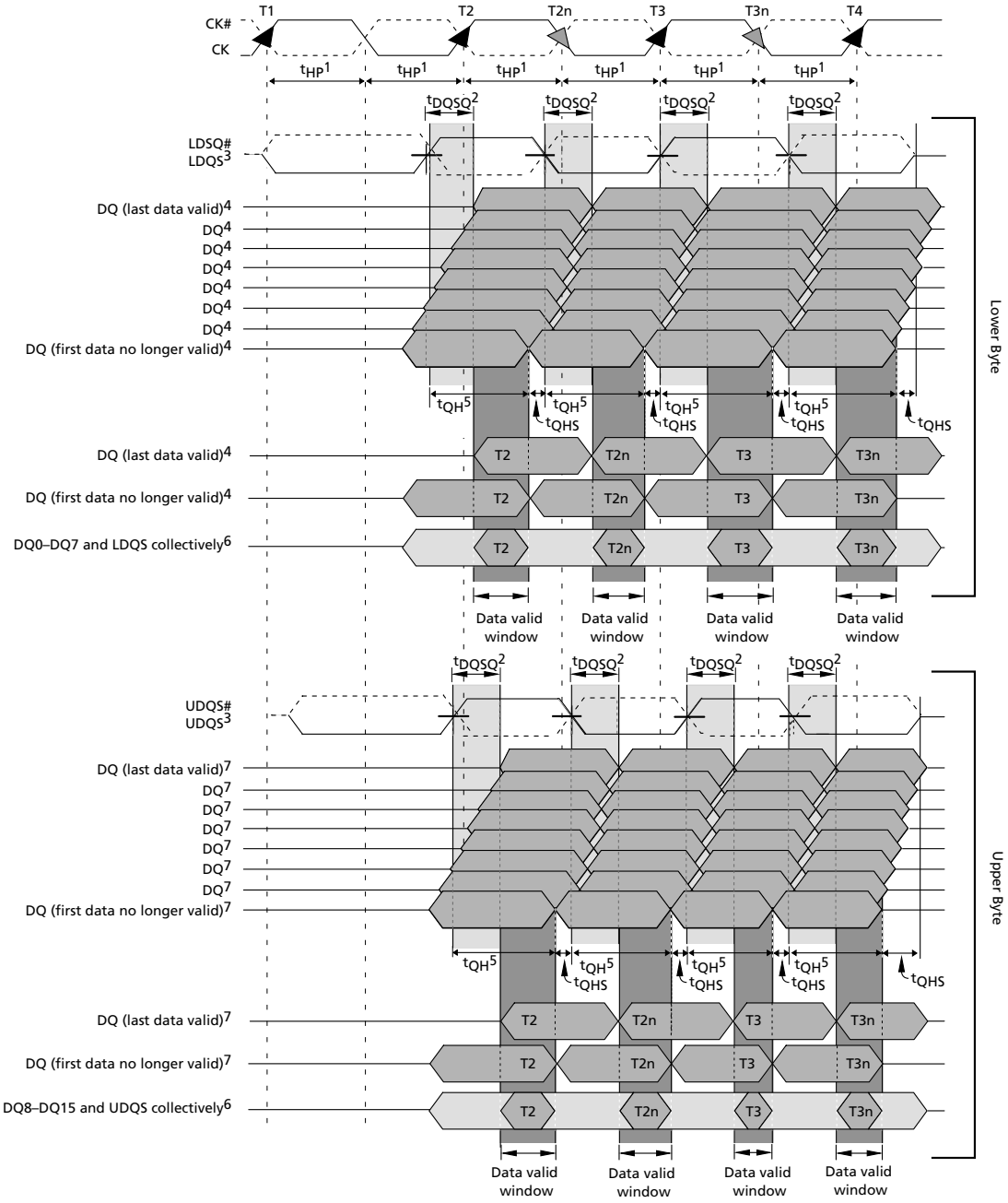
Figure 56: x16 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



Notes:
1. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transitions collectively when a bank is active.
2. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
3. DQ transitioning after the DQS transitions define the ^{t}DQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
4. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
5. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
6. The data valid window is derived for each DQS transition and is ^{t}QH - ^{t}DQSQ.

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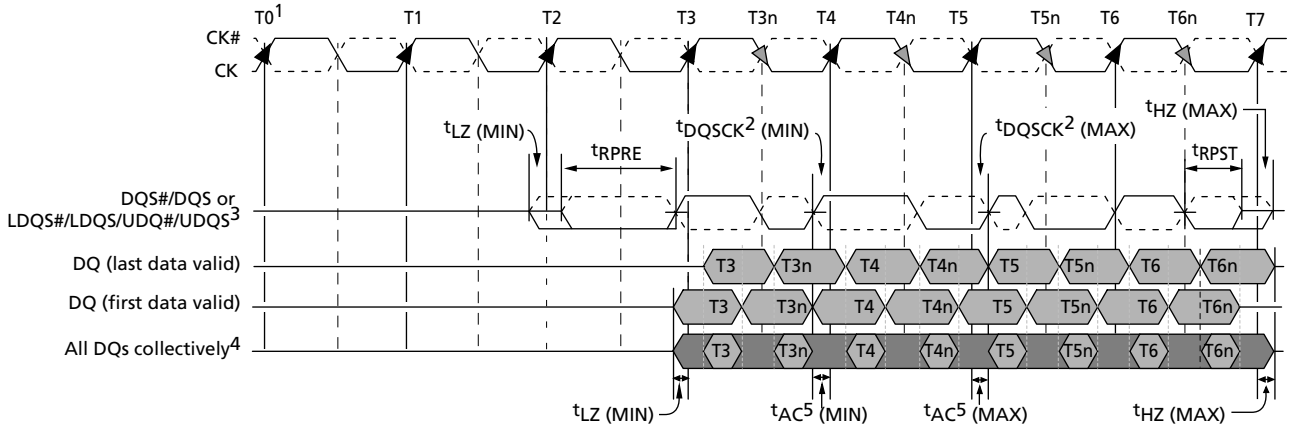
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

Figure 57: Data Output Timing – ^{t}AC and ^{t}DQSCK



Notes:
1. READ command with CL = 3, AL = 0 issued at T0.
2. ^{t}DQSCK is the DQS output window relative to CK and is the long-term component of DQS skew.
3. DQ transitioning after DQS transitions define ^{t}DQSQ window.
4. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
5. ^{t}AC is the DQ output window relative to CK and is the "long term" component of DQ skew.
6. ^{t}LZ (MIN) and ^{t}AC (MIN) are the first valid signal transitions.
7. ^{t}HZ (MAX) and ^{t}AC (MAX) are the latest valid signal transitions.
8. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.

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WRITE

WRITE bursts are initiated with a WRITE command. DDR2 SDRAM uses WL equal to RL minus one clock cycle (WL = RL - 1CK) (see READ (page 79)). The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

Note: For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first rising DQS edge is WL ± ^{t}DQSS. Subsequent DQS positive rising edges are timed, relative to the associated clock edge, as ±^{t}DQSS. ^{t}DQSS is specified with a relatively wide range (25% of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Figure 58 (page 110) shows the nominal case and the extremes of ^{t}DQSS for BL = 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals BL/2.

Figure 59 (page 111) shows concatenated bursts of BL = 4 and how full-speed random write accesses within a page or pages can be performed. An example of nonconsecutive WRITEs is shown in Figure 60 (page 111). DDR2 SDRAM supports concurrent auto precharge options, as shown in Table 43.

DDR2 SDRAM does not allow interrupting or truncating any WRITE burst using BL = 4 operation. Once the BL = 4 WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE BL = 8 operation (with auto precharge disabled) might be interrupted and truncated *only* by another WRITE burst as long as the interruption occurs on a 4-bit boundary due to the 4*n*-prefetch architecture of DDR2 SDRAM. WRITE burst BL = 8 operations may *not* be interrupted or truncated with any command except another WRITE command, as shown in Figure 61 (page 113).

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE, ^{t}WTR should be met, as shown in Figure 62 (page 114). The number of clock cycles required to meet ^{t}WTR is either 2 or ^{t}WTR/^{t}CK, whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command. ^{t}WR must be met, as shown in Figure 63 (page 115). ^{t}WR starts at the end of the data burst, regardless of the data mask condition.

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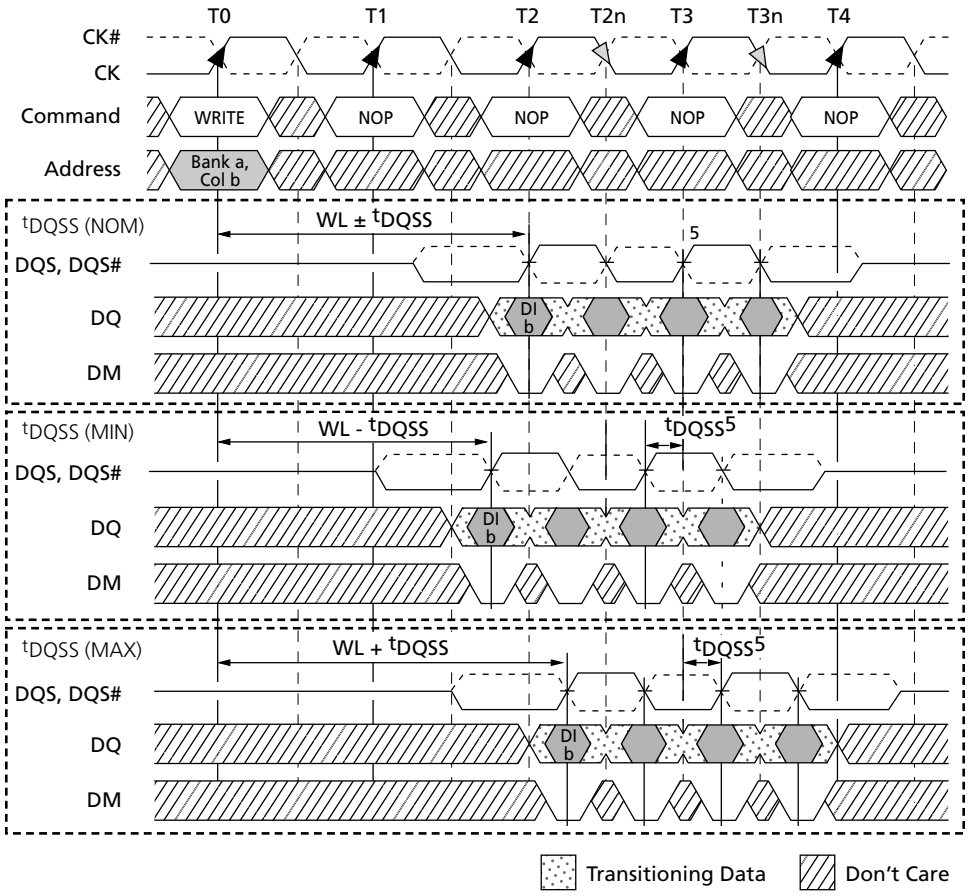
Table 43: WRITE Using Concurrent Auto Precharge

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (with Concurrent Auto Precharge)	Units
WRITE with auto precharge	READ or READ with auto precharge	(CL - 1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE with auto precharge	(BL/2)	^{t}CK
	PRECHARGE or ACTIVATE	1	^{t}CK

Figure 58: Write Burst



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b* = data-in for column *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

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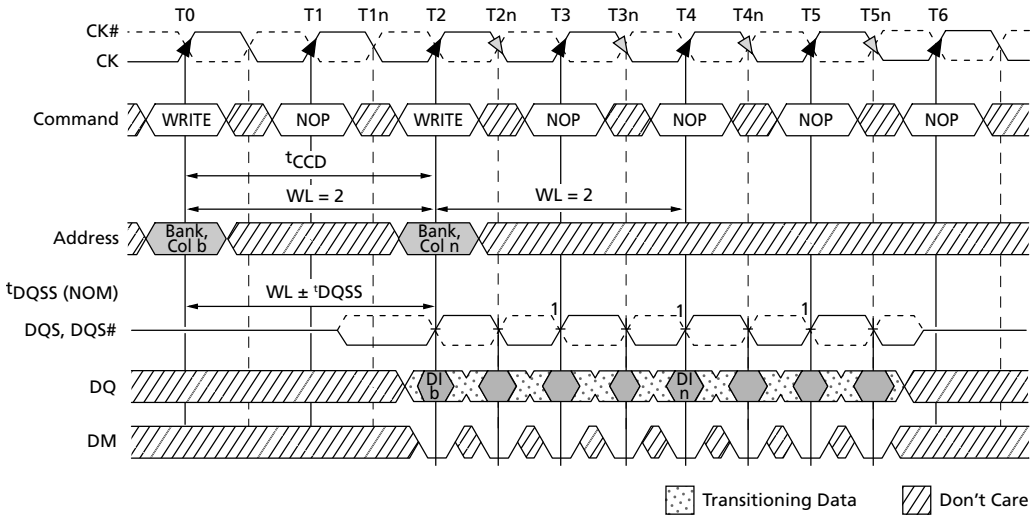
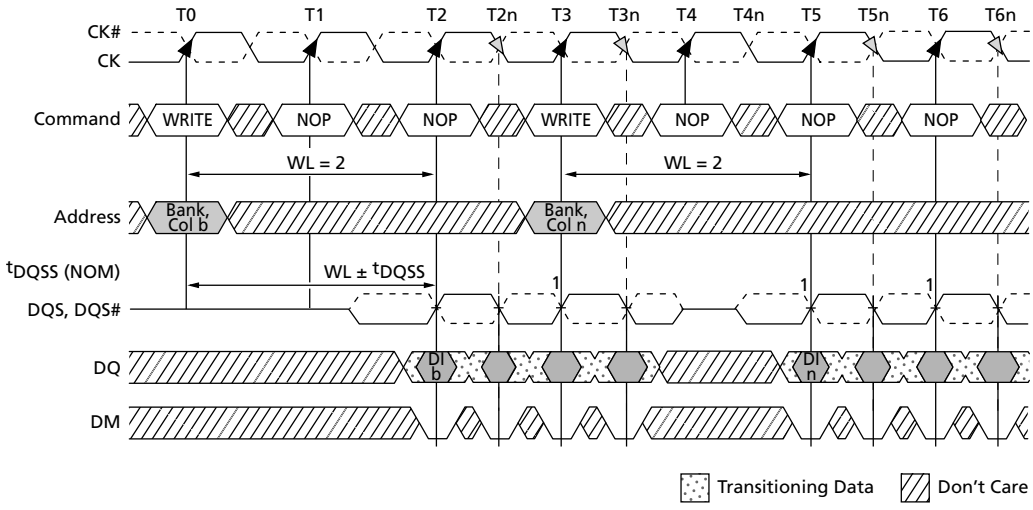
Figure 59: Consecutive WRITE-to-WRITE



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b*, etc. = data-in for column *b*, etc.
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
5. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
6. Each WRITE command may be to any bank.

Figure 60: Nonconsecutive WRITE-to-WRITE



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b* (or *n*), etc. = data-in for column *b* (or column *n*).
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. Three subsequent elements of data-in are applied in the programmed order following DI *n*.

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5. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
6. Each WRITE command may be to any bank.

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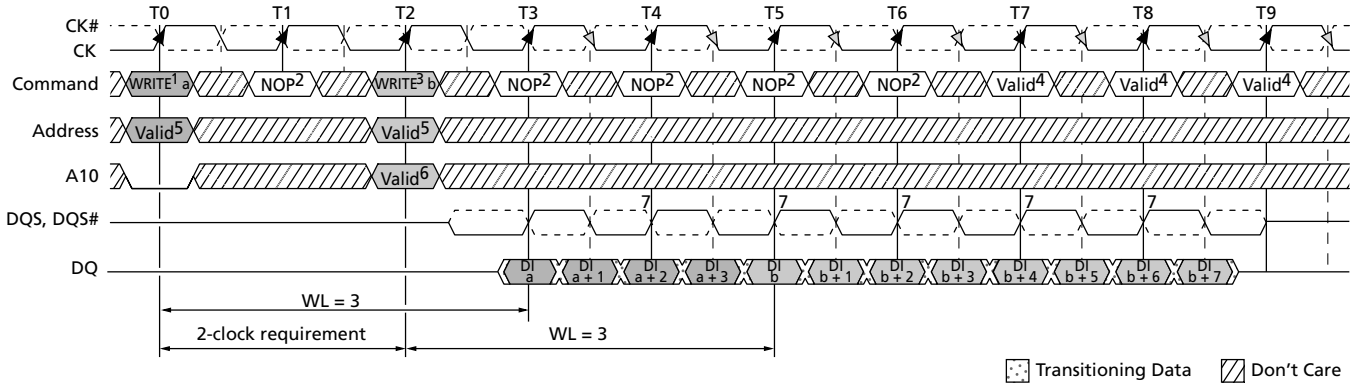
Figure 61: WRITE Interrupted by WRITE



Notes:
1. BL = 8 required and auto precharge must be disabled (A10 = LOW).
2. The NOP or COMMAND INHIBIT commands are valid. The PRECHARGE command cannot be issued to banks used for WRITEs at T0 and T2.
3. The interrupting WRITE command must be issued exactly 2 × ^{t}CK from previous WRITE.
4. The earliest WRITE-to-PRECHARGE timing for WRITE at T0 is WL + BL/2 + ^{t}WR where ^{t}WR starts with T7 and not T5 (because BL = 8 from MR and not the truncated length).
5. The WRITE command can be issued to any valid bank and row address (WRITE command at T0 and T2 can be either same bank or different bank).
6. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting WRITE command.
7. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
8. Example shown uses AL = 0; CL = 4, BL = 8.

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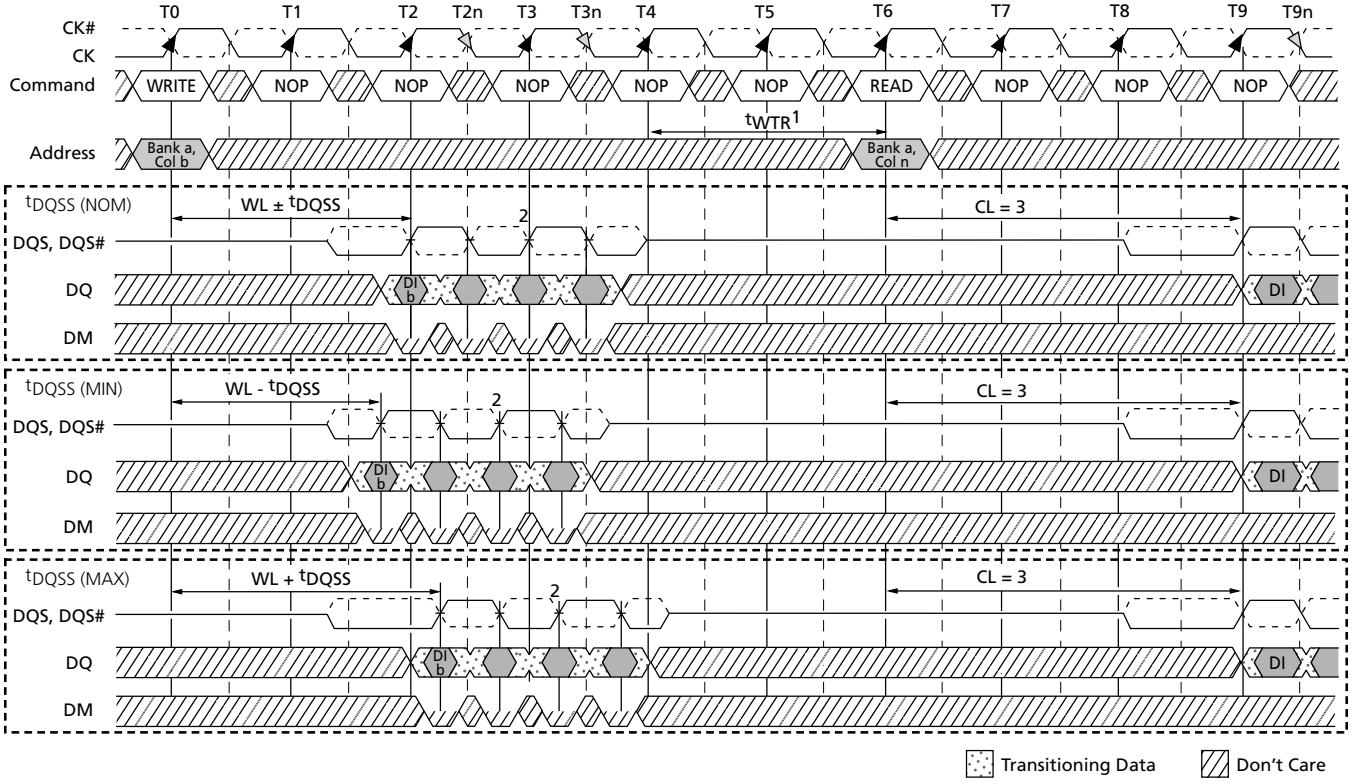
Figure 62: WRITE-to-READ



Notes:
1. tWTR is required for any READ following a WRITE to the same device, but it is not required between module ranks.
2. Subsequent rising DQS signals must align to the clock within tDQSS.
3. DI *b* = data-in for column *b*; DO *n* = data-out from column *n*.
4. BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. One subsequent element of data-in is applied in the programmed order following DI *b*.
6. tWTR is referenced from the first positive CK edge after the last data-in pair.
7. A10 is LOW with the WRITE command (auto precharge is disabled).
8. The number of clock cycles required to meet tWTR is either 2 or tWTR/tCK, whichever is greater.

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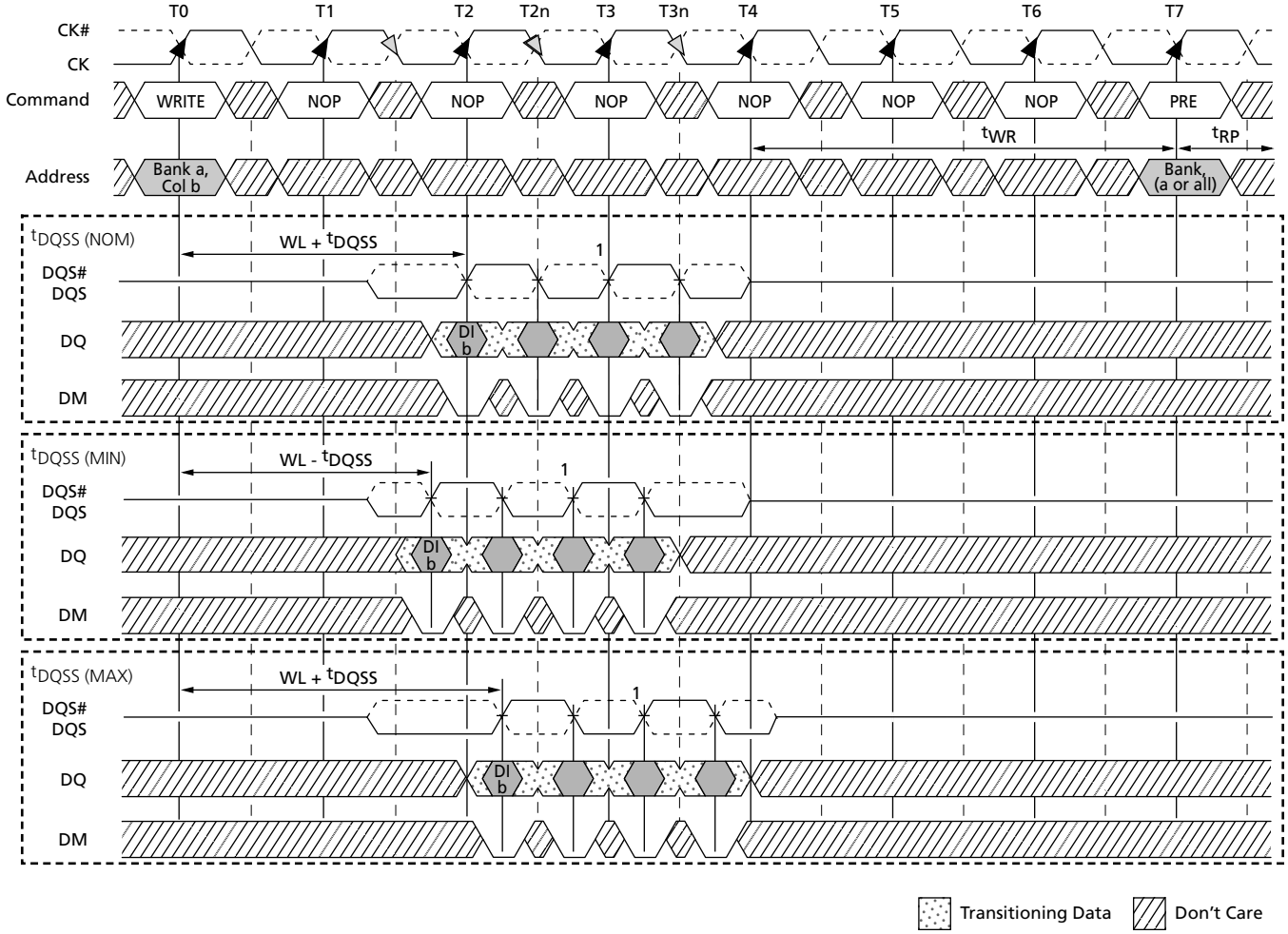
Figure 63: WRITE-to-PRECHARGE



Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI *b* = data-in for column *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
4. BL = 4, CL = 3, AL = 0; thus, WL = 2.
5. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
6. The PRECHARGE and WRITE commands are to the same bank. However, the PRECHARGE and WRITE commands may be to different banks, in which case ^{t}WR is not required and the PRECHARGE command could be applied earlier.
7. A10 is LOW with the WRITE command (auto precharge is disabled).

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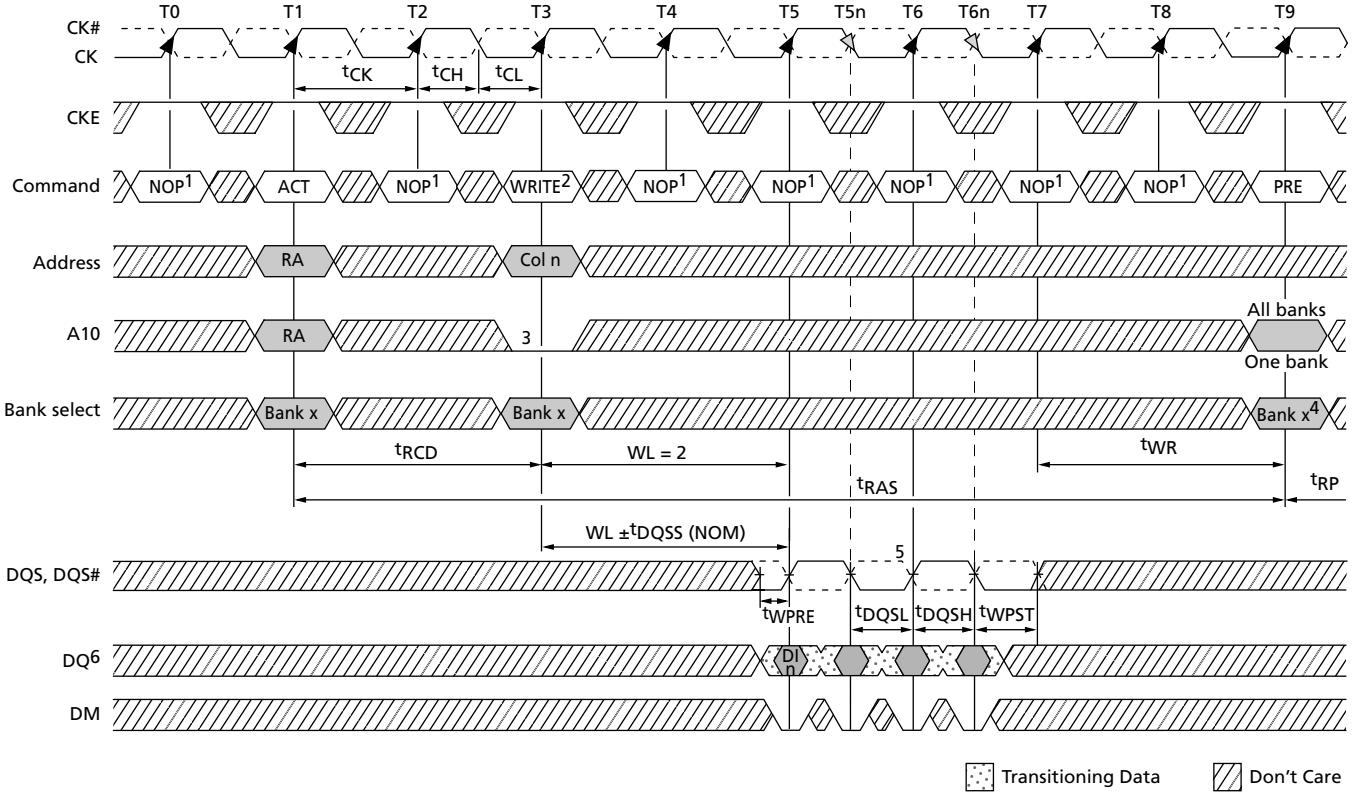
Figure 64: Bank Write – Without Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T9.
5. Subsequent rising DQS signals must align to the clock within tDQSS.
6. DI *n* = data-in for column *n*; subsequent elements are applied in the programmed order.
7. tDSH is applicable during tDQSS (MIN) and is referenced from CK T5 or T6.
8. tDSS is applicable during tDQSS (MAX) and is referenced from CK T6 or T7.

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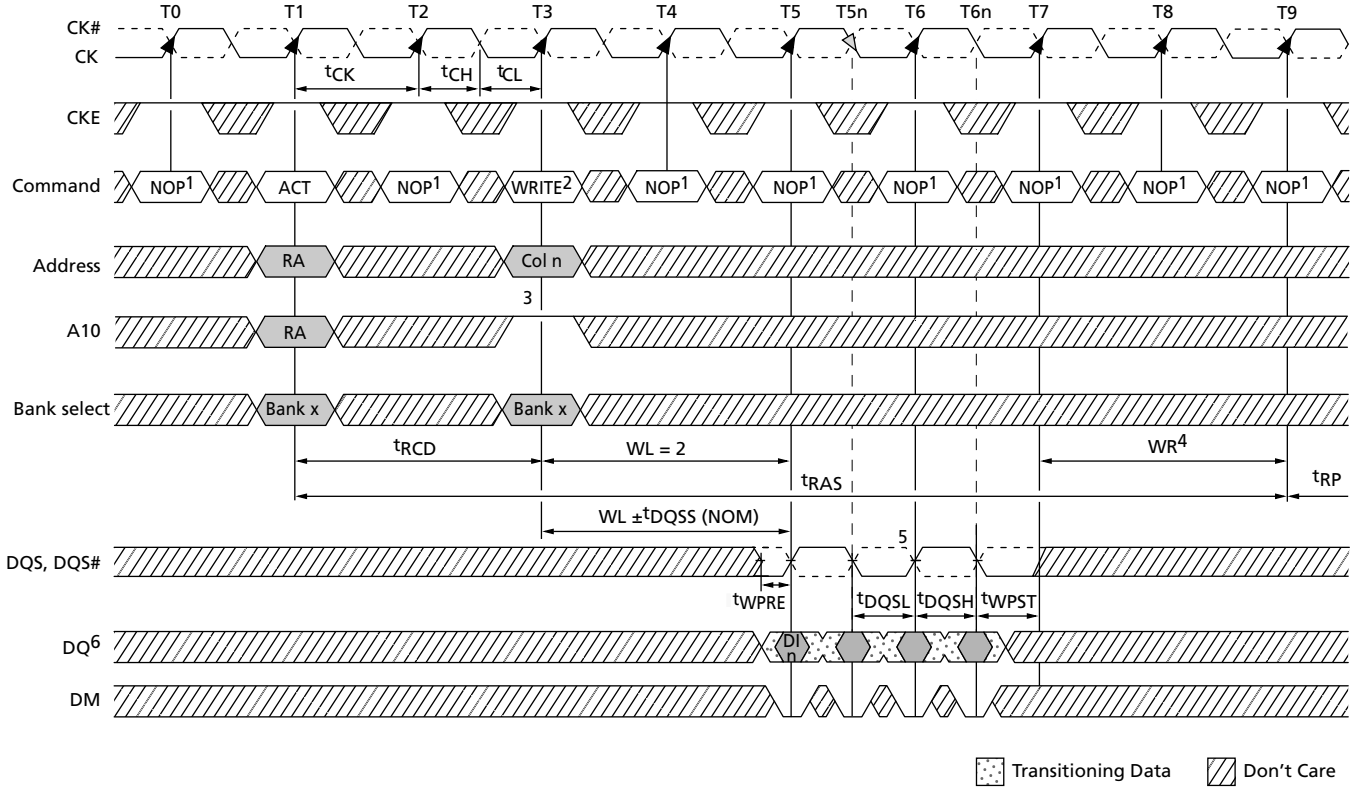
Figure 65: Bank Write – with Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. Enable auto precharge.
4. WR is programmed via MR9–MR11 and is calculated by dividing ^{t}WR (in ns) by ^{t}CK and rounding up to the next integer value.
5. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
6. DI *n* = data-in from column *n*; subsequent elements are applied in the programmed order.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.

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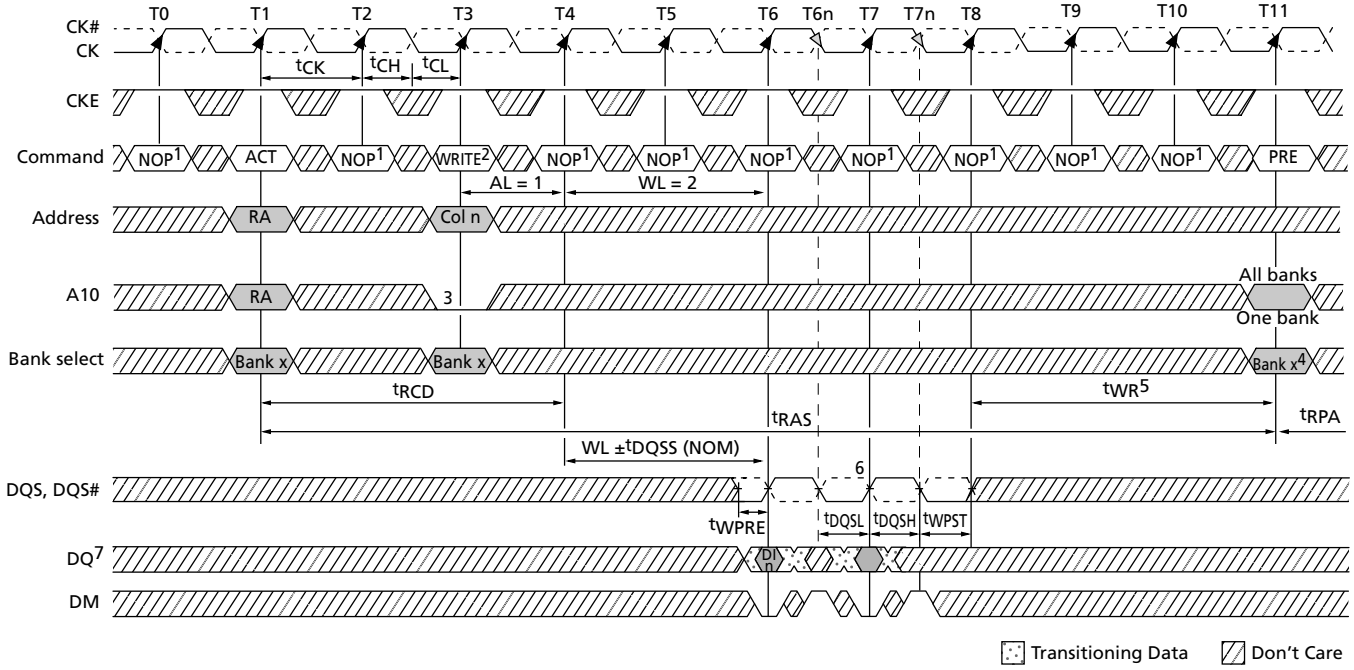
Figure 66: WRITE – DM Operation



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4, AL = 1, and WL = 2 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T11.
5. ^{t}WR starts at the end of the data burst regardless of the data mask condition.
6. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
7. DI *n* = data-in for column *n*; subsequent elements are applied in the programmed order.
8. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T6 or T7.
9. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T7 or T8.

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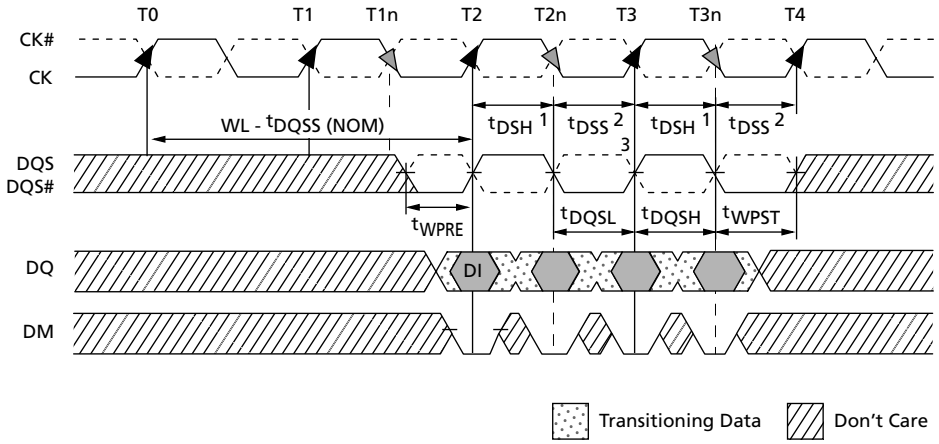
Figure 67: Data Input Timing



Notes:
1. tDSH (MIN) generally occurs during tDQSS (MIN).
2. tDSS (MIN) generally occurs during tDQSS (MAX).
3. Subsequent rising DQS signals must align to the clock within tDQSS.
4. WRITE command issued at T0.
5. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
6. WRITE command with WL = 2 (CL = 3, AL = 0) issued at T0.

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PRECHARGE

Precharge can be initiated by either a manual PRECHARGE command or by an autoprecharge in conjunction with either a READ or WRITE command. Precharge will deactivate the open row in a particular bank or the open row in all banks. The PRECHARGE operation is shown in the previous READ and WRITE operation sections.

During a manual PRECHARGE command, the A10 input determines whether one or all banks are to be precharged. In the case where only one bank is to be precharged, bank address inputs determine the bank to be precharged. When all banks are to be precharged, the bank address inputs are treated as "Don't Care."

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. When a single-bank PRECHARGE command is issued, ^{t}RP timing applies. When the PRECHARGE (ALL) command is issued, ^{t}RPA timing applies, regardless of the number of banks opened.

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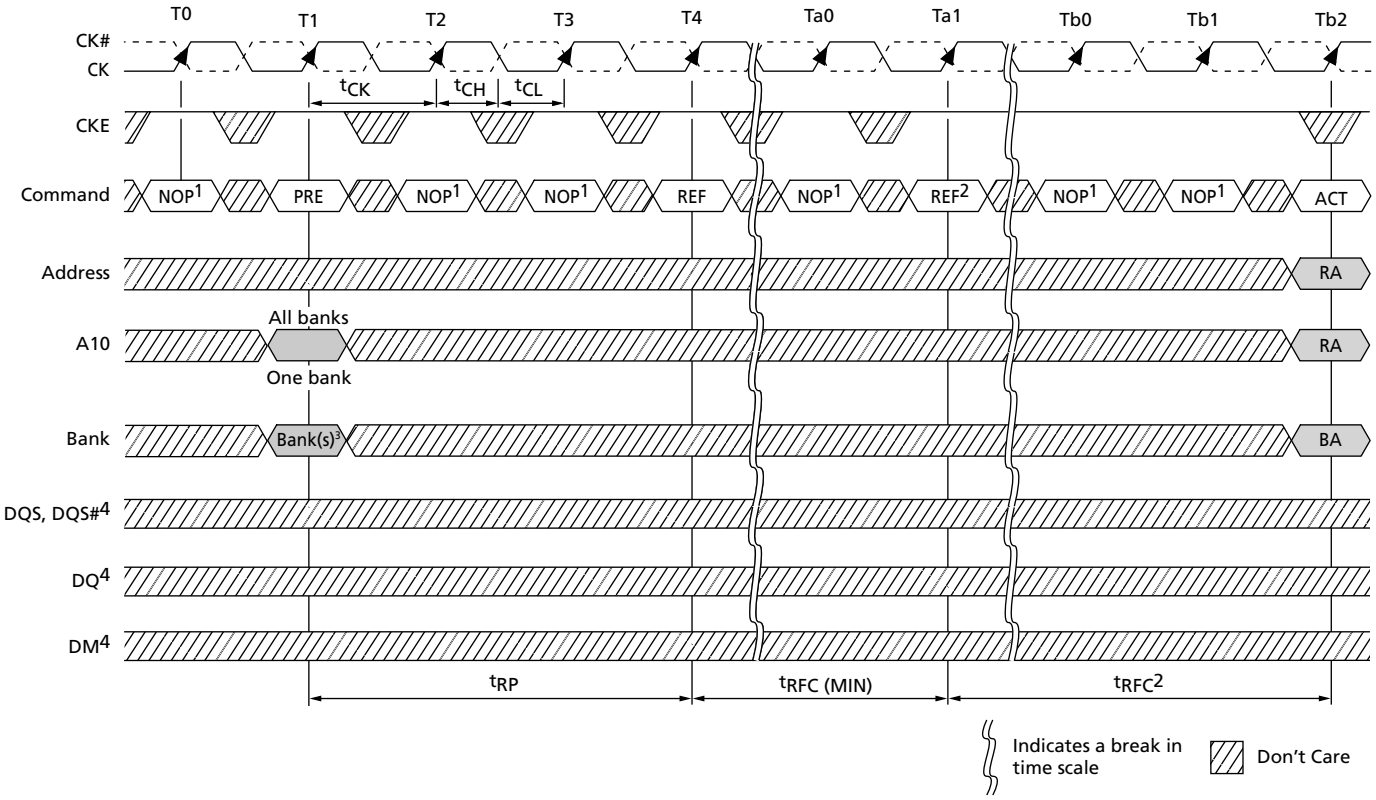
REFRESH

The commercial temperature DDR2 SDRAM requires REFRESH cycles at an average interval of 7.8125µs (MAX) and all rows in all banks must be refreshed at least once every 64ms. The refresh period begins when the REFRESH command is registered and ends ^{t}RFC (MIN) later. The average interval must be reduced to 3.9µs (MAX) when T_C exceeds 85°C.

Figure 68: Refresh Mode



Notes:
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
2. The second REFRESH is not required and is only shown as an example of two back-to-back REFRESH commands.
3. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.

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SELF REFRESH

The SELF REFRESH command is initiated when CKE is LOW. The differential clock should remain stable and meet ^{t}CKE specifications at least 1 × ^{t}CK after entering self refresh mode. The procedure for exiting self refresh requires a sequence of commands. First, the differential clock must be stable and meet ^{t}CK specifications at least 1 × ^{t}CK prior to CKE going back to HIGH. Once CKE is HIGH (^{t}CKE [MIN] has been satisfied with three clock registrations), the DDR2 SDRAM must have NOP or DESELECT commands issued for ^{t}XSNR. A simple algorithm for meeting both refresh and DLL requirements is used to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

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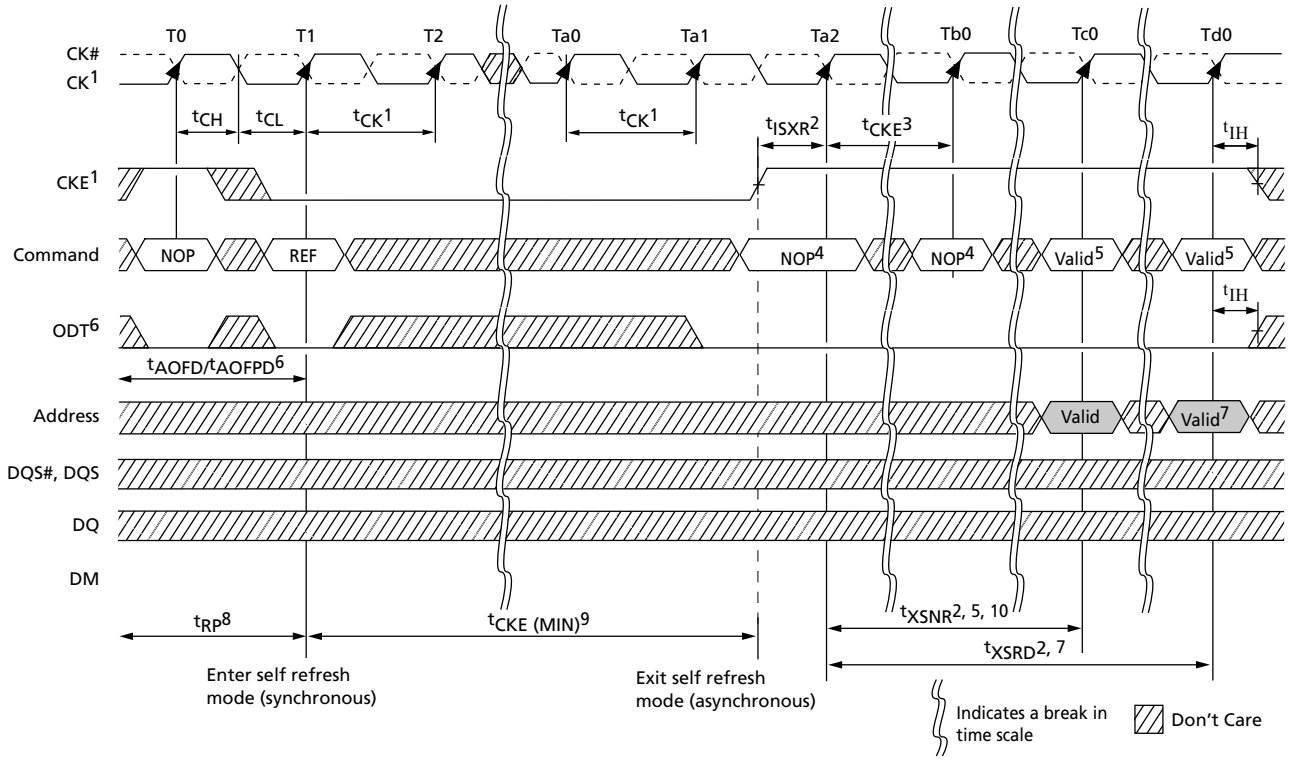
Figure 69: Self Refresh



Notes:
1. Clock must be stable and meeting ^{t}CK specifications at least 1 × ^{t}CK after entering self refresh mode and at least 1 × ^{t}CK prior to exiting self refresh mode.
2. Self refresh exit is asynchronous; however, ^{t}XSNR and ^{t}XSRD timing starts at the first rising clock edge where CKE HIGH satisfies ^{t}ISXR.
3. CKE must stay HIGH until ^{t}XSRD is met; however, if self refresh is being re-entered, CKE may go back LOW after ^{t}XSNR is satisfied.
4. NOP or DESELECT commands are required prior to exiting self refresh until state Tc0, which allows any nonREAD command.
5. ^{t}XSNR is required before any nonREAD command can be applied.
6. ODT must be disabled and R_{TT} off (^{t}AOFD and ^{t}AOFPD have been satisfied) prior to entering self refresh at state T1.
7. ^{t}XSRD (200 cycles of CK) is required before a READ command can be applied at state Td0.
8. Device must be in the all banks idle state prior to entering self refresh mode.
9. After self refresh has been entered, ^{t}CKE (MIN) must be satisfied prior to exiting self refresh.
10. Upon exiting SELF REFRESH, ODT must remain LOW until ^{t}XSRD is satisfied.

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Power-Down Mode

DDR2 SDRAM supports multiple power-down modes that allow significant power savings over normal operating modes. CKE is used to enter and exit different power-down modes. Power-down entry and exit timings are shown in Figure 70 (page 125). Detailed power-down entry conditions are shown in Figure 71 (page 127)–Figure 78 (page 130). Table 44 (page 126) is the CKE Truth Table.

DDR2 SDRAM requires CKE to be registered HIGH (active) at all times that an access is in progress—from the issuing of a READ or WRITE command until completion of the burst. Thus, a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; for WRITEs, a burst completion is defined when the write postamble and ^{t}WR (WRITE-to-PRECHARGE command) or ^{t}WTR (WRITE-to-READ command) are satisfied, as shown in Figure 73 (page 128) and Figure 74 (page 128) on Figure 74 (page 128). The number of clock cycles required to meet ^{t}WTR is either two or ^{t}WTR/^{t}CK, whichever is greater.

Power-down mode (see Figure 70 (page 125)) is entered when CKE is registered low coincident with an NOP or DESELECT command. CKE is not allowed to go LOW during a mode register or extended mode register command time, or while a READ or WRITE operation is in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, and CKE. For maximum power savings, the DLL is frozen during precharge power-down. Exiting active power-down requires the device to be at the same voltage and frequency as when it entered power-down. Exiting precharge power-down requires the device to be at the same voltage as when it entered power-down; however, the clock frequency is allowed to change (see Precharge Power-Down Clock Frequency Change (page 131)).

The maximum duration for either active or precharge power-down is limited by the refresh requirements of the device ^{t}RFC (MAX). The minimum duration for power-down entry and exit is limited by the ^{t}CKE (MIN) parameter. The following must be maintained while in power-down mode: CKE LOW, a stable clock signal, and stable power supply signals at the inputs of the DDR2 SDRAM. All other input signals are “Don’t Care” except ODT. Detailed ODT timing diagrams for different power-down modes are shown in Figure 83 (page 137)–Figure 88 (page 141).

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command), as shown in Figure 70 (page 125).

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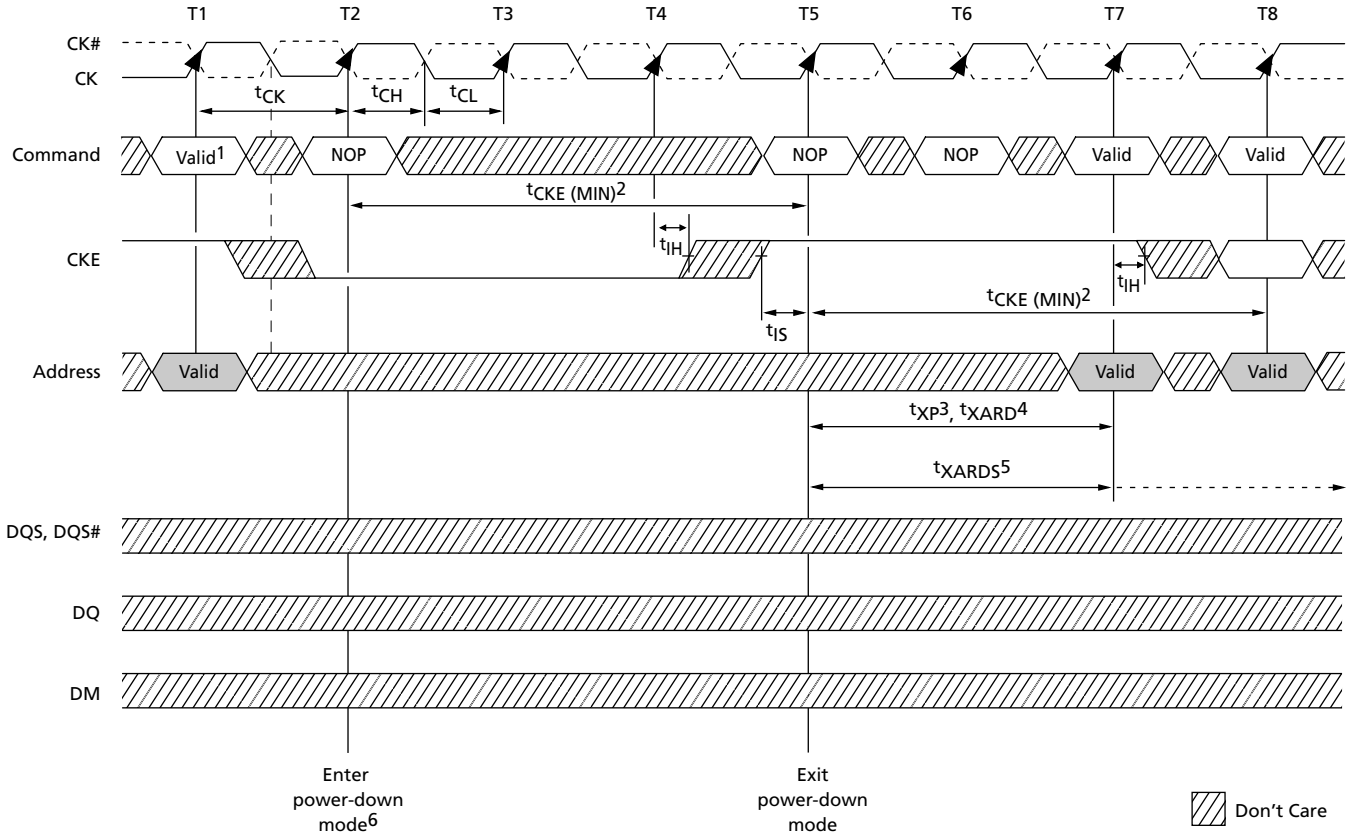
Figure 70: Power-Down



Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVATE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. ^{t}CKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 × ^{t}CK + ^{t}IH. CKE must not transition during its ^{t}IS and ^{t}IH window.
3. ^{t}XP timing is used for exit precharge power-down and active power-down to any non-READ command.
4. ^{t}XARD timing is used for exit active power-down to READ command if fast exit is selected via MR (bit 12 = 0).
5. ^{t}XARDS timing is used for exit active power-down to READ command if slow exit is selected via MR (bit 12 = 1).
6. No column accesses are allowed to be in progress at the time power-down is entered. If the DLL was not in a locked state when CKE went LOW, the DLL must be reset after exiting power-down mode for proper READ operation.

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Table 44: Truth Table – CKE

Notes 1–4 apply to the entire table

Current State	CKE		Command (*n*) CS#, RAS#, CAS#, WE#	Action (*n*)	Notes
	Previous Cycle (*n* - 1)	Current Cycle (*n*)			
Power-down	L	L	X	Maintain power-down	5, 6
	L	H	DESELECT or NOP	Power-down exit	7, 8
Self refresh	L	L	X	Maintain self refresh	6
	L	H	DESELECT or NOP	Self refresh exit	7, 9, 10
Bank(s) active	H	L	DESELECT or NOP	Active power-down entry	7, 8, 11, 12
All banks idle	H	L	DESELECT or NOP	Precharge power-down entry	7, 8, 11
	H	L	Refresh	Self refresh entry	10, 12, 13
	H	H	Shown in Table 37 (page 74)		14

Notes:
1. CKE (*n*) is the logic state of CKE at clock edge *n*; CKE (*n* - 1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge *n*.
3. Command (*n*) is the command registered at clock edge *n*, and action (*n*) is a result of command (*n*).
4. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh (see ODT Timing (page 134) for more details and specific restrictions).
5. Power-down modes do not perform any REFRESH operations. The duration of power-down mode is therefore limited by the refresh requirements.
6. "X" means "Don't Care" (including floating around V_{REF}) in self refresh and power-down. However, ODT must be driven high or low in power-down if the ODT function is enabled via EMR.
7. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
8. Valid commands for power-down entry and exit are NOP and DESELECT only.
9. On self refresh exit, DESELECT or NOP commands must be issued on every clock edge occurring during the ^{t}XSNR period. READ commands may be issued only after ^{t}XSRD (200 clocks) is satisfied.
10. Valid commands for self refresh exit are NOP and DESELECT only.
11. Power-down and self refresh can not be entered while READ or WRITE operations, LOAD MODE operations, or PRECHARGE operations are in progress. See SELF REFRESH (page 122) and SELF REFRESH (page 80) for a list of detailed restrictions.
12. Minimum CKE high time is ^{t}CKE = 3 × ^{t}CK. Minimum CKE LOW time is ^{t}CKE = 3 × ^{t}CK. This requires a minimum of 3 clock cycles of registration.
13. Self refresh mode can only be entered from the all banks idle state.
14. Must be a legal command, as defined in Table 37 (page 74).

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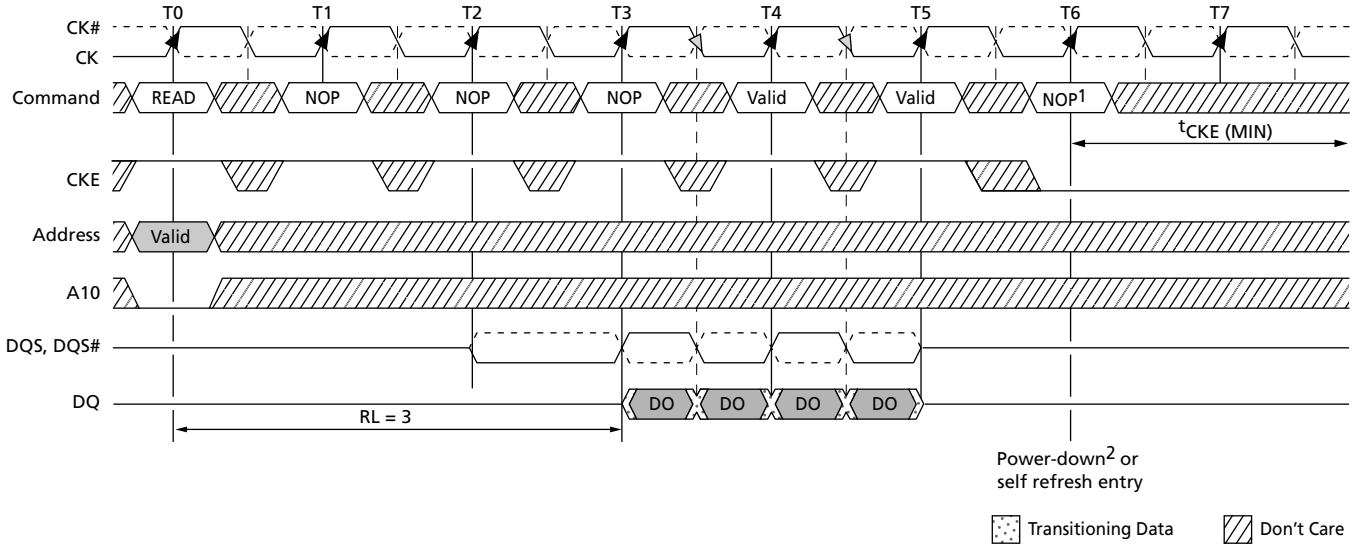
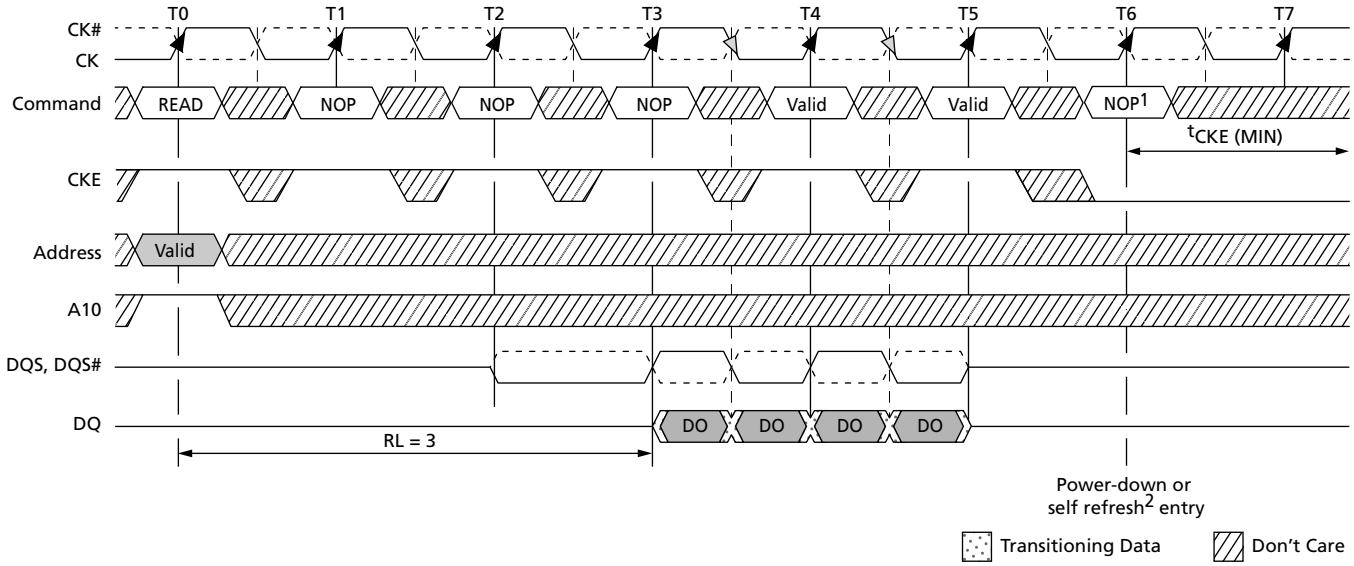
Figure 71: READ-to-Power-Down or Self Refresh Entry



Notes: 1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.
2. Power-down or self refresh entry may occur after the READ burst completes.

Figure 72: READ with Auto Precharge-to-Power-Down or Self Refresh Entry



Notes: 1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.
2. Power-down or self refresh entry may occur after the READ burst completes.

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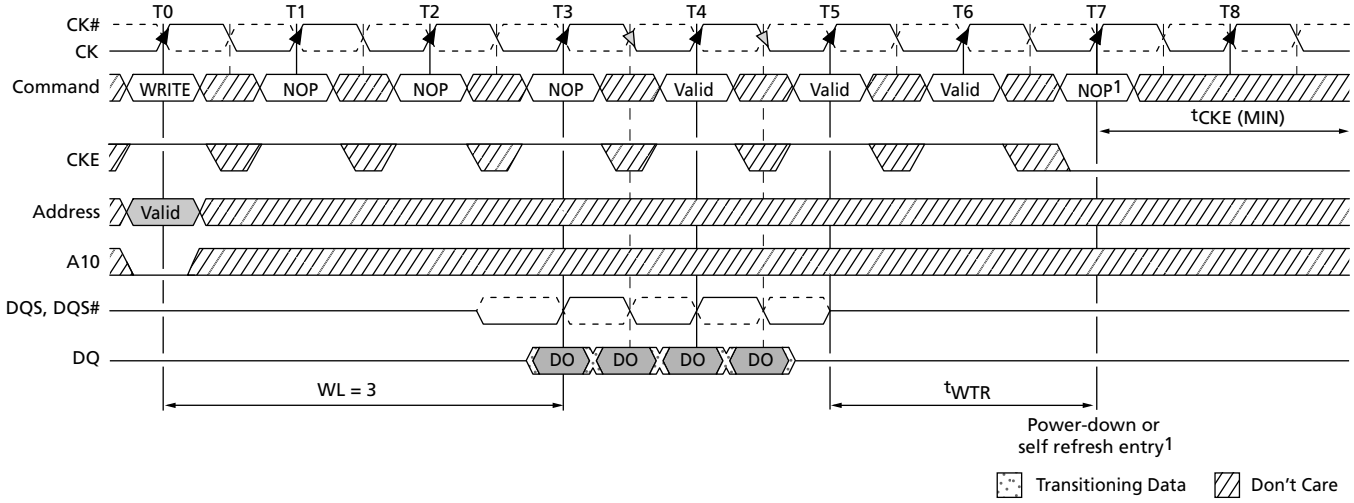
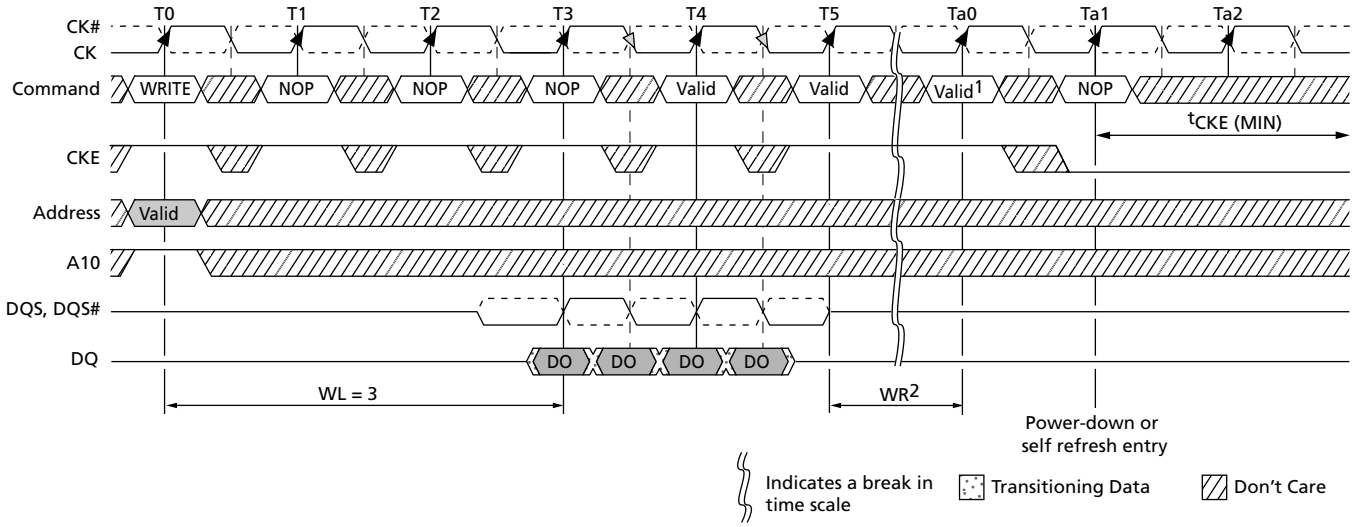
Figure 73: WRITE-to-Power-Down or Self Refresh Entry



Note: 1. Power-down or self refresh entry may occur after the WRITE burst completes.

Figure 74: WRITE with Auto Precharge-to-Power-Down or Self Refresh Entry



Notes: 1. Internal PRECHARGE occurs at Ta0 when WR has completed; power-down entry may occur 1 x ^{t}CK later at Ta1, prior to ^{t}RP being satisfied.
2. WR is programmed through MR9–MR11 and represents (^{t}WR [MIN] ns/^{t}CK) rounded up to next integer ^{t}CK.

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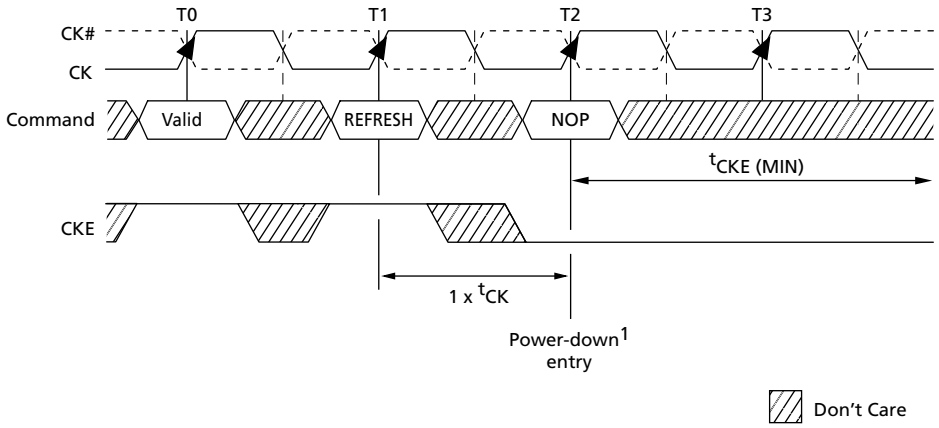
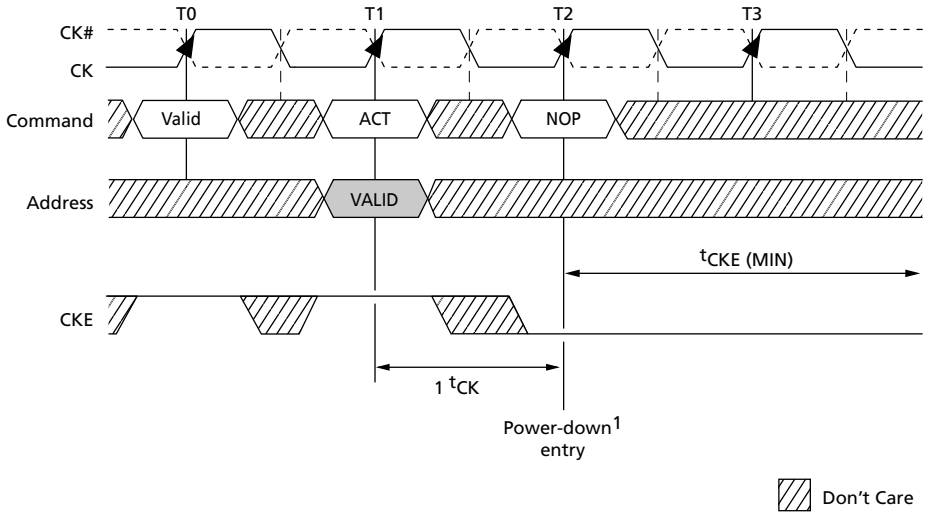
Figure 75: REFRESH Command-to-Power-Down Entry



Note: 1. The earliest precharge power-down entry may occur is at T2, which is 1 × ^{t}CK after the REFRESH command. Precharge power-down entry occurs prior to ^{t}RFC (MIN) being satisfied.

Figure 76: ACTIVATE Command-to-Power-Down Entry



Note: 1. The earliest active power-down entry may occur is at T2, which is 1 × ^{t}CK after the ACTIVATE command. Active power-down entry occurs prior to ^{t}RCD (MIN) being satisfied.

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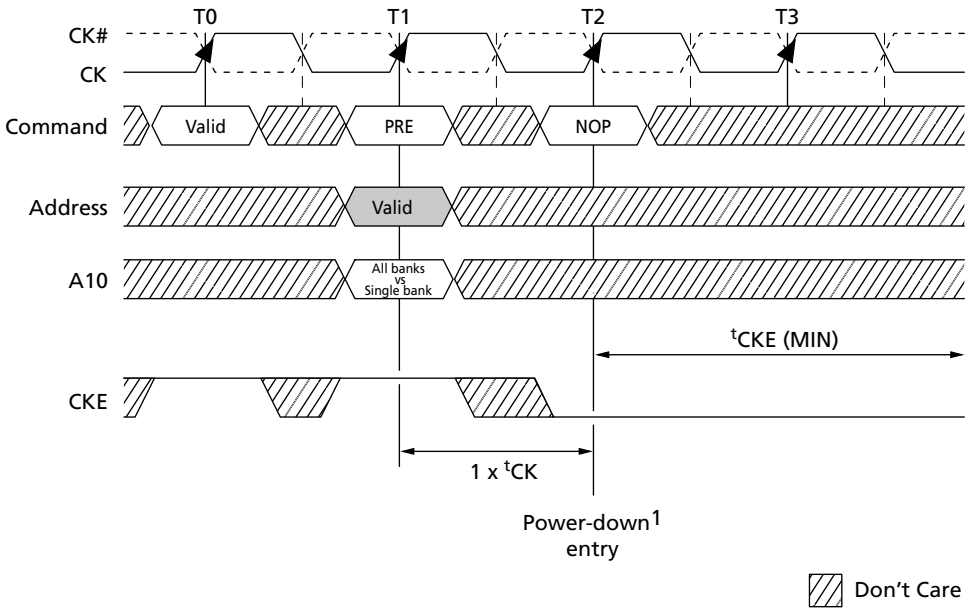
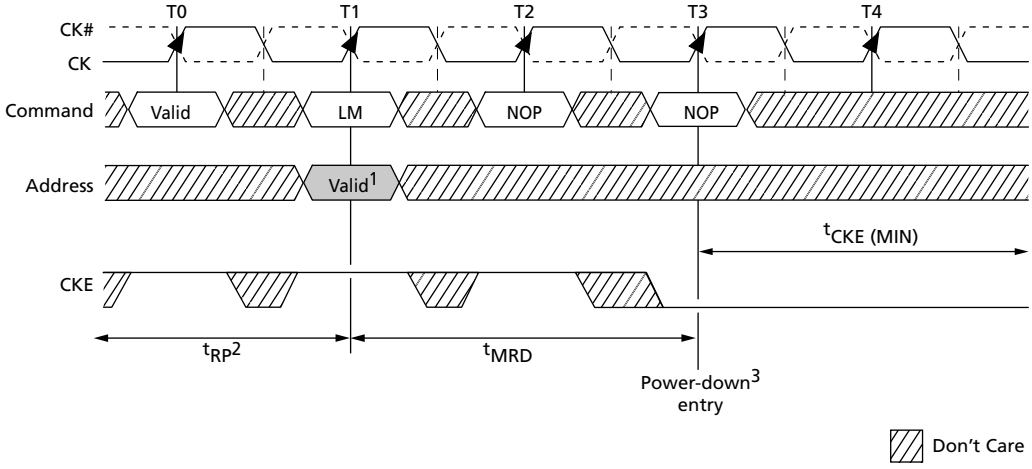
Figure 77: PRECHARGE Command-to-Power-Down Entry



Note: 1. The earliest precharge power-down entry may occur is at T2, which is 1 × ^{t}CK after the PRECHARGE command. Precharge power-down entry occurs prior to ^{t}RP (MIN) being satisfied.

Figure 78: LOAD MODE Command-to-Power-Down Entry



Notes: 1. Valid address for LM command includes MR, EMR, EMR(2), and EMR(3) registers.
2. All banks must be in the precharged state and ^{t}RP met prior to issuing LM command.
3. The earliest precharge power-down entry is at T3, which is after ^{t}MRD is satisfied.

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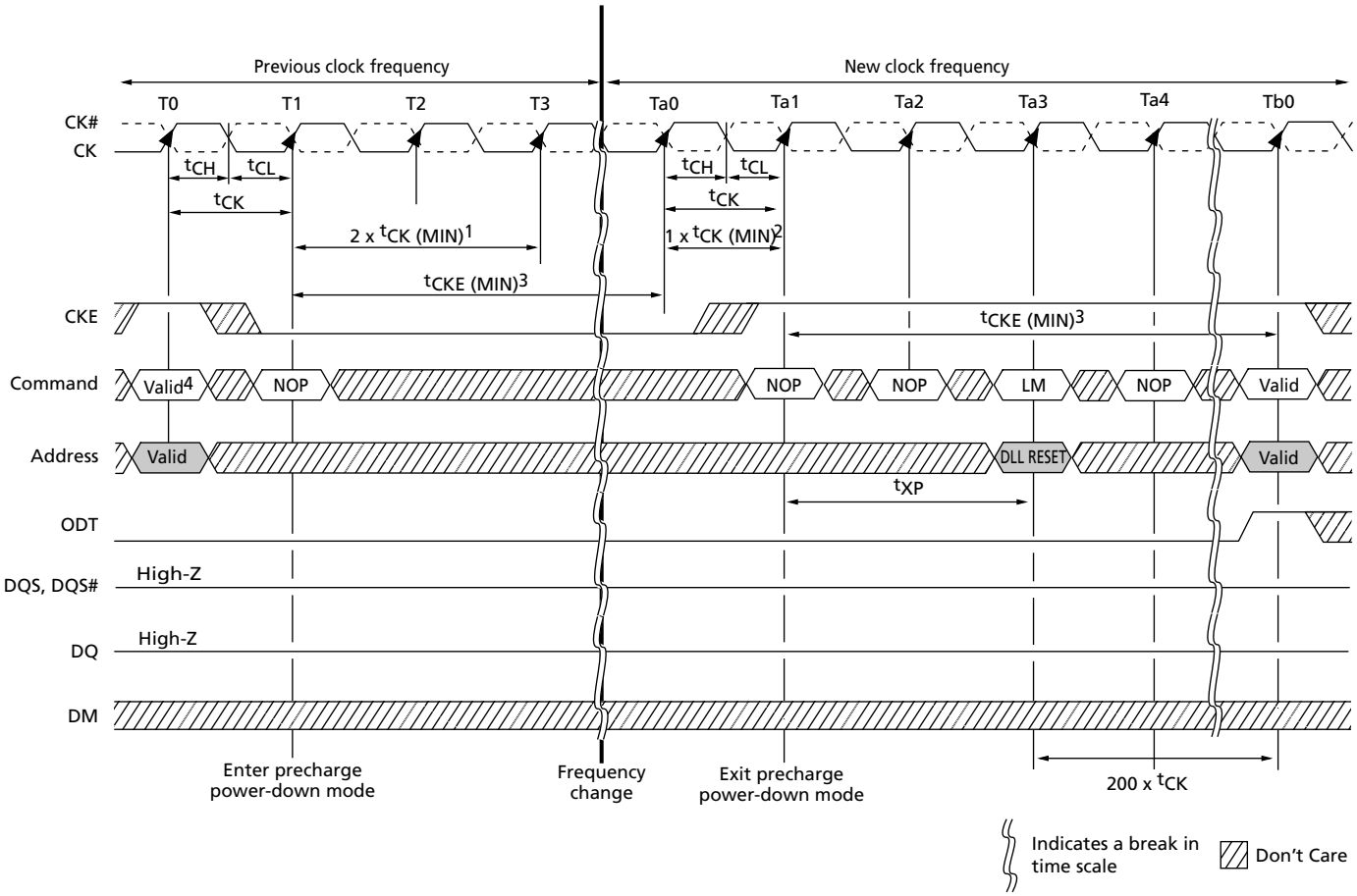
Precharge Power-Down Clock Frequency Change

When the DDR2 SDRAM is in precharge power-down mode, ODT must be turned off and CKE must be at a logic LOW level. A minimum of two differential clock cycles must pass after CKE goes LOW before clock frequency may change. The device input clock frequency is allowed to change only within minimum and maximum operating frequencies specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. When the input clock frequency is changed, new stable clocks must be provided to the device before precharge power-down may be exited, and DLL must be reset via MR after precharge power-down exit. Depending on the new clock frequency, additional LM commands might be required to adjust the CL, WR, AL, and so forth. Depending on the new clock frequency, an additional LM command might be required to appropriately set the WR MR9, MR10, MR11. During the DLL relock period of 200 cycles, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

Figure 79: Input Clock Frequency Change During Precharge Power-Down Mode



Notes:
1. A minimum of 2 × ^{t}CK is required after entering precharge power-down prior to changing clock frequencies.
2. When the new clock frequency has changed and is stable, a minimum of 1 × ^{t}CK is required prior to exiting precharge power-down.

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3. Minimum CKE high time is ^{t}CKE = 3 × ^{t}CK. Minimum CKE LOW time is ^{t}CKE = 3 × ^{t}CK. This requires a minimum of three clock cycles of registration.
4. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down, which is required prior to the clock frequency change.

Reset

CKE Low Anytime

DDR2 SDRAM applications may go into a reset state anytime during normal operation. If an application enters a reset condition, CKE is used to ensure the DDR2 SDRAM device resumes normal operation after reinitializing. All data will be lost during a reset condition; however, the DDR2 SDRAM device will continue to operate properly if the following conditions outlined in this section are satisfied.

The reset condition defined here assumes all supply voltages (V_{DD}, V_{DDQ}, V_{DDL}, and V_{REF}) are stable and meet all DC specifications prior to, during, and after the RESET operation. All other input balls of the DDR2 SDRAM device are a "Don't Care" during RESET with the exception of CKE.

If CKE asynchronously drops LOW during any valid operation (including a READ or WRITE burst), the memory controller must satisfy the timing parameter ^{t}DELAY before turning off the clocks. Stable clocks must exist at the CK, CK# inputs of the DRAM before CKE is raised HIGH, at which time the normal initialization sequence must occur (see Initialization). The DDR2 SDRAM device is now ready for normal operation after the initialization sequence. Figure 80 (page 133) shows the proper sequence for a RESET operation.

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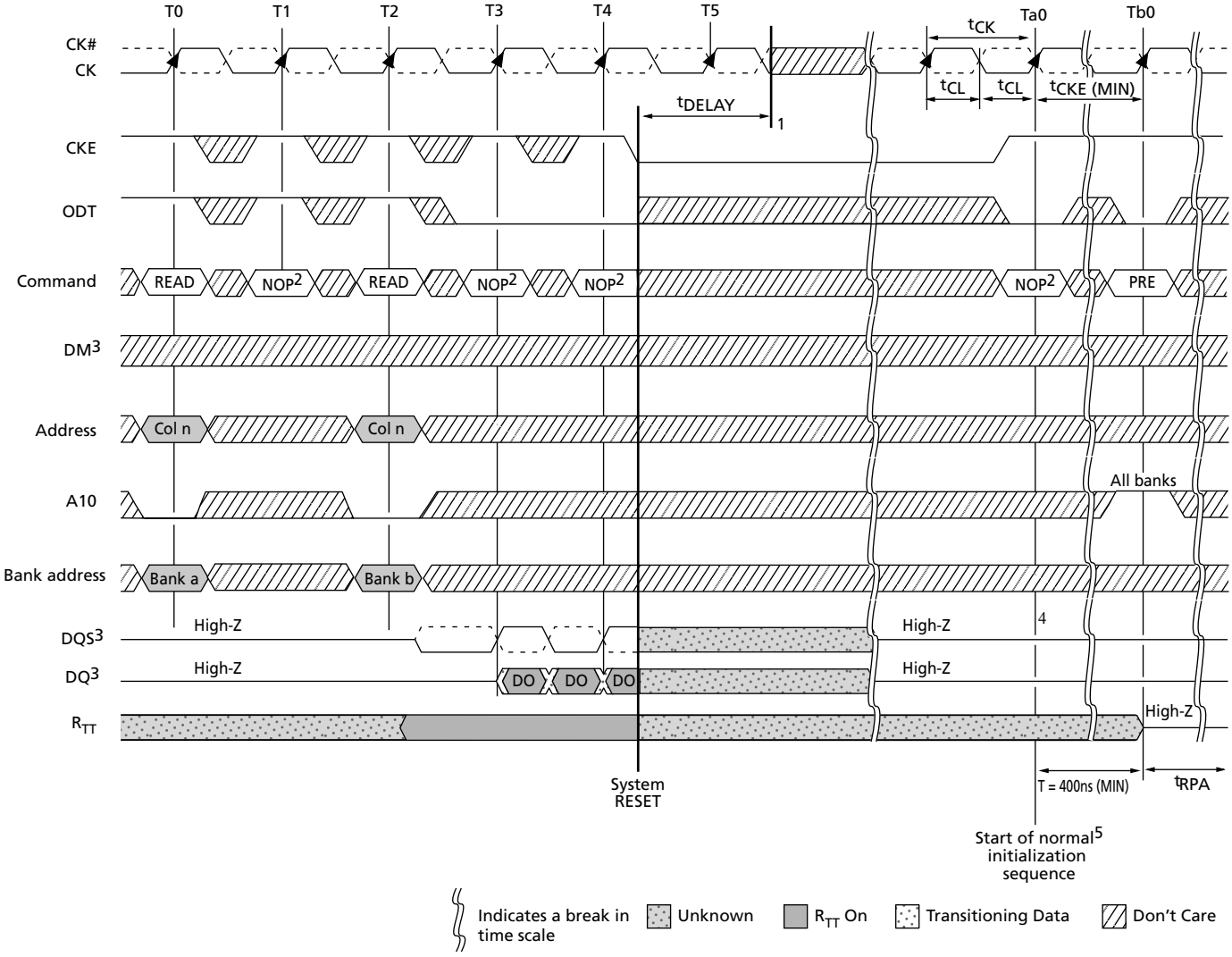
Figure 80: RESET Function



Notes:
1. V_{DD}, V_{DDL}, V_{DDQ}, V_{TT}, and V_{REF} must be valid at all times.
2. Either NOP or DESELECT command may be applied.
3. DM represents DM for x4/x8 configuration and UDM, LDM for x16 configuration. DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, and RDQS# for the appropriate configuration (x4, x8, x16).
4. In certain cases where a READ cycle is interrupted, CKE going HIGH may result in the completion of the burst.
5. Initialization timing is shown in Figure 43 (page 92).

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ODT Timing

Once a 12ns delay (^{t}MOD) has been satisfied, and after the ODT function has been enabled via the EMR LOAD MODE command, ODT can be accessed under two timing categories. ODT will operate either in synchronous mode or asynchronous mode, depending on the state of CKE. ODT can switch anytime except during self refresh mode and a few clocks after being enabled via EMR, as shown in Figure 81 (page 135).

There are two timing categories for ODT—turn-on and turn-off. During active mode (CKE HIGH) and fast-exit power-down mode (any row of any bank open, CKE LOW, MR[12 = 0]), ^{t}AOND, ^{t}AON, ^{t}AOFD, and ^{t}AOF timing parameters are applied, as shown in Figure 83 (page 137).

During slow-exit power-down mode (any row of any bank open, CKE LOW, MR[12] = 1) and precharge power-down mode (all banks/rows precharged and idle, CKE LOW), ^{t}AONPD and ^{t}AOFPD timing parameters are applied, as shown in Figure 84 (page 137).

ODT turn-off timing, prior to entering any power-down mode, is determined by the parameter ^{t}ANPD (MIN), as shown in Figure 85 (page 138). At state T2, the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 85 (page 138) also shows the example where ^{t}ANPD (MIN) is **not** satisfied because ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is **not** satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing prior to entering any power-down mode is determined by the parameter ^{t}ANPD, as shown in Figure 86 (page 139). At state T2, the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 86 (page 139) also shows the example where ^{t}ANPD (MIN) is **not** satisfied because ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is **not** satisfied, ^{t}AONPD timing parameters apply.

ODT turn-off timing after exiting any power-down mode is determined by the parameter ^{t}AXPD (MIN), as shown in Figure 87 (page 140). At state Ta1, the ODT LOW signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 87 (page 140) also shows the example where ^{t}AXPD (MIN) is **not** satisfied because ODT LOW occurs at state Ta0. When ^{t}AXPD (MIN) is not satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing after exiting either slow-exit power-down mode or precharge power-down mode is determined by the parameter ^{t}AXPD (MIN), as shown in Figure 88 (page 141). At state Ta1, the ODT HIGH signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 88 (page 141) also shows the example where ^{t}AXPD (MIN) is not satisfied because ODT HIGH occurs at state Ta0. When ^{t}AXPD (MIN) is not satisfied, ^{t}AONPD timing parameters apply.

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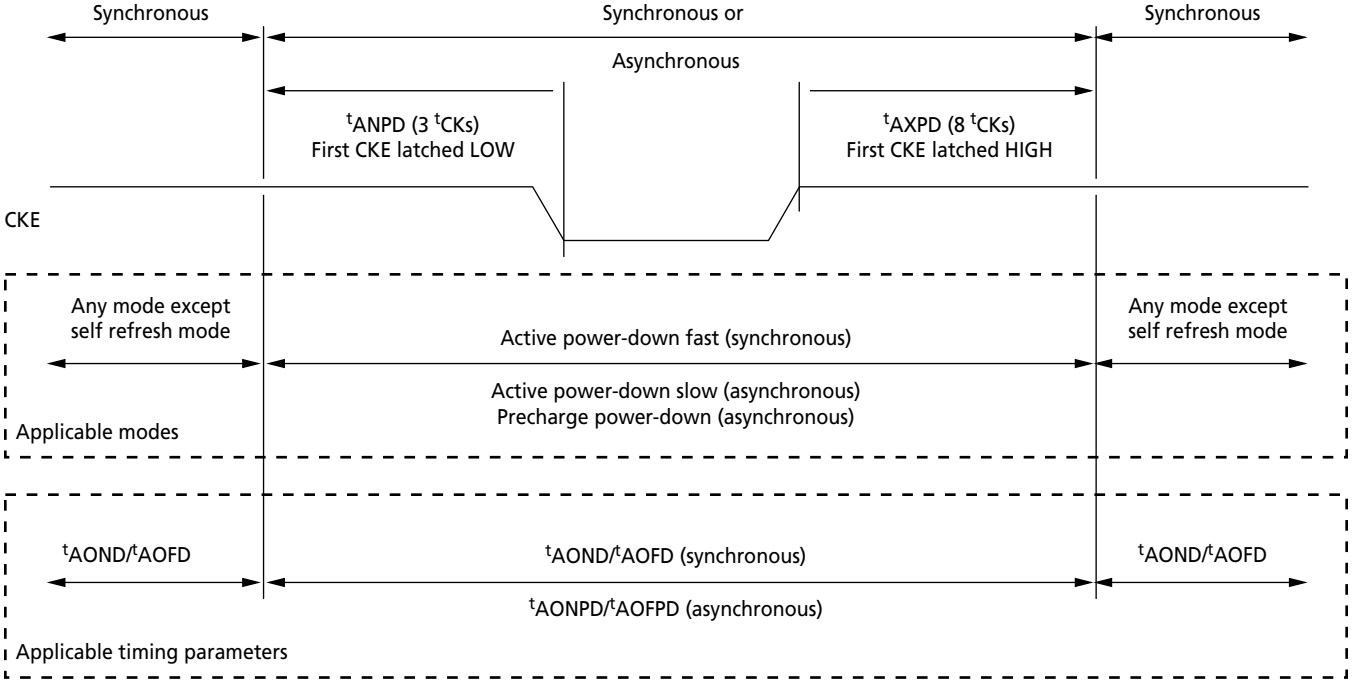
Figure 81: ODT Timing for Entering and Exiting Power-Down Mode



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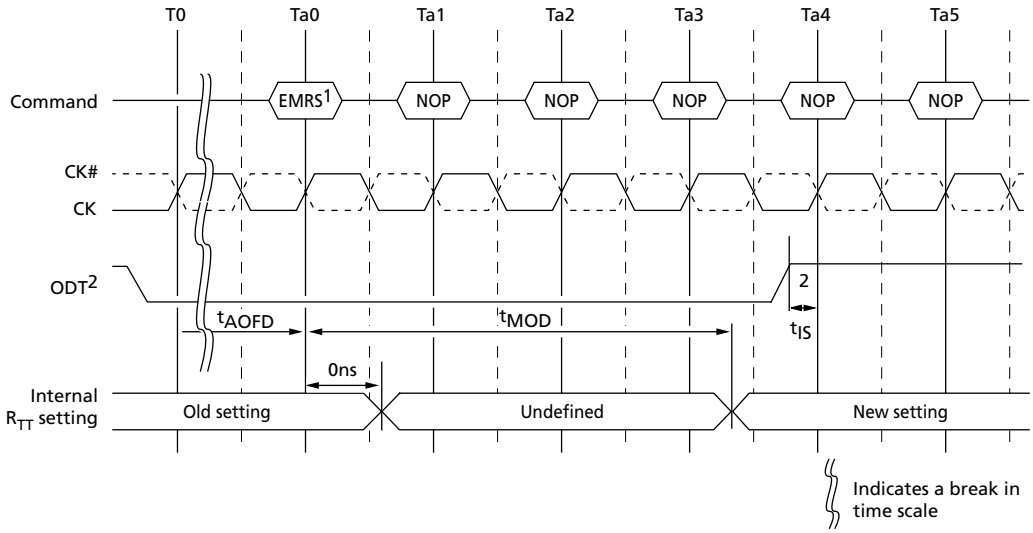
MRS Command to ODT Update Delay

During normal operation, the value of the effective termination resistance can be changed with an EMRS set command. ^{t}MOD (MAX) updates the R_{TT} setting.

Figure 82: Timing for MRS Command to ODT Update Delay



Notes:
1. The LM command is directed to the mode register, which updates the information in EMR (A6, A2), that is, R_{TT} (nominal).
2. To prevent any impedance glitch on the channel, the following conditions must be met: ^{t}AOFD must be met before issuing the LM command; ODT must remain LOW for the entire duration of the ^{t}MOD window until ^{t}MOD is met.

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Figure 83: ODT Timing for Active or Fast-Exit Power-Down Mode

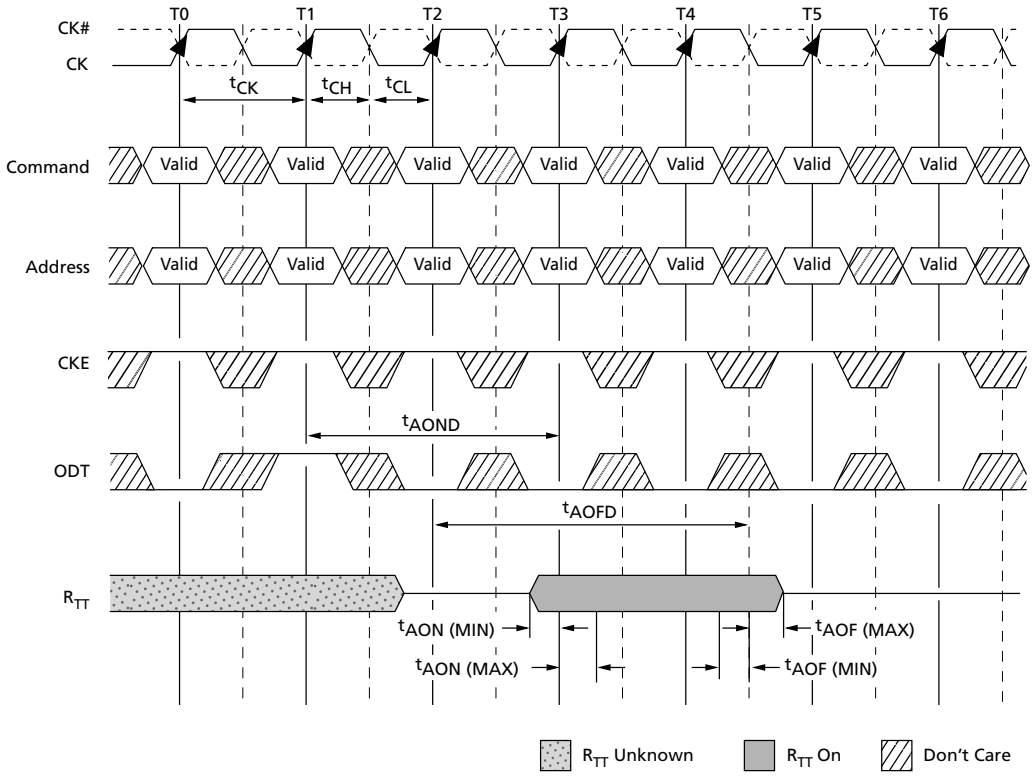

Figure 84: ODT Timing for Slow-Exit or Precharge Power-Down Modes

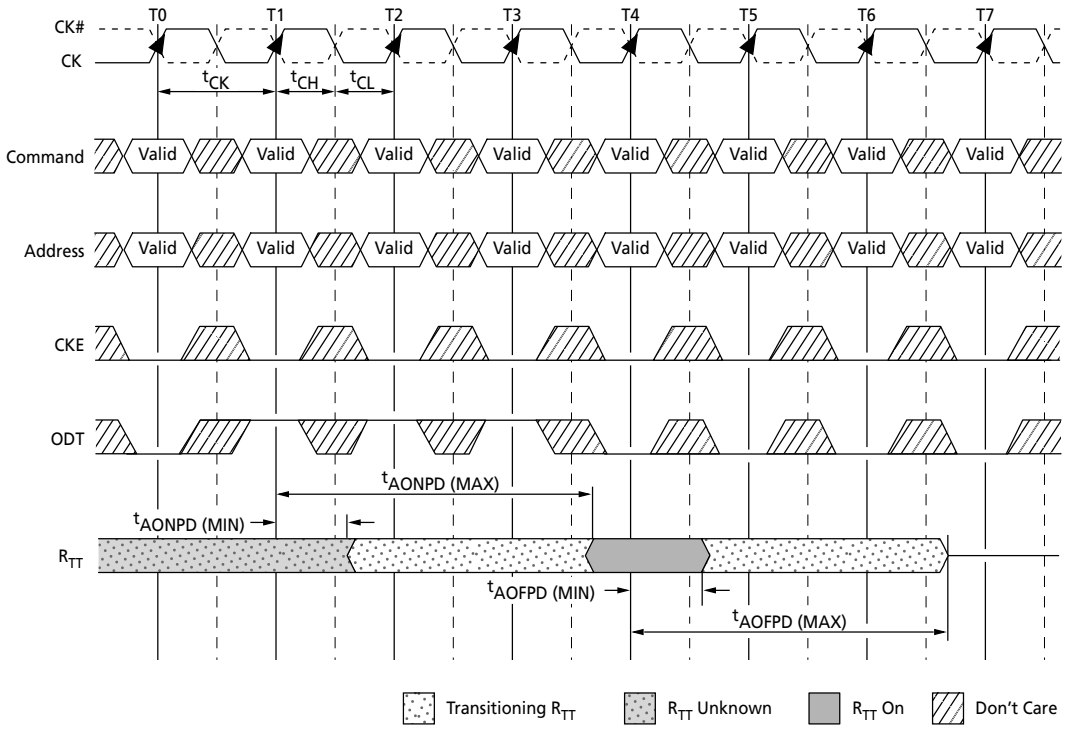

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Figure 85: ODT Turn-Off Timings When Entering Power-Down Mode

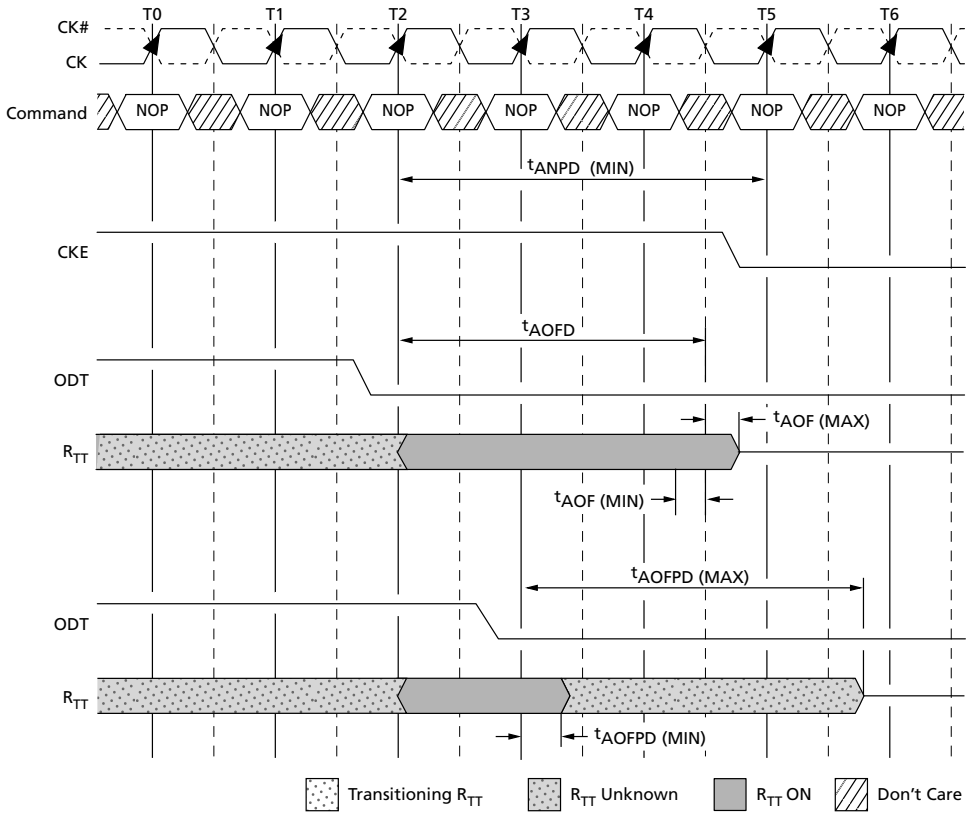

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Figure 86: ODT Turn-On Timing When Entering Power-Down Mode

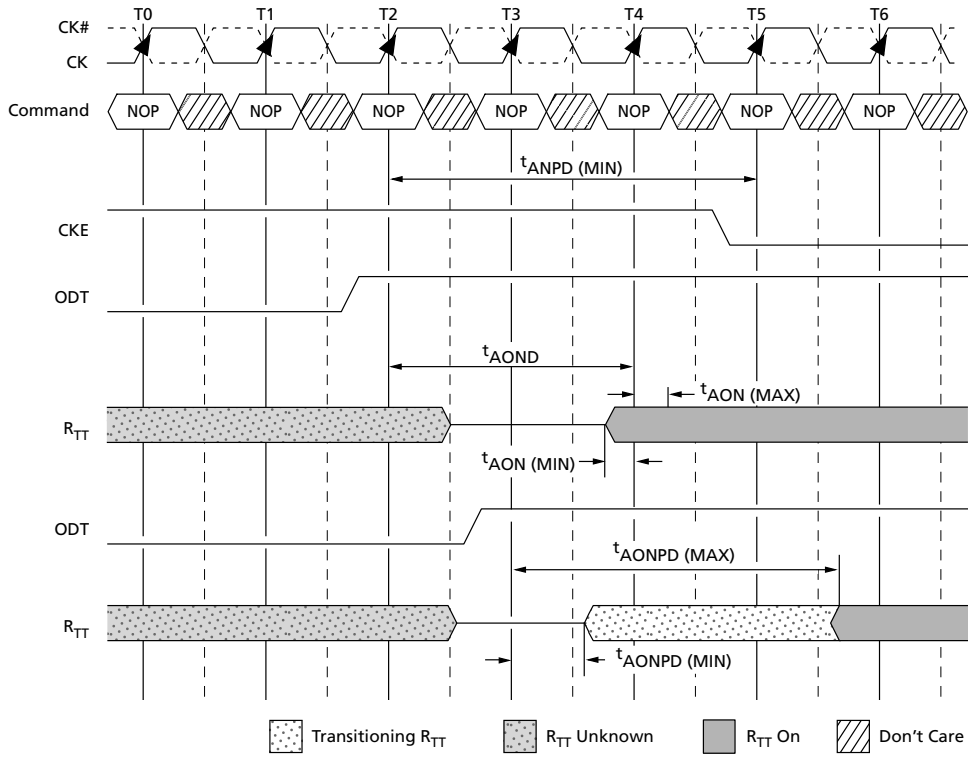

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Figure 87: ODT Turn-Off Timing When Exiting Power-Down Mode

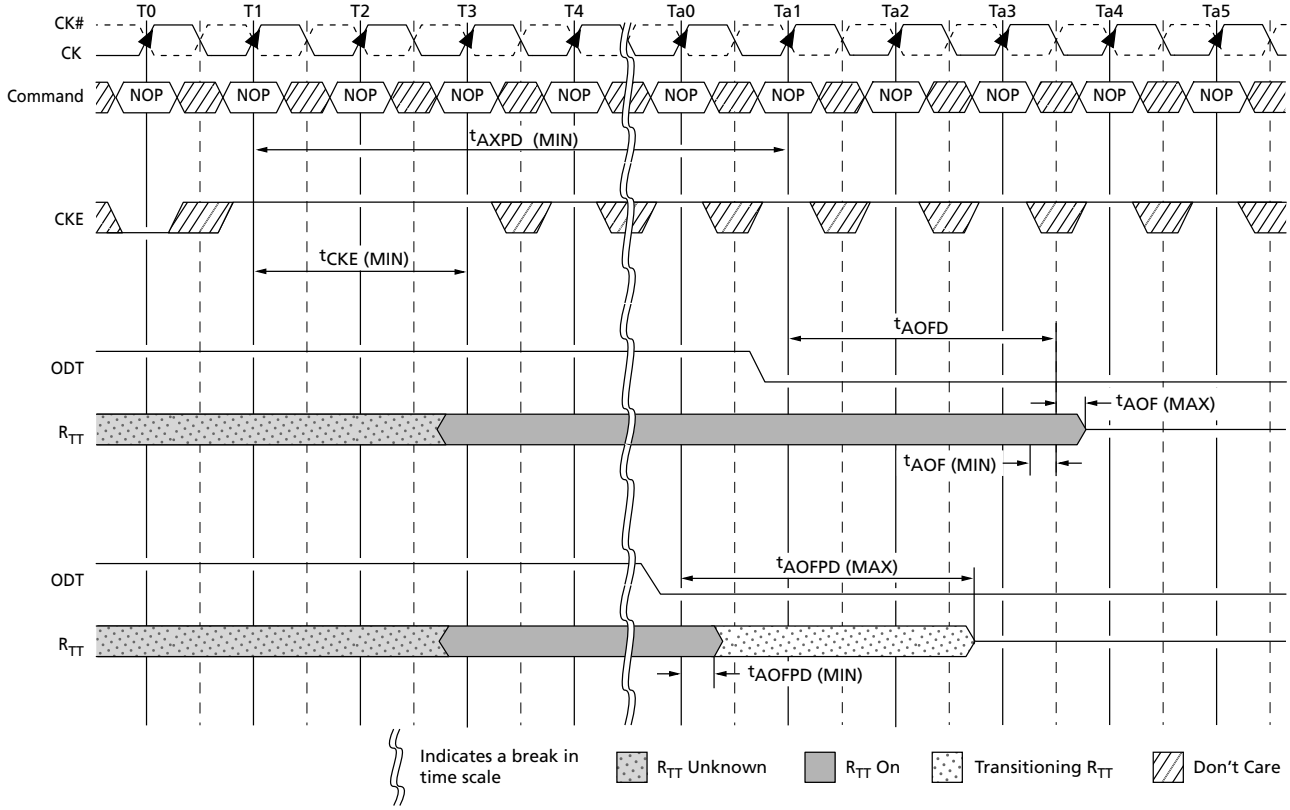

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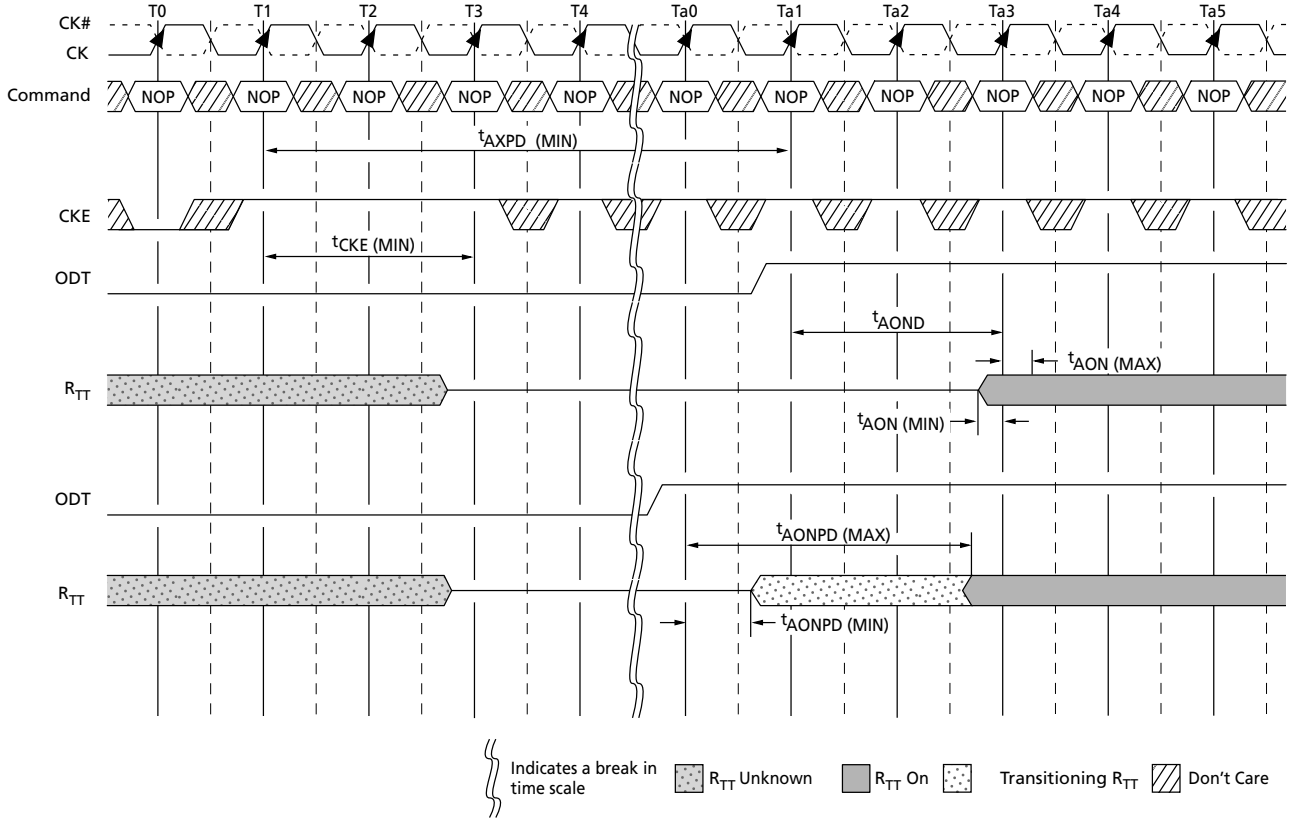
Figure 88: ODT Turn-On Timing When Exiting Power-Down Mode



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