WINSOURCE ELECTRONICS

THE DATASHEET OF

MTD6N15T4G

MTD6N15

Power Field Effect Transistor DPAK for Surface Mount

N−Channel Enhancement−Mode Silicon Gate

This Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

Features

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.3 Ω Max
- Rugged — SOA is Power Dissipation Limited
- Source−to−Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4.0 V Max
- Surface Mount Package on 16 mm Tape
- Pb−Free Package is Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	150	Vdc
Drain−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	150	Vdc
Gate−Source Voltage − Continuous − Non−Repetitive ($t_p \le 50$ μs)	 V_{GS} V_{GSM}	 ± 20 ± 40	 Vdc Vpk
Drain Current − Continuous − Pulsed	I_D I_{DM}	6.0 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C (Note 1)	P_D	1.25 0.01	W W/°C
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above 25°C (Note 2)	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance − Junction−to−Case − Junction−to−Ambient (Note 1) − Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 6.25 100 71.4	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

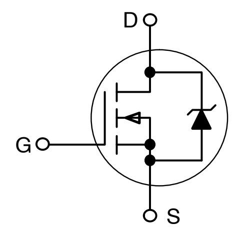
1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.

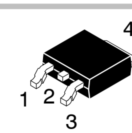
ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
150 V	0.3 Ω	6.0 A

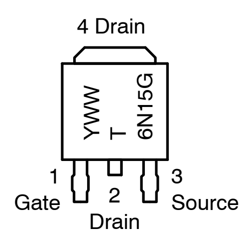
N−CHANNEL





CASE 369C
DPAK
(Surface Mount)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year
WW = Work Week
6N15 = Device Code
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MTD6N15T4	DPAK	2500/Tape & Reel
MTD6N15T4G	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	150	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0 Vdc) T_J = 125°C		I_{DSS}	– –	10 100	μAdc
Gate−Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	–	100	nAdc
Gate−Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	–	100	nAdc
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mAdc) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Static Drain−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	–	0.3	Ω
Drain−Source On−Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 100°C)		$V_{DS(on)}$	– –	1.8 1.5	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3.0 Adc)		g_{FS}	2.5	–	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz) (See Figure 11)	C_{iss}	–	1200	pF
Output Capacitance		C_{oss}	–	500	
Reverse Transfer Capacitance		C_{rss}	–	120	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn−On Delay Time	(V_{DD} = 25 Vdc, I_D = 3.0 Adc, R_G = 50 Ω) (See Figures 13 and 14)	$t_{d(on)}$	–	50	ns
Rise Time		t_r	–	180	
Turn−Off Delay Time		$t_{d(off)}$	–	200	
Fall Time		t_f	–	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 Vdc) (See Figure 12)	Q_g	15 (Typ)	30	nC
Gate−Source Charge		Q_{gs}	8.0 (Typ)	–	
Gate−Drain Charge		Q_{gd}	7.0 (Typ)	–	
SOURCE−DRAIN DIODE CHARACTERISTICS*					
Forward On−Voltage	(I_S = 6.0 Adc, di/dt = 25 A/μs, V_{GS} = 0 Vdc)	V_{SD}	1.3 (Typ)	2.0	Vdc
Forward Turn−On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	–	ns

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

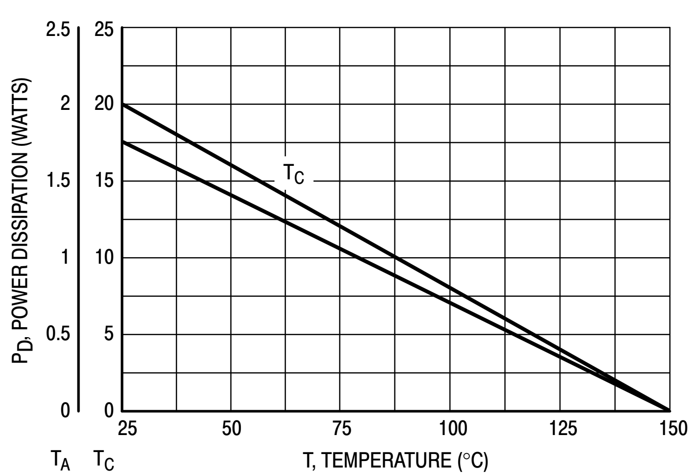


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

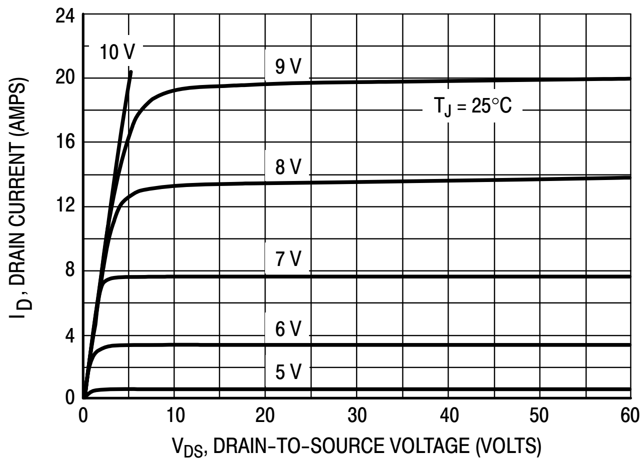


Figure 2. On−Region Characteristics

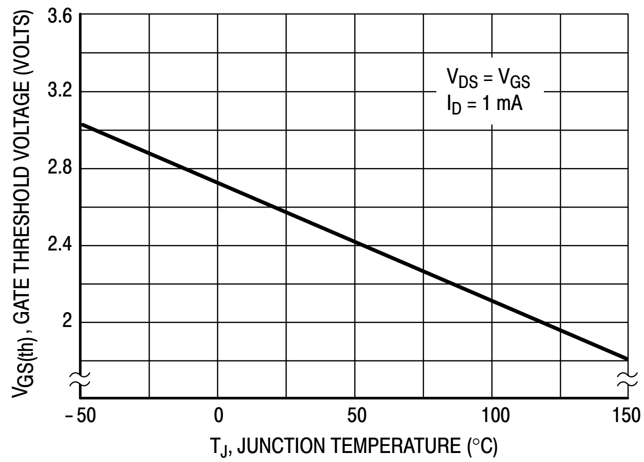


Figure 3. Gate−Threshold Voltage Variation With Temperature

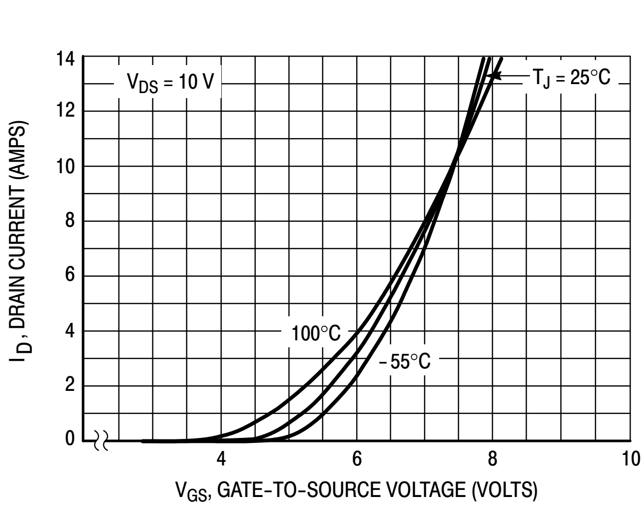


Figure 4. Transfer Characteristics

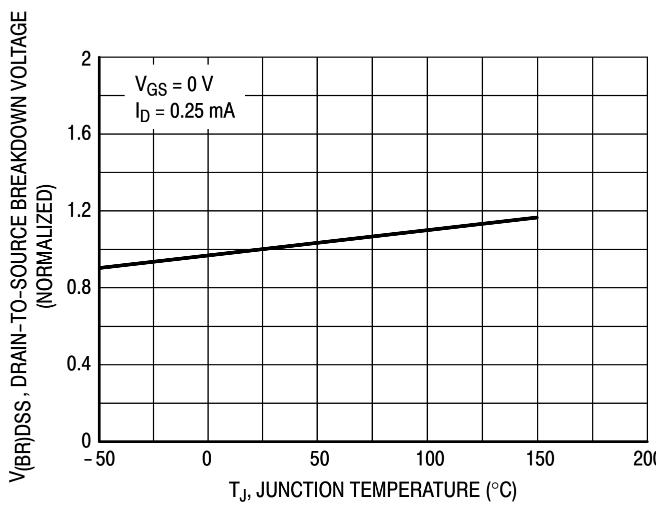


Figure 5. Breakdown Voltage Variation With Temperature

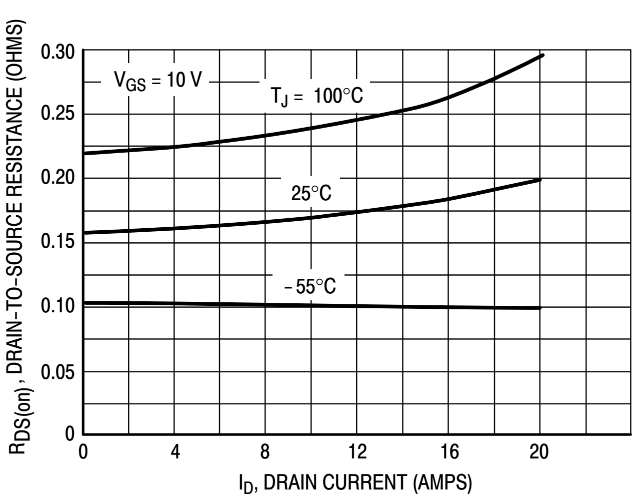


Figure 6. On−Resistance versus Drain Current

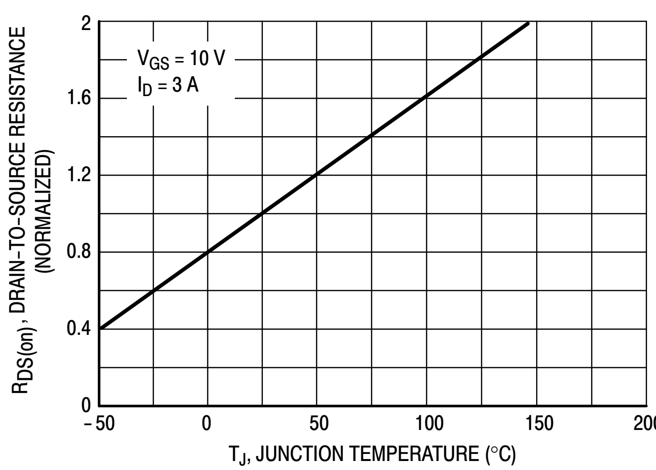


Figure 7. On−Resistance Variation With Temperature

SAFE OPERATING AREA

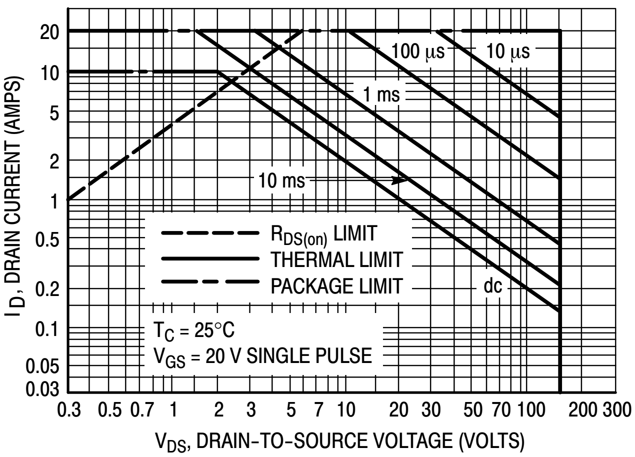


Figure 8. Maximum Rated Forward Biased Safe Operating Area

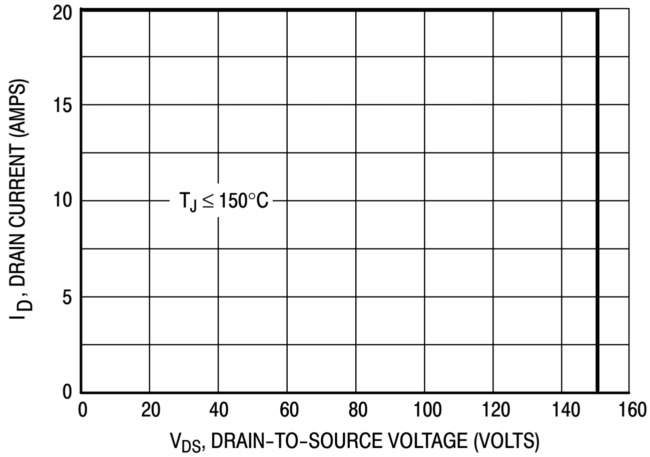


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain−to−source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance−General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn−on and turn−off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

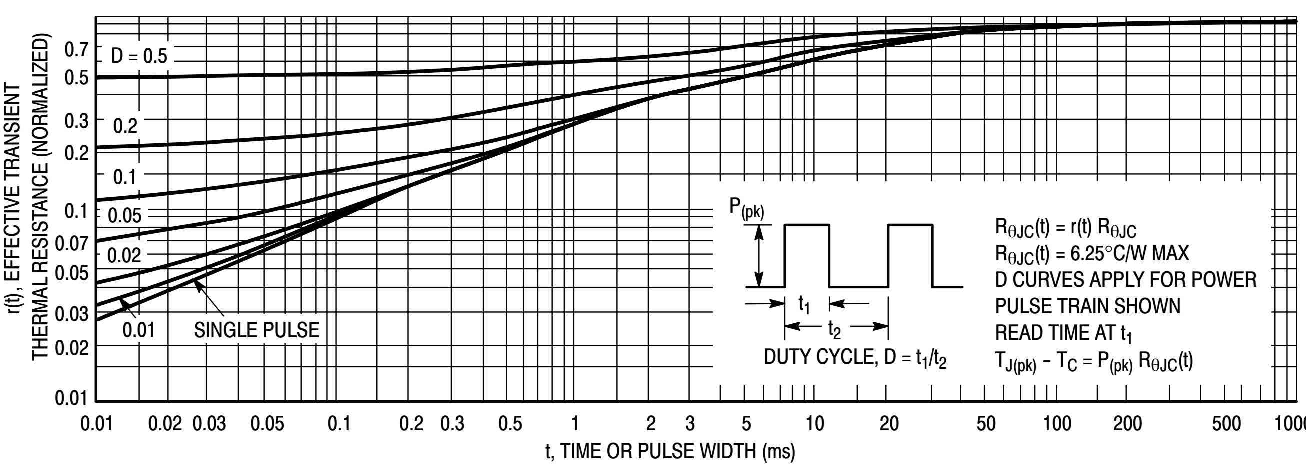


Figure 10. Thermal Response

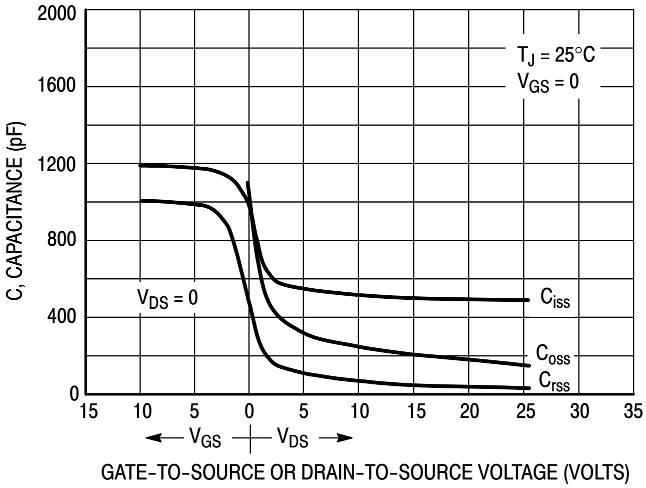


Figure 11. Capacitance Variation

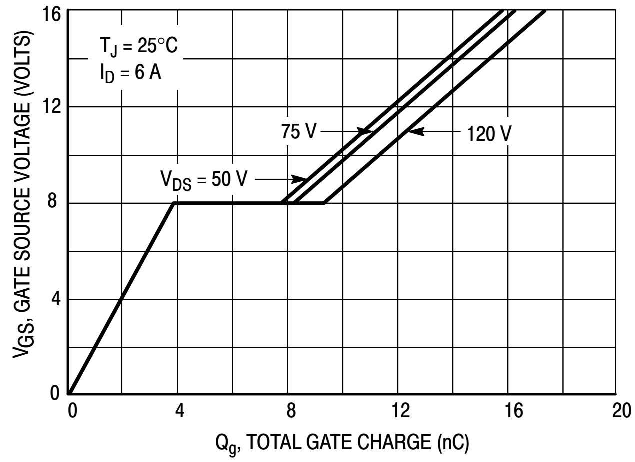


Figure 12. Gate Charge versus Gate−To−Source Voltage

RESISTIVE SWITCHING

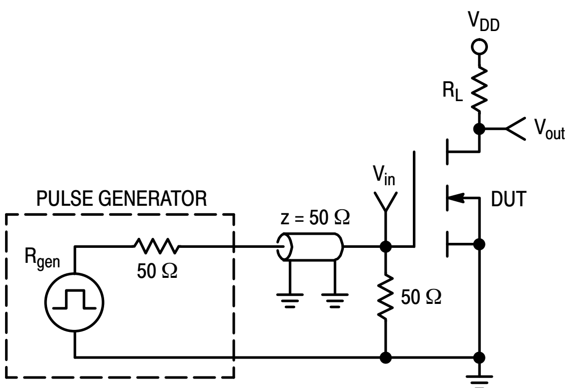


Figure 13. Switching Test Circuit

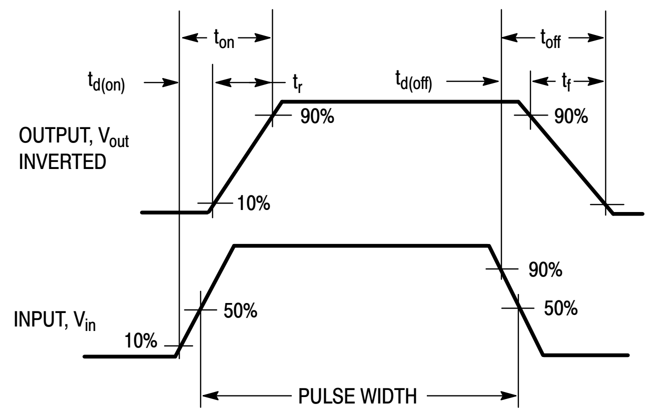
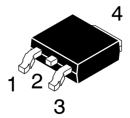


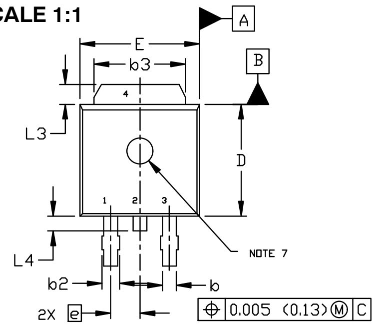
Figure 14. Switching Waveforms



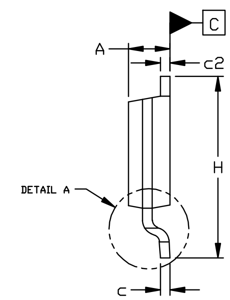
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

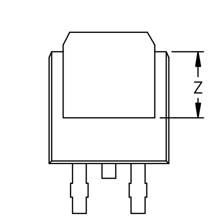


SIDE VIEW

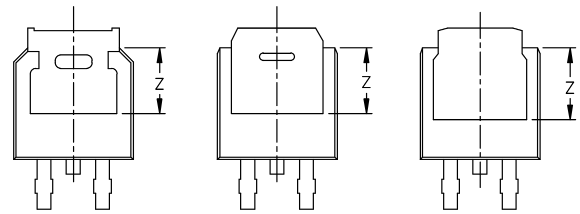
NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

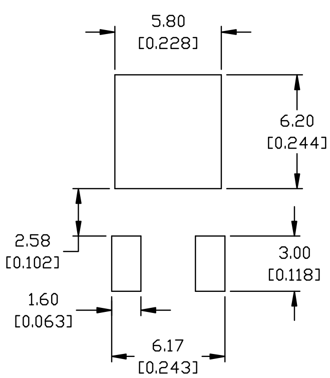


BOTTOM VIEW



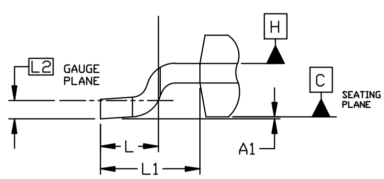
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



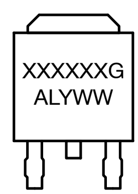
RECOMMENDED MOUNTING FOOTPRINT*

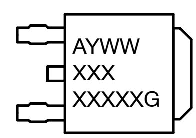
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL A
ROTATED 90° CW

GENERIC
MARKING DIAGRAM*





IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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