

# MTM23123

## Silicon P-channel MOSFET

For digital circuits

### ■ Features

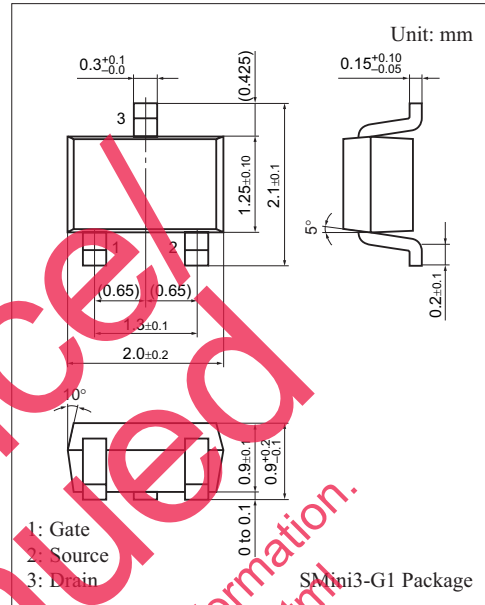
- Low voltage drive (2.5 V, 4 V)
- Realization of low on-resistance, using extremely fine process

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	$V_{DSS}$	-20	V
Gate-source surrender voltage	$V_{GSS}$	$\pm 10$	V
Drain current	$I_D$	-3.0	A
Peak drain current *1	$I_{DP}$	-16	A
Power dissipation *2	$P_D$	500	mW
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

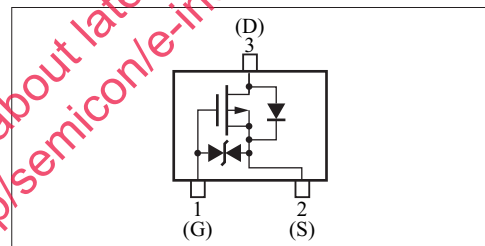
Note) \*1: Pulse width  $\leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2: Measuring on ceramic substrate at  $40 \text{ mm} \times 38 \text{ mm} \times 0.1 \text{ mm}$   
 Absolute maximum rating without heat sink for  $P_D$  is 150 mW



Marking Symbol: BL

Internal Connection



### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

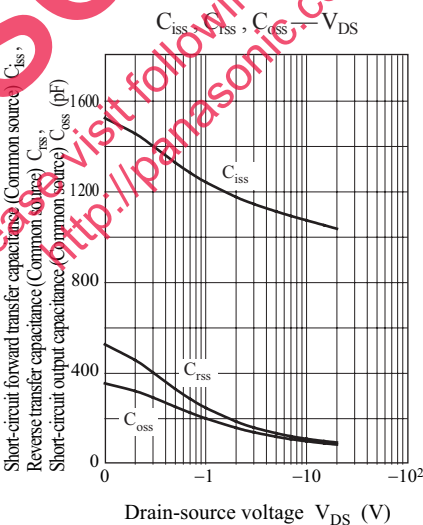
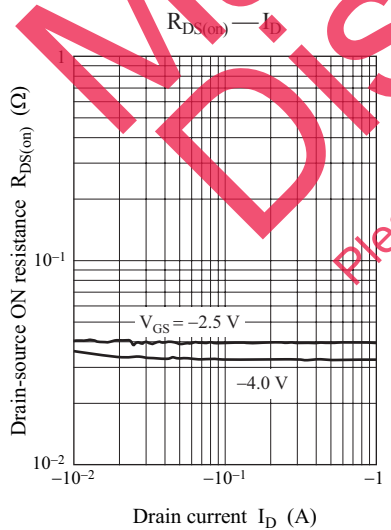
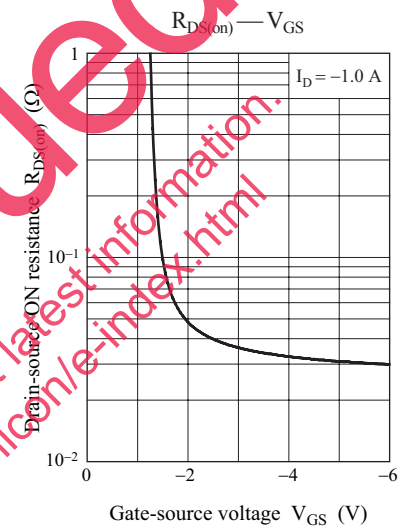
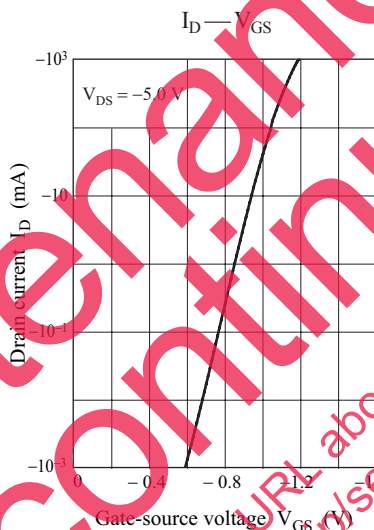
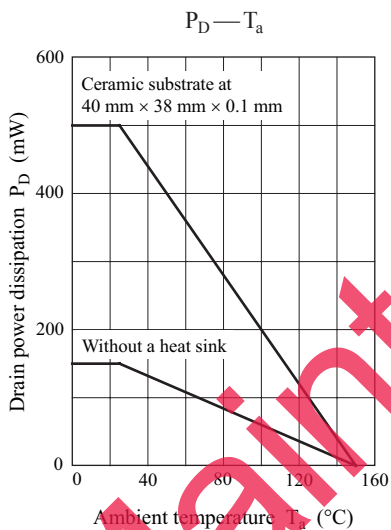
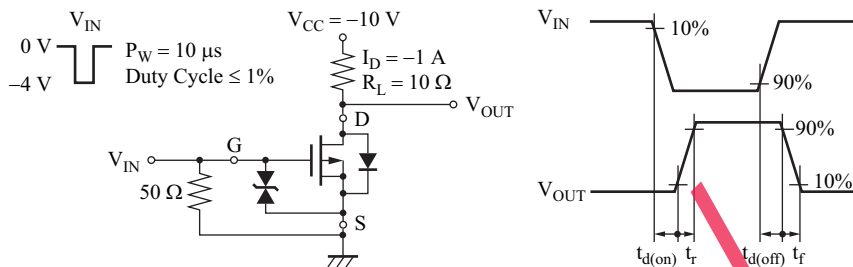
Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Drain-source surrender voltage	$V_{DSS}$	$I_D = -1 \text{ mA}$ , $V_{GS} = 0$	-20			V	
Drain-source cutoff current	$I_{DSS}$	$V_{DS} = -20 \text{ V}$ , $V_{GS} = 0$			-1.0	$\mu\text{A}$	
Gate-source cutoff current	$I_{GSS}$	$V_{GS} = \pm 8 \text{ V}$ , $V_{DS} = 0$			$\pm 10$	$\mu\text{A}$	
Gate threshold voltage	$V_{TH}$	$I_D = -1.0 \text{ mA}$ , $V_{DS} = -10.0 \text{ V}$	-0.4	-0.85	-1.3	V	
Drain-source ON resistance *1	$R_{DS(on)}$	$I_D = -1 \text{ A}$ , $V_{GS} = -4.0 \text{ V}$		40	55	m $\Omega$	
		$I_D = -0.5 \text{ A}$ , $V_{GS} = -2.5 \text{ V}$		45	70		
Forward transfer admittance *1	$ Y_{fs} $	$I_D = -1.0 \text{ A}$ , $V_{DS} = -10 \text{ V}$ , $f = 1 \text{ kHz}$	3.5			S	
Short-circuit forward transfer capacitance (Common source)	$C_{iss}$	$V_{DS} = -10 \text{ V}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$		1000		pF	
Short-circuit output capacitance (Common source)	$C_{oss}$				120		pF
Reverse transfer capacitance (Common source)	$C_{rss}$				120		pF
Turn-on delay time *2	$t_{d(on)}$	$V_{DD} = -10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ to $-4 \text{ V}$ , $I_D = -1 \text{ A}$		25		ns	
Rise time *2	$t_r$	$V_{DD} = -10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ to $-4 \text{ V}$ , $I_D = -1 \text{ A}$		25		ns	
Fall time *2	$t_f$	$V_{DD} = -10 \text{ V}$ , $V_{GS} = -4 \text{ V}$ to $0 \text{ V}$ , $I_D = -1 \text{ A}$		70		ns	
Turn-off delay time *2	$t_{d(off)}$	$V_{DD} = -10 \text{ V}$ , $V_{GS} = -4 \text{ V}$ to $0 \text{ V}$ , $I_D = -1 \text{ A}$		120		ns	

■ Electrical Characteristics (continued)  $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*1: Pulse measurement: Pulse width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

\*2: Measurement circuit



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