



THE DATASHEET OF 2SK3065T100

Small switching (60V, 2A)

2SK3065

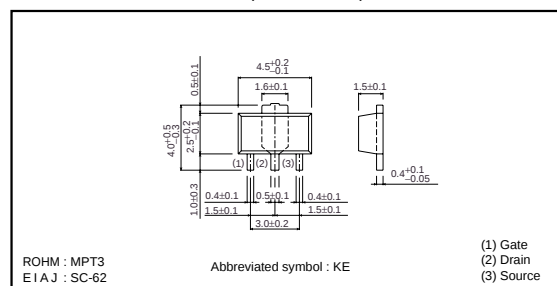
●Features

- 1) Low on resistance.
- 2) High-speed switching.
- 3) Optimum for a pocket resource etc. because of undervoltage actuation (2.5V actuation).
- 4) Driving circuit is easy.
- 5) Easy to use parallel.
- 6) It is strong to an electrostatic discharge.

●Structure

Silicon N-channel
MOS FET transistor

●External dimensions (Units : mm)



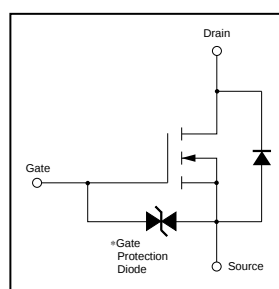
●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Drain current	Continuous	I_D	2
	Pulsed	I_{DP}^{*1}	8
Reverse drain current	Continuous	I_{DR}	2
	Pulsed	I_{DRP}^{*1}	8
Total power dissipation (Tc=25°C)	P_D	$\frac{0.5}{2^{*2}}$	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55~+150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 When mounted on a $40 \times 40 \times 0.7$ mm alumina board.

●Internal equivalent circuit



* A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	0.8	—	1.5	V	$V_{DS} = 10V, I_D = 1mA$
Static drain-source on-state resistance	$R_{DS(on)}$	—	0.25	0.32	Ω	$I_D = 1A, V_{GS} = 4V$
	$R_{DS(on)}$	—	0.35	0.45	Ω	$I_D = 1A, V_{GS} = 2.5V$
Forward transfer admittance	$ Y_{fs} $	1.5	—	—	S	$I_D = 1A, V_{DS} = 10V$
Input capacitance	C_{iss}	—	160	—	pF	$V_{DS} = 10V$
Output capacitance	C_{oss}	—	85	—	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	—	25	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$I_D = 1A, V_{DD} \approx 30V$
Rise time	t_r	—	50	—	ns	$V_{GS} = 4V$
Turn-off delay time	$t_{d(off)}$	—	120	—	ns	$R_L = 30\Omega$
Fall time	t_f	—	70	—	ns	$R_G = 10\Omega$

* $P_w \leq 300\mu s$, Duty cycle $\leq 1\%$

Type	Package	Taping
	Code	T100
	Basic ordering unit (pieces)	1000
2SK3065		○

When mounted on a 40 x 40 x 0.7 mm aluminum-ceramic board.

The graph shows the relationship between total power dissipation and ambient temperature for the 40 x 40 x 0.7 mm aluminum-ceramic board. The y-axis represents Total Power Dissipation in Watts (W), ranging from 0 to 3. The x-axis represents Ambient Temperature in degrees Celsius (°C), ranging from 0 to 175. Two lines are plotted: a solid line for the maximum power dissipation and a dashed line for the recommended power dissipation. Both lines show a linear decrease in power dissipation as ambient temperature increases, starting from a constant value at 25°C and reaching zero at 150°C.

Ambient Temperature (T_a) (°C)	Maximum Power Dissipation (W)	Recommended Power Dissipation (W)
0	2.0	0.5
25	2.0	0.5
50	1.6	0.4
75	1.2	0.3
100	0.8	0.2
125	0.4	0.1
150	0.0	0.0
175	0.0	0.0

Figure 10 is a graph showing the Pulsed Drain Current (I_d) versus Drain-Source Voltage (V_{ds}) for the device. The Y-axis represents Drain Current: I_d (A), ranging from 0 to 2. The X-axis represents Drain-Source Voltage: V_{ds} (V), ranging from 0 to 10. The graph includes curves for $V_{gs} = 1.5V$ and $T_a = 25^\circ C$. The curves are labeled with V_{ds} values: 2.5V, 3V, 3.5V, 4V, and 2V. The 2V curve shows a significant increase in current with V_{ds} , while the others are nearly flat.

Figure 10 is a line graph showing the relationship between Gate Threshold Voltage (V_{th}) and Channel Temperature (T_{ch}) for a MOSFET at $V_{ds}=10V$. The Y-axis represents V_{th} in Volts (V), ranging from 0 to 4. The X-axis represents T_{ch} in degrees Celsius ($^{\circ}C$), ranging from -50 to 150. Two curves are plotted: one for $I_d=10mA$ and one for $I_d=1mA$. Both curves show a decrease in V_{th} as T_{ch} increases. The $I_d=10mA$ curve is consistently higher than the $I_d=1mA$ curve.

Channel Temperature (T_{ch}) [$^{\circ}C$]	V_{th} (V) at $I_d=10mA$	V_{th} (V) at $I_d=1mA$
-25	~1.4	~1.3
0	~1.3	~1.2
25	~1.2	~1.1
50	~1.1	~1.0
75	~1.0	~0.9
100	~0.9	~0.8
125	~0.8	~0.7

Figure 10 is a log-log plot showing the relationship between Static Drain-Source On-State Resistance ($R_{DS(on)}$) and Drain Current (I_D) for the 75°C, 25°C, and -25°C temperature conditions. The y-axis is labeled "STATIC DRAIN-SOURCE ON-STATE RESISTANCE : $R_{DS(on)}(\Omega)$ " and ranges from 0.1 to 10. The x-axis is labeled "DRAIN CURRENT : $I_D(A)$ " and ranges from 0.01 to 10. The plot shows that resistance decreases as current increases and as temperature decreases. A legend indicates $V_{GS}=4V$ and Pulsed conditions.

Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(I)

Transistors

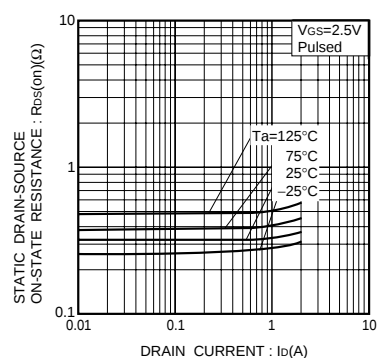


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(I)

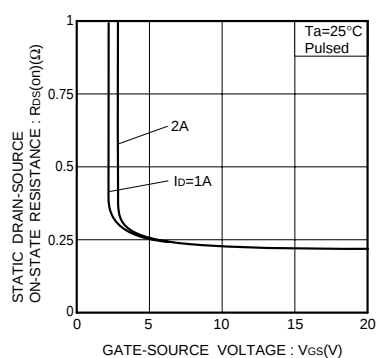


Fig.8 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

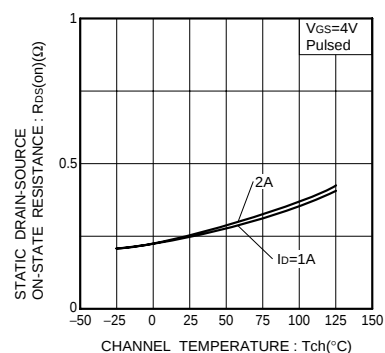


Fig.9 Static Drain-Source On-State Resistance vs. Channel Temperature

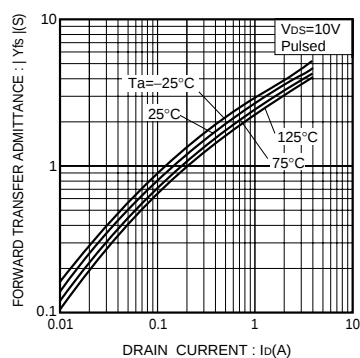


Fig.10 Forward Transfer Admittance vs. Drain Current

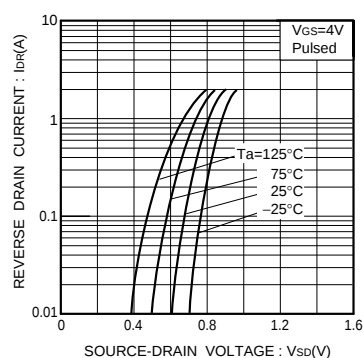


Fig.11 Reverse Drain Current vs. Source-Drain Voltage(I)

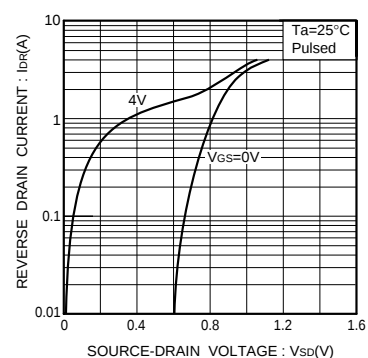


Fig.12 Reverse Drain Current vs. Source-Drain Voltage(II)

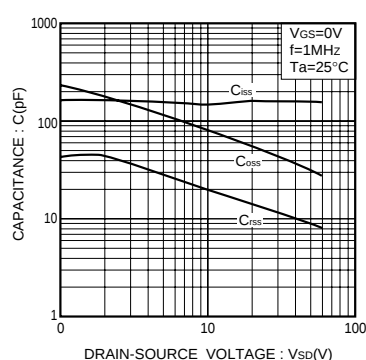


Fig.13 Typical Capacitance vs. Drain-Source Voltage

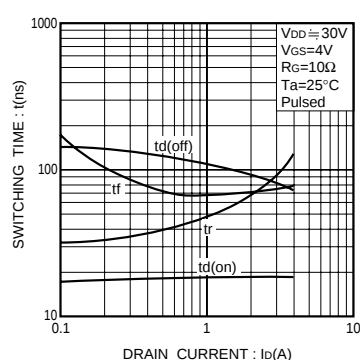


Fig.14 Switching Characteristics
(a measurement circuit diagram Fig.17, it refers 18 times)

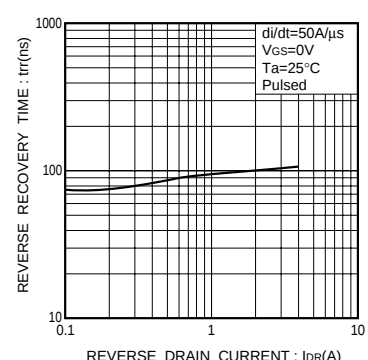


Fig.15 Reverse Recovery Time vs. Reverse Drain Current

Transistors

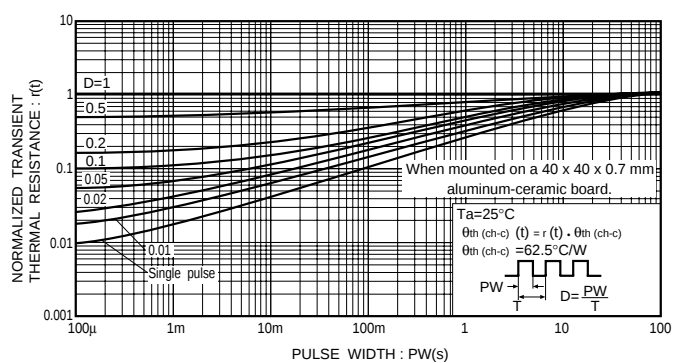


Fig.16 Normalized Transient Thermal Resistance vs. Pulse Width

● Switching characteristics measurement circuit

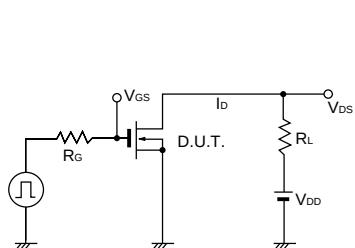


Fig.17 Switching Time Test Circuit

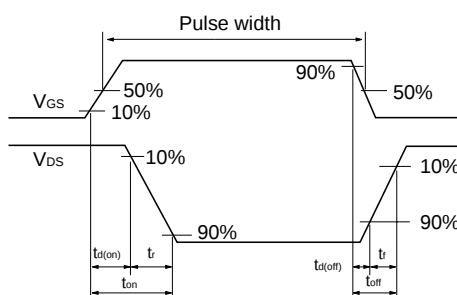


Fig.18 Switching Time Waveforms

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