THE DATASHEET OF

NAND512W3A2BZA6

NAND128-A, NAND256-A
NAND512-A, NAND01G-A

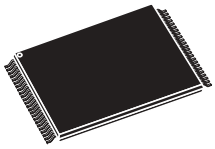
128 Mbit, 256 Mbit, 512 Mbit, 1 Gbit (x8/x16)
528 Byte/264 Word Page, 1.8V/3V, NAND Flash Memories

PRELIMINARY DATA

FEATURES SUMMARY

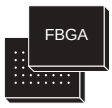
- HIGH DENSITY NAND FLASH MEMORIES
  - Up to 1 Gbit memory array
  - Up to 32 Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND INTERFACE
  - x8 or x16 bus width
  - Multiplexed Address/ Data
  - Pinout compatibility for all densities
- SUPPLY VOLTAGE
  - 1.8V device: V_{DD} = 1.7 to 1.95V
  - 3.0V device: V_{DD} = 2.7 to 3.6V
- PAGE SIZE
  - x8 device: (512 + 16 spare) Bytes
  - x16 device: (256 + 8 spare) Words
- BLOCK SIZE
  - x8 device: (16K + 512 spare) Bytes
  - x16 device: (8K + 256 spare) Words
- PAGE READ / PROGRAM
  - Random access: 12µs (max)
  - Sequential access: 50ns (min)
  - Page program time: 200µs (typ)
- COPY BACK PROGRAM MODE
  - Fast page copy without external buffering
- FAST BLOCK ERASE
  - Block erase time: 2ms (Typ)
- STATUS REGISTER
- ELECTRONIC SIGNATURE
- CHIP ENABLE 'DON'T CARE' OPTION
  - Simple interface with microcontroller
- AUTOMATIC PAGE 0 READ AT POWER-UP OPTION
  - Boot from NAND support
  - Automatic Memory Download
- SERIAL NUMBER OPTION

Figure 1. Packages



TSOP48 12 x 20mm

WSOP48 12 x 17 x 0.65mm



VFBGA55 8 x 10 x 1mm
TFBGA55 8 x 10 x 1.2mm
VFBGA63 8.5 x 15 x 1mm
TFBGA63 8.5 x 15 x 1.2mm

- HARDWARE DATA PROTECTION
  - Program/Erase locked during Power transitions
- DATA INTEGRITY
  - 100,000 Program/Erase cycles
  - 10 years Data Retention
- DEVELOPMENT TOOLS
  - Error Correction Code software and hardware models
  - Bad Blocks Management and Wear Leveling algorithms
  - PC Demo board with simulation software
  - File System OS Native reference software
  - Hardware simulation models

Table 1. Product List

Reference	Part Number
NAND128-A	NAND128R3A
	NAND128W3A
	NAND1282R4A
	NAND128W4A
NAND256-A	NAND256R3A
	NAND256W3A
	NAND256R4A
	NAND256W4A
NAND512-A	NAND512R3A
	NAND512W3A
	NAND512R4A
	NAND512W4A
NAND01G-A	NAND01GR3A
	NAND01GW3A
	NAND01GR4A
	NAND01GW4A

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The NAND Flash 528 Byte/ 264 Word Page is a family of non-volatile Flash memories that uses NAND cell technology. The devices range from 128Mbits to 1Gbit and operate with either a 1.8V or 3V voltage supply. The size of a Page is either 528 Bytes (512 + 16 spare) or 264 Words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 or x16 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC). A Write Protect pin is available to give a hardware protection against program and erase operations.

The devices feature an open-drain Ready/Busy output that can be used to identify if the Program/ Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/ Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back command is available to optimize the management of defective blocks. When a Page Program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

The devices are available in the following packages:

- TSOP48 12 x 20mm for all products
- WSOP48 12 x 17 x 0.65mm for 128Mb, 256Mb and 512Mb products
- VFBGA55 (8 x 10 x 1mm, 6 x 8 ball array, 0.8mm pitch) for 128Mb and 256Mb products
- TFBGA55 (8 x 10 x 1.2mm, 6 x 8 ball array, 0.8mm pitch) for 512Mb Dual Die product
- VFBGA63 (8.5 x 15 x 1mm, 6 x 8 ball array, 0.8mm pitch) for the 512Mb product
- TFBGA63 (8.5 x 15 x 1.2mm, 6 x 8 ball array, 0.8mm pitch) for the 1Gb Dual Die product

Three options are available for the NAND Flash family:

- Automatic Page 0 Read after Power-up, which allows the microcontroller to directly download the boot code from page 0.
- Chip Enable Don't Care, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation.
- A Serial Number, which allows each device to be uniquely identified. The Serial Number options is subject to an NDA (Non Disclosure Agreement) and so not described in the datasheet. For more details of this option contact your nearest ST Sales office.

For information on how to order these options refer to Table 28., Ordering Information Scheme. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See Table 2., Product Description, for all the devices available in the family.

Table 2. Product Description

Reference	Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings				Package
								Random Access Max	Sequential Access Min	Page Program Typical	Block Erase Typical	
NAND128-A	NAND128R3A	128Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 1024 Blocks	1.7 to 1.95V	10µs	60ns	200µs	2ms	TSOP48 WSOP48 VFBGA55
	NAND128W3A						2.7 to 3.6V	10µs	50ns	200µs		
	NAND128R4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	10µs	60ns	200µs		
	NAND128W4A						2.7 to 3.6V	10µs	50ns	200µs		
NAND256-A	NAND256R3A	256Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 2048 Blocks	1.7 to 1.95V	10µs	60ns	200µs	2ms	TSOP48 WSOP48 VFBGA55
	NAND256W3A						2.7 to 3.6V	10µs	50ns	200µs		
	NAND256R4A		x16	256+8 Words	8K+256 Words		1.7to 1.95V	10µs	60ns	200µs		
	NAND256W4A						2.7 to 3.6V	10µs	50ns	200µs		
NAND512-A	NAND512R3A	512Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 4096 Blocks	1.7to 1.95V	10µs	60ns	200µs	2ms	TFBGA55
	NAND512W3A						2.7 to 3.6V	10µs	50ns	200µs		
	NAND512R4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	10µs	60ns	200µs		
	NAND512W4A						2.7 to 3.6V	10µs	50ns	200µs		
NAND512-A	NAND512R3A	512Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 4096 Blocks	1.7to 1.95V	15µs	60ns	200µs	2ms	TSOP48 WSOP48 VFBGA63
	NAND512W3A						2.7 to 3.6V	12µs	50ns	200µs		
	NAND512R4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	15µs	60ns	200µs		
	NAND512W4A						2.7 to 3.6V	12µs	50ns	200µs		
NAND01G-A	NAND01GR3A	1Gbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 8192 Blocks	1.7 to 1.95V	15µs	60ns	200µs	2ms	TSOP48 TFBGA63
	NAND01GW3A						2.7 to 3.6V	12µs	50ns	200µs		
	NAND01GR4A		x16	256+8 Words	8K+256 Words		1.7 to 1.95V	15µs	60ns	200µs		
	NAND01GW4A						2.7 to 3.6V	12µs	50ns	200µs		

Figure 2. Logic Diagram

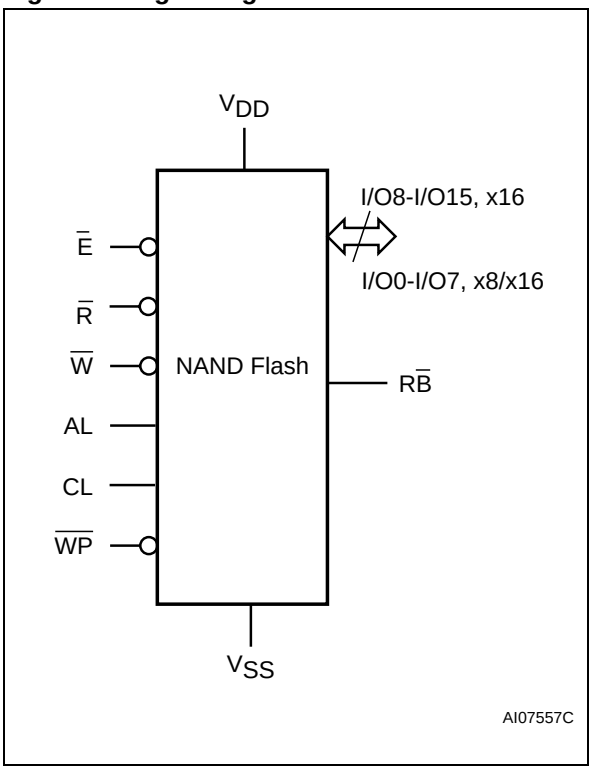


Table 3. Signal Names

I/O8-15	Data Input/Outputs for x16 devices
I/O0-7	Data Input/Outputs, Address Inputs, or Command Inputs for x8 and x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}$	Chip Enable
$\overline{R}$	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
V_{DD}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use

Figure 3. Logic Block Diagram

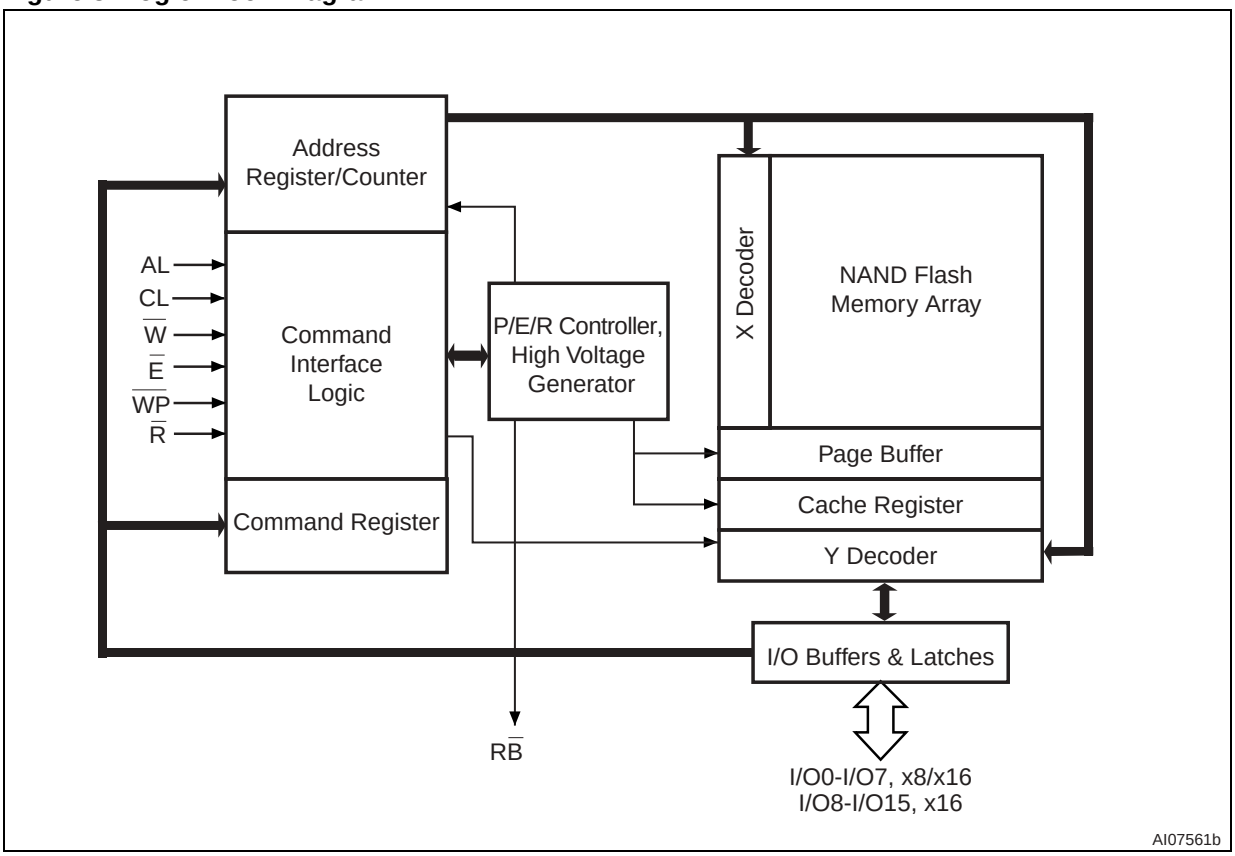


Figure 4. TSOP48 and WSOP48 Connections, x8 devices

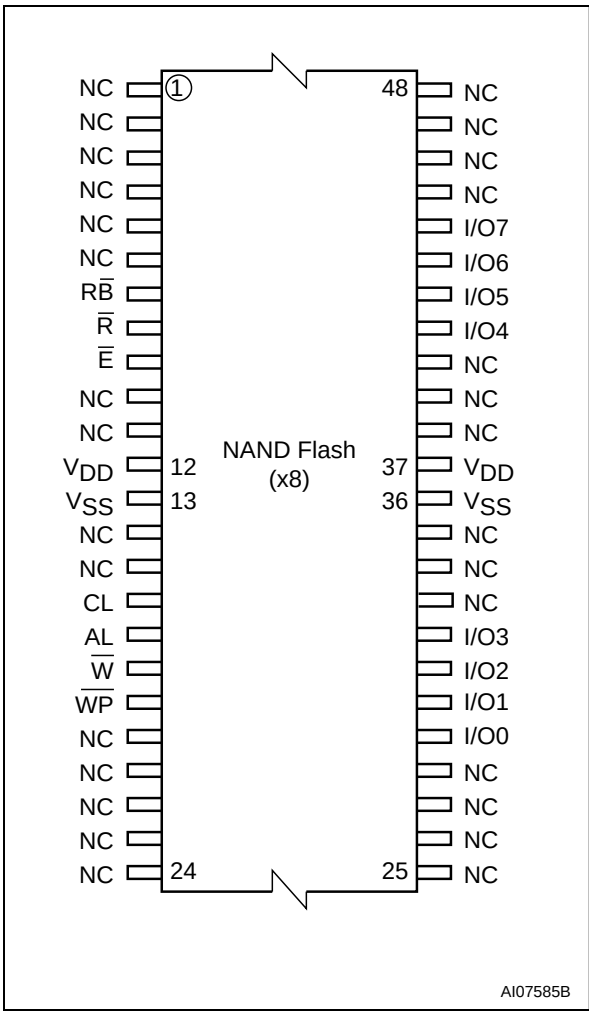


Figure 5. TSOP48 and WSOP48 Connections, x16 devices

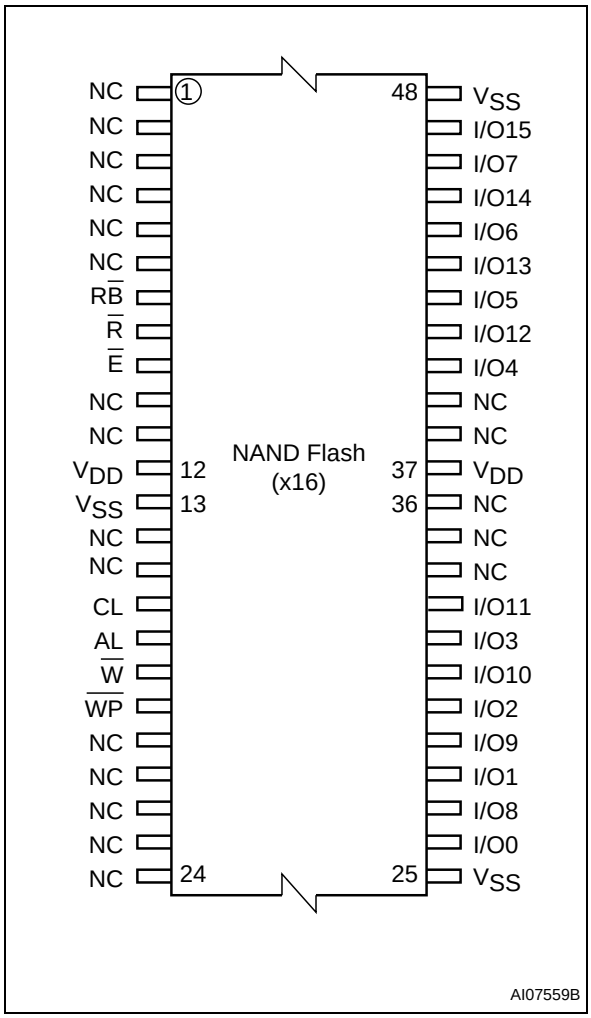


Figure 6. FBGA55 Connections, x8 devices (Top view through package)

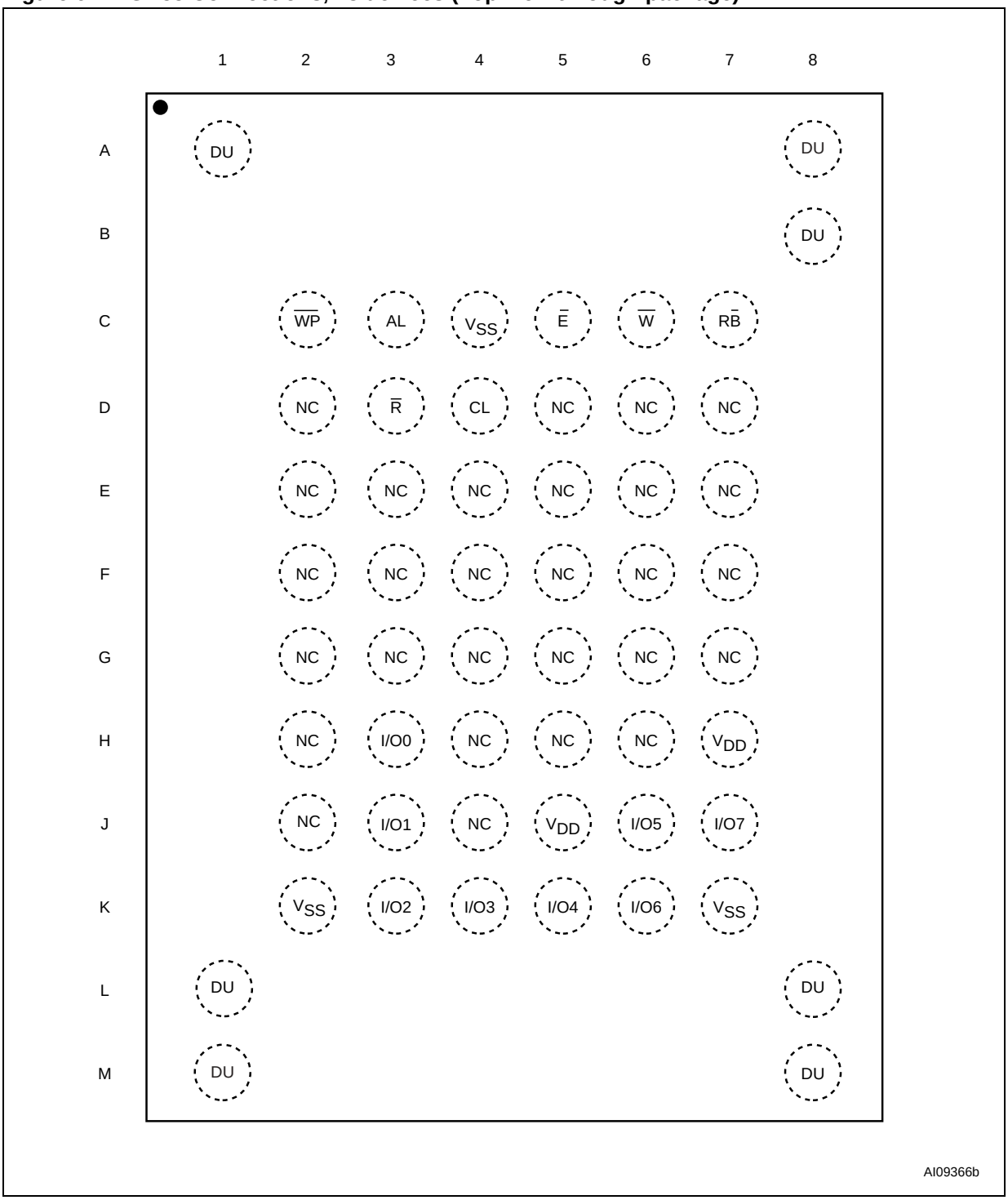


Figure 7. FBGA55 Connections, x16 devices (Top view through package)

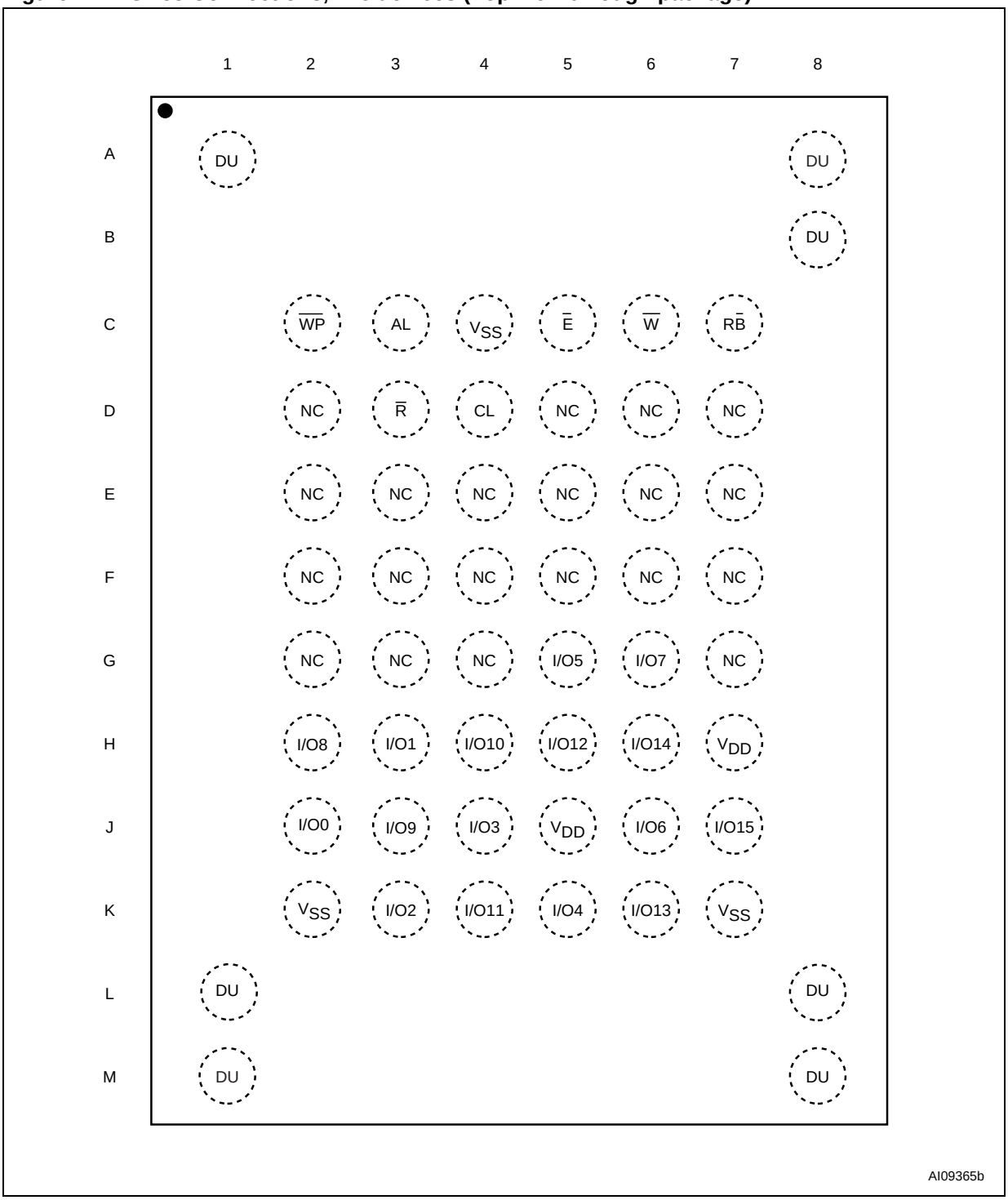


Figure 8. FBGA63 Connections, x8 devices (Top view through package)

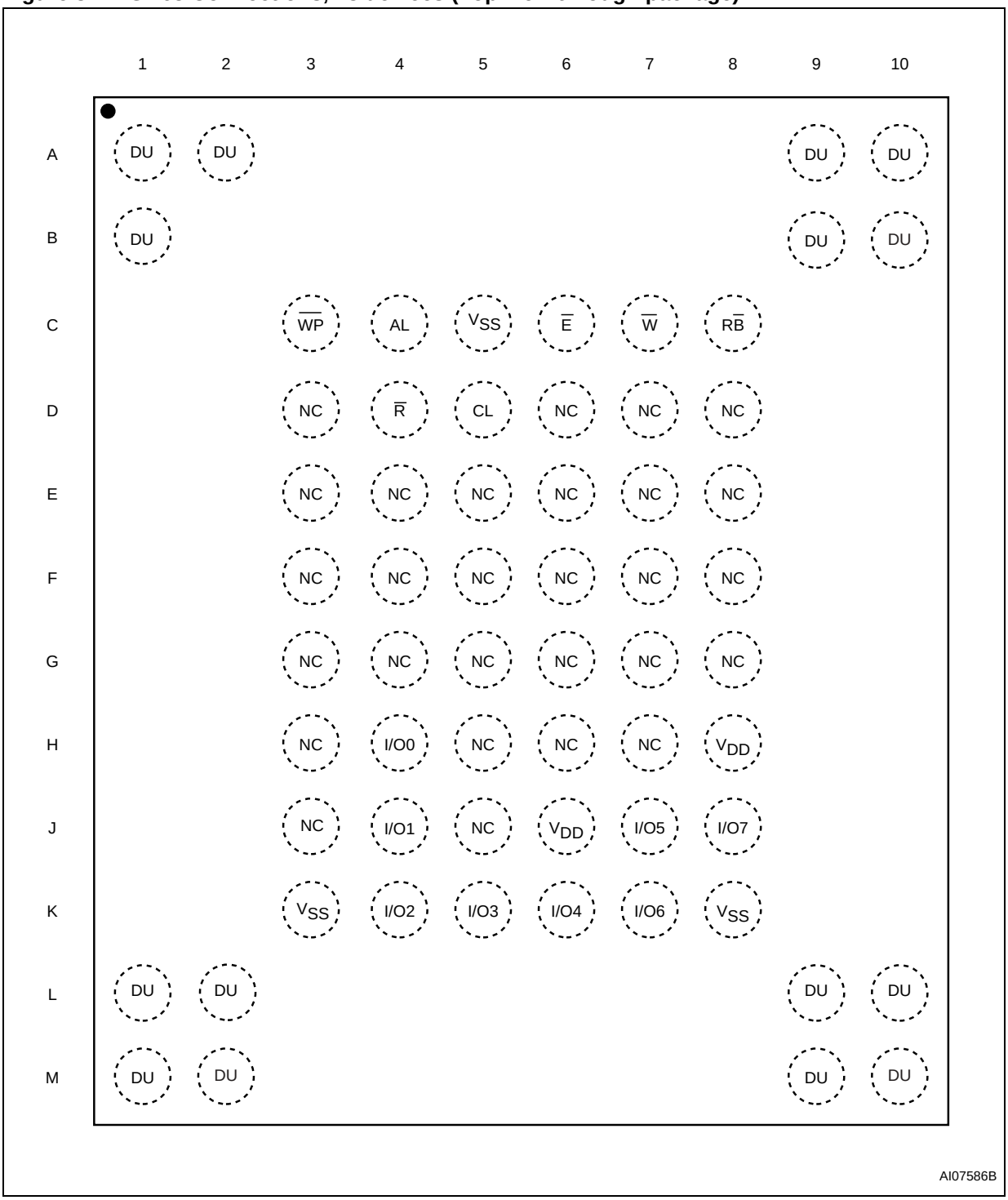
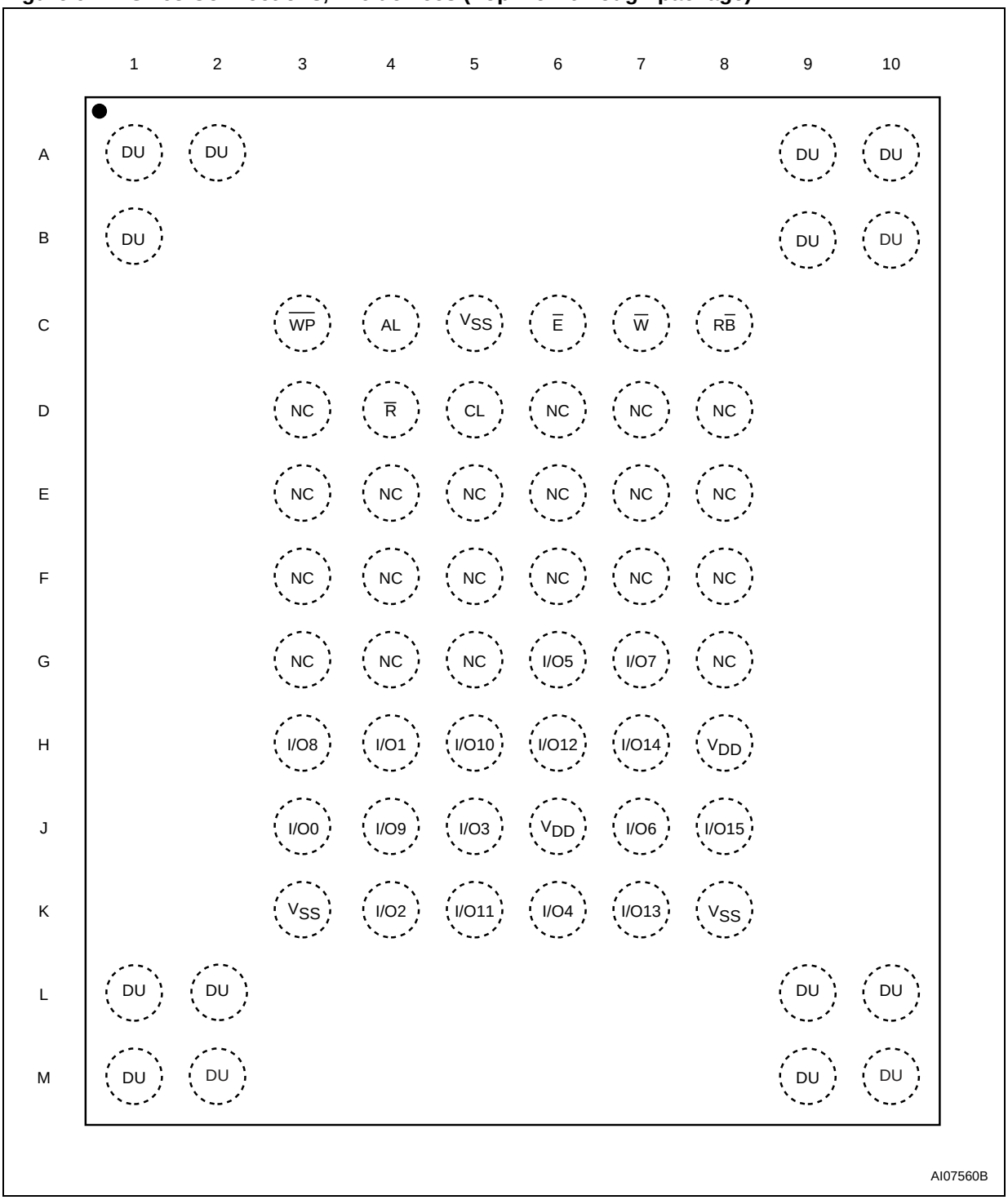


Figure 9. FBGA63 Connections, x16 devices (Top view through package)



MEMORY ARRAY ORGANIZATION

The memory array is made up of NAND structures where 16 cells are connected in series.

The memory array is organized in blocks where each block contains 32 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store Error correction Codes, software flags or Bad Block identification.

In x8 devices the pages are split into a main area with two half pages of 256 Bytes each and a spare area of 16 Bytes. In the x16 devices the pages are split into a 256 Word main area and an 8 Word spare area. Refer to Figure 10., Memory Array Organization.

Bad Blocks

The NAND Flash 528 Byte/ 264 Word Page devices may contain Bad Blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional Bad Blocks may develop during the lifetime of the device.

The Bad Block Information is written prior to shipping (refer to Bad Block Management section for more details).

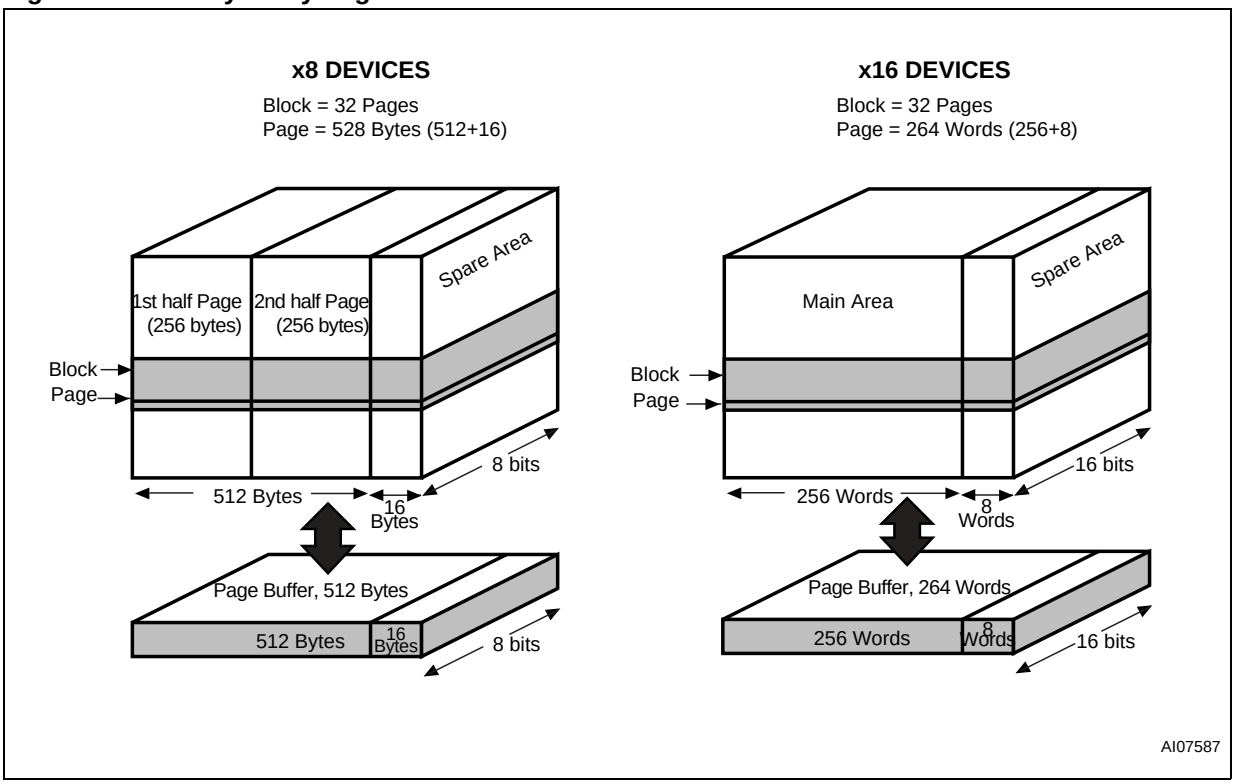
Table 4. shows the minimum number of valid blocks in each device. The values shown include both the Bad Blocks that are present when the device is shipped and the Bad Blocks that could develop later on.

These blocks need to be managed using Bad Blocks Management, Block Replacement or Error Correction Codes (refer to SOFTWARE ALGORITHMS section).

Table 4. Valid Blocks

Density of Device	Min	Max
1Gbit	8032	8192
512Mbits	4016	4096
256Mbits	2008	2048
128Mbits	1004	1024

Figure 10. Memory Array Organization



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 3., Signal Names, for a brief overview of the signals connected to this device.

Inputs/Outputs (I/O0-I/O7). Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

Inputs/Outputs (I/O8-I/O15). Input/Outputs 8 to 15 are only available in x16 devices. They are used to output the data during a Read operation or input data during a Write operation. Command and Address Inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

Address Latch Enable (AL). The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

Command Latch Enable (CL). The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes high, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

When the device is executing a Sequential Row Read operation, Chip Enable must be held low (from the second page read onwards) during the time that the device is busy (t_{BLBH1}). If Chip Enable goes high during t_{BLBH1} the operation is aborted.

Read Enable ($\overline{R}$). The Read Enable, $\overline{R}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 1µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

Write Protect ($\overline{WP}$). The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

Ready/Busy ($\overline{RB}$). The Ready/Busy output, $\overline{RB}$, is an open-drain output that can be used to identify if the P/E/R Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the Ready/Busy Signal Electrical Characteristics section for details on how to calculate the value of the pull-up resistor.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below 2.5V (for 3V devices) or 1.5V (for 1.8V devices) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents

V_{SS} Ground. Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

BUS OPERATIONS

There are six standard bus operations that control the memory. Each of these is described in this section, see Table 5., Bus Operations, for a summary.

Command Input

Command Input bus operations are used to give commands to the memory. Command are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See Figure 25. and Table 20. for details of the timings requirements.

Address Input

Address Input bus operations are used to input the memory address. Three bus cycles are required to input the addresses for the 128Mb and 256Mb devices and four bus cycles are required to input the addresses for the 512Mb and 1Gb devices (refer to Tables 6 and 7, Address Insertion).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See Figure 26. and Table 20. for details of the timings requirements.

Data Input

Data Input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See Figure 27. and Table 20. and Table 21. for details of the timings requirements.

Data Output

Data Output bus operations are used to read: the data in the memory array, the Status Register, the Electronic Signature and the Serial Number.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

See Figure 28. and Table 21. for details of the timings requirements.

Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

Standby

When Chip Enable is High the memory enters Standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus Operations

Bus Operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15(1)
Command Input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address Input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data Input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	X	Data Input	Data Input
Data Output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data Output	Data Output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	X	X	X

Note: 1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address Insertion, x8 Devices

Bus Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	A16	A15	A14	A13	A12	A11	A10	A9
3rd	A24	A23	A22	A21	A20	A19	A18	A17
4th(4)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A26	A25

Note: 1. A8 is set Low or High by the 00h or 01h Command, see Pointer Operations section.
2. Any additional address input cycles will be ignored.
3. The 4th cycle is only required for 512Mb and 1Gb devices.

Table 7. Address Insertion, x16 Devices

Bus Cycle	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	A16	A15	A14	A13	A12	A11	A10	A9
3rd	X	A24	A23	A22	A21	A20	A19	A18	A17
4th(4)	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A26	A25

Note: 1. A8 is Don't Care in x16 devices.
2. Any additional address input cycles will be ignored.
3. The 01h Command is not used in x16 devices.
4. The 4th cycle is only required for 512Mb and 1Gb devices.

Table 8. Address Definitions

Address	Definition
A0 - A7	Column Address
A9 - A26	Page Address
A9 - A13	Address in Block
A14 - A26	Block Address
A8	A8 is set Low or High by the 00h or 01h Command, and is Don't Care in x16 devices

COMMAND SET

All bus write operations to the device are interpreted by the Command Interface. The Commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The Commands are summarized in Table 9., Commands.

Table 9. Commands

Command	Bus Write Operations(1)			Command accepted during busy
	1st CYCLE	2nd CYCLE	3rd CYCLE	
Read A	00h	-	-	
Read B	01h(2)	-	-	
Read C	50h	-	-	
Read Electronic Signature	90h	-	-	
Read Status Register	70h	-	-	Yes
Page Program	80h	10h	-	
Copy Back Program	00h	8Ah	10h	
Block Erase	60h	D0h	-	
Reset	FFh	-	-	Yes

Note: 1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. Any undefined command sequence will be ignored by the device.

DEVICE OPERATIONS

Pointer Operations

As the NAND Flash memories contain two different areas for x16 devices and three different areas for x8 devices (see Figure 11.) the read command codes (00h, 01h, 50h) are used to act as pointers to the different areas of the memory array (they select the most significant column address).

The Read A and Read B commands act as pointers to the main memory area. Their use depends on the bus width of the device.

- In x16 devices the Read A command (00h) sets the pointer to Area A (the whole of the main area) that is Words 0 to 255.
- In x8 devices the Read A command (00h) sets the pointer to Area A (the first half of the main area) that is Bytes 0 to 255, and the Read B command (01h) sets the pointer to Area B (the second half of the main area) that is Bytes 256 to 511.

In both the x8 and x16 devices the Read C command (50h), acts as a pointer to Area C (the spare memory area) that is Bytes 512 to 527 or Words 256 to 263.

Once the Read A and Read C commands have been issued the pointer remains in the respective areas until another pointer code is issued. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A.

The pointer operations can also be used before a program operation, that is the appropriate code (00h, 01h or 50h) can be issued before the program command 80h is issued (see Figure 12.).

Figure 11. Pointer Operations

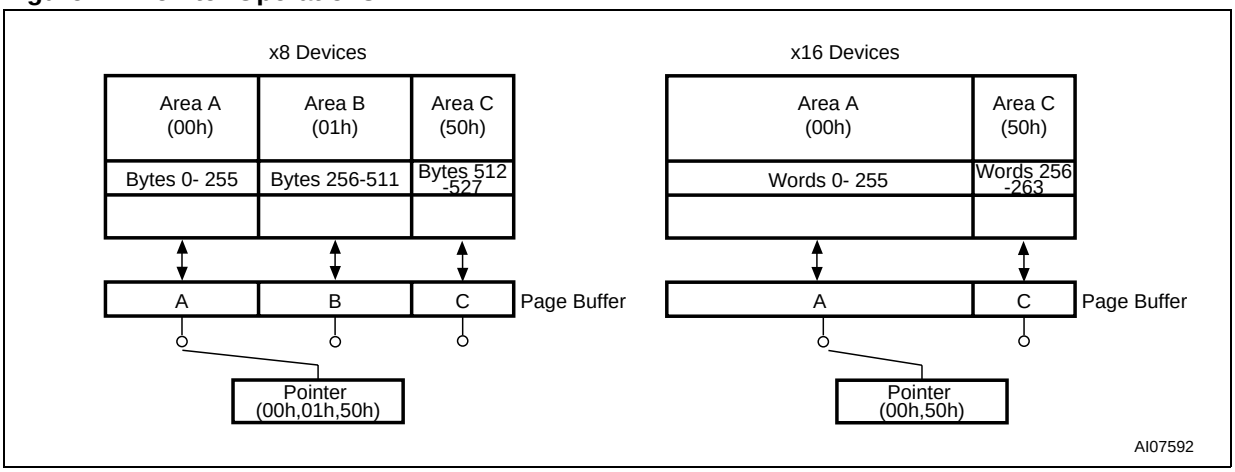
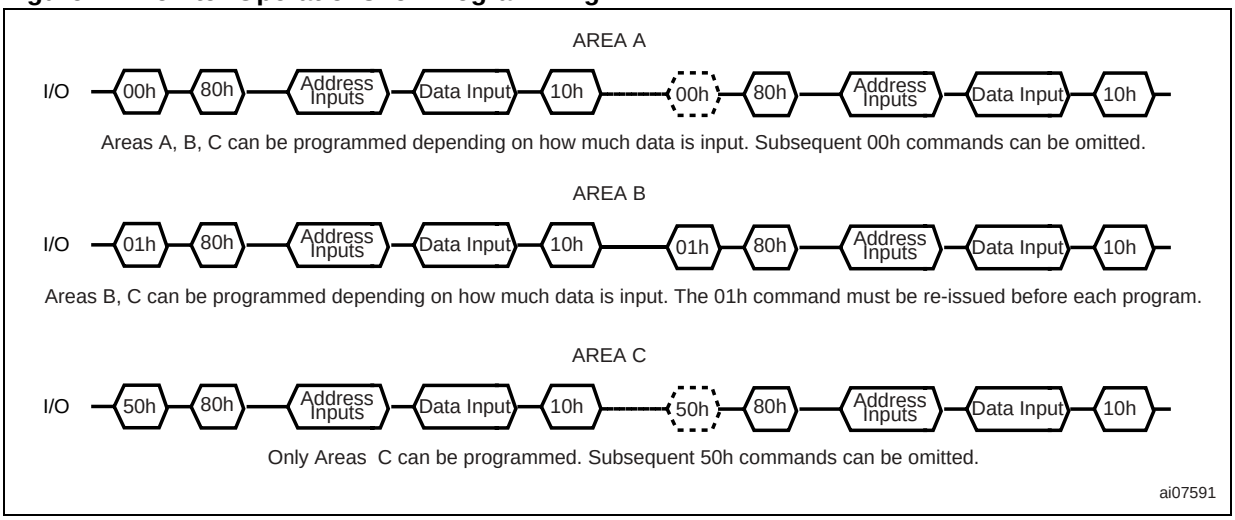


Figure 12. Pointer Operations for Programming



Read Memory Array

Each operation to read the memory area starts with a pointer operation as shown in the Pointer Operations section. Once the area (main or spare) has been selected using the Read A, Read B or Read C commands four bus cycles (for 512Mb and 1Gb devices) or three bus cycles (for 128Mb and 256Mb devices) are required to input the address (refer to Table 6.) of the data to be read.

The device defaults to Read A mode after power-up or a Reset operation. Devices, where page0 is read automatically at power-up, are available on request.

When reading the spare area addresses:

- A0 to A3 (x8 devices)
- A0 to A2 (x16 devices)

are used to set the start address of the spare area while addresses:

- A4 to A7 (x8 devices)
- A3 to A7 (x16 devices)

are ignored.

Once the Read A or Read C commands have been issued they do not need to be reissued for subsequent read operations as the pointer remains in the respective area. However, the Read B command is effective for only one operation, once an operation has been executed in Area B the pointer returns automatically to Area A and so another Read B command is required to start another read operation in Area B.

Once a read command is issued three types of operations are available: Random Read, Page Read and Sequential Row Read.

Random Read. Each time the command is issued the first read is Random Read.

Page Read. After the Random Read access the page data is transferred to the Page Buffer in a time of t_{WHBH} (refer to Table 21. for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

Sequential Row Read. After the data in last column of the page is output, if the Read Enable signal is pulsed and Chip Enable remains Low then the next page is automatically loaded into the Page Buffer and the read operation continues. A Sequential Row Read operation can only be used to read within a block. If the block changes a new read command must be issued.

Refer to Figure 15. and Figure 16. for details of Sequential Row Read operations.

To terminate a Sequential Row Read operation set the Chip Enable signal to High for more than t_{EHEL}.

Sequential Row Read is not available when the Chip Enable Don't Care option is enabled.

Figure 13. Read (A,B,C) Operations

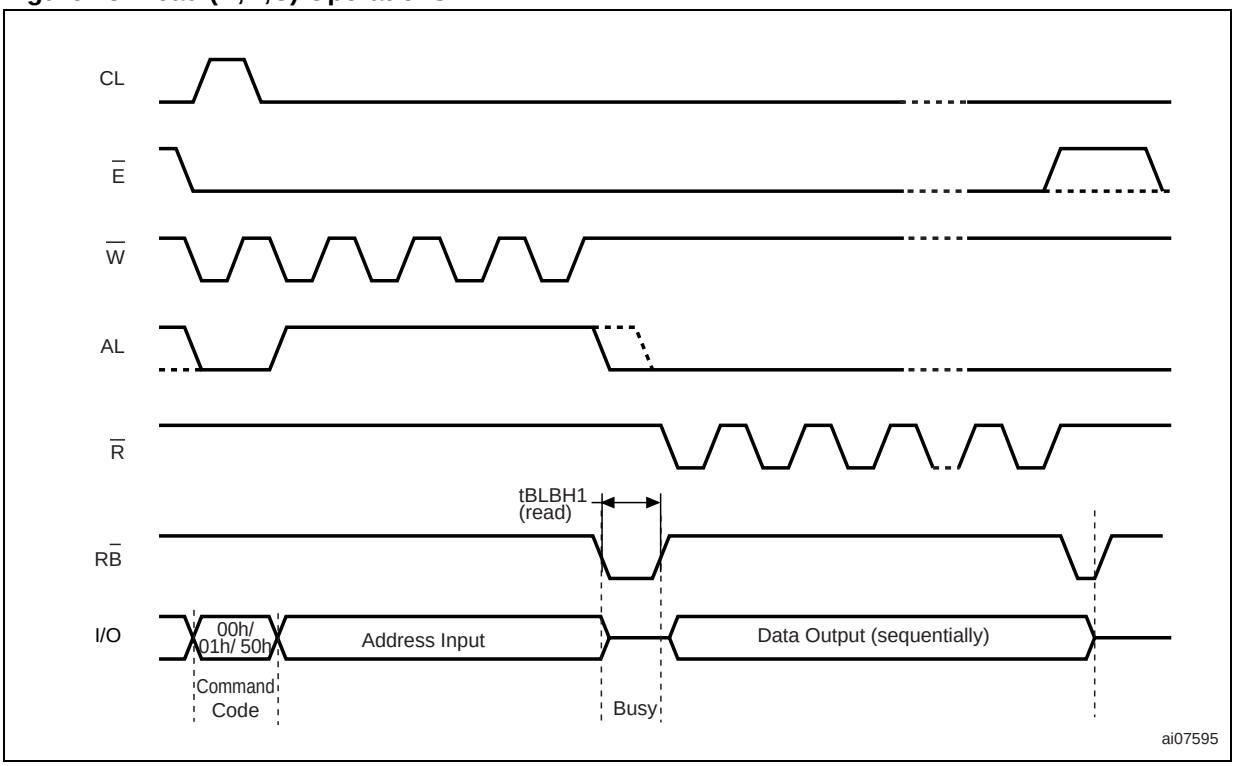
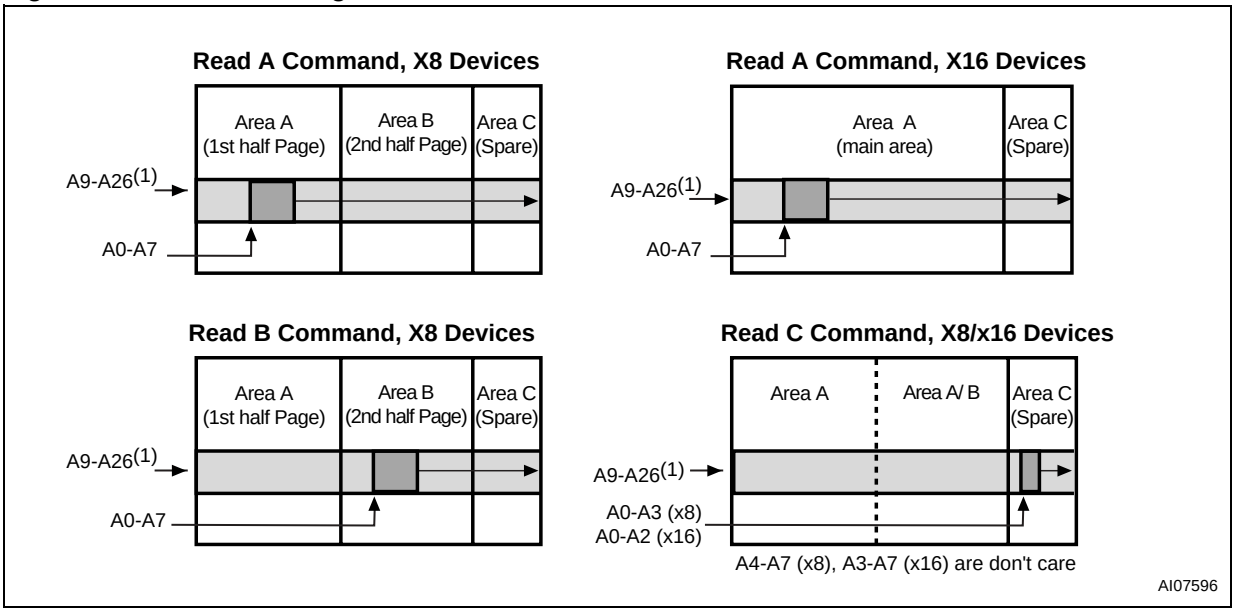


Figure 14. Read Block Diagrams



Note: 1. Highest address depends on device density.

Figure 15. Sequential Row Read Operations

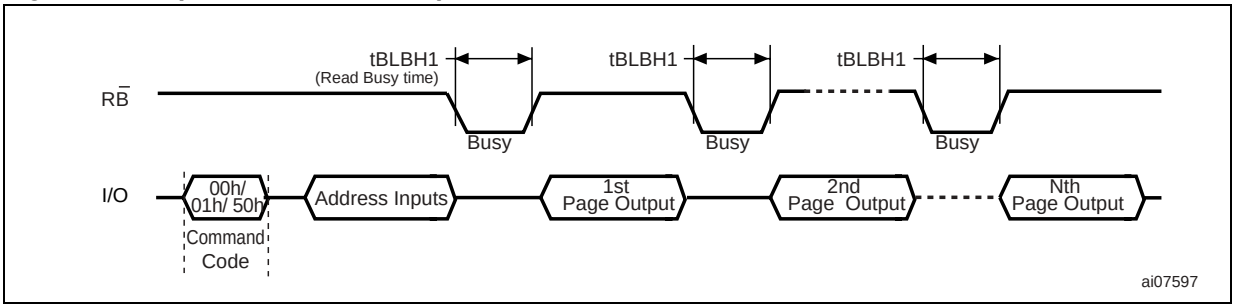
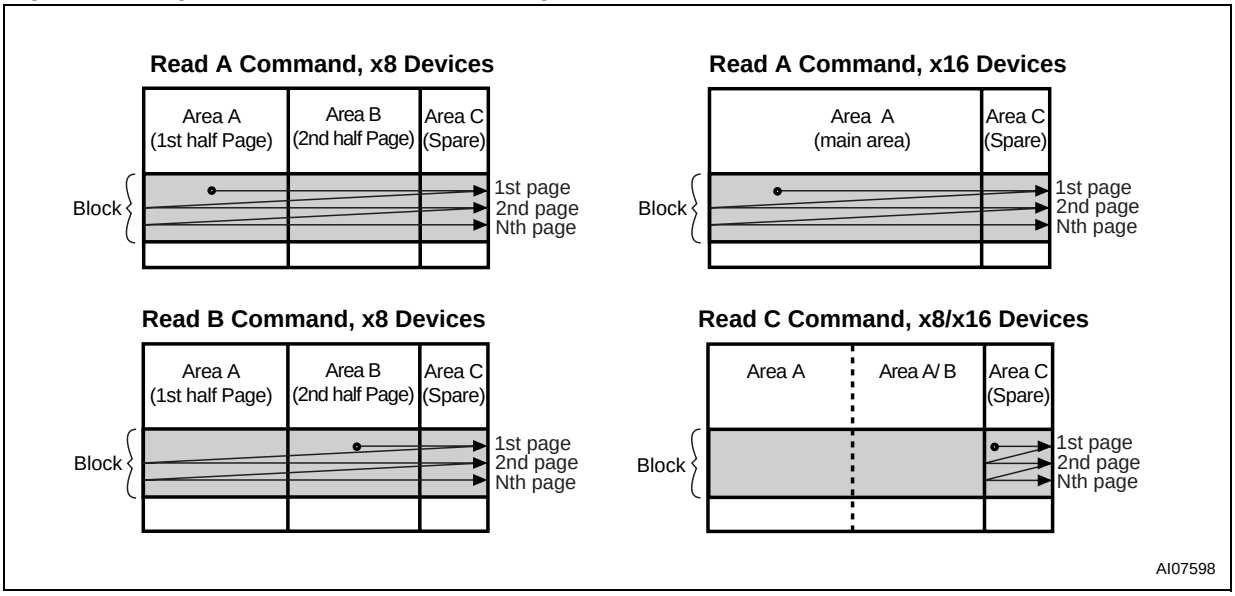


Figure 16. Sequential Row Read Block Diagrams



Page Program

The Page Program operation is the standard operation to program data to the memory array.

The main area of the memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 528) or words (1 to 264) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is three. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

Before starting a Page Program operation a Pointer operation can be performed to point to the area to be programmed. Refer to the Pointer Operations section and Figure 12. for details.

Each Page Program operation consists of five steps (see Figure 17.):

1. one bus cycle is required to setup the Page Program command
2. four bus cycles are then required to input the program address (refer to Table 6.)
3. the data is then input (up to 528 Bytes/ 264 Words) and loaded into the Page Buffer
4. one bus cycle is required to issue the confirm command to start the P/E/R Controller.
5. The P/E/R Controller then programs the data into the array.

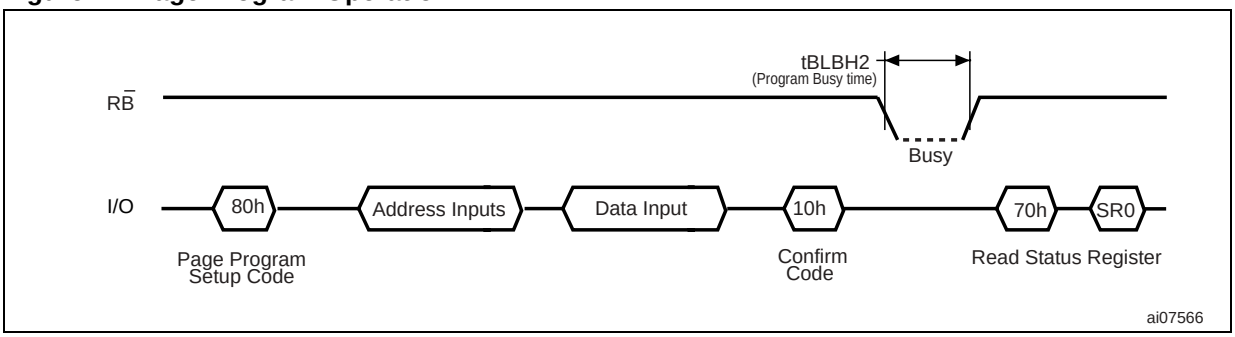
Once the program operation has started the Status Register can be read using the Read Status Register command. During program operations the Status Register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R Controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in Read Status Register mode until another valid command is written to the Command Interface.

Figure 17. Page Program Operation



Note: Before starting a Page Program operation a Pointer operation can be performed. Refer to Pointer Operations section for details.

Copy Back Program

The Copy Back Program operation is used to copy the data stored in one page and reprogram it in another page.

The Copy Back Program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the Copy Back Program operation fails an error is signalled in the Status Register. However as the standard external ECC cannot be used with the Copy Back operation bit error due to charge loss cannot be detected. For this reason it is recommended to limit the number of Copy Back operations on the same data and or to improve the performance of the ECC.

The Copy Back Program operation requires three steps:

1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 bus write cycles to input the source page address). This operation copies all 264 Words/ 528 Bytes from the page into the Page Buffer.
2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4 bus cycles to input the target page address. Refer to Table 10. for the addresses that must be the same for the Source and Target pages.
3. Then the confirm command is issued to start the P/E/R Controller.

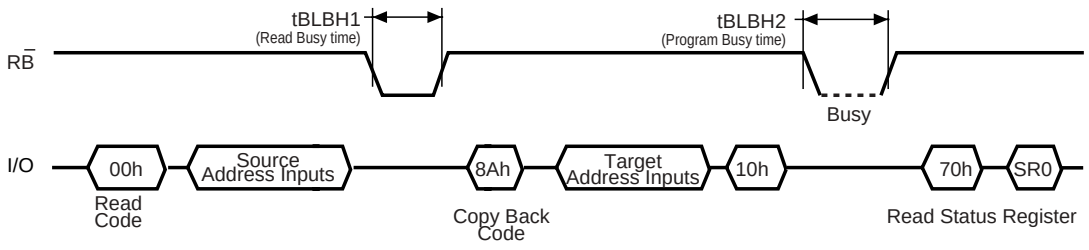
After a Copy Back Program operation, a partial-page program is not allowed in the target page until the block has been erased.

See Figure 18. for an example of the Copy Back operation.

Table 10. Copy Back Program Addresses

Density	Same Address for Source and Target Pages
128Mbit	A23
256Mbit	A24
512Mbit	A25
1Gbit	A25,A26

Figure 18. Copy Back Operation



Block Erase

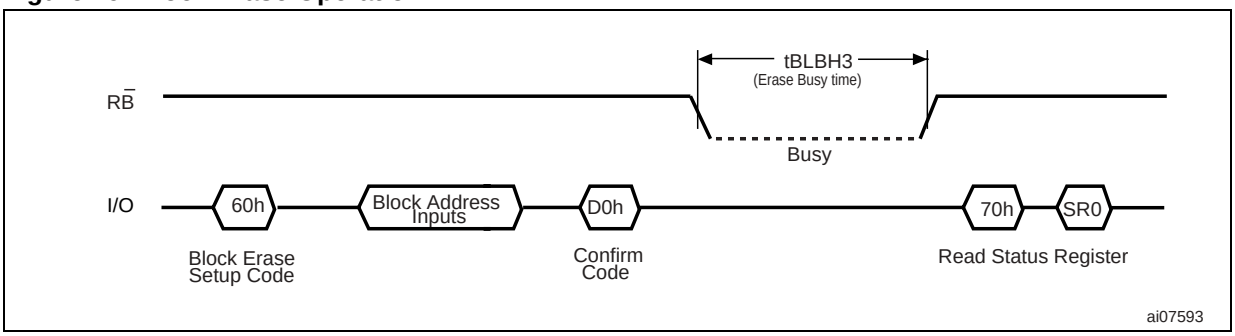
Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to '1'. All previous data in the block is lost.

An erase operation consists of three steps (refer to Figure 19.):

1. One bus cycle is required to setup the Block Erase command.
2. Only three bus cycles for 512Mb and 1Gb devices, or two for 128Mb and 256Mb devices are required to input the block address. The first cycle (A0 to A7) is not required as only addresses A14 to A26 (highest address depends on device density) are valid, A9 to A13 are ignored. In the last address cycle I/O0 to I/O7 must be set to V_{IL}.
3. One bus cycle is required to issue the confirm command to start the P/E/R Controller.

Once the erase operation has completed the Status Register can be checked for errors.

Figure 19. Block Erase Operation



Reset

The Reset command is used to reset the Command Interface and Status Register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.

If the device has already been reset then the new Reset command will not be accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued, refer to Table 21. for the values.

Read Status Register

The device contains a Status Register which provides information on the current or previous Program or Erase operation. The various bits in the Status Register convey information and errors on the operation.

The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the Status Register.

After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued. Therefore if a Read Status Register command is issued during a Random Read cycle a new read command must be issued to continue with a Page Read or Sequential Row Read operation.

The Status Register bits are summarized in Table 11., Status Register Bits. Refer to Table 11. in conjunction with the following text descriptions.

Write Protection Bit (SR7). The Write Protection bit can be used to identify if the device is protected or not. If the Write Protection bit is set to '1' the device is not protected and program or erase operations are allowed. If the Write Protection bit is set to '0' the device is protected and program or erase operations are not allowed.

P/E/R Controller Bit (SR6). The Program/Erase/Read Controller bit indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to '0', the P/E/R Controller is active (device is busy); when the bit is set to '1', the P/E/R Controller is inactive (device is ready).

Error Bit (SR0). The Error bit is used to identify if any errors have been detected by the P/E/R Controller. The Error Bit is set to '1' when a program or erase operation has failed to write the correct data to the memory. If the Error Bit is set to '0' the operation has completed successfully.

SR5, SR4, SR3, SR2 and SR1 are Reserved.

Table 11. Status Register Bits

Bit	Name	Logic Level	Definition
SR7	Write Protection	'1'	Not Protected
		'0'	Protected
SR6	Program/ Erase/ Read Controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR5, SR4, SR3, SR2, SR1	Reserved	Don't Care	
SR0	Generic Error	'1'	Error – operation failed
		'0'	No Error – operation successful

Read Electronic Signature

The device contains a Manufacturer Code and Device Code. To read these codes two steps are required:

1. first use one Bus Write cycle to issue the Read Electronic Signature command (90h)
2. then perform two Bus Read operations – the first will read the Manufacturer Code and the second, the Device Code. Further Bus Read operations will be ignored.

Refer to Table 12., Electronic Signature, for information on the addresses.

Table 12. Electronic Signature

Part Number	Manufacturer Code	Device code
NAND128R3A	20h	33h
NAND128W3A		73h
NAND128R4A	0020h	0043h
NAND128W4A		0053h
NAND256R3A	20h	35h
NAND256W3A		75h
NAND256R4A	0020h	0045h
NAND256W4A		0055h
NAND512R3A	20h	36h
NAND512W3A		76h
NAND512R4A	0020h	0046h
NAND512W4A		0056h
NAND01GR3A	20h	39h
NAND01GW3A		79h
NAND01GR4A	0020h	0049h
NAND01GW4A		0059h

Automatic Page 0 Read at Power-Up

Automatic Page 0 Read at Power-Up is an option available on all devices belonging to the NAND Flash 528 Byte/264 Word Page family. It allows the microcontroller to directly download boot code from page 0, without requiring any command or address input sequence. The Automatic Page 0 Read option is particularly suited for applications that boot from the NAND.

Devices delivered with Automatic Page 0 Read at Power-Up can have the Chip Enable Don't Care option either enabled or disabled. For details on how to order the different options, refer to Table 28., Ordering Information Scheme.

Automatic Page 0 Read Description. At power-up, once the supply voltage has reached the threshold level, V_{DDth}, all digital outputs revert to their reset state and the internal NAND device functions (reading, writing, erasing) are enabled.

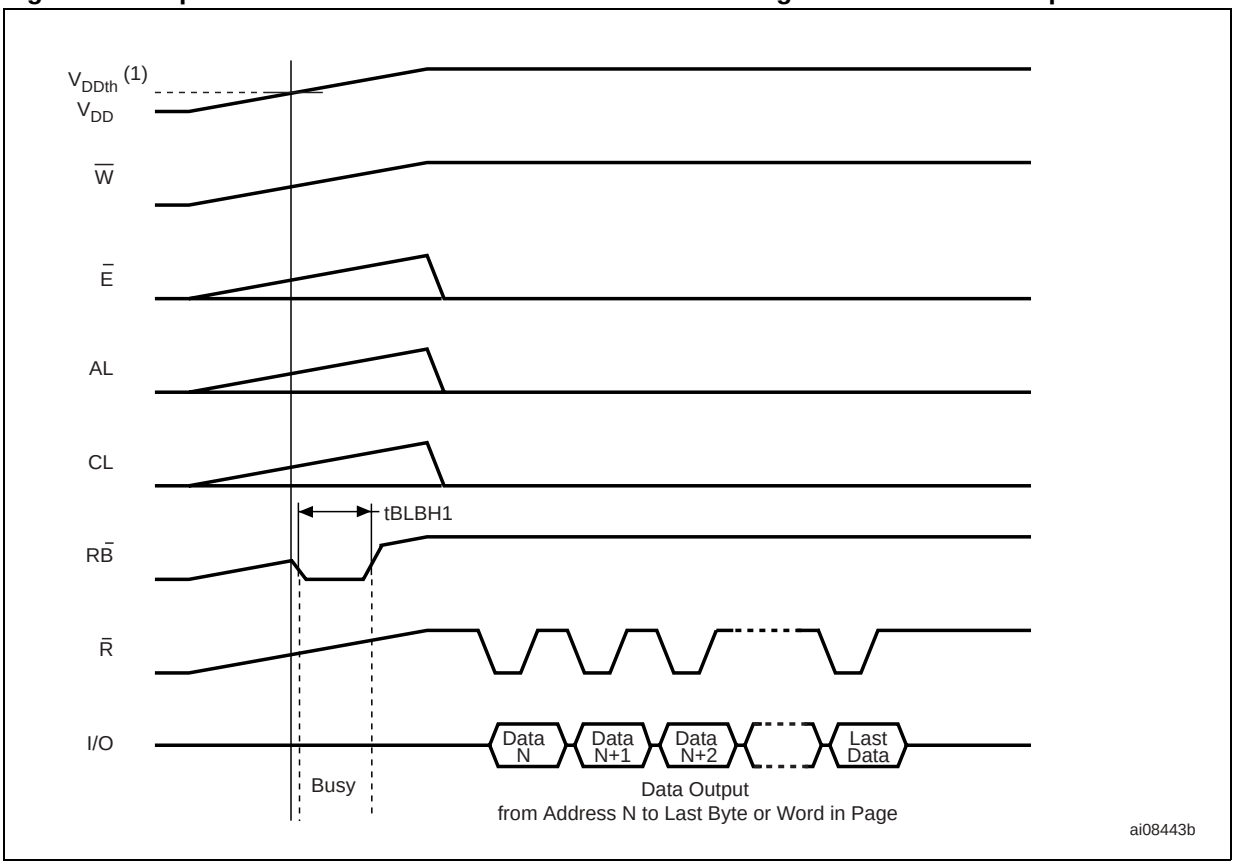
The device then automatically switches to read mode where, as in any read operation, the device is busy for a time t_{BLBH1} during which data is transferred to the Page Buffer. Once the data transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially on the I/O bus by pulsing the Read Enable, $\overline{R}$, signal. Figure 20. and Figure 21. show the power-up waveforms for devices featuring the Automatic Page 0 Read option.

Chip Enable Don't Care Enabled. If the device is delivered with Chip Enable Don't Care and Automatic Page 0 Read at Power-up, only the first page (Page 0) will be automatically read after the power-up sequence. Refer to Figure 20..

Chip Enable Don't Care Disabled. If the device is delivered with the Automatic Page 0 Read option only (Chip Enable Don't Care disabled), the device will automatically enter Sequential Row Read mode (Automatic Memory Download) after the power-up sequence, and start reading Page 0, Page 1, etc., until the last memory location is reached, each new page being accessed after a time t_{BLBH1}.

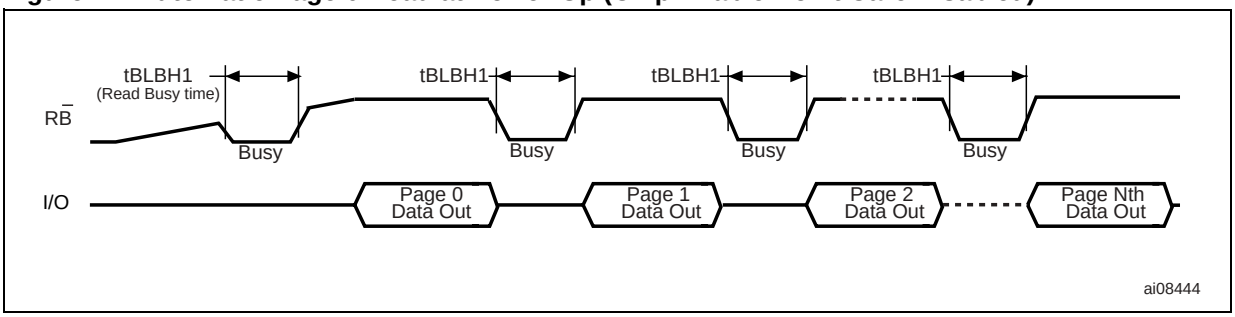
The Sequential Row Read operation can be inhibited or interrupted by de-asserting $\overline{E}$ (set to V_{IH}) or by issuing a command.

Figure 20. Chip Enable Don't Care Enabled and Automatic Page 0 Read at Power-Up



Note: 1. V_{DDth} is equal to 2.5V for 3V Power Supply devices and to 1.5V for 1.8V Power Supply devices.

Figure 21. Automatic Page 0 Read at Power-Up (Chip Enable Don't Care Disabled)



SOFTWARE ALGORITHMS

This section gives information on the software algorithms that ST recommends to implement to manage the Bad Blocks and extend the lifetime of the NAND device.

NAND Flash memories are programmed and erased by Fowler-Nordheim tunneling using a high voltage. Exposing the device to a high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see Table 14. for value) and it is recommended to implement Garbage Collection, a Wear-Leveling Algorithm and an Error Correction Code, to extend the number of program and erase cycles and increase the data retention.

To help integrate a NAND memory into an application ST Microelectronics can provide:

- A Demo board with NAND simulation software for PCs
- File System OS Native reference software, which supports the basic commands of file management.

Contact the nearest ST Microelectronics sales office for more details.

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 6th Byte/ 1st Word in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block.

The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 22.

Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block.

See the "Copy Back Program" section for more details.

Refer to Table 13. for the recommended procedure to follow if an error occurs during an operation.

Table 13. Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC
Read	ECC

Figure 22. Bad Block Management Flowchart

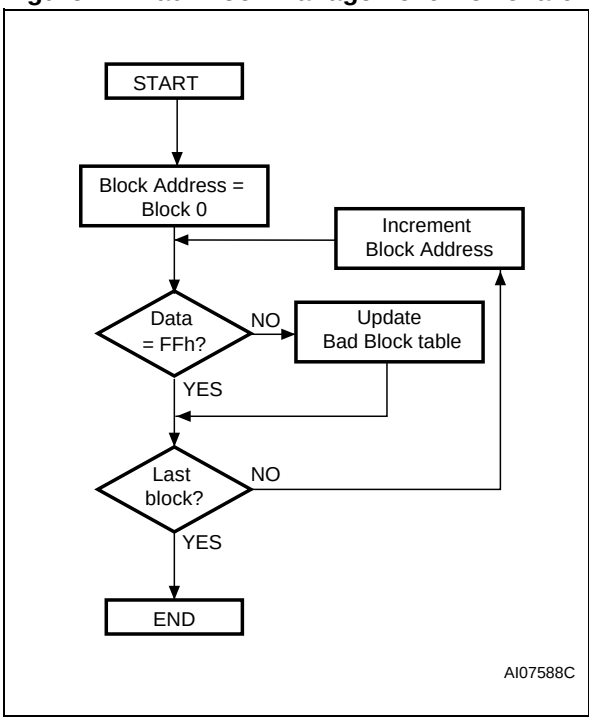
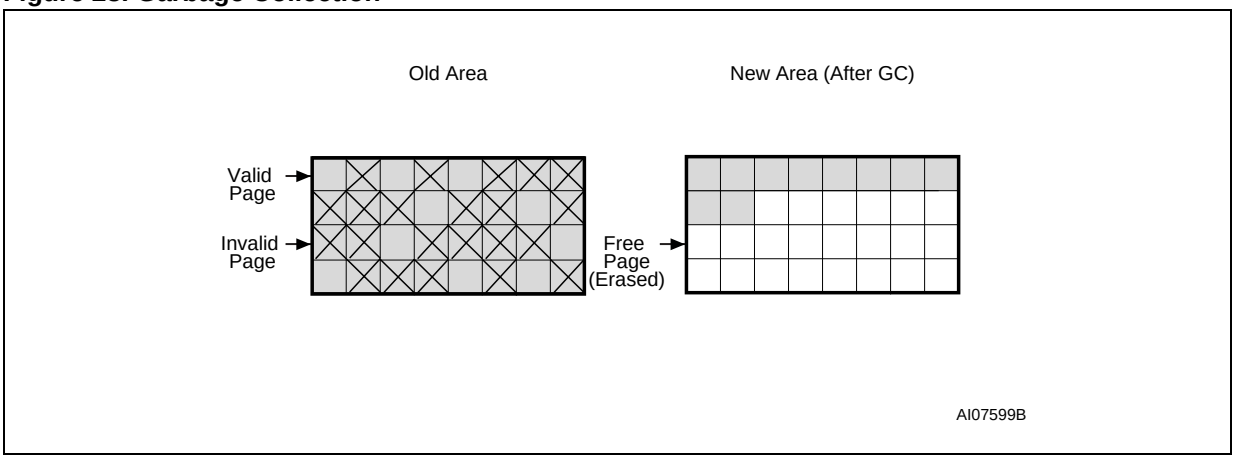


Figure 23. Garbage Collection



Garbage Collection

When a data page needs to be modified, it is faster to write to the first available page, and the previous page is marked as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations it is recommended to implement a Garbage Collection algorithm. In a Garbage Collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see Figure 23.).

Wear-leveling Algorithm

For write-intensive applications, it is recommended to implement a Wear-leveling Algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a Wear-Leveling Algorithm not all blocks get used at the same rate. Blocks with long-lived data do not endure as many write cycles as the blocks with frequently-changed data.

The Wear-leveling Algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

- First Level Wear-leveling, new data is programmed to the free blocks that have had the fewest write cycles
- Second Level Wear-leveling, long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

The Second Level Wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

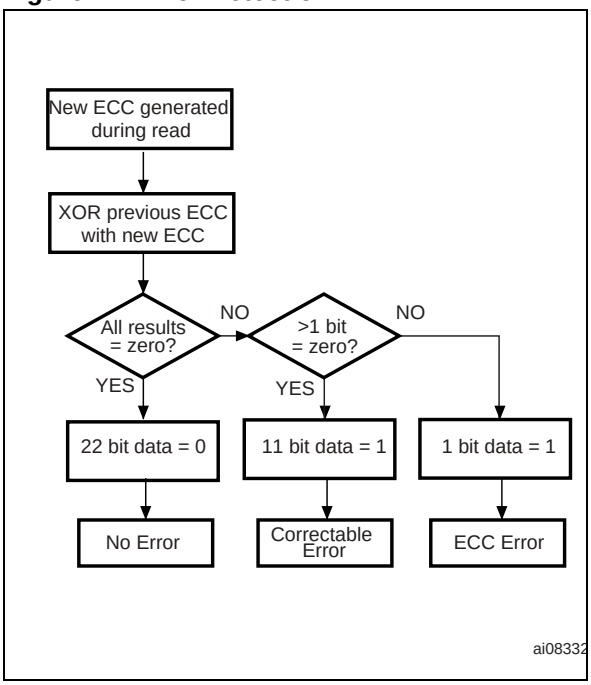
Error Correction Code

An Error Correction Code (ECC) can be implemented in the Nand Flash memories to identify and correct errors in the data.

For every 2048 bits in the device it is recommended to implement 22 bits of ECC (16 bits for line parity plus 6 bits for column parity).

An ECC model is available in VHDL or Verilog. Contact the nearest ST Microelectronics sales office for more details.

Figure 24. Error Detection



Hardware Simulation Models

Behavioral simulation models. Denali Software Corporation models are platform independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND Flash devices, and so allow software to be developed before hardware.

IBIS simulations models. IBIS (I/O Buffer Information Specification) models describe the behavior of the I/O buffers and electrical characteristics of Flash devices.

These models provide information such as AC characteristics, rise/fall times and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

PROGRAM AND ERASE TIMES AND ENDURANCE CYCLES

The Program and Erase times and the number of Program/ Erase cycles per block are shown in Table 14.

Table 14. Program, Erase Times and Program Erase Endurance Cycles

Parameters	NAND Flash			Unit
	Min	Typ	Max	
Page Program Time		200	500	µs
Block Erase Time		2	3	ms
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	10			years

MAXIMUM RATING

Stressing the device above the ratings listed in Table 15., Absolute Maximum Ratings, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 15. Absolute Maximum Ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_{BIAS}	Temperature Under Bias		– 50	125	°C
T_{STG}	Storage Temperature		– 65	150	°C
V_{IO} (1)	Input or Output Voltage	1.8V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V
V_{DD}	Supply Voltage	1.8V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V

Note: 1. Minimum Voltage may undershoot to –2V for less than 20ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2V for less than 20ns during transitions on I/O pins.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 16., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 16. Operating and AC Measurement Conditions

Parameter		NAND Flash		Units
		Min	Max	
Supply Voltage (V_{DD})	1.8V devices	1.7	1.95	V
	3V devices	2.7	3.6	V
Ambient Temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load Capacitance (C_L) (1 TTL GATE and C_L)	1.8V devices	30		pF
	3V devices (2.7 - 3.6V)	50		pF
	3V devices (3.0 - 3.6V)	100		pF
Input Pulses Voltages	1.8V devices	0	V_{DD}	V
	3V devices	0.4	2.4	V
Input and Output Timing Ref. Voltages	1.8V devices	0.9		V
	3V devices	1.5		V
Input Rise and Fall Times		5		ns

Table 17. Capacitance

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V		10	pF

Note: T_A = 25°C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.

Table 18. DC Characteristics, 1.8V Devices

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{DD1}	Operating Current	Sequential Read	$\overline{E}$ t_{RLRL} minimum $\overline{E}=V_{IL}$, I_{OUT} = 0 mA	-	8	15	mA
I_{DD2}		Program	-	-	8	15	mA
I_{DD3}		Erase	-	-	8	15	mA
I_{DD5}	Stand-By Current (CMOS) 128Mb, 256Mb, 512Mb devices		$\overline{E}=V_{DD}$-0.2, $\overline{WP}=0/V_{DD}$	-	10	50	µA
	Stand-By Current (CMOS) 512Mb and 1Gb Dual Die devices			-	20	100	µA
I_{LI}	Input Leakage Current		V_{IN}= 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output Leakage Current		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input High Voltage		-	V_{DD}-0.4	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-	-0.3	-	0.4	V
V_{OH}	Output High Voltage Level		I_{OH} = -100µA	V_{DD}-0.1	-	-	V
V_{OL}	Output Low Voltage Level		I_{OL} = 100µA	-	-	0.1	V
I_{OL} ($R\overline{B}$)	Output Low Current ($R\overline{B}$)		V_{OL} = 0.1V	3	4		mA
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)		-	-	-	1.5	V

Table 19. DC Characteristics, 3V Devices

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{DD1}	Operating Current	Sequential Read	$\overline{E}$=V_{IL}, I_{OUT} = 0 mA	-	10	20	mA
I_{DD2}		Program	-	-	10	20	mA
I_{DD3}		Erase	-	-	10	20	mA
I_{DD4}	Stand-by Current (TTL), 128Mb, 256Mb, 512Mb devices		$\overline{E}$=V_{IH}, $\overline{WP}$=0V/V_{DD}	-	-	1	mA
	Stand-by Current (TTL) 512Mb and 1Gb Dual Die devices			-	-	2	mA
I_{DD5}	Stand-By Current (CMOS) 128Mb, 256Mb, 512Mb devices		$\overline{E}$=V_{DD}-0.2, $\overline{WP}$=0/V_{DD}	-	10	50	µA
	Stand-By Current (CMOS) 512Mb and 1Gb Dual Die devices			-	20	100	µA
I_{LI}	Input Leakage Current		V_{IN}= 0 to V_{DD}max	-	-	±10	µA
I_{LO}	Output Leakage Current		V_{OUT}= 0 to V_{DD}max	-	-	±10	µA
V_{IH}	Input High Voltage		-	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-	–0.3	-	0.8	V
V_{OH}	Output High Voltage Level		I_{OH} = –400µA	2.4	-	-	V
V_{OL}	Output Low Voltage Level		I_{OL} = 2.1mA	-	-	0.4	V
I_{OL} ($R\overline{B}$)	Output Low Current ($R\overline{B}$)		V_{OL} = 0.4V	8	10		mA
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)		-	-	-	2.5	V

Table 20. AC Characteristics for Command, Address, Data Input

Symbol	Alt. Symbol	Parameter			1.8V Devices	3V Devices	Unit
t_{ALLWL}	t_{ALS}	Address Latch Low to Write Enable Low	AL Setup time	Min	0	0	ns
t_{ALHWL}		Address Latch High to Write Enable Low					
t_{CLHWL}	t_{CLS}	Command Latch High to Write Enable Low	CL Setup time	Min	0	0	ns
t_{CLLWL}		Command Latch Low to Write Enable Low					
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data Setup time	Min	20	20	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	$\overline{E}$ Setup time	Min	0	0	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL Hold time	Min	10	10	ns
t_{WHALL}		Write Enable High to Address Latch Low					
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	10	10	ns
t_{WHCLL}		Write Enable High to Command Latch Low					
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data Hold time	Min	10	10	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ Hold time	Min	10	10	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High Hold time	Min	20	15	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ Pulse Width	Min	40	25(1)	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	60	50	ns

Note: 1. If t_{ELWL} is less than 10ns, t_{WLWH} must be minimum 35ns, otherwise, t_{WLWH} may be minimum 25ns.

Table 21. AC Characteristics for Operations

Symbol	Alt. Symbol	Parameter			1.8V Devices	3V Devices	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read Electronic Signature	Min	10	10	ns
t_{ALLRL2}			Read cycle	Min	10	10	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	20	ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read Busy time, 128Mb, 256Mb, 512Mb Dual Die	Max	10	10	µs
			Read Busy time, 512Mb, 1Gb	Max	15	12	µs
t_{BLBH2}	t_{PROG}		Program Busy time	Max	500	500	µs
t_{BLBH3}	t_{BERS}		Erase Busy time	Max	3	3	ms
t_{BLBH4}			Reset Busy time, during ready	Max	5	5	µs
t_{WHBH1}	t_{RST}	Write Enable High to Ready/Busy High	Reset Busy time, during read	Max	5	5	µs
			Reset Busy time, during program	Max	10	10	µs
			Reset Busy time, during erase	Max	500	500	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10	10	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	0	ns
t_{EHBH}	t_{CRY}	Chip Enable High to Ready/Busy High (E intercepted read)		Max	60 + t_r(1)	60 + t_r(1)	ns
t_{EHEL}	t_{CEH}	Chip Enable High to Chip Enable Low(2)		Min	100	100	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	20	20	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	45	45	ns
t_{RHBL}	t_{RB}	Read Enable High to Ready/Busy Low		Max	100	100	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	Min	15	15	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z		Min	15	15	ns
				Max	30	30	
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable Pulse Width	Min	30	30	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read Cycle time	Min	60	50	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable Access time	Max	35	35	ns
			Read ES Access time(3)				
t_{WHBH}	t_R	Write Enable High to Ready/Busy High	Read Busy time, 128Mb, 256Mb, 512Mb Dual Die	Max	10	10	µs
			Read Busy time, 512Mb, 1Gb	Max	15	12	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	80	60	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	60	50	ns

Note: 1. The time to Ready depends on the value of the pull-up resistor tied to the Ready/Busy pin. See Figures 36, 37 and 38.
2. To break the sequential read cycle, $\overline{E}$ must be held High for longer than t_{EHEL}.
3. ES = Electronic Signature.

Figure 25. Command Latch AC Waveforms

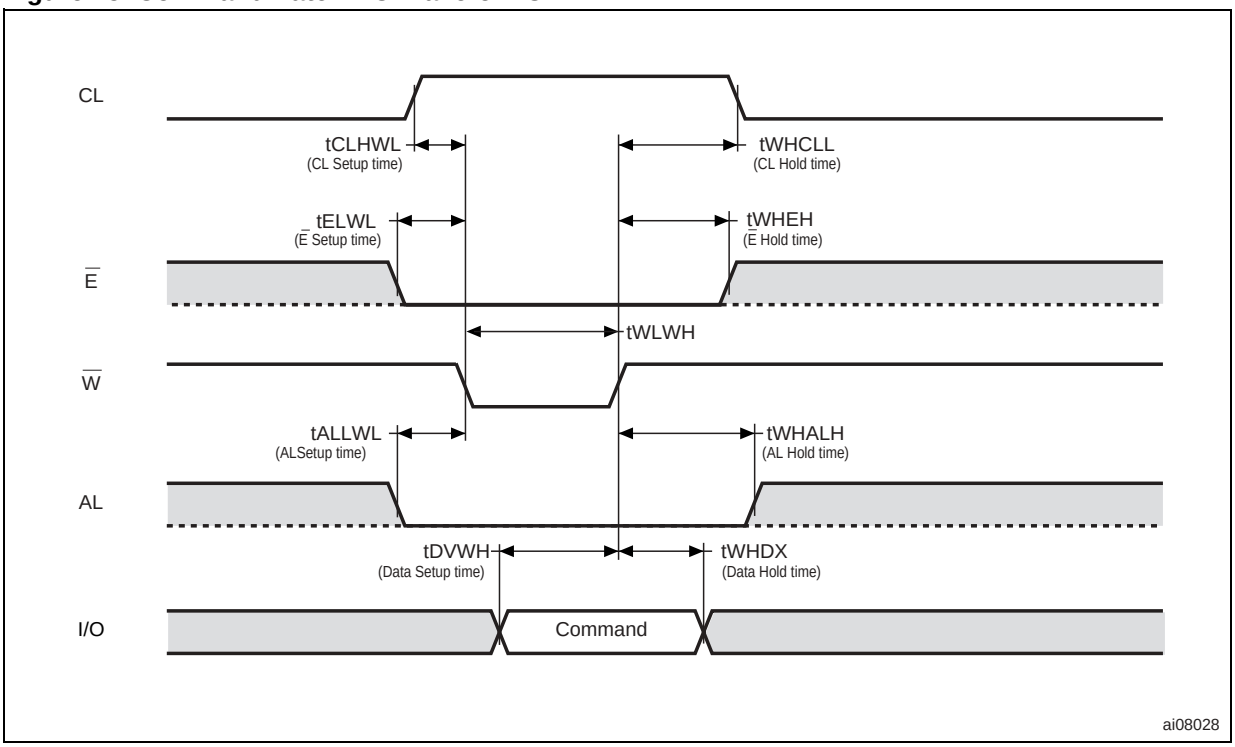
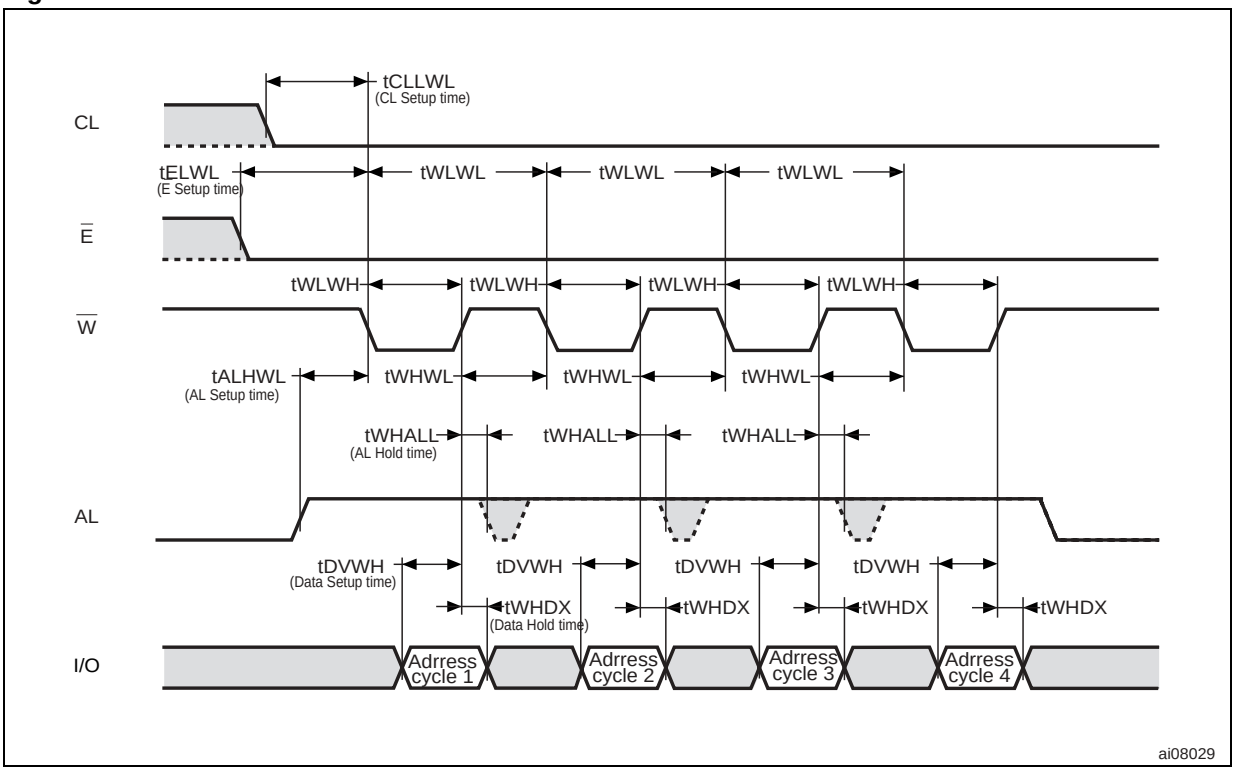


Figure 26. Address Latch AC Waveforms



Note: Address cycle 4 is only required for 512Mb and 1Gb devices.

Figure 27. Data Input Latch AC Waveforms

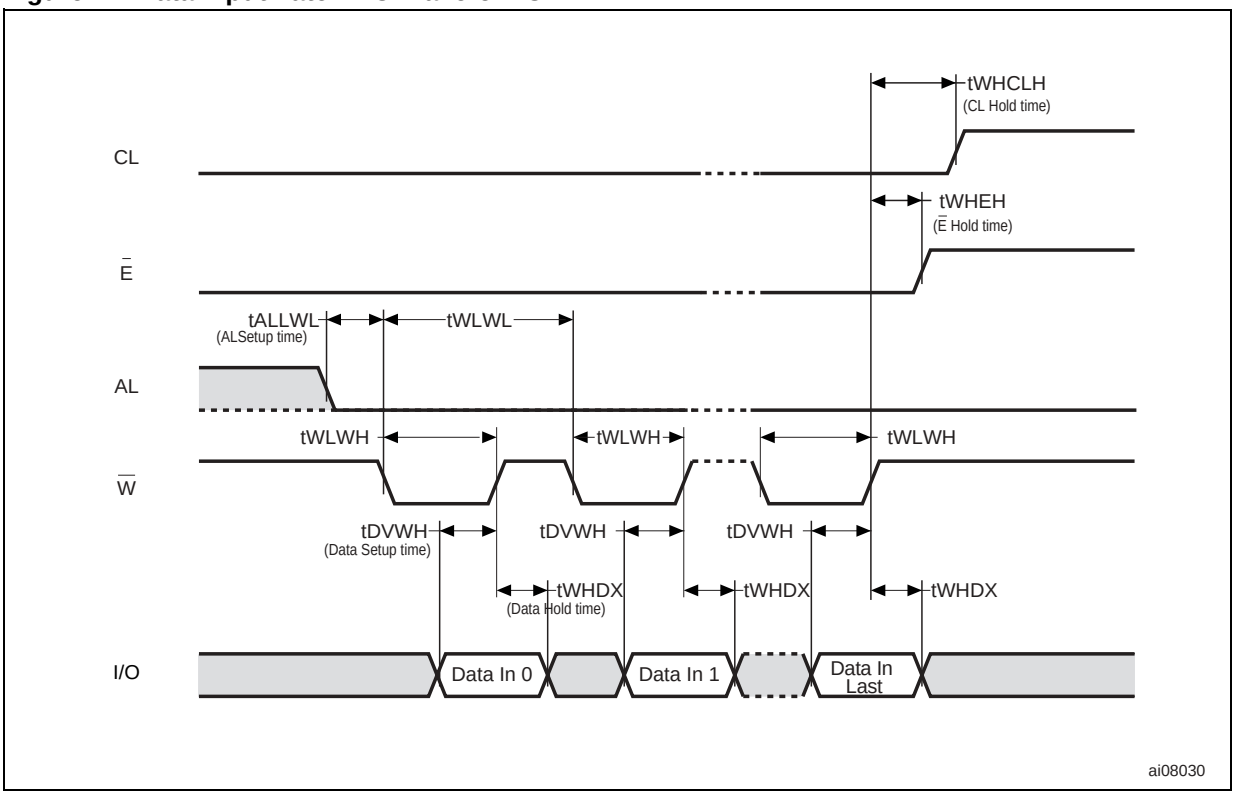
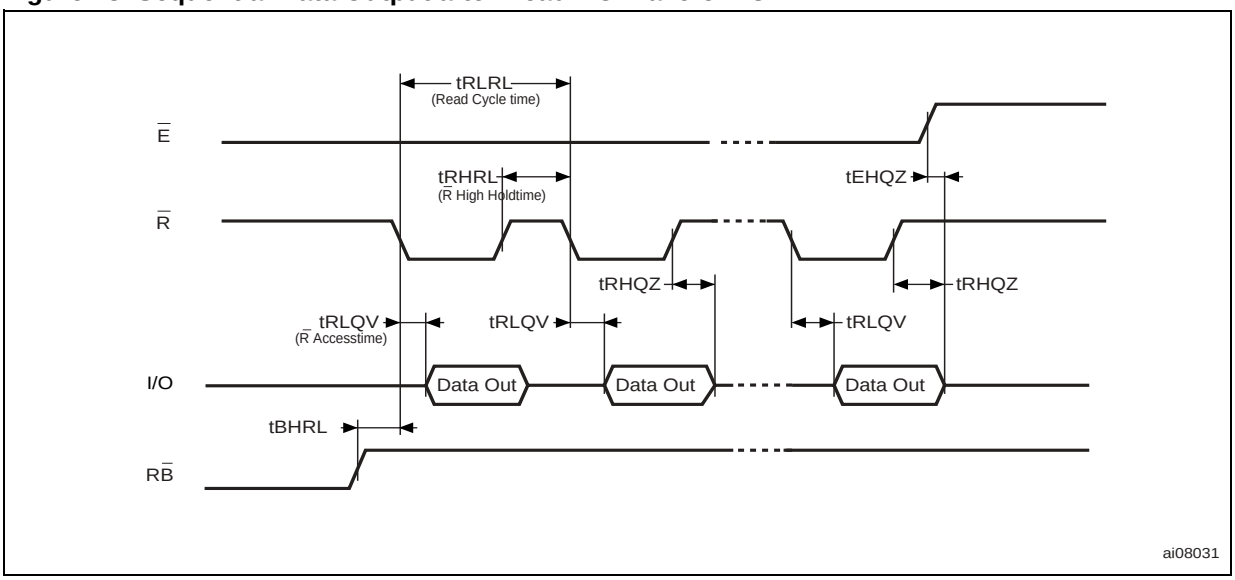


Figure 28. Sequential Data Output after Read AC Waveforms



Note: 1. CL = Low, AL = Low, $\overline{W}$ = High.

Figure 29. Read Status Register AC Waveform

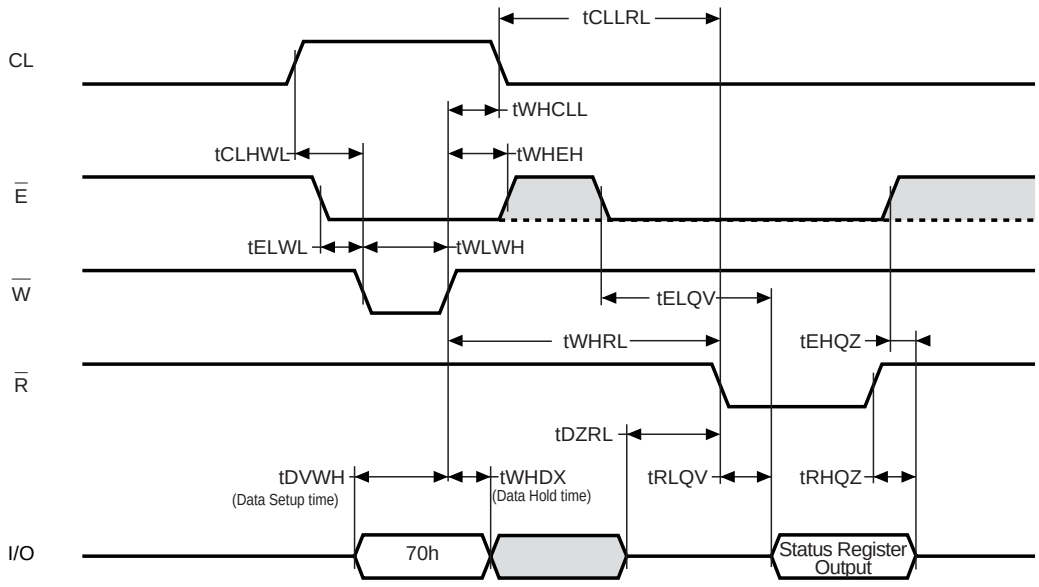
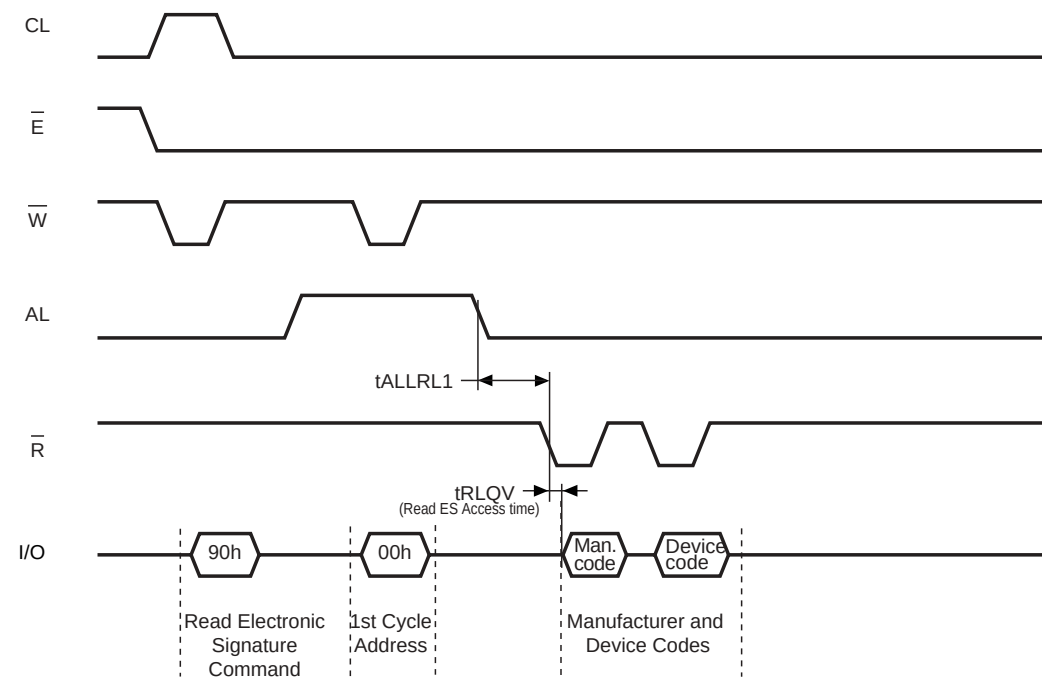
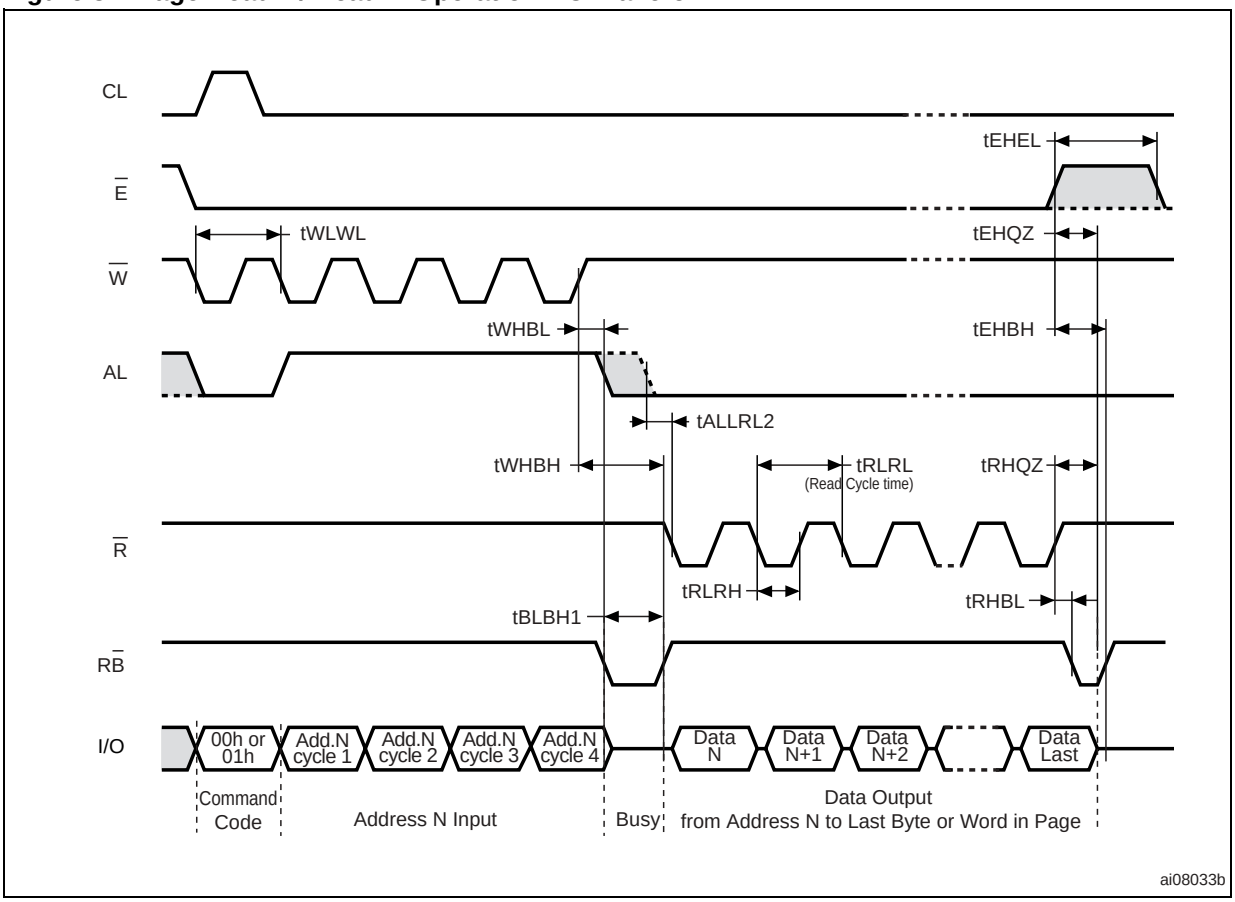


Figure 30. Read Electronic Signature AC Waveform



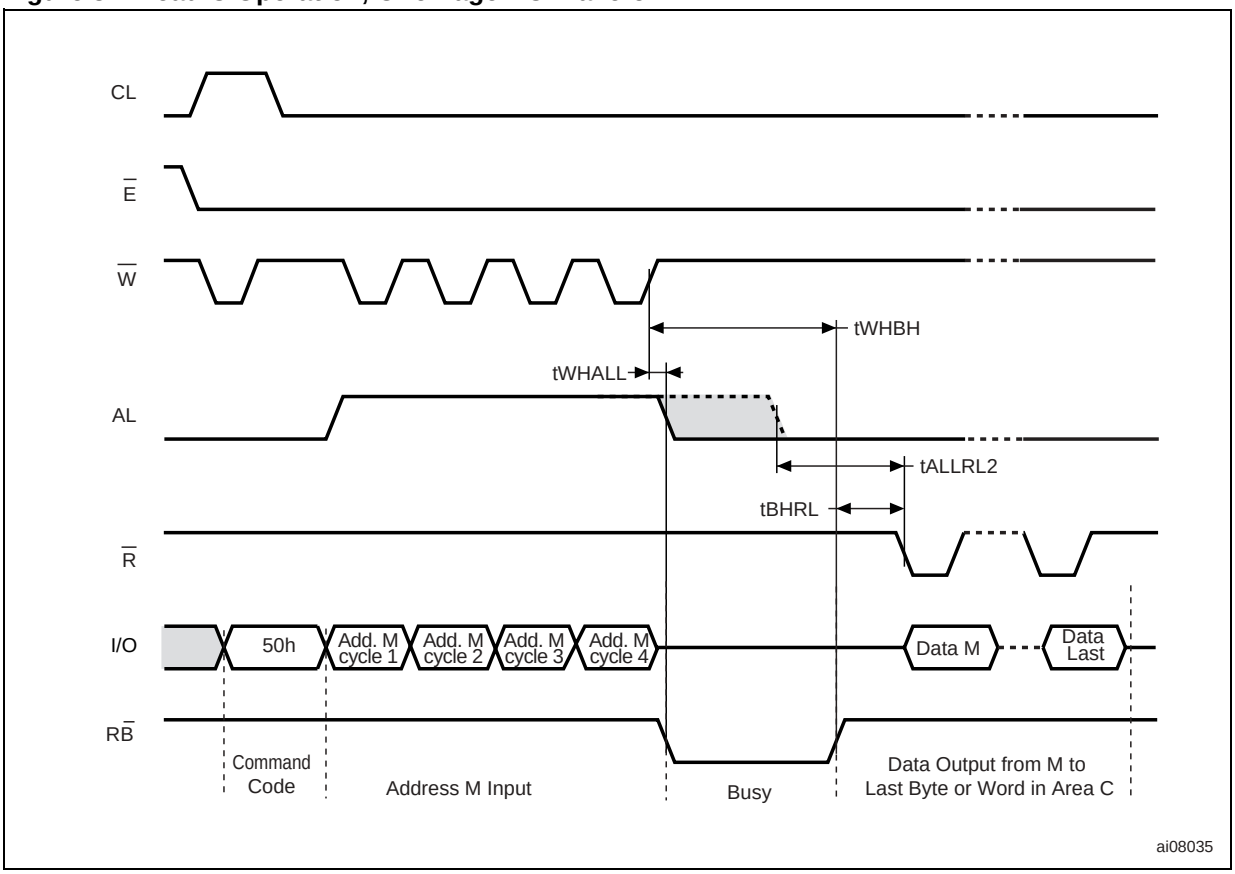
Note: Refer to Table 12. for the values of the Manufacturer and Device Codes.

Figure 31. Page Read A/ Read B Operation AC Waveform



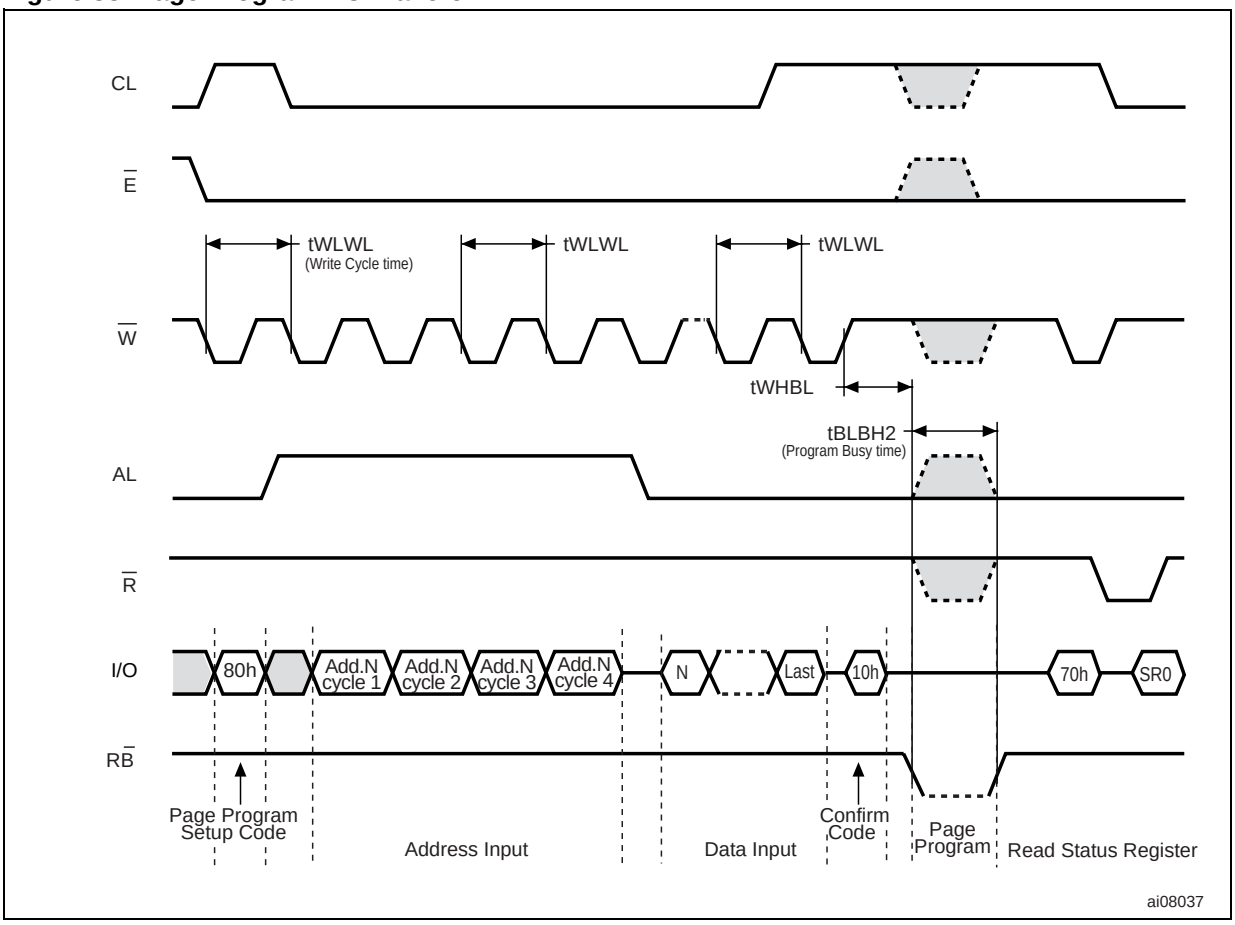
Note: Address cycle 4 is only required for 512Mb and 1Gb devices.

Figure 32. Read C Operation, One Page AC Waveform



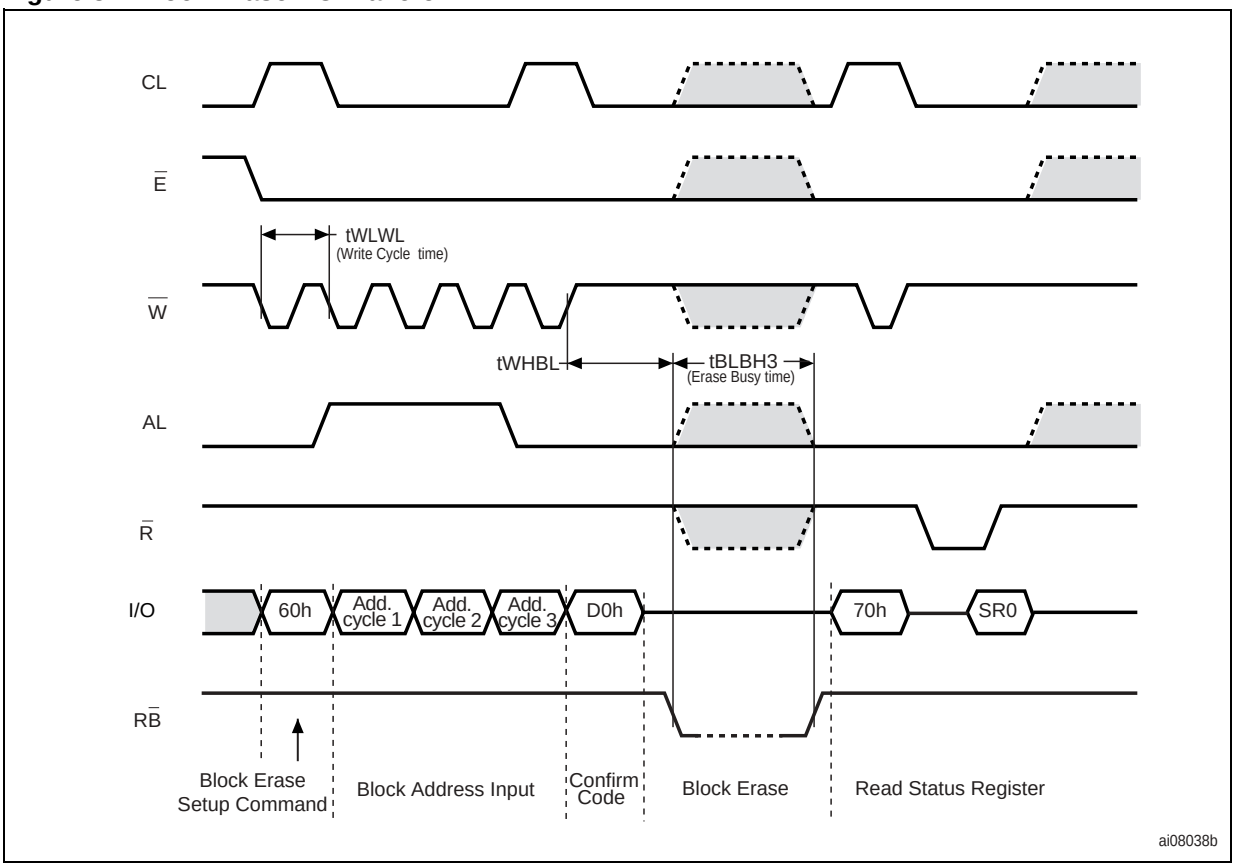
Note: 1. A0-A7 is the address in the Spare Memory area, where A0-A3 are valid and A4-A7 are ‘don’t care’.

Figure 33. Page Program AC Waveform



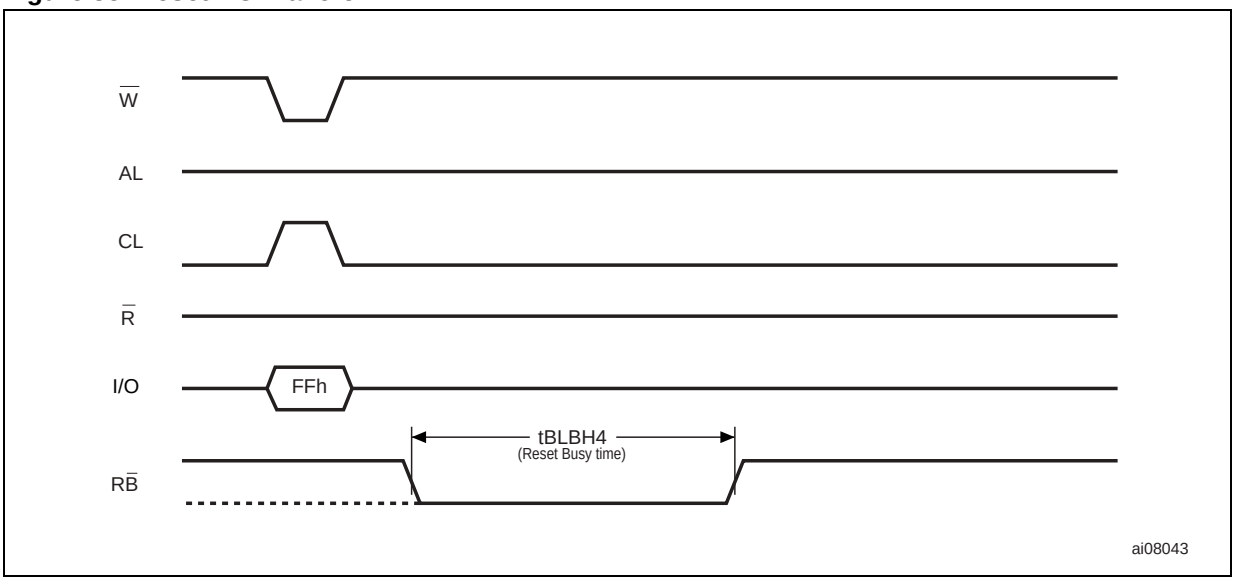
Note: Address cycle 4 is only required for 512Mb and 1Gb devices.

Figure 34. Block Erase AC Waveform



Note: Address cycle 3 is required for 512Mb and 1Gb devices only.

Figure 35. Reset AC Waveform



Ready/Busy Signal Electrical Characteristics

Figures 37, 36 and 38 show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + \Sigma I_L}$$

So,

$$R_P min(1{,}8V) = \frac{1{,}85V}{3mA + \Sigma I_L}$$

$$R_P min(3V) = \frac{3{,}2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 36. Ready/Busy AC Waveform

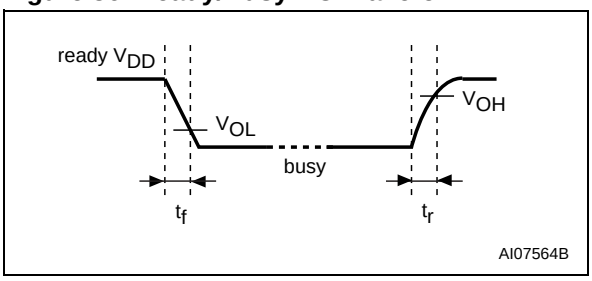


Figure 37. Ready/Busy Load Circuit

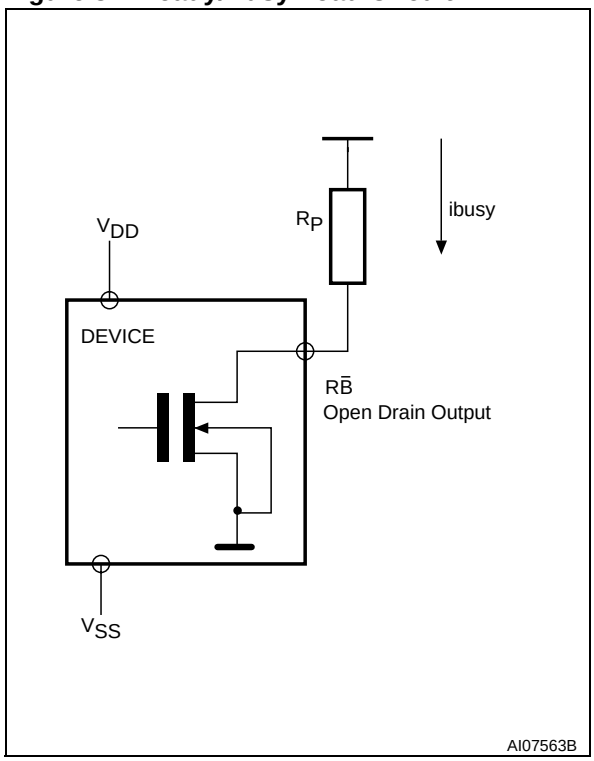
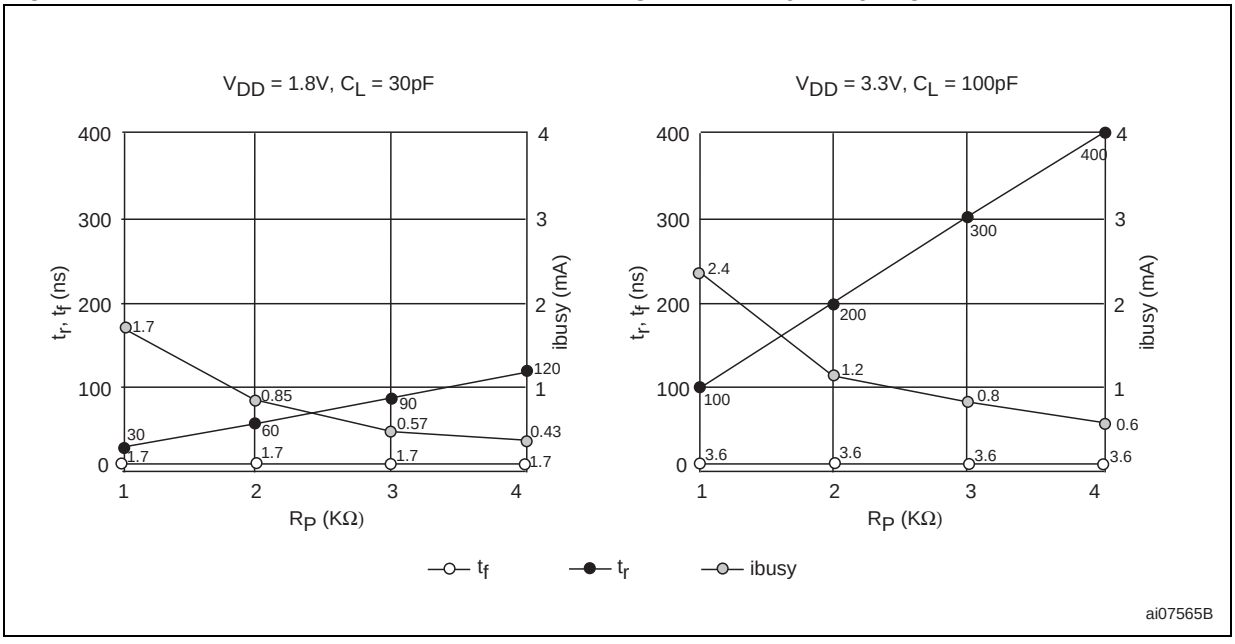


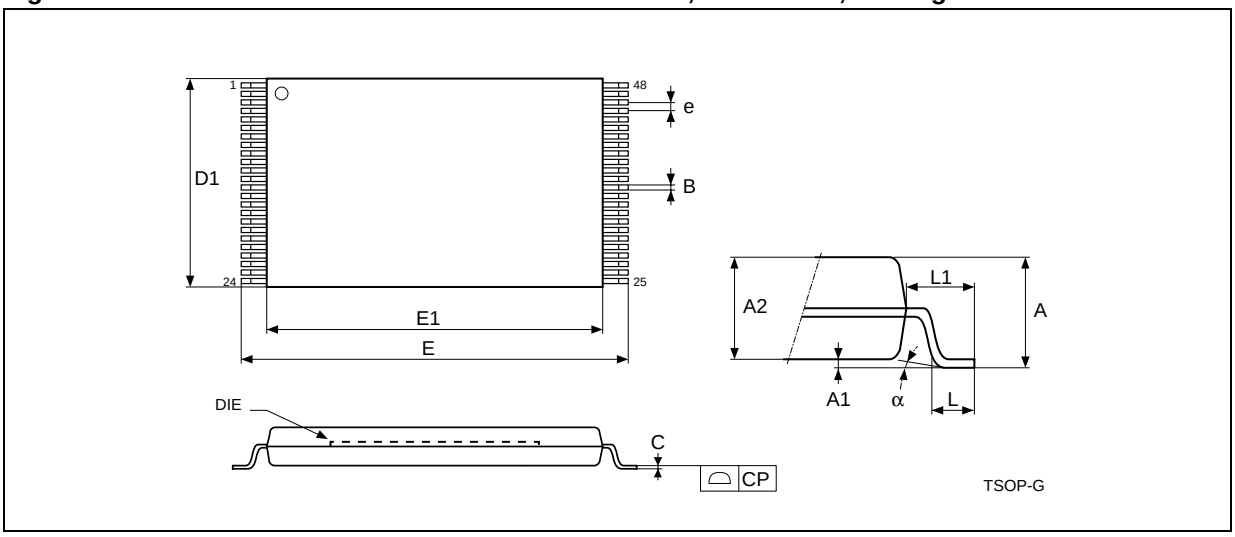
Figure 38. Resistor Value Versus Waveform Timings For Ready/Busy Signal



Note: T = 25°C.

PACKAGE MECHANICAL

Figure 39. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

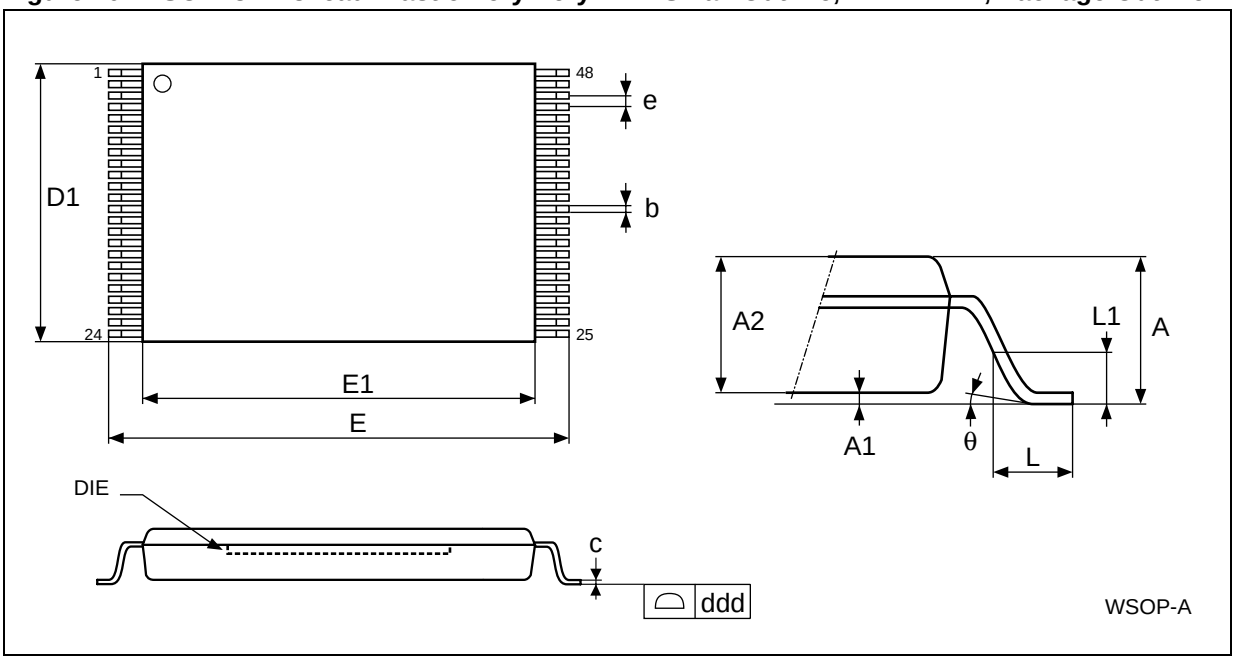


Note: Drawing is not to scale.

Table 22. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.080			0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	–
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
α	3°	0°	5°	3°	0°	5°

Figure 40. WSOP48 – 48 lead Plastic Very Very Thin Small Outline, 12 x 17mm, Package Outline

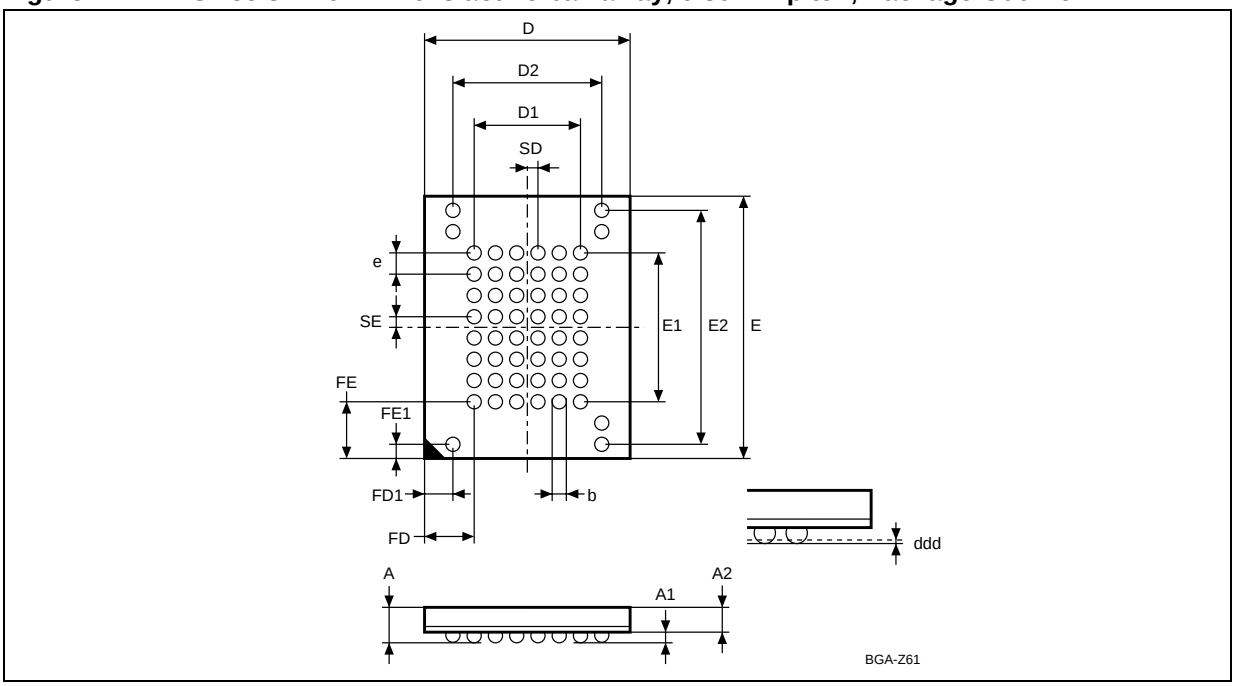


Note: Drawing not to scale.

Table 23. WSOP48 lead Plastic Very Very Thin Small Outline, 12 x 17mm, Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			0.65			0.026
A1			0.10			0.004
A2	0.52	0.47	0.57	0.020	0.019	0.022
b	0.16	0.13	0.23	0.006	0.005	0.009
c	0.10	0.08	0.17	0.004	0.003	0.007
D1	12.00	11.90	12.10	0.472	0.469	0.476
ddd			0.06			0.002
E	17.00	16.80	17.20	0.669	0.661	0.677
E1	15.40	15.30	15.50	0.606	0.602	0.610
e	0.50	–	–	0.020	–	–
L	0.55	0.45	0.65	0.022	0.018	0.026
L1	0.25	–	–	0.010	–	–
θ		0°	5°		0°	5°

Figure 41. VFBGA55 8 x 10mm - 6x8 active ball array, 0.80mm pitch, Package Outline

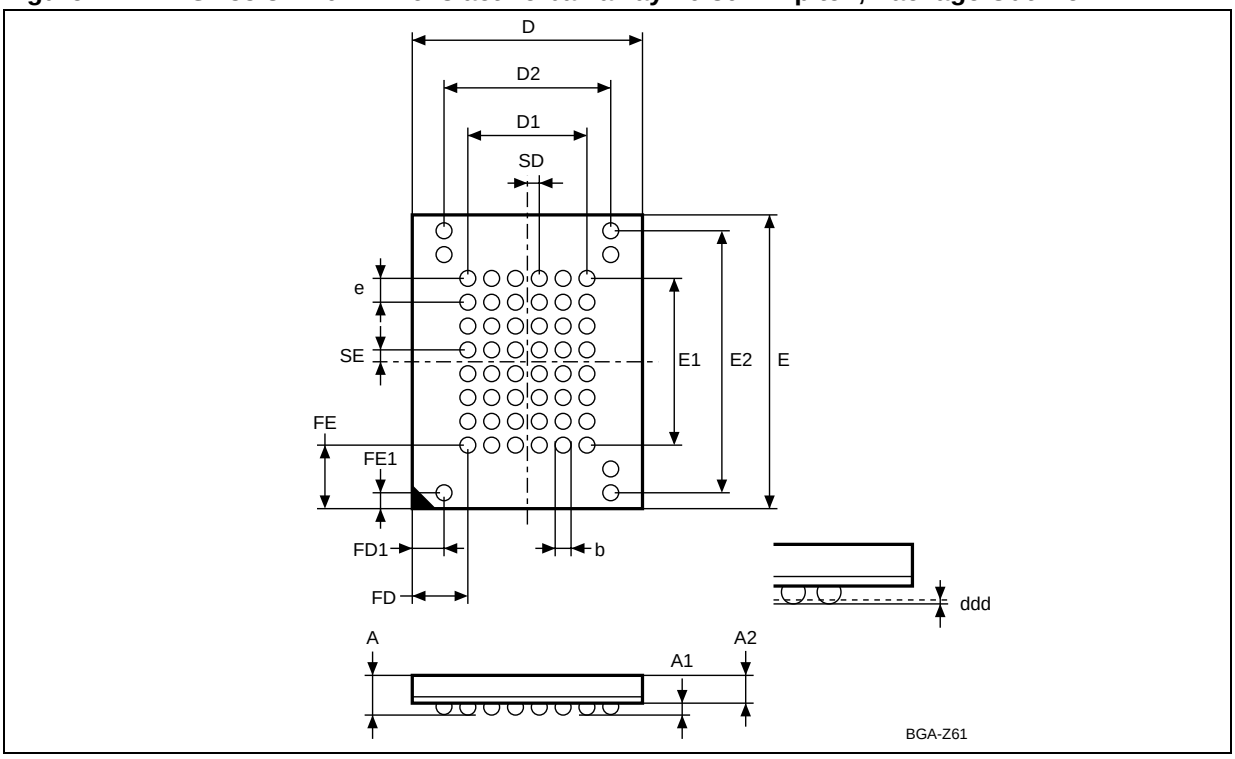


Note: Drawing is not to scale

Table 24. VFBGA55 8 x 10mm - 6x8 active ball array, 0.80mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.05			0.041
A1		0.25			0.010	
A2			0.70			0.028
b	0.45	0.40	0.50	0.018	0.016	0.020
D	8.00	7.90	8.10	0.315	0.311	0.319
D1	4.00			0.157		
D2	5.60			0.220		
ddd			0.10			0.004
E	10.00	9.90	10.10	0.394	0.390	0.398
E1	5.60			0.220		
E2	8.80			0.346		
e	0.80	–	–	0.031	–	–
FD	2.00			0.079		
FD1	1.20			0.047		
FE	2.20			0.087		
FE1	0.60			0.024		
SD	0.40			0.016		
SE	0.40			0.016		

Figure 42. TFBGA55 8 x 10mm - 6x8 active ball array - 0.80mm pitch, Package Outline

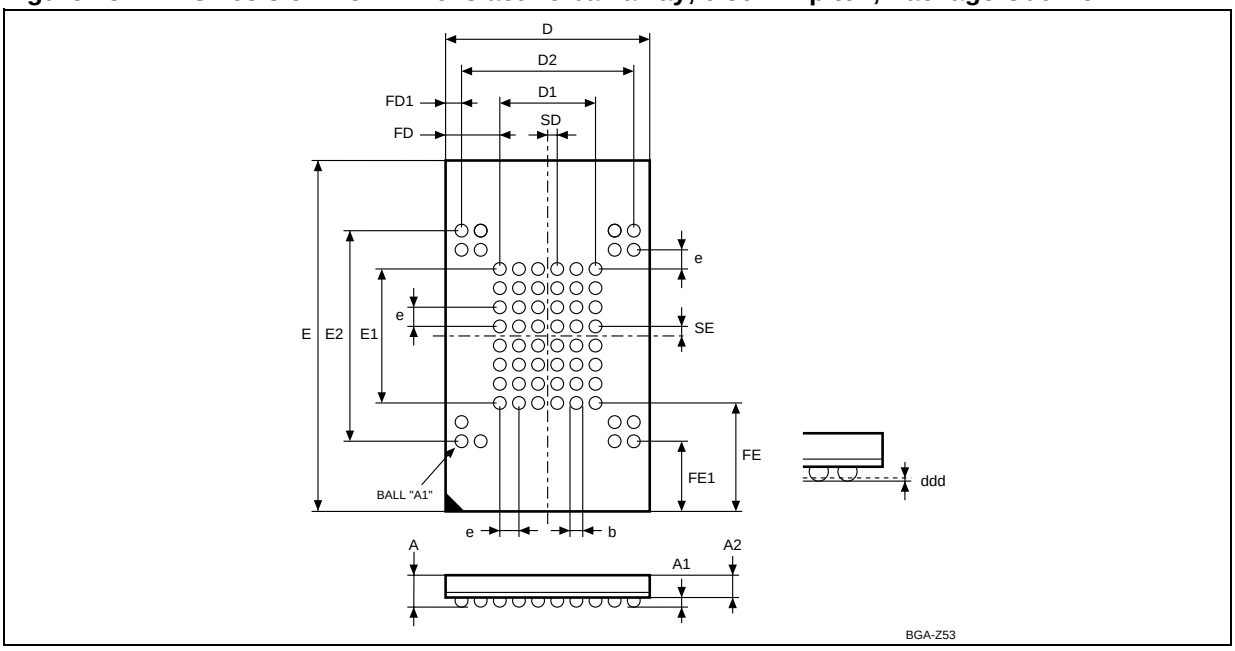


Note: Drawing is not to scale

Table 25. TFBGA55 8 x 10mm - 6x8 active ball array - 0.80mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.25			0.010	
A2	0.80			0.031		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	8.00	7.90	8.10	0.315	0.311	0.319
D1	4.00			0.157		
D2	5.60			0.220		
ddd			0.10			0.004
E	10.00	9.90	10.10	0.394	0.390	0.398
E1	5.60			0.220		
E2	8.80			0.346		
e	0.80	–	–	0.031	–	–
FD	2.00			0.079		
FD1	1.20			0.047		
FE	2.20			0.087		
FE1	0.60			0.024		
SD	0.40			0.016		
SE	0.40			0.016		

Figure 43. VFBGA63 8.5 x 15mm - 6x8 active ball array, 0.80mm pitch, Package Outline

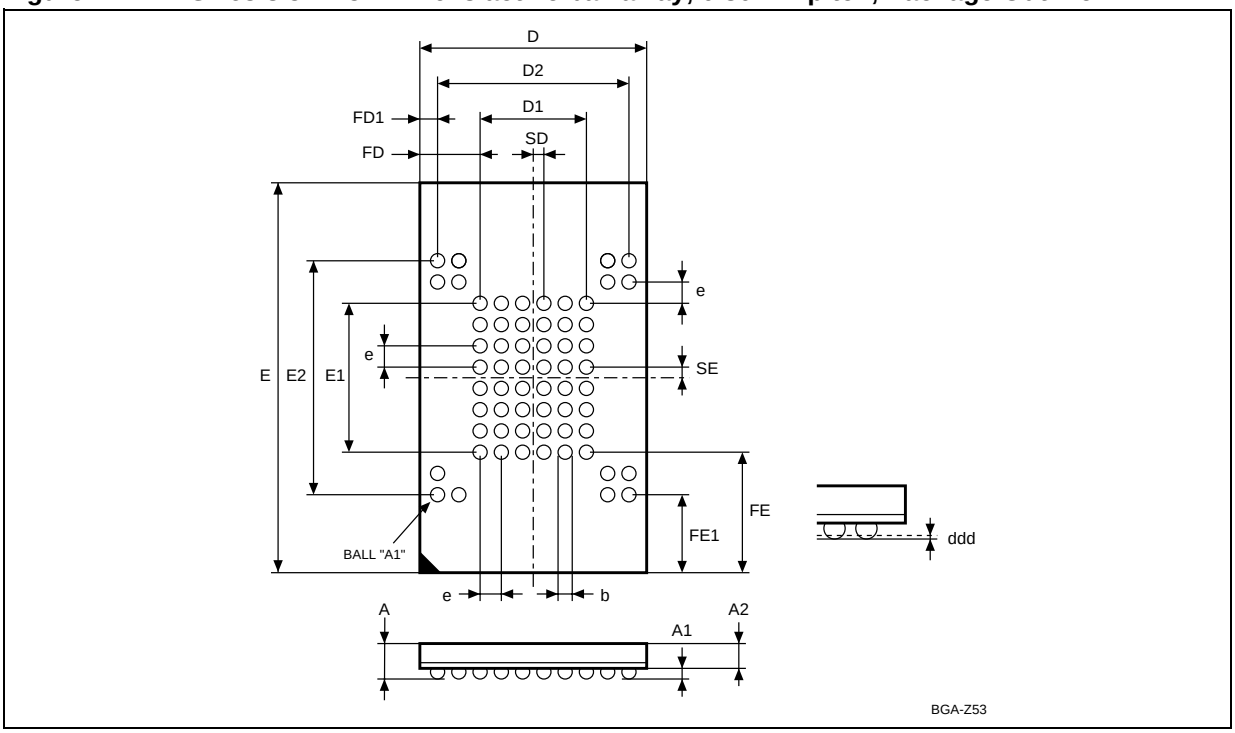


Note: Drawing is not to scale.

Table 26. VFBGA63 8.5 x 15mm - 6x8 active ball array, 0.80mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.050			0.0413
A1		0.250			0.0098	
A2			0.700			0.0276
b	0.450	0.400	0.500	0.0177	0.0157	0.0197
D	8.500	8.400	8.600	0.3346	0.3307	0.3386
D1	4.000			0.1575		
D2	7.200			0.2835		
ddd			0.100			0.0039
E	15.000	14.900	15.100	0.5906	0.5866	0.5945
E1	5.600			0.2205		
E2	8.800			0.3465		
e	0.800			0.0315		
FD	2.250			0.0886		
FD1	0.650			0.0256		
FE	4.700			0.1850		
FE1	3.100			0.1220		
SD	0.400			0.0157		
SE	0.400			0.0157		

Figure 44. TFBGA63 8.5 x 15mm - 6x8 active ball array, 0.80mm pitch, Package Outline



Note: Drawing is not to scale

Table 27. TFBGA63 8.5 x 15mm - 6x8 active ball array, 0.80mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.250			0.0098	
A2		0.600			0.0236	
b	0.450	0.400	0.500	0.0177	0.0157	0.0197
D	8.500	8.400	8.600	0.3346	0.3307	0.3386
D1	4.000			0.1575		
D2	7.200			0.2835		
ddd			0.100			0.0039
E	15.000	14.900	15.100	0.5906	0.5866	0.5945
E1	5.600			0.2205		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	2.250			0.0886		
FD1	0.650			0.0256		
FE	4.700			0.1850		
FE1	3.100			0.1220		
SD	0.400			0.0157		
SE	0.400			0.0157		

PART NUMBERING

Table 28. Ordering Information Scheme

Example: NAND512R3A 0 A ZA 1 T

Device Type
NAND = NAND Flash Memory

Density
128 = 128Mb
256 = 256Mb
512 = 512Mb
01G = 1Gb

Operating Voltage
R = V_{DD} = 1.7 to 1.95V
W = V_{DD} = 2.7 to 3.6V

Bus Width
3 = x8
4 = x16

Family Identifier
A = 528 Bytes/ 264 Word Page

Device Options
0 = No Options
1 = Automatic Page 0 Read at Power-up
2 = Chip Enable Don't Care Enabled
3 = Chip Enable Don't Care Enabled and Automatic Page 0 Read at Power-up

Product Version
A = 120nm process technology
(Single Die 128Mb, 256Mb, 512Mb) (Dual Die 512Mb, 1Gb)

Package
N = TSOP48 12 x 20mm (all devices)
V = WSOP48 12 x 17 x 0.65mm (128Mbit, 256Mbit and 512Mbit devices)
ZA = VFBGA55 8 x 10 x 1mm, 6x8 ball array, 0.8mm pitch (128Mbit and 256Mbit devices)
ZB = TFBGA55 8 x 10 x 1.2mm, 6x8 ball array, 0.8mm pitch (512Mbit Dual Die devices)
ZA = VFBGA63 8.5 x 15 x 1mm, 6x8 ball array, 0.8mm pitch (512Mbit devices)
ZB = TFBGA63 8.5 x 15 x 1.2mm, 6x8 ball array, 0.8mm pitch (1Gbit Dual Die devices)

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
blank = Standard Packing
T = Tape & Reel Packing
E = Lead Free Package, Standard Packing
F = Lead Free Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'.
For further information on any aspect of this device, please contact your nearest ST Sales Office.

APPENDIX A. HARDWARE INTERFACE EXAMPLES

Nand Flash devices can be connected to a microcontroller system bus for code and data storage. For microcontrollers that have an embedded NAND controller the NAND Flash can be connected without the addition of glue logic (see Figure 45.). However a minimum of glue logic is required for general purpose microcontrollers that do not have an embedded NAND controller. The glue logic usually consists of a flip-flop to hold the Chip Enable, Address Latch Enable and Command Latch Enable signals stable during command and address latch operations, and some logic gates to simplify the firmware or make the design more robust.

Figure 46. gives an example of how to connect a NAND Flash to a general purpose microcontroller. The additional OR gates allow the microcontroller's Output Enable and Write Enable signals to be used for other peripherals. The OR gate between A3 and CSn maps the flip-flop and NAND I/O in different address spaces inside the same chip select unit, which improves the setup and hold times and simplifies the firmware. The structure uses the microcontroller DMA (Direct Memory Access) engines to optimize the transfer between the NAND Flash and the system RAM.

For any interface with glue logic, the extra delay caused by the gates and flip-flop must be taken into account. This delay must be added to the microcontroller's AC characteristics and register settings to get the NAND Flash setup and hold times.

For mass storage applications (hard disk emulations or systems where a huge amount of storage is required) NAND Flash memories can be connected together to build storage modules (see Figure 47.).

Figure 45. Connection to Microcontroller, Without Glue Logic

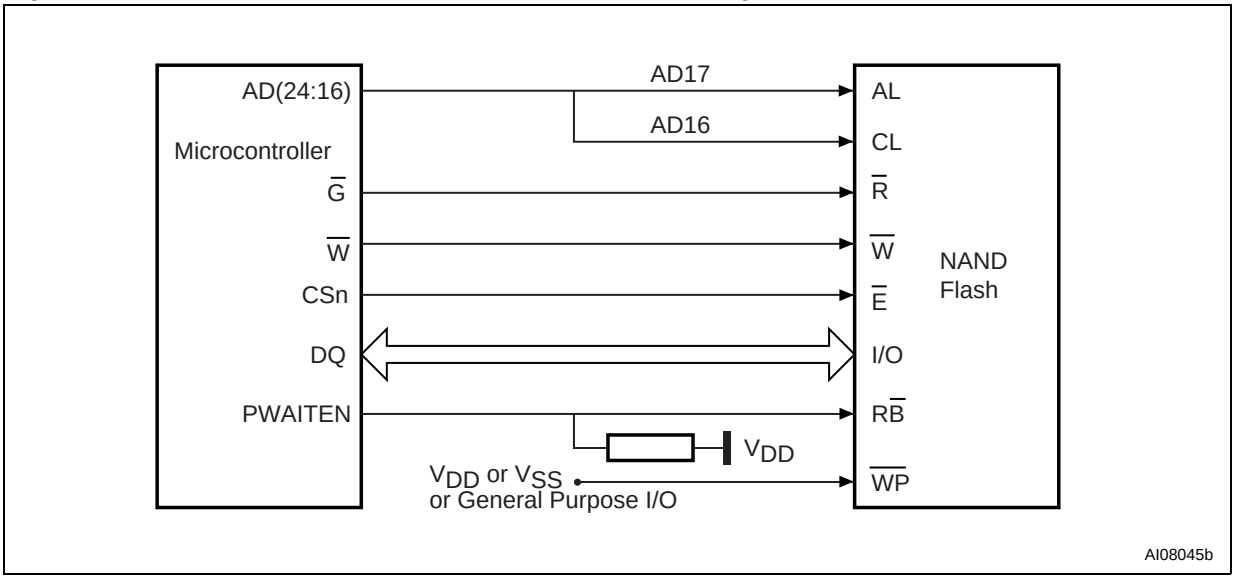


Figure 46. Connection to Microcontroller, With Glue Logic

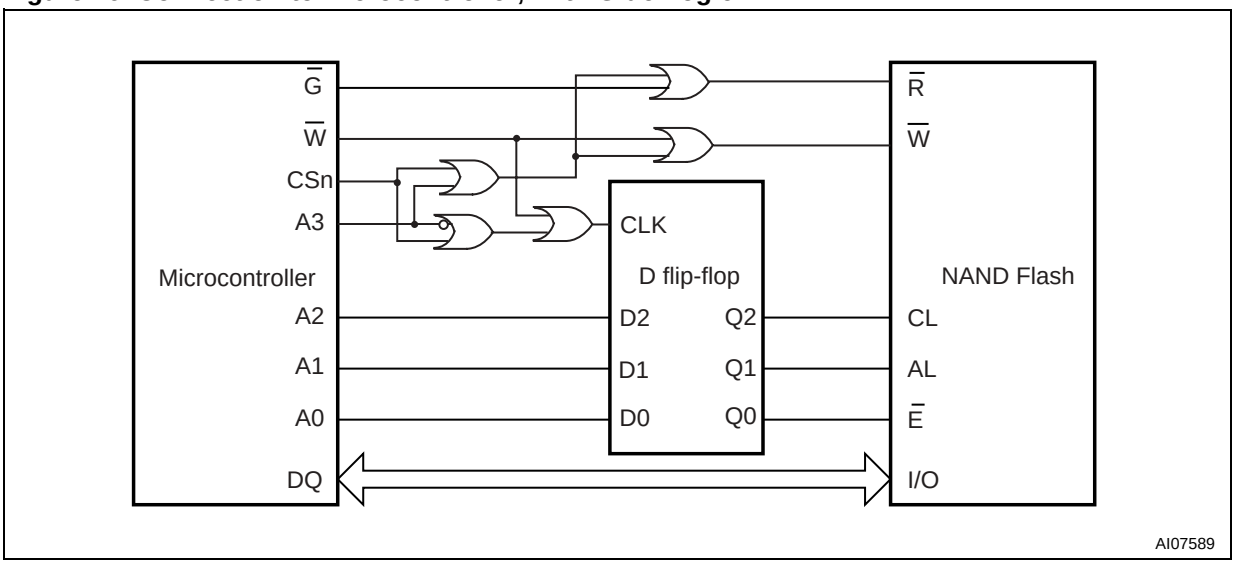
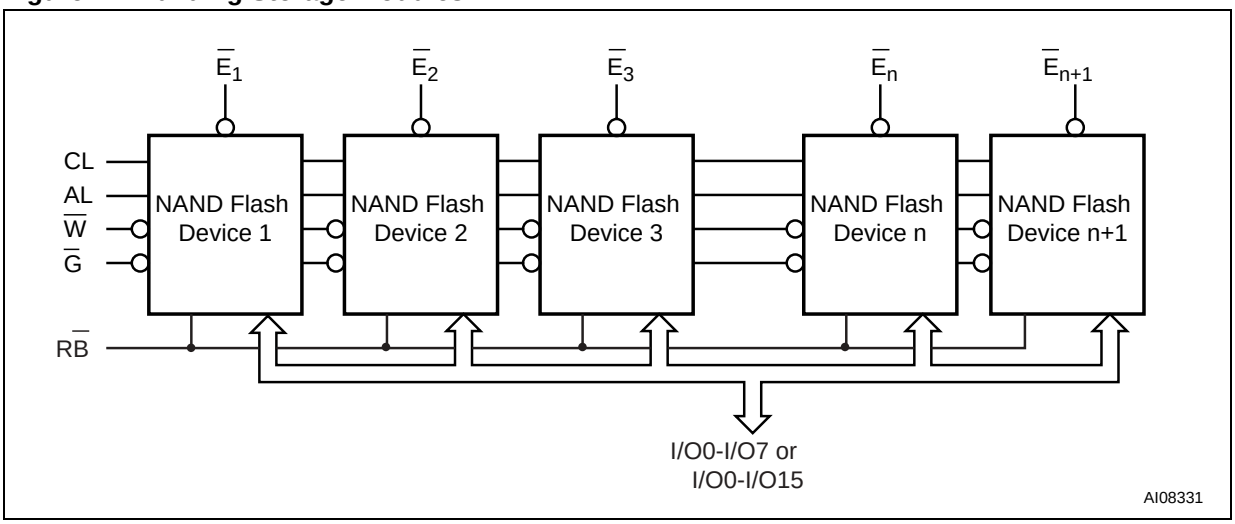


Figure 47. Building Storage Modules



RELATED DOCUMENTATION

STMicroelectronics has published a set of application notes to support the NAND Flash memories. They are available from the ST Website *www.st.com*. or from your local ST Distributor.

REVISION HISTORY

Table 29. Document Revision History

Date	Version	Revision Details
06-Jun-2003	1.0	First Issue
07-Aug-2003	2.0	Design Phase
27-Oct-2003	3.0	Engineering Phase
03-Dec-2003	4.0	Document promoted from Target Specification to Preliminary Data status. V_{CC} changed to V_{DD} and I_{CC} to I_{DD}. Title of Table 2.. changed to "Product Description" and Page Program Typical Timing for NANDXXXR3A devices corrected. Table 1., Product List, inserted on page 2.
13-Apr-2004	5.0	WSOP48 and VFBGA55 packages added, VFBGA63 (9 x 11 x 1mm) removed. Figure 19., Cache Program Operation, modified and note 2 modified. Note removed for t_{WLWH} timing in Table 20., AC Characteristics for Command, Address, Data Input. Meaning of t_{BLBH4} modified, partly replaced by t_{WHBH1} and t_{WHRL} min for 3V devices modified in Table 21., AC Characteristics for Operations. References removed from RELATED DOCUMENTATION section and reference made to ST Website instead. Figure 6., Figure 7., Figure 31. and Figure 34. modified. Read Electronic Signature paragraph clarified and Figure 30., Read Electronic Signature AC Waveform, modified. Note 2 to Figure 32., Read C Operation, One Page AC Waveform, removed. Note 3 to Table 7., Address Insertion, x16 Devices removed. Only 00h Pointer operations are valid before a Cache Program operation. I_{DD4} removed from Table 18., DC Characteristics, 1.8V Devices. Note added to Figure 34., Block Erase AC Waveform. Small text changes.
28-May-2004	6.0	TFBGA55 package added (mechanical data to be announced). 512Mb Dual Die devices added. Figure 19., Cache Program Operation modified. Package code changed for TFBGA63 8.5 x 15 x 1.2mm, 6x8 ball array, 0.8mm pitch (1Gbit Dual Die devices) in Table 28., Ordering Information Scheme.
02-Jul-2004	7.0	Cache Program removed from document. TFBGA55 package specifications added (Figure 42., TFBGA55 8 x 10mm - 6x8 active ball array - 0.80mm pitch, Package Outline and Table 25., TFBGA55 8 x 10mm - 6x8 active ball array - 0.80mm pitch, Package Mechanical Data). Test conditions modified for V_{OL} and V_{OH} parameters in Table 19., DC Characteristics, 3V Devices.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View NAND512W3A2BZA6 on WIN SOURCE
- STMicroelectronics Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management