THE DATASHEET OF

NCP1203D60R2G

NCP1203

PWM Current-Mode Controller for Universal Off-Line Supplies Featuring Standby and Short Circuit Protection

Housed in SOIC−8 or PDIP−8 package, the NCP1203 represents a major leap toward ultra−compact Switchmode Power Supplies and represents an excellent candidate to replace the UC384X devices. Due to its proprietary SMARTMOS™ Very High Voltage Technology, the circuit allows the implementation of complete off−line AC−DC adapters, battery charger and a high−power SMPS with few external components.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz switching frequency, the controller features a high−voltage startup FET which ensures a clean and loss−less startup sequence. Its current−mode control naturally provides good audio−susceptibility and inherent pulse−by−pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip cycle mode and provides improved efficiency at light loads while offering excellent performance in standby conditions. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The NCP1203 also includes an efficient protective circuitry which, in presence of an output over load condition, disables the output pulses while the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto−recovers. Finally, a temperature shutdown with hysteresis helps building safe and robust power supplies.

Features

- High−Voltage Startup Current Source
- Auto−Recovery Internal Output Short−Circuit Protection
- Extremely Low No−Load Standby Power
- Current−Mode with Adjustable Skip−Cycle Capability
- Internal Leading Edge Blanking
- 250 mA Peak Current Capability
- Internally Fixed Frequency at 40 kHz, 60 kHz and 100 kHz
- Direct Optocoupler Connection
- Undervoltage Lockout at 7.8 V Typical
- SPICE Models Available for TRANsient and AC Analysis
- Pin to Pin Compatible with NCP1200
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- AC−DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

ON Semiconductor®

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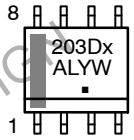
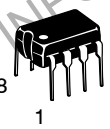
MARKING DIAGRAM

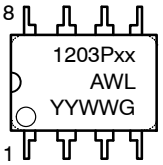
SOIC−8
D1, D2 SUFFIX
CASE 751



x	= 4, 6, or 1
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

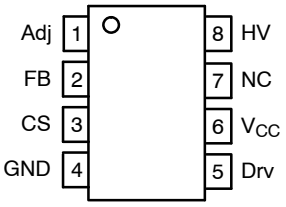


PDIP−8
N SUFFIX
CASE 626



xx	= 40, 60, or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

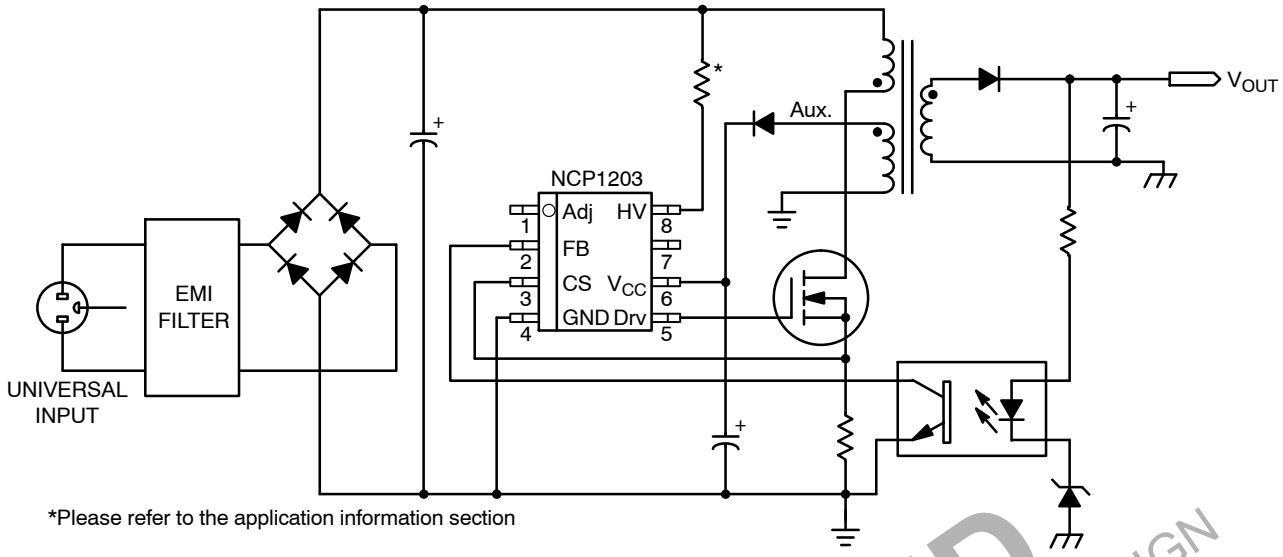


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	Adj	Adjust the skipping peak current	This pin lets you adjust the level at which the cycle skipping process takes place. Shorting this pin to ground, permanently disables the skip cycle feature.
2	FB	Sets the peak current setpoint	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. Skip cycle occurs when FB falls below Vpin1.
3	CS	Current sense input	This pin senses the primary current and routes it to the internal comparator via an L.E.B.
4	GND	The IC ground	–
5	Drv	Driving pulses	The driver's output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 22 μF.
7	NC	–	This unconnected pin ensures adequate creepage distance.
8	HV	Ensure a clean and lossless startup sequence	Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} capacitor during the startup sequence.

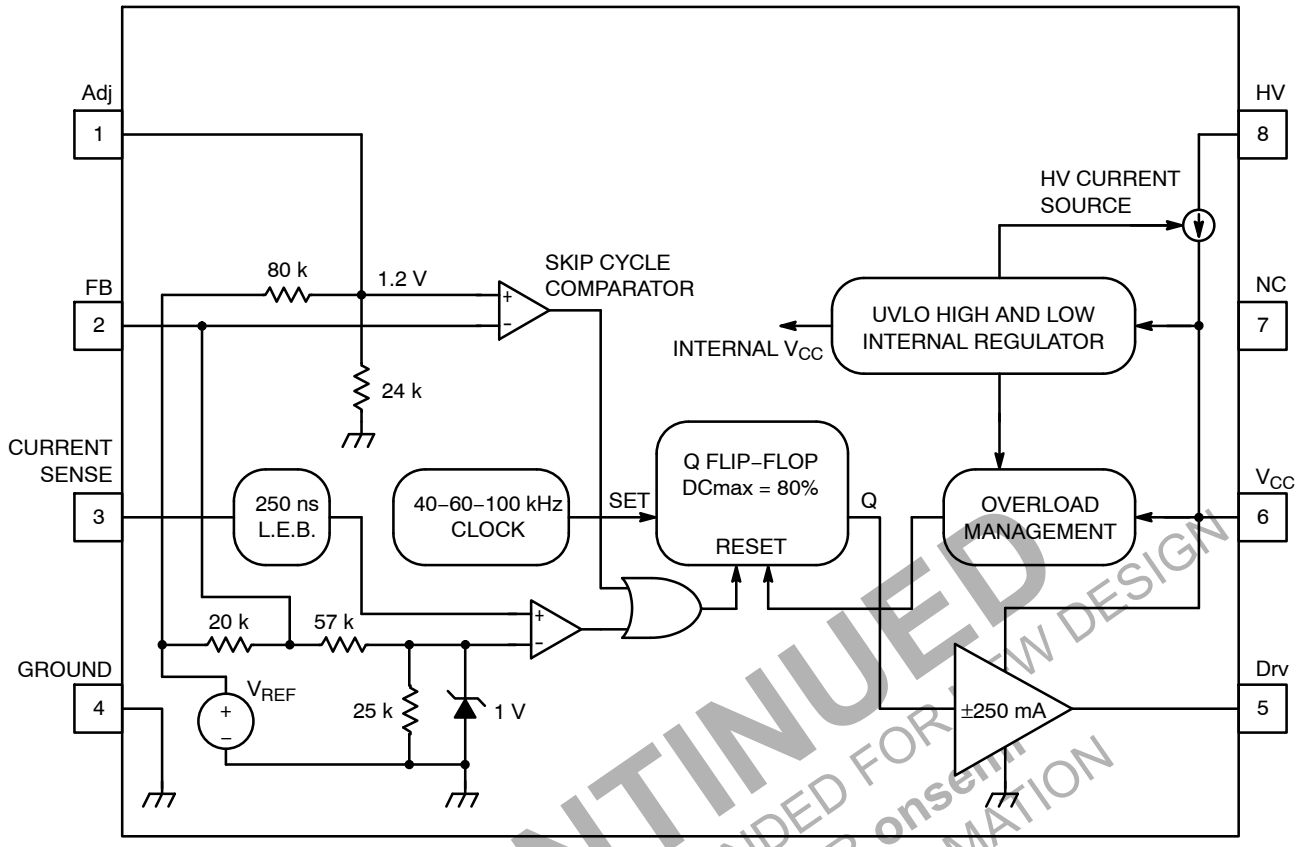


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, Drv	16	V
Power Supply Voltage on all other pins except Pin 5 (Drv), Pin 6 (V_{CC}) and Pin 8 (HV)	–	−0.3 to 10	V
Maximum Current into all pins except Pin 6 (V_{CC}) and Pin 8 (HV) when 10 V ESD diodes are activated	–	5.0	mA
Thermal Resistance, Junction−to−Air, PDIP−8 Version Thermal Resistance, Junction−to−Air, SOIC Version Thermal Resistance, Junction−to−Case	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JC}$	100 178 57	°C/W
Maximum Junction Temperature	TJ_{MAX}	150	°C
Temperature Shutdown	–	170	°C
Hysteresis in Shutdown	–	30	°C
Operating Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Capability, Human Body Model, All pins except Pin 6 (V_{CC}) and Pin 8 (HV)	–	2.0	kV
ESD Capability, Machine Model	–	200	V
Maximum Voltage on Pin 8 (HV) with Pin 6 (V_{CC}) Decoupled to Ground with 10 μF	–	500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection rated using the following tests:
   Human Body Model (HBM) 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V unless otherwise noted.)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Supply Section (All frequency versions, otherwise noted)						
Turn−on Threshold Level, V_{CC} Going Up	$V_{CC(on)}$	6	12.2	12.8	14	V
Minimum Operating Voltage after Turn−on	$V_{CC(min)}$	6	7.2	7.8	8.4	V
V_{CC} Decreasing Level at which the Latchoff Phase Ends	$V_{CClatch}$	6	–	4.9	–	V
Internal IC Consumption, No Output Load on Pin 5	ICC1	6	–	750	880 (Note 1)	μA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 40 kHz	ICC2	6	–	1.2	1.4 (Note 2)	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 60 kHz	ICC2	6	–	1.4	1.6 (Note 2)	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 100 kHz	ICC2	6	–	2.0	2.2 (Note 2)	mA
Internal IC Consumption, Latch−off Phase, V_{CC} = 6.0 V	ICC3	6	–	250	–	μA
Internal Startup Current Source (Pin 8 biased at 50 V)						
High−Voltage Current Source, V_{CC} = 10 V	IC1	8	3.5	6.0	9.0	mA
High−Voltage Current Source, V_{CC} = 0	IC2	8	–	11	–	mA
Drive Output						
Output Voltage Rise−Time @ CL = 1.0 nF, 10−90% of Output Signal	T_r	5	–	67	–	ns
Output Voltage Fall−Time @ CL = 1.0 nF, 10−90% of Output Signal	T_f	5	–	28	–	ns
Source Resistance	R_{OH}	5	27	40	61	Ω
Sink Resistance	R_{OL}	5	5.0	10	20	Ω
Current Comparator (Pin 5 loaded unless otherwise noted)						
Input Bias Current @ 1.0 V Input Level on Pin 3	I_{IB}	3	–	0.02	–	μA
Maximum Internal Current Setpoint (Note 3)	I_{Limit}	3	0.85	0.92	1.0	V
Default Internal Current Setpoint for Skip Cycle Operation	I_{Lskip}	3	–	360	–	mV
Propagation Delay from Current Detection to Gate OFF State	T_{DEL}	3	–	90	160	ns
Leading Edge Blanking Duration (Note 3)	T_{LEB}	3	–	230	–	ns
Internal Oscillator (V_{CC} = 11 V, Pin 5 loaded by 1 nF)						
Oscillation Frequency, 40 kHz Version	f_{OSC}	–	37	42	47	kHz
Oscillation Frequency, 60 kHz Version	f_{OSC}	–	57	65	73	kHz
Oscillation Frequency, 100 kHz Version	f_{OSC}	–	90	103	115	kHz
Maximum Duty−Cycle	Dmax	–	74	80	87	%
Feedback Section (V_{CC} = 11 V, Pin 5 unloaded)						
Internal Pullup Resistor	Rup	2	–	20	–	kΩ
Pin 3 to Current Setpoint Division Ratio	Iratio	–	–	3.3	–	–
Skip Cycle Generation						
Default Skip Mode Level	Vskip	1	1.0	1.2	1.4	V
Pin 1 Internal Output Impedance	Zout	1	–	22	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Max value at T_J = 0°C.
2. Maximum value @ T_J = 25°C, please see characterization curves.
3. Pin 5 loaded by 1 nF.

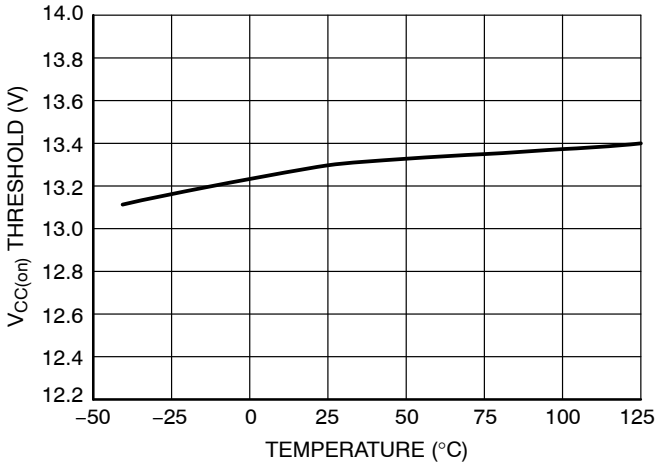


Figure 3. $V_{CC(on)}$ Threshold versus Temperature

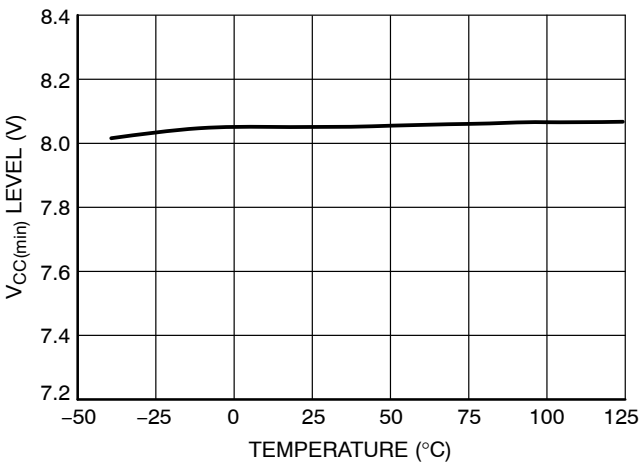


Figure 4. $V_{CC(min)}$ Level versus Temperature

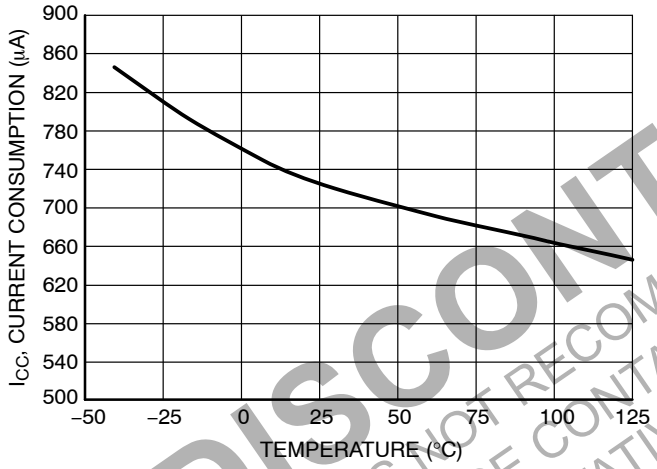


Figure 5. I_C Current Consumption (No Load) versus Temperature

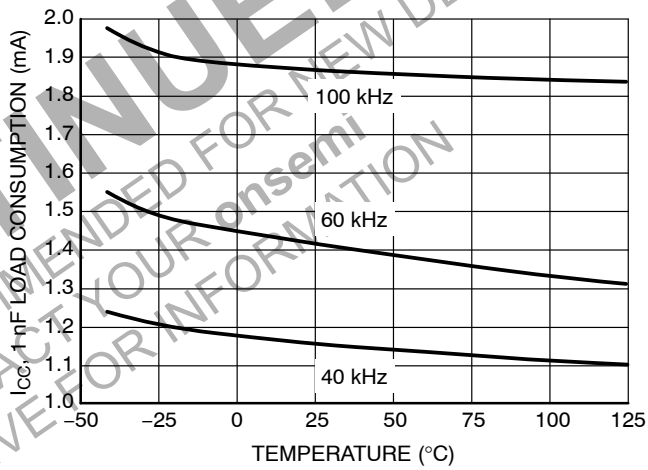


Figure 6. I_{CC} Consumption (Loaded by 1 nF) versus Temperature

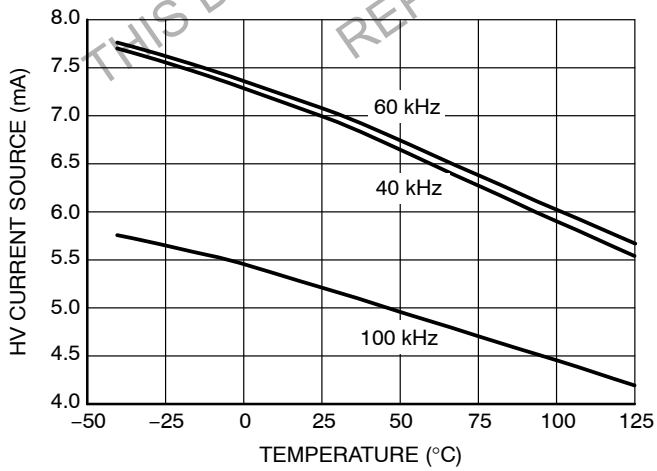


Figure 7. HV Current Source at V_{CC} = 10 V versus Temperature

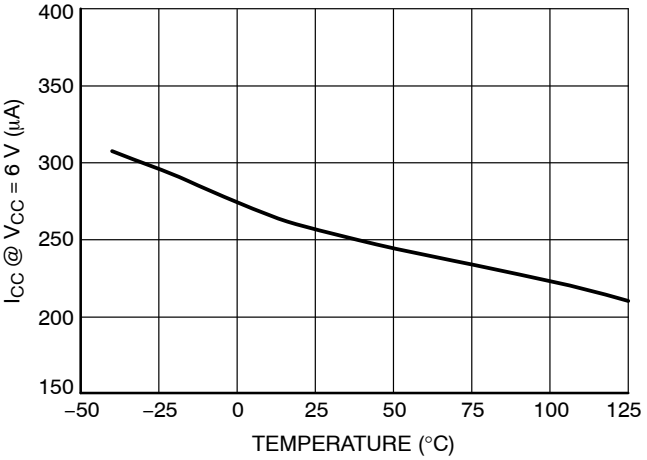


Figure 8. I_C Consumption at V_{CC} = 6 V versus Temperature

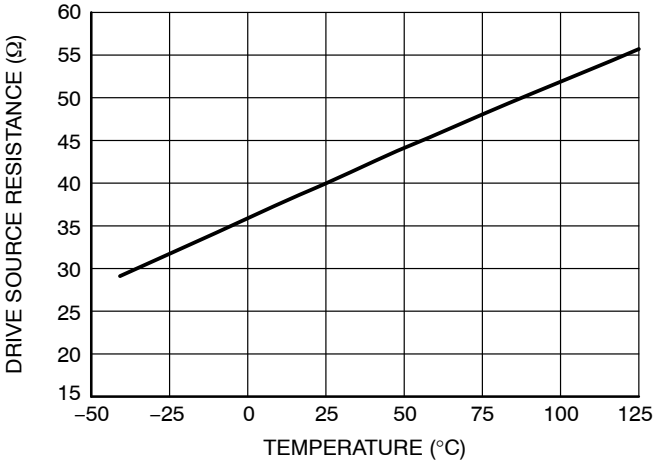


Figure 9. Drive Source Resistance versus Temperature

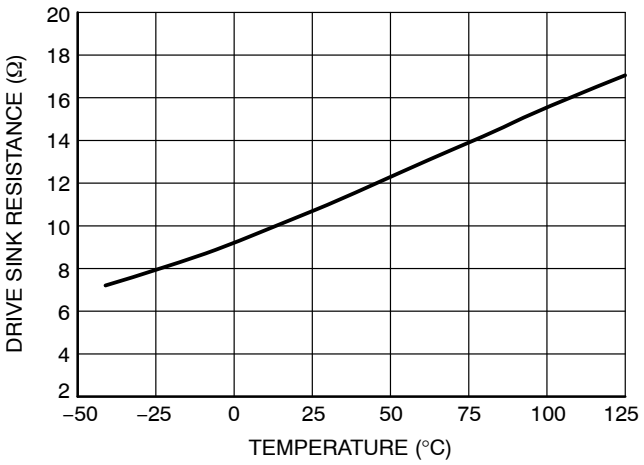


Figure 10. Drive Sink Resistance versus Temperature

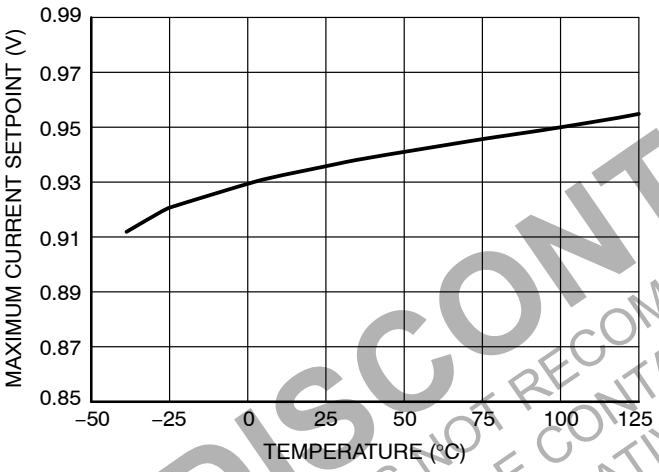


Figure 11. Maximum Current Setpoint versus Temperature

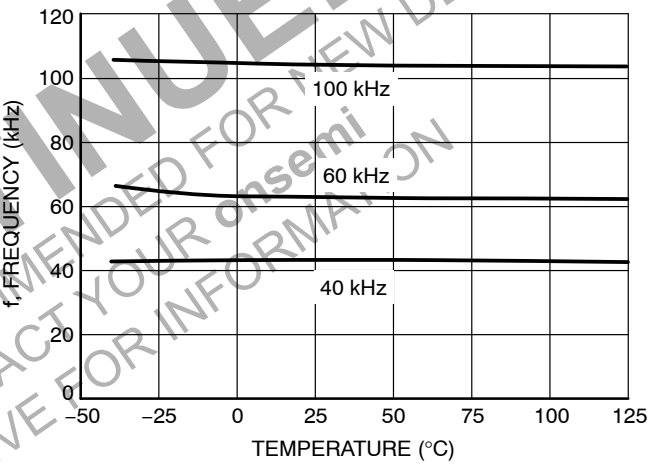


Figure 12. Frequency versus Temperature

APPLICATION INFORMATION

Introduction

The NCP1203 implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC−DC adapters, auxiliary supplies etc. Due to its high−performance SMARTMOS High−Voltage technology, the NCP1203 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low−pass filter and startup device. This later point emphasizes the fact that ON Semiconductor's NCP1203 does not need an external startup resistance but supplies the startup current directly from the high−voltage rail. On the other hand, more and more applications are requiring low no−load standby power, e.g. for AC−DC adapters, VCRs etc. UC384X series have a lot of difficulty to reduce the switching losses at low power levels. NCP1203 elegantly solves this problem by skipping unwanted switching cycles at a user−adjustable power level. By ensuring that skip cycles take place at low peak current, the device ensures quiet, noise free operation. Finally, an auto−recovery output short−circuit protection (OCP) prevents from any lethal thermal runaway in overload conditions.

Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 6.0 mA) is biased and charges up the V_{CC} capacitor. When the voltage on this V_{CC} capacitor reaches the $V_{CC(on)}$ level (typically 12.8 V), the current source turns off and no longer wastes any power. At this time, the V_{CC} capacitor only supplies the controller and the auxiliary supply is supposed to take over before V_{CC} collapses below $V_{CC(min)}$. Figure 13 shows the internal arrangement of this structure:

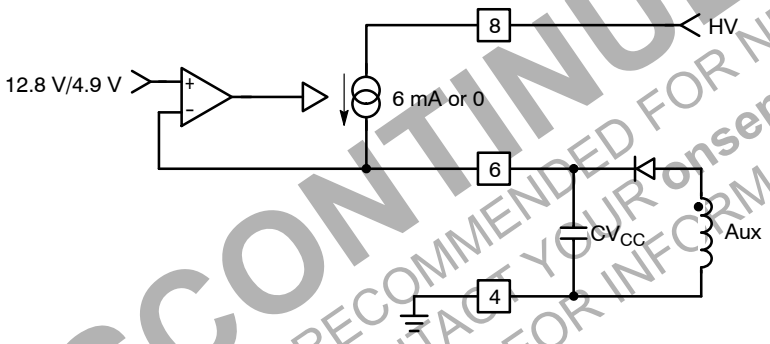


Figure 13. The Current Source Brings V_{CC} Above 12.8 V and then Turns Off

Once the power supply has started, the V_{CC} shall be constrained below 16 V, which is the maximum rating on pin 6. Figure 14 portrays a typical startup sequence with a V_{CC} regulated at 12.5 V:

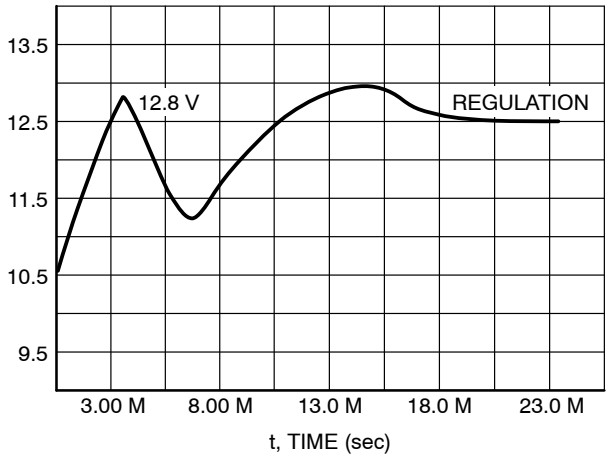


Figure 14. A Typical Startup Sequence for the NCP1203

Current−Mode Operation

As the UC384X series, the NCP1203 features a well−known current mode control architecture which provides superior input audio−susceptibility compared to traditional voltage−mode controllers. Primary current pulse−by−pulse checking together with a fast over current comparator offers greater security in the event of a difficult fault condition, e.g. a saturating transformer.

Adjustable Skip Cycle Level

By offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise−free operation with cheap transformers. Skip cycle offers a proven mean to reduce the standby power in no or light loads situations.

Wide Switching−Frequency Offer

Four different options are available: 40 kHz − 65 kHz − 100 kHz. Depending on the application, the designer can pick up the right device to help reducing magnetics or improve the EMI signature before reaching the 150 kHz starting point.

Overcurrent Protection (OCP)

When the auxiliary winding collapses below UVLOlow, the controller stops switching and reduces its consumption. It stays in this mode until Vcc reaches 4.9 V typical, where the startup source is reactivated and a new startup sequence is attempted. The power supply is thus operated in burst mode and avoids any lethal thermal runaway. When the default goes way, the power supply automatically resumes operation.

Wide Duty−Cycle Operation

Wide mains operation requires a large duty−cycle excursion. The NCP1203 can go up to 80% typically.

Low Standby Power

If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un−needed switching cycles, the NCP1203 drastically reduces the power wasted during light load conditions. In no−load conditions, the NCP1203 allows the total standby power to easily reach next International Energy Agency (IEA) recommendations.

No Acoustic Noise while Operating

Instead of skipping cycles at high peak currents, the NCP1203 waits until the peak current demand falls below a user−adjustable 1/3rd of the maximum limit. As a result, cycle skipping can take place without having a singing transformer … You can thus select cheap magnetic components free of noise problems.

External MOSFET Connection

By leaving the external MOSFET external to the IC, you can select avalanche proof devices which, in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).

SPICE Model

A dedicated model to run transient cycle−by−cycle simulations is available but also an averaged version to help you closing the loop. Ready−to−use templates can be downloaded in OrCAD's Pspice and INTUSOFT's from ON Semiconductor web site, NCP1203 related section.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the auxiliary voltage also decreases because it also operates in Flyback and thus duplicates the output voltage, providing the leakage inductance between windings is kept low. To account for this situation and properly protect the power supply, NCP1203 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty−cycle. The system auto−recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. The auxiliary voltage takes place after a few switching cycles and self−supplies the IC. In presence of a short circuit on the output, the auxiliary voltage will go down until it crosses the undervoltage lockout level of typically 7.8 V. When this happens, NCP1203 immediately stops the switching pulses and unbias all unnecessary logical blocks. The overall consumption drops, while keeping the gate grounded, and the V_{CC} slowly falls down. As soon as V_{CC} reaches typically 4.8 V, the startup source turns−on again and a new startup sequence occurs, bringing V_{CC} toward 12.8 V as an attempt to restart. If the default has gone, then the power supply normally restarts. If not, a new protective burst is initiated, shielding the SMPS from any runaway. Figure 15, on the following page, portrays the typical operating signals in short circuit.

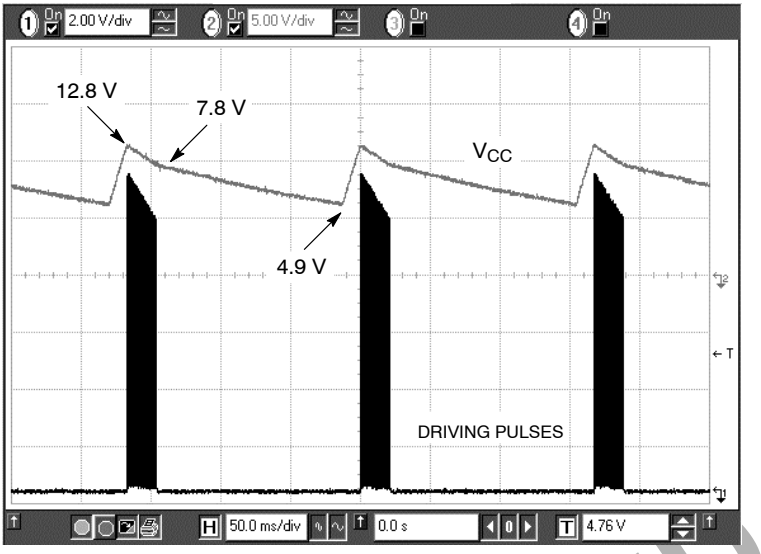


Figure 15. Typical Waveforms in Short Circuit Conditions

Calculating the V_{CC} Capacitor

The V_{CC} capacitor can be calculated knowing the IC consumption as soon as V_{CC} reaches 12.8 V. Suppose that a NCP1203P60 is used and drives a MOSFET with a 30 nC total gate charge (Qg). The total average current is thus made of ICC1 (700 μA) plus the driver current, Fsw x Qg or 1.8 mA. The total current is therefore 2.5 mA. The ΔV available to fully startup the circuit (e.g. never reach the 7.8 V UVLO during power on) is 12.8–7.8 = 5 V. We have a capacitor who then needs to supply the NCP1203 with 2.5 mA during a given time until the auxiliary supply takes over. Suppose that this time was measured at around 15 ms. CV_{CC} is calculated using the equation $C = \frac{\Delta t \cdot i}{\Delta V}$ or $C \geq 7.5$ μF. Select a 22 μF/16 V and this will fit.

Skipping Cycle Mode

The NCP1203 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level (Vpin 1), the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 17). Suppose we have the following component values:

Lp, primary inductance = 350 μH
Fsw , switching frequency = 61 kHz
Ip skip = 600 mA (or 333 mV/Rsense)

The theoretical power transfer is therefore:

$$\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw = 3.8\ W$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 3.8 . 0.1 = 380 mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

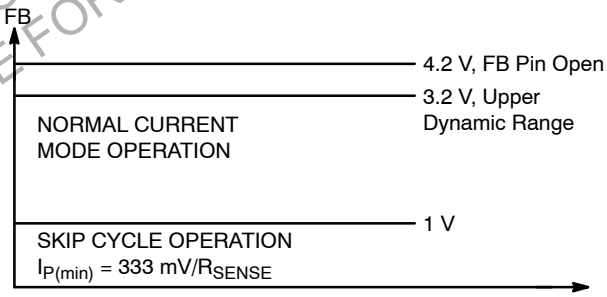


Figure 16.

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V/Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1/3.3/Rsense. The user still has the flexibility to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. Grounding pin 1 permanently invalidates the skip cycle operation. However, given the extremely low standby power the controller can reach, the PWM in no−load conditions can quickly enter the minimum t_{on} and still transfer too much power. An instability can take place. We recommend in that case to leave a little bit of skip level to always allow 0% duty cycle.

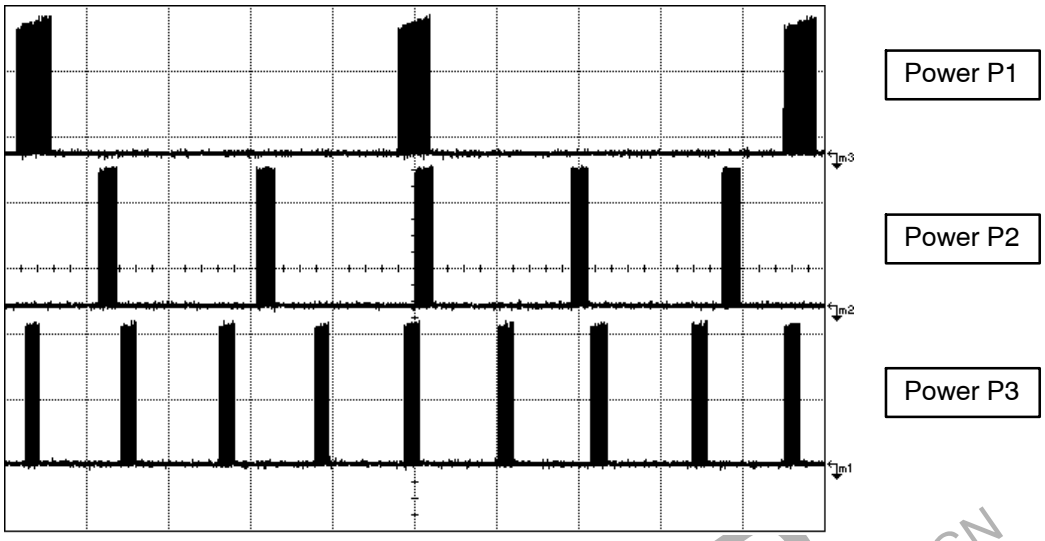


Figure 17. Output Pulses at Various Power Levels (X = 5.0 μs/div) P1 < P2 < P3

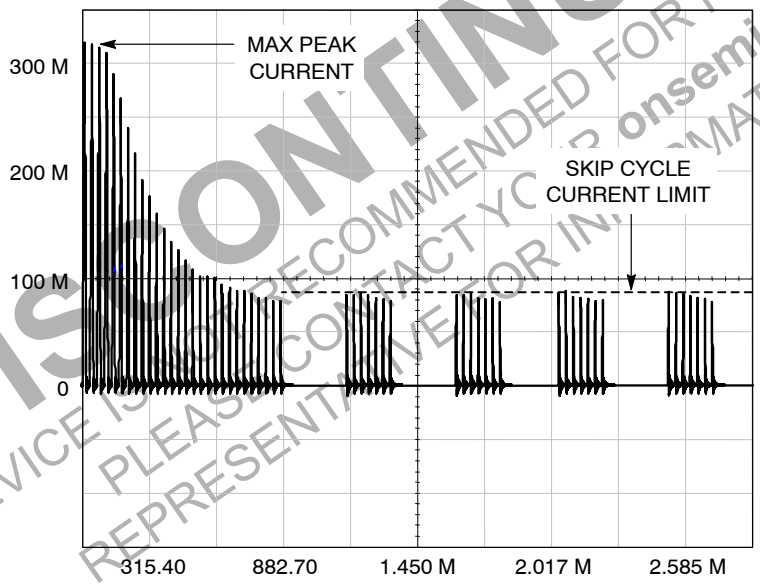


Figure 18. The Skip Cycle Takes Place at Low Peak Currents which Guaranties Noise−Free Operation

We recommend a pin 1 operation between 400 mV and 1.3 V that will fix the skip peak current level between 120 mV/Rsense and 390 mV/Rsense.

Non−Latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj pin 1 level, the output pulses are disabled as long as FB is pulled below pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 19 depicts the application example.

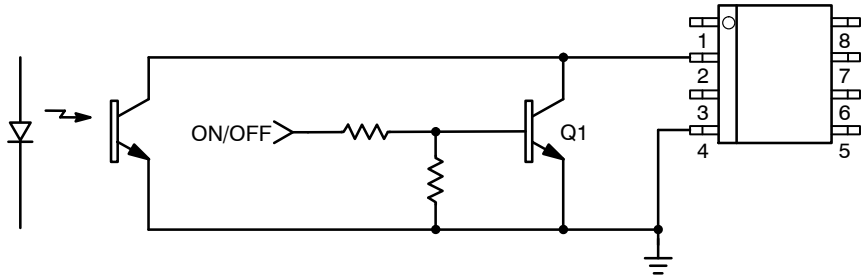


Figure 19. Another Way of Shutting Down the IC without a Definitive Latch−Off State

Full Latching Shutdown

Other applications require a full latching shutdown, e.g. when an abnormal situation is detected (overtemperature or overvoltage). This feature can easily be implemented through two external transistors wired as a discrete SCR. When the V_{CC} level exceeds the zener breakdown voltage, the NPN biases the PNP and fires the equivalent SCR, permanently bringing down the FB pin. The switching pulses are disabled until the user unplugs the power supply.

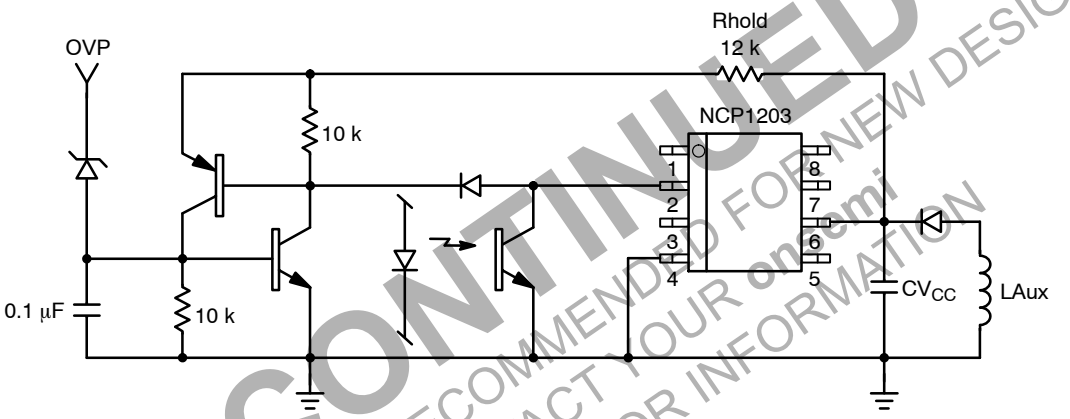


Figure 20. Two Bipolars Ensure a Total Latch−Off of the SMPS in Presence of an OVP

Rhold ensures that the SCR stays on when fired. The bias current flowing through Rhold should be small enough to let the V_{CC} ramp up (12.8 V) and down (4.9 V) when the SCR is fired. The NPN base can also receive a signal from a temperature sensor. Typical bipolars can be MMBT2222 and MMBT2907 for the discrete latch. The MMBT3946 features two bipolars NPN+PNP in the same package and could also be used.

Protecting the Controller Against Negative Spikes

As with any controller built upon a CMOS technology, it is the designer's duty to avoid the presence of negative spikes on sensitive pins. Negative signals have the bad habit to forward bias the controller substrate and induce erratic behaviors. Sometimes, the injection can be so strong that internal parasitic SCRs are triggered, engendering irremediable damages to the IC if they are a low impedance path is offered between V_{CC} and GND. If the current sense pin is often the seat of such spurious signals, the high−voltage pin can also be the source of problems in certain circumstances. During the turn−off sequence, e.g. when the user un−plugs the power supply, the controller is still fed by its V_{CC} capacitor and keeps activating the MOSFET ON and OFF with a peak current limited by Rsense. Unfortunately, if the quality coefficient Q of the resonating network formed by Lp and Cbulk is low (e.g. the MOSFET Rdson + Rsense are small), conditions are met to make the circuit resonate and thus negatively bias the controller. Since we are talking about ms pulses, the amount of injected charge (Q = I x t) immediately latches the controller which brutally discharges its V_{CC} capacitor. If this V_{CC} capacitor is of sufficient value, its stored energy damages the controller. Figure 21 depicts a typical negative shot occurring on the HV pin where the brutal V_{CC} discharge testifies for latchup.

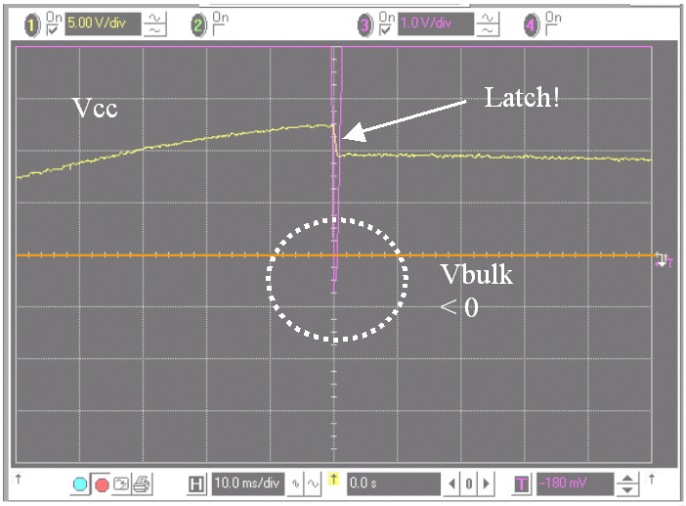


Figure 21. A negative spike takes place on the Bulk capacitor at the switch−off sequence

Simple and inexpensive cures exist to prevent from internal parasitic SCR activation. One of them consists in inserting a resistor in series with the high−voltage pin to keep the negative current to the lowest when the bulk becomes negative (Figure 22). Please note that the negative spike is clamped to –2 x Vf due to the diode bridge. Also, the power dissipation of this resistor is extremely small since it only heats up during the startup sequence.

Another option (Figure 23) consists in wiring a diode from V_{CC} to the bulk capacitor to force V_{CC} to reach UVLOlow sooner and thus stops the switching activity before the bulk capacitor gets deeply discharged. For security reasons, two diodes can be connected in series.

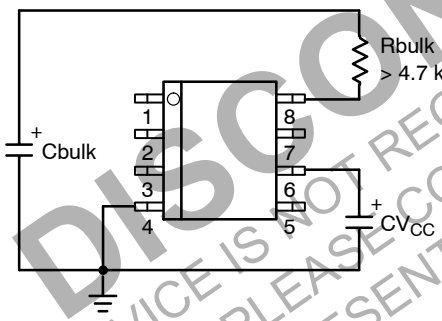


Figure 22. A simple resistor in series avoids any latchup in the controller

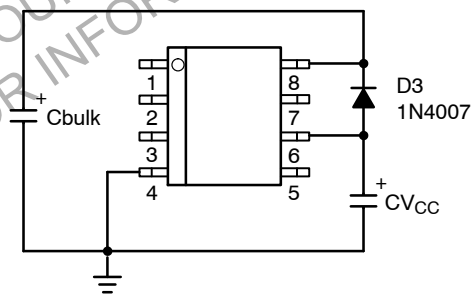


Figure 23. or a diode forces V_{CC} to reach UVLOlow sooner

ORDERING INFORMATION

Device	Package	Shipping†
NCP1203P40G	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1203D40R2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCP1203P60G	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1203D60R2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCP1203P100G	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1203D100R2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

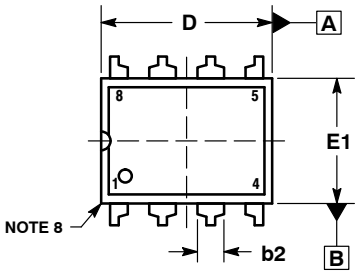
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

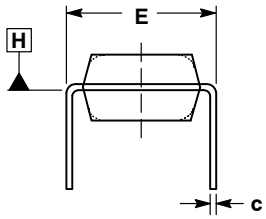
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

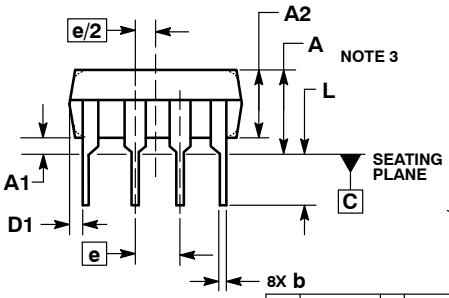
DATE 22 APR 2015



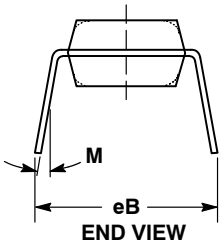
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



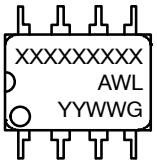
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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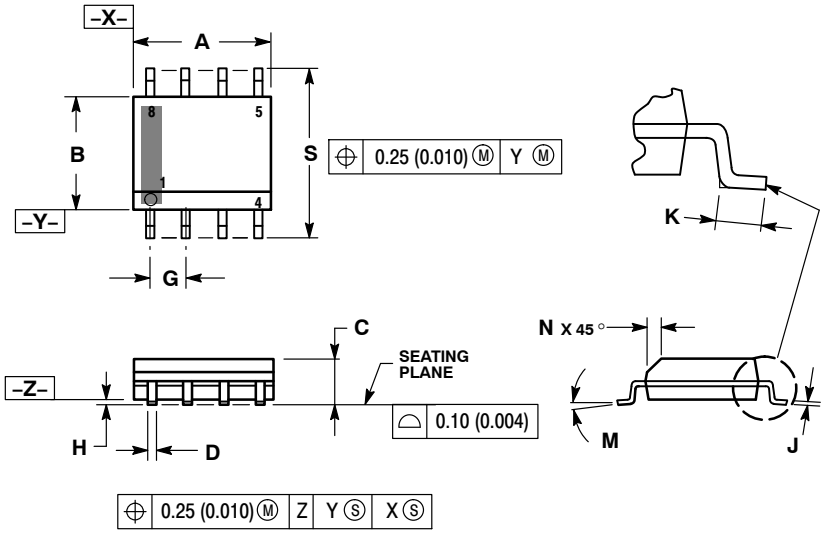
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

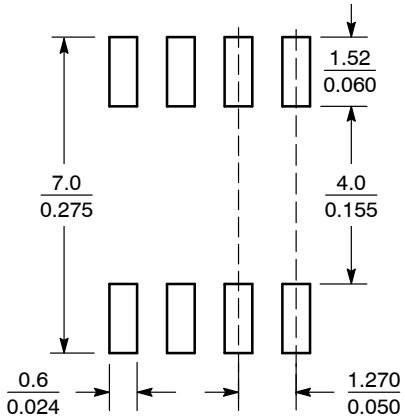
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

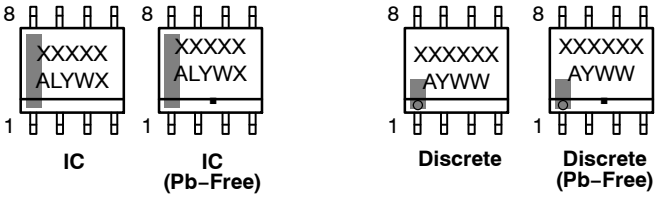
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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