# THE DATASHEET OF

# NCP3012DTBR2G

# NCP3012

# Synchronous PWM Controller

The NCP3012 is a PWM device designed to operate from a wide input range and is capable of producing an output voltage as low as 0.8 V. The NCP3012 provides integrated gate drivers and an internally set 75 kHz oscillator. The NCP3012 has an externally compensated transconductance error amplifier with an internally fixed soft−start. The NCP3012 incorporates output voltage monitoring with a Power Good pin to indicate that the system is in regulation. The dual function SYNC pin synchronizes the device to a higher frequency (Slave Mode) or outputs a 180° out−of−phase clock signal to drive another NCP3012 (Master Mode). Protection features include lossless current limit and short circuit protection, output overvoltage and undervoltage protection, and input undervoltage lockout. The NCP3012 is available in a 14−pin TSSOP package.

### Features

- Input Voltage Range from 4.7 V to 28 V
- 75 kHz Operation
- 0.8 V ±1.0% Reference Voltage
- Buffered External +1.25 V Reference
- Current Limit and Short Circuit Protection
- Power Good
- Enable/Disable Pin
- Input Undervoltage Lockout
- External Synchronization
- Output Overvoltage and Undervoltage Protection
- This is a Pb−Free Device

### Typical Applications

- Set Top Box
- Power Modules
- ASIC / DSP Power Supply

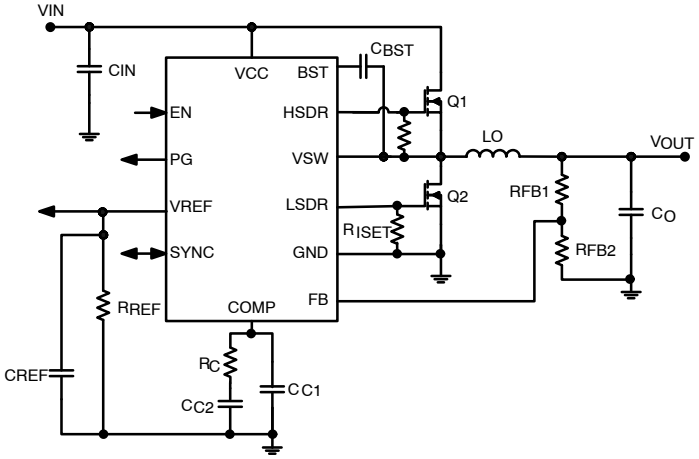


**Figure 1. Typical Application Circuit**

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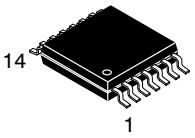
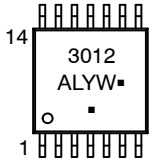


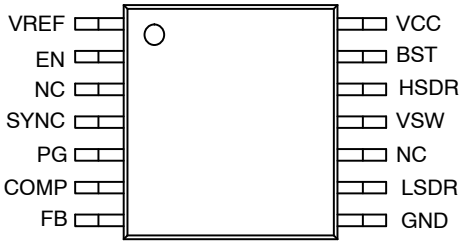

**TSSOP−14**
**DT SUFFIX**
**CASE 948G**

### MARKING DIAGRAM




3012= Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

### PIN CONNECTIONS




(TOP VIEW)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCP3012DTBR2G | TSSOP−14 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

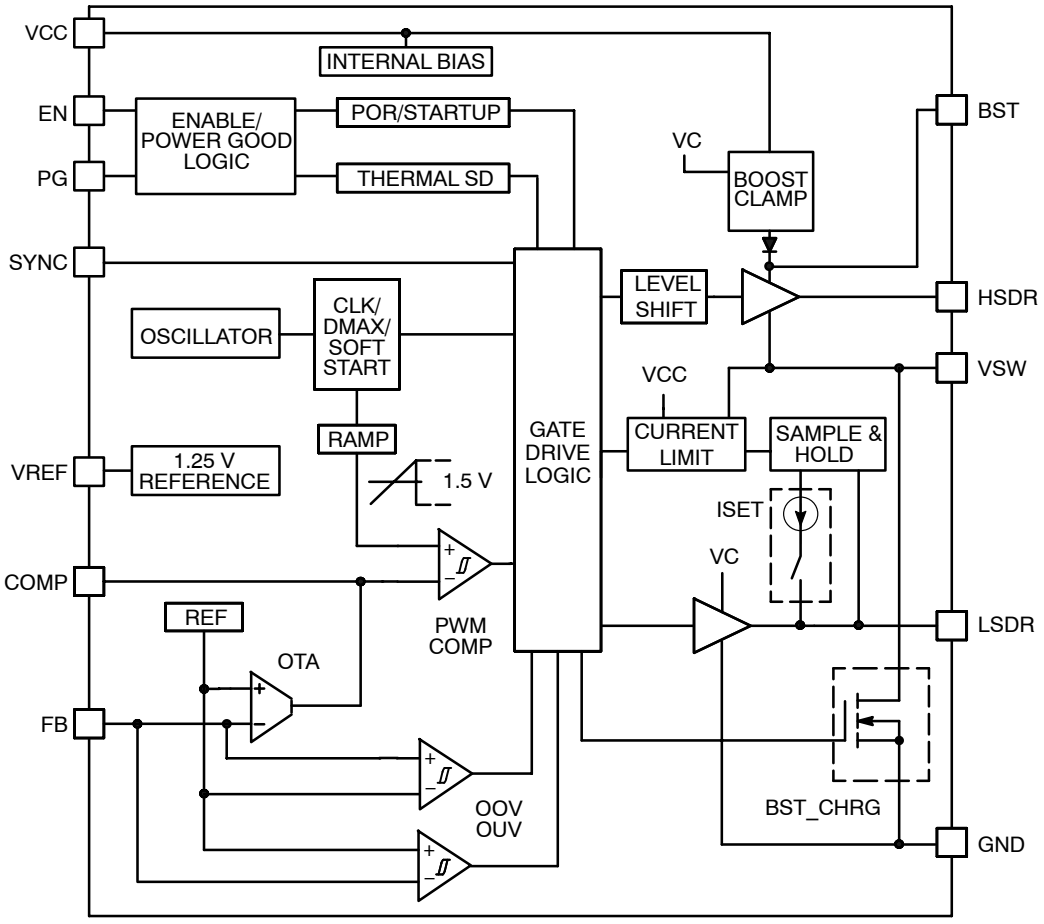



**Figure 2. NCP3012 Block Diagram**

**PIN FUNCTION DESCRIPTION**

| Pin | Pin Name | Description |
|---|---|---|
| 1 | VREF | The VREF pin is the output for a 1.25 V reference (1 mA max). A 100 kΩ resistor in parallel with a 1 μF ceramic capacitor must be connected from this pin to GND to ensure external reference stability. |
| 2 | EN | The EN pin is the enable/disable input. A logic high on this pin enables the device. This pin has also an internal current source pull up. A 10 kΩ resistor should be connected in series with this pin if $V_{EN}$ is externally biased from a separate supply. |
| 3 | NC | Not Connected |
| 4 | SYNC | The dual function SYNC pin synchronizes the device to a higher frequency (Slave Mode). Alternately, it outputs an 85 kHz clock signal with 180° of phase shift (Master Mode). Connect a 60 kΩ resistor from SYNC to GND to enable Master Mode. No resistor is required for Slave Mode. |
| 5 | PG | The Power Good pin is an open drain output that is low when the regulated output voltage is beyond the “Power Good” upper and lower thresholds. Otherwise, it is a high impedance pin. |
| 6 | COMP | The COMP pin connects to the output of the Operational Transconductance Amplifier (OTA) and the positive terminal of the PWM comparator. This pin is used in conjunction with the FB pin to compensate the voltage mode control feedback loop. |
| 7 | FB | The FB pin is connected to the inverting input of the OTA. This pin is used in conjunction with the COMP pin to compensate the voltage mode control feedback loop. |
| 8 | GND | Ground Pin |
| 9 | LSDR | The LSDR pin is connected to the output of the low side driver which connects to the gate of the low side N−FET. It is also used to set the threshold of the current limit circuit ($I_{SET}$) by connecting a resistor from LSDR to GND. |
| 10 | NC | Not Connected |
| 11 | VSW | The VSW pin is the return path for the high side driver. It is also used in conjunction with the $V_{CC}$ pin to sense current in the high side MOSFET. |
| 12 | HSDR | The HSDR pin is connected to the output of the high side driver which connects to the gate of the high side N−FET. |
| 13 | BST | The BST pin is the supply rail for the gate drivers. A capacitor must be connected between this pin and the VSW pin. |
| 14 | $V_{CC}$ | The $V_{CC}$ pin is the main voltage supply input. It is also used in conjunction with the VSW pin to sense current in the high side MOSFET. |

**ABSOLUTE MAXIMUM RATINGS** (measured vs. GND pin 8, unless otherwise noted)

| Rating | Symbol | $V_{MAX}$ | $V_{MIN}$ | Unit |
|---|---|---|---|---|
| High Side Drive Boost Pin | BST | 45 | −0.3 | V |
| Boost to $V_{SW}$ differential voltage | BST−$V_{SW}$ | 13.2 | −0.3 | V |
| COMP | COMP | 5.5 | −0.3 | V |
| Enable | EN | 5.5 | −0.3 | V |
| Feedback | FB | 5.5 | −0.3 | V |
| High−Side Driver Output | HSDR | 40 | −0.3 | V |
| Low−Side Driver Output | LSDR | 13.2 | −0.3 | V |
| Power Good | PG | 5.5 | −0.3 | V |
| Synchronization | SYNC | 5.5 | −0.3 | V |
| Main Supply Voltage Input | $V_{CC}$ | 40 | −0.3 | V |
| External Reference | VREF | 5.5 | −0.3 | V |
| Switch Node Voltage | $V_{SW}$ | 40 | −0.6 | V |
| Maximum Average Current<br>$V_{CC}$, BST, HSDRV, LSDRV, $V_{SW}$, GND<br>REF<br>EN<br>SYNC<br>PG | $I_{max}$ | 130<br>7.1<br>2.5<br>11<br>4 | | mA |
| Operating Junction Temperature Range (Note 1) | $T_J$ | −40 to +140 | | °C |
| Maximum Junction Temperature | $T_{J(MAX)}$ | +150 | | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | | °C |
| Thermal Characteristics (Note 2)<br>TSSOP−14 Plastic Package<br>Thermal Resistance Junction−to−Air | $R_{\theta JA}$ | 190 | | °C/W |
| Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free (Note 3) | $R_F$ | 260 Peak | | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. When mounted on minimum recommended FR−4 or G−10 board
3. 60−180 seconds minimum above 237°C.

**ELECTRICAL CHARACTERISTICS** (−40°C < $T_J$ < +125°C, $V_{CC}$ = 12 V, for min/max values unless otherwise noted)

| Characteristic | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage Range | – | 4.7 | | 28 | V |
| **SUPPLY CURRENT** | | | | | |
| Quiescent Supply Current | EN = 0 $V_{CC}$ = 12 V | – | 2.5 | 4.0 | mA |
| $V_{CC}$ Supply Current | $V_{FB}$ = 0.75 V, Switching, $V_{CC}$ = 4.7 V | – | 5.8 | 8.0 | mA |
| $V_{CC}$ Supply Current | $V_{FB}$ = 0.75 V, Switching, $V_{CC}$ = 28 V | – | 6.0 | 12 | mA |
| **UNDER VOLTAGE LOCKOUT** | | | | | |
| UVLO Rising Threshold | $V_{CC}$ Rising Edge | 3.8 | 4.3 | 4.7 | V |
| UVLO Falling Threshold | $V_{CC}$ Falling Edge | 3.5 | 4.0 | 4.3 | V |
| **OSCILLATOR** | | | | | |
| Oscillator Frequency | $T_J$ = +25°C, 4.7 V ≤ $V_{CC}$ ≤ 28 V | 65 | 75 | 85 | kHz |
| | $T_J$ = −40°C to +125°C, 4.7 V ≤ $V_{CC}$ ≤ 28 V | 62 | 75 | 88 | kHz |
| Ramp−Amplitude Voltage | $V_{peak}$ − $V_{alley}$ | – | 1.5 | – | V |
| Ramp Valley Voltage | | 0.44 | 0.8 | 0.96 | V |
| **PWM** | | | | | |
| Minimum Duty Cycle | | – | 7 | – | % |
| Maximum Duty Cycle | | 82 | 86 | – | % |
| Soft Start Ramp Time | $V_{FB}$ = $V_{COMP}$ | – | 14 | – | ms |
| **EXTERNAL VOLTAGE REFERENCE** | | | | | |
| VREF Voltage | $I_{REF}$ = 1 mA | 1.14 | 1.25 | 1.35 | V |
| VREF Line Regulation | $V_{CC}$ = 4.7 V − 28 V | −1 | – | +1 | % |
| VREF Load Regulation | $I_{REF}$ = 0 mA to 1.5 mA | −2 | −0.2 | +2 | % |
| Short Circuit Output Current | $V_{REF}$ = 0 V | 4.5 | 5.7 | 7.0 | mA |
| **ENABLE** | | | | | |
| Enable Threshold High | | – | – | 3.4 | V |
| Enable Threshold Low | | 1.0 | – | – | V |
| Enable Source Current | | 20 | 50 | 90 | μA |
| **POWER GOOD** | | | | | |
| Power Good High Threshold | $V_{CC}$ = 12 V | 0.72 | 0.89 | 1.06 | V |
| Power Good Low Threshold | $V_{CC}$ = 12 V | 0.65 | 0.71 | 0.75 | V |
| Power Good Low Voltage | $V_{CC}$ = 12 V, $I_{PG}$ = 4 mA | 0.13 | 0.22 | 0.35 | V |
| **SYNC** | | | | | |
| SYNC Input High Threshold | | – | – | 2.0 | V |
| SYNC Output High | 10 μA load | – | 5.0 | – | V |
| SYNC Output Low | | – | 90 | – | mV |
| Phase Delay | (Note 4) | – | 200 | – | ° |
| SYNC Drive Current (Sourcing) | | – | 1.6 | – | mA |
| Master Threshold Current | | 5.0 | 14.4 | 25 | μA |
| Master Frequency | | 70 | 85 | 100 | kHz |

4. Guaranteed by design.
5. The voltage sensed across the high side MOSFET during conduction.
6. This assumes 100 pF capacitance to ground on the COMP Pin and a typical internal $R_o$ of > 10 MΩ.
7. This is not a protection feature.

**ELECTRICAL CHARACTERISTICS** ($-40°C < T_J < +125°C$, $V_{CC}$ = 12 V, for min/max values unless otherwise noted)

| Characteristic | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ERROR AMPLIFIER (GM)** | | | | | |
| Transconductance | | 0.9 | 1.33 | 1.9 | mS |
| Open Loop dc Gain | (Notes 4 and 6) | – | 70 | – | dB |
| Output Source Current<br>Output Sink Current | | 45<br>45 | 70<br>70 | 100<br>100 | μA<br>μA |
| FB Input Bias Current | | – | 0.5 | 500 | nA |
| Feedback Voltage | $T_J$ = 25 C<br><br>$-40°C < T_J < +125°C$,<br>4.7 V < $V_{IN}$ < 28 V | 0.792<br><br>0.788 | 0.8<br><br>0.8 | 0.808<br><br>0.812 | V<br><br>V |
| COMP High Voltage | $V_{FB}$ = 0.75 V | 4.0 | 4.4 | 5.0 | V |
| COMP Low Voltage | $V_{FB}$ = 0.85 V | – | 60 | – | mV |
| **OUTPUT VOLTAGE FAULTS** | | | | | |
| Feedback OOV Threshold | | 0.8 | 1.0 | 1.1 | V |
| Feedback OUV Threshold | | 0.55 | 0.59 | 0.65 | V |
| **OVER CURRENT** | | | | | |
| ISET Source Current | | 7.0 | 14 | 18 | μA |
| Current Limit Set Voltage (Note 5) | $R_{SET}$ = 22.2 kΩ | 140 | 240 | 360 | mV |
| **GATE DRIVERS AND BOOST CLAMP** | | | | | |
| HSDRV Pullup Resistance | $V_{CC}$ = 8 V and $V_{BST}$ = 7.5 V<br>$V_{SW}$ = GND, 100 mA out of HSDR pin | 4.0 | 10.5 | 20 | Ω |
| HSDRV Pulldown Resistance | $V_{CC}$ = 8 V and $V_{BST}$ = 7.5 V<br>$V_{SW}$ = GND, 100 mA into HSDR pin | 2.0 | 5.0 | 11.5 | Ω |
| LSDRV Pullup Resistance | $V_{CC}$ = 8 V and $V_{BST}$ = 7.5 V<br>$V_{SW}$ = GND, 100 mA out of LSDR pin | 3.0 | 8.9 | 16 | Ω |
| LSDRV Pulldown Resistance | $V_{CC}$ = 8 V and $V_{BST}$ = 7.5 V<br>$V_{SW}$ = GND, 100 mA into LSDR pin | 1.0 | 2.8 | 6.0 | Ω |
| HSDRV falling to LSDRV Rising Delay | $V_{CC}$ and $V_{BST}$ = 8 V | 50 | 85 | 110 | ns |
| LSDRV Falling to HSDRV Rising Delay | $V_{CC}$ and $V_{BST}$ = 8 V | 60 | 85 | 120 | ns |
| Boost Clamp Voltage | $V_{IN}$ = 12 V, $V_{SW}$ = GND, $V_{COMP}$ = 1.3 V | 5.5 | 7.5 | 9.6 | V |
| **THERMAL SHUTDOWN** | | | | | |
| Thermal Shutdown | (Notes 4 and 7) | – | 150 | – | °C |
| Hysteresis | (Notes 4 and 7) | – | 15 | – | °C |

4. Guaranteed by design.
5. The voltage sensed across the high side MOSFET during conduction.
6. This assumes 100 pF capacitance to ground on the COMP Pin and a typical internal $R_o$ of > 10 MΩ.
7. This is not a protection feature.

## TYPICAL PERFORMANCE CHARACTERISTICS

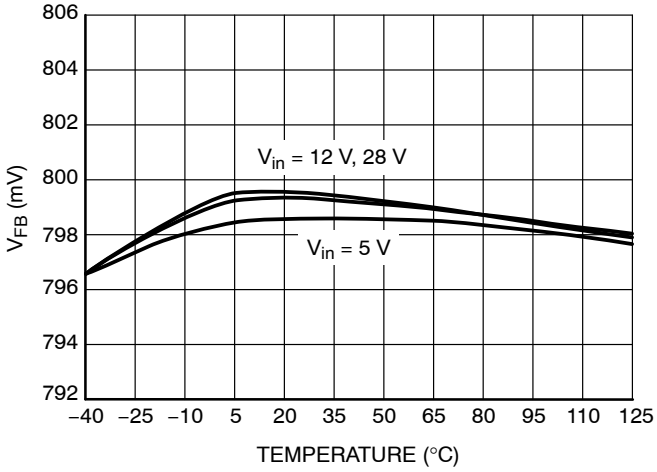



**Figure 3. Feedback Reference Voltage vs. Input Voltage and Temperature**

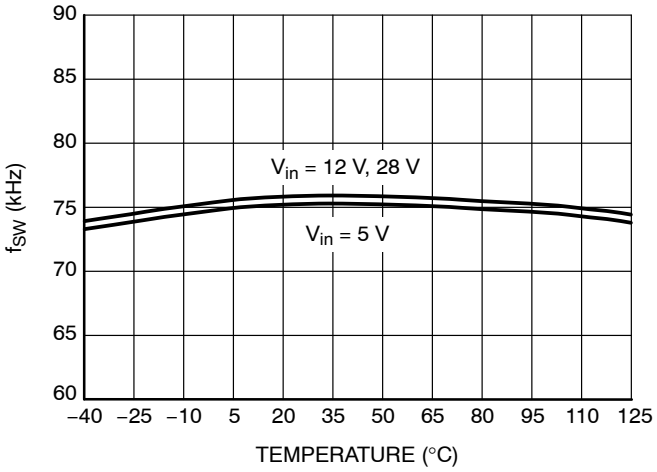



**Figure 4. Switching Frequency vs. Input Voltage and Temperature**

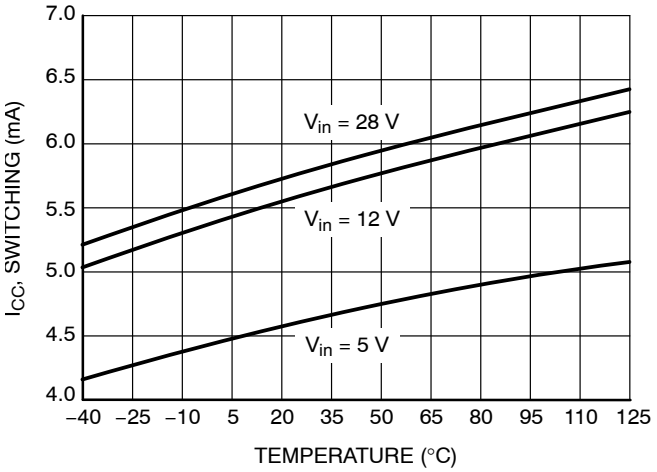



**Figure 5. Supply Current vs. Input Voltage and Temperature**

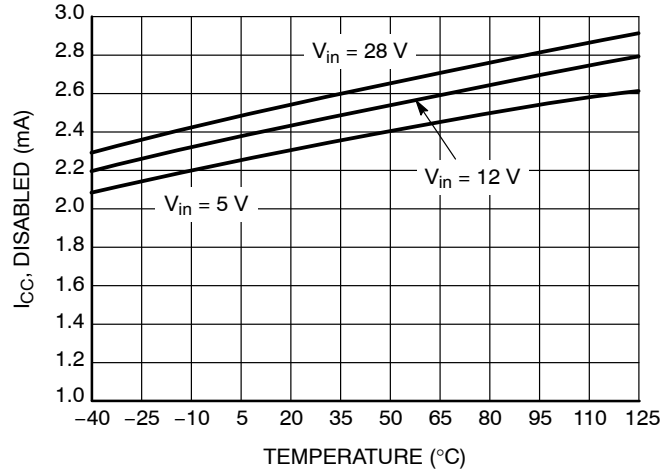



**Figure 6. Supply Current (Disabled) vs. Input Voltage and Temperature**

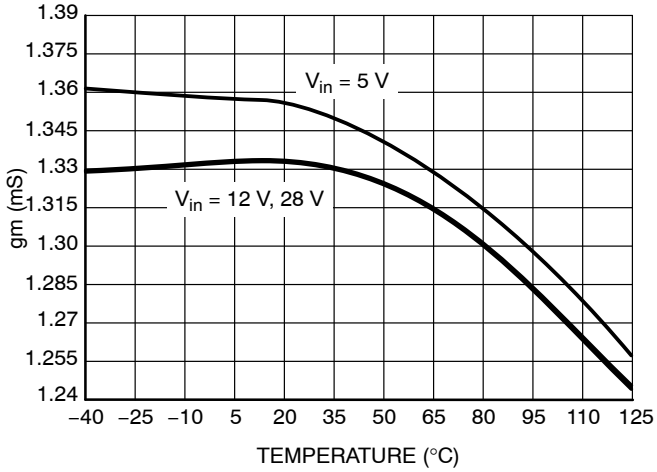



**Figure 7. Transconductance vs. Input Voltage and Temperature**

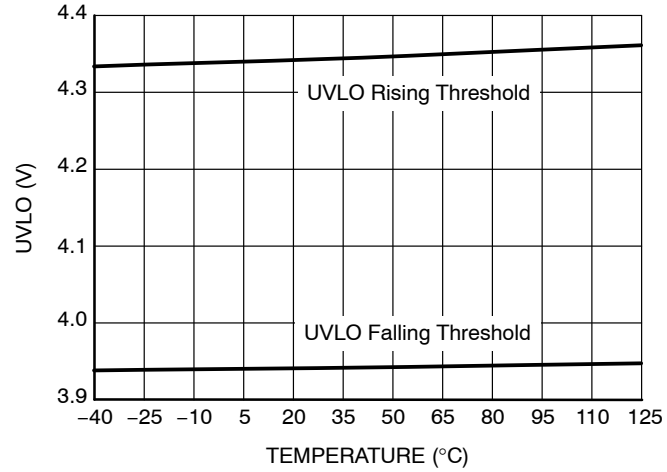



**Figure 8. Input Undervoltage Lockout vs. Temperature**

## TYPICAL PERFORMANCE CHARACTERISTICS

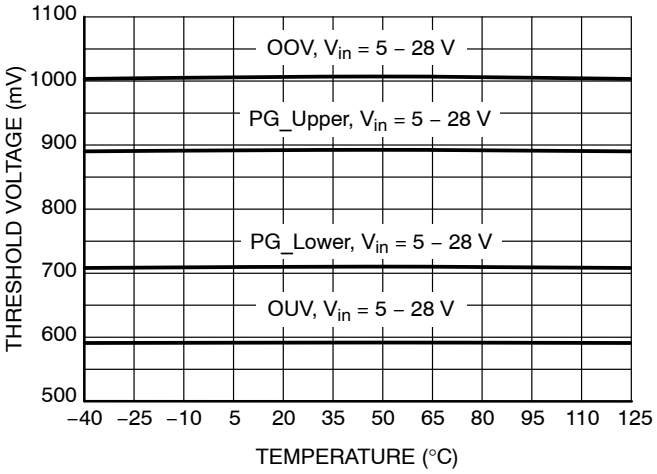



**Figure 9. Output Voltage Thresholds vs. Input Voltage and Temperature**

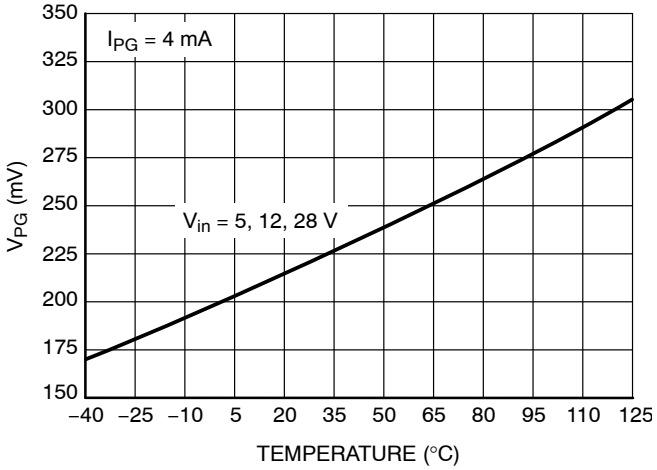



**Figure 10. Power Good Output Low Voltage vs. Input Voltage and Temperature**

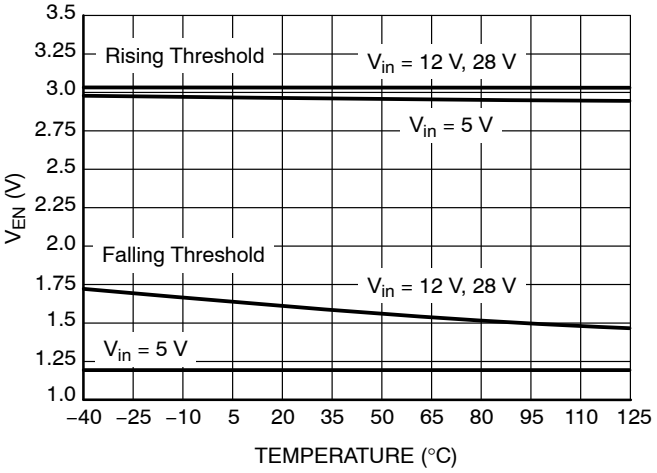



**Figure 11. Enable Thresold vs. Input Voltage and Temperature**

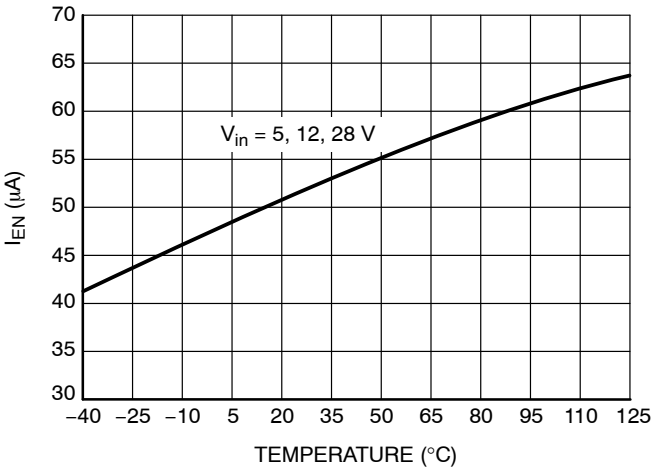



**Figure 12. Enable Pullup Current vs. Input Voltage and Temperature**

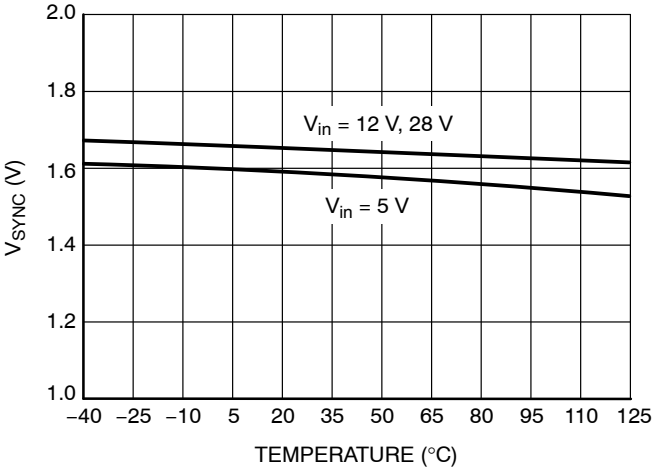



**Figure 13. SYNC Threshold vs. Input Voltage and Temperature**

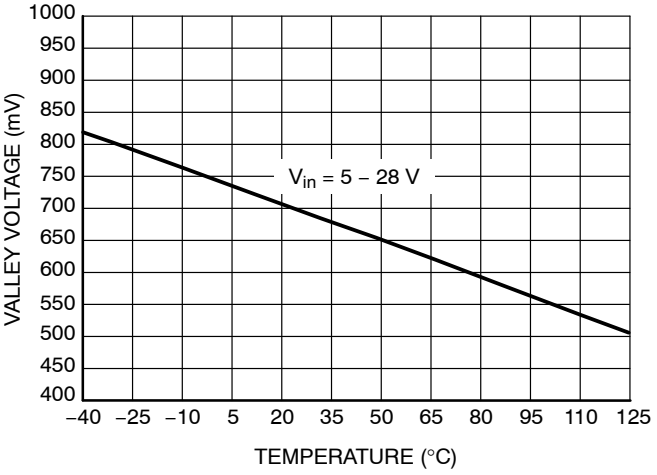



**Figure 14. Valley Voltage vs. Input Voltage and Temperature**

## TYPICAL PERFORMANCE CHARACTERISTICS

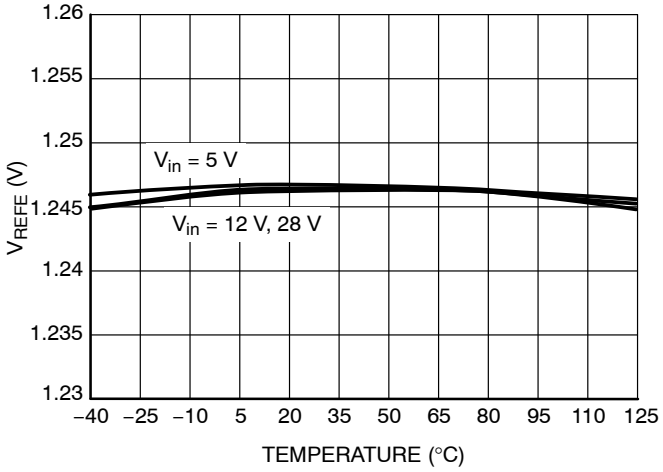



**Figure 15. External Reference Voltage vs. Input Voltage and Temperature**

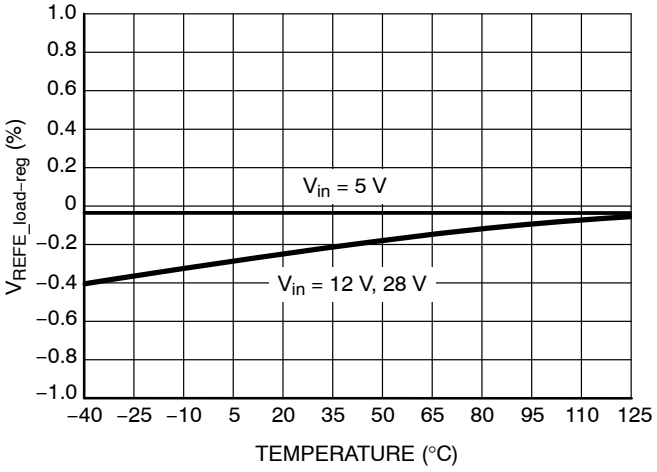



**Figure 16. External Reference Voltage vs. Input Voltage and Temperature**

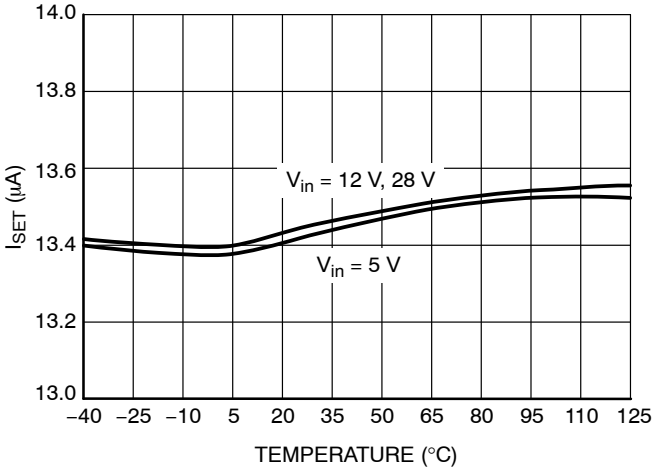



**Figure 17. Current Limit Set Current vs. Temperature**

## DETAILED DESCRIPTION

### OVERVIEW

The NCP3012 operates as a 75 kHz, voltage−mode, pulse−width−modulated, (PWM) synchronous buck converter. It drives high−side and low−side N−channel power MOSFETs. The NCP3012 incorporates an internal boost circuit consisting of a boost Clamp and boost diode to provide supply voltage for the high side MOSFET Gate driver. The NCP3012 also integrates several protection features including input undervoltage lockout (UVLO), output undervoltage (OUV), output overvoltage (OOV), adjustable high−side current limit ($I_{SET}$ and $I_{LIM}$), and thermal shutdown (TSD). The NCP3012 includes a Power Good (PG) open drain output which flags out of regulation conditions.

The operational transconductance amplifier (OTA) provides a high gain error signal which is compared to the internal ramp signal using the PWM comparator. This results in a voltage mode PWM feedback stage. The PWM signal is sent to the internal gate drivers to modulate MOSFET on and off times. The gate driver stage incorporates symmetrical fixed non−overlap time between the high−side and low−side MOSFET gate drives.

The NCP3012 has a dual function Master/Slave SYNC pin In Slave mode, the NCP3012 synchronizes to an external clock signal. In Master mode, the NCP3012 can output a phase shifted clock signal to drive another master slave equipped power stage to provide a 180° switching relationship between the power stages. This can help to reduce the required input filter capacitance in multi−stage power converters.

The external 1.25 V reference voltage (VREF) is provided for system level use. It remains active even when the NCP3012 is disabled.

### POR and UVLO

The device contains an internal Power On Reset (POR) and input Undervoltage Lockout (UVLO) that inhibits the internal logic and the output stage from operating until $V_{CC}$ reaches their respective predefined voltage levels. The internal logic takes approximately 50 μs to check the SYNC pin and determine if the device is in Master mode or Slave mode once the voltage at $V_{CC}$ exceeds the rising UVLO threshold. The device remains in Standby if enable is not asserted following the 50 μs time period.

### Enable/Disable

The device has an enable pin (EN) with internal 50 μA pullup current. This gives the user the option of driving EN with a push−pull or open−drain/collector enable signal. When driving EN with an external logic supply a 10 kΩ series current limiting resistor must be placed in series with EN. See Figure 18. The maximum enable threshold is 3.4 V. If no external drive voltage is available, the internal pullup can be used to enable the device, and an open drain/collector input, such as a MOSFET or BJT can be used to disable the device. A capacitor connected between EN and ground can be used with the internal pullup current source to provide a fixed delay to turn−on and turn off. See Equation 1.

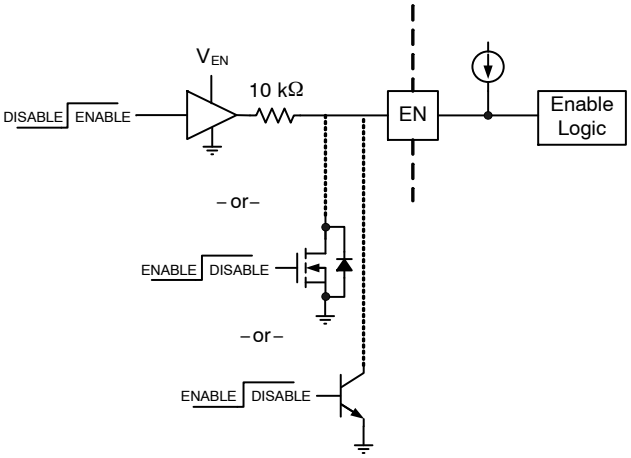



**Figure 18. Enable Circuits: Push−Pull, Open−Drain, or Open−Collector**

$$C_{EN\_DLY} = \frac{I_{PU} \times T_{EN\_DLY}}{V_{EN\_TH}} \qquad \text{(eq. 1)}$$

$C_{EN\_DLY}$ = Delay Capacitance (F)
$I_{PU}$ = Pullup Current
$V_{EN\_TH}$ = Enable Input High Threshold Voltage
$T_{EN\_DLY}$ = Desired Delay Time

### Startup and Shutdown

Once enable is asserted the device begins its startup process. Closed−loop soft−start begins after a 400 μs delay wherein the boost capacitor is charged, and the current limit threshold is set. During the 400 μs delay the OTA output is set to just below the valley voltage of the internal ramp. This is done to reduce delays and to ensure a consistent pre soft−start condition. The device increases the internal reference from 0 V to 0.8 V in 32 discrete steps while maintaining closed loop regulation at each step. Some overshoot may be evident at the start of each step depending on the voltage loop phase margin and bandwidth. See Figure 19. The total soft−start time is 14 ms.

The soft−stop process begins once the EN pin voltage goes below the input low threshold. Soft−stop decreases the internal reference from 0.8 V − 0 V in 32 steps as with Soft−Start. Soft−Stop finishes with one “last” high side gate pulse at half the period of the prior pulse. This helps ensure positive inductor current following turn off at light loads, which prevents negative output voltage.

Enable low during Soft−Start will result in Soft−Stop down counting from that step. Likewise, Enable high during Soft−Stop will result in Soft−Start up counting from that step.

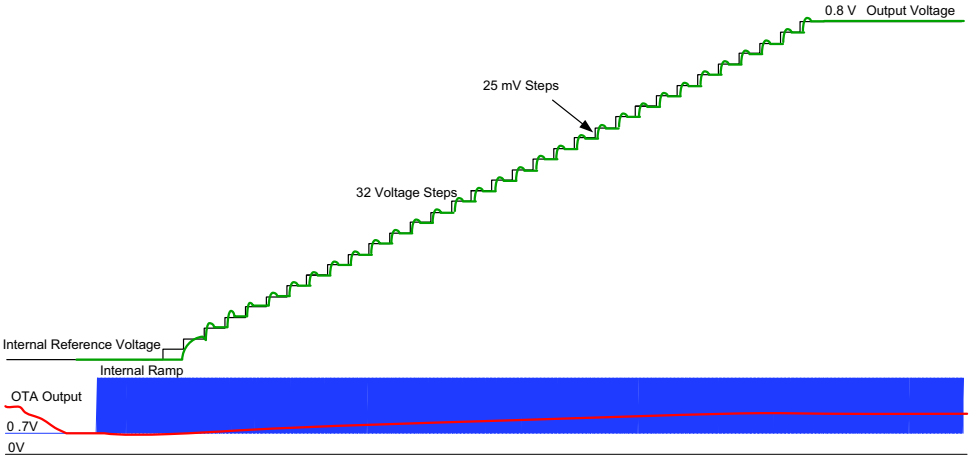



**Figure 19. Soft−Start Details**

### Master/Slave Synchronization

The SYNC pin performs two functions. The first function is to identify if the device is a master or a slave. The second function is to either synchronize to an external clock (Slave Mode) or provide an external clock that is shifted by 180° from the high side switch (Master Mode). The typical application circuit for this is shown in Figure 20.

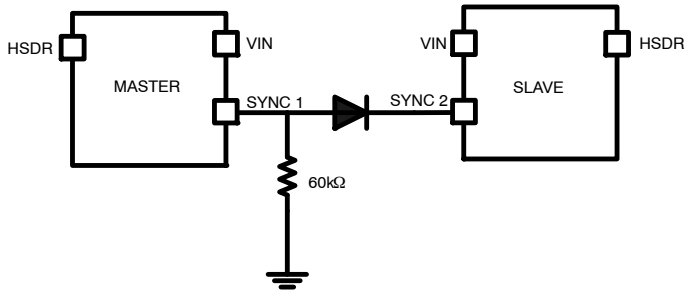



**Figure 20. Master Slave Typical Application**

Upon initial power up, the device determines if it is a Master or Slave by applying 1.25 V to the SYNC pin and determining whether the current draw from the pin is greater than the Master Threshold Current ($ISYNC_{TRIP}$). If $ISYNC_{TRIP}$ is exceeded then the device enters master mode. If the current is less than $ISYNC_{TRIP}$ the device enters slave mode. Once identified as a Master, the device switching frequency is increased by 15%. See Equation 2.

$$R_{Master} = \frac{SYNC_{ref}}{ISYNC_{TRIP}} \quad \text{(eq. 2)}$$

$R_{Master}$ = Master Select Resistor (Ω)

$SYNC_{ref}$ = Sync Reference Voltage (V)

$ISYNC_{TRIP}$ = Master Threshold Current (A)

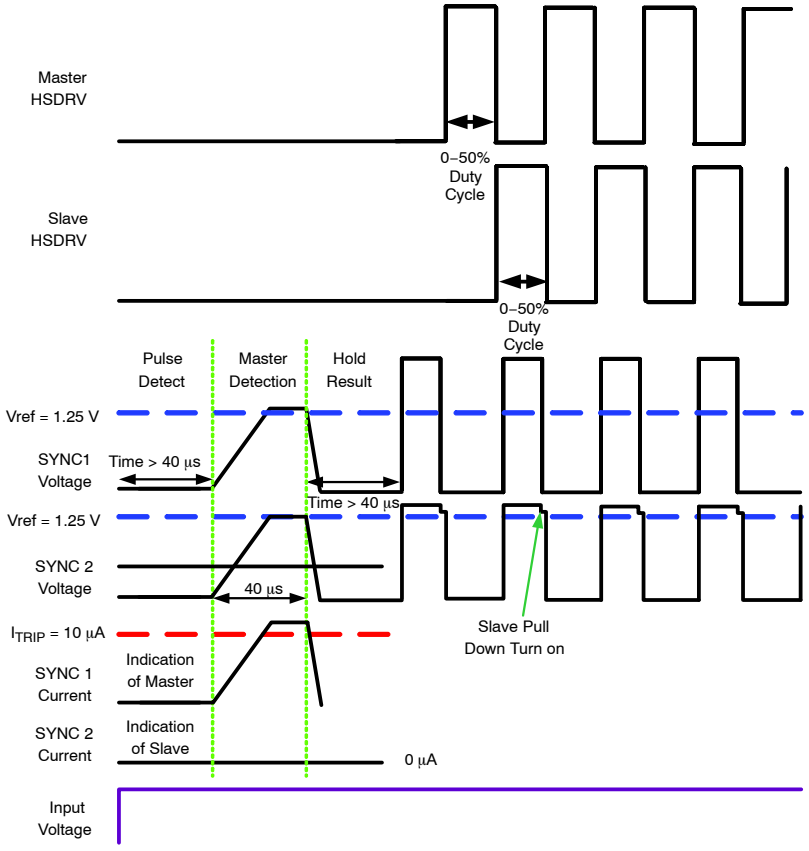



**Figure 21. Master Slave Typical Waveforms**

The master slave identification begins when input voltage is applied prior to POR. Upon application of input voltage, the device waits for input pulses for a minimum of 40 μs as shown in Figure 21. During the pulse detection period if concurrent edges occur on the SYNC pin from an external source, the device enters slave mode and skips the master detection sequence. The device will remain in the detected state until power is cycled.

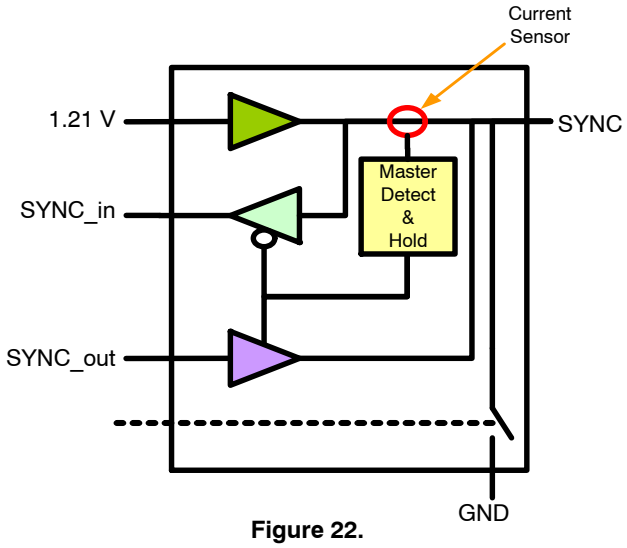



**Figure 22.**

### External Synchronization

The device can sync to frequencies that are 15% to 60% higher than the nominal switching frequency. If an external sync pulse is present at the SYNC pin prior to input voltage application to the device, then no additional external components are needed. If the external clock is not present following power on reset of the device, the voltage on the SYNC pin will determine whether the device is a master or a slave. If the external clock source is meant to start after device operation, its off state should be high or tristate. It is also important to note that the slope of the internal ramp is fixed and synchronizing to a faster clock which will truncate the ramp signal. The equation for calculating the remaining ramp height is shown below:

$$V_{RAMP} = VRAMP_{typ} * \frac{F_{nom}}{F_{SYNC}} \rightarrow 1.5\ V * \frac{75\ kHz}{100\ kHz} \approx 1.125\ V \quad \text{(eq. 3)}$$

### OOV, OUV, and Power Good

The output voltage of the buck converter is monitored at the Feedback pin of the output power stage. Four comparators are placed on the feedback node of the OTA to monitor the operating window of the feedback voltage as shown in Figures 23 and 24. All comparator outputs are ignored during the soft−start sequence as soft−start is regulated by the OTA and false trips would be generated. Further, the Power Good pin is held low until the comparators are evaluated. After the soft−start period has ended, if the feedback is below the reference voltage of comparator 4 ($0.6 < V_{FB}$), the output is considered "undervoltage," the device will initiate a restart, and the Power Good pin remains low with a 55 Ω pulldown resistance. If the voltage at the Feedback pin is between the reference voltages of comparator 4 and comparator 3 ($0.60 < V_{FB} < 0.72$), then the output voltage is considered "power not good low" and the Power Good pin remains low. When the Feedback pin voltage rises between the reference voltages of comparator 3 and comparator 2 ($0.72 < V_{FB} < 0.88$), then the output voltage is considered "Power Good" and the Power Good pin is released. If the voltage at the Feedback pin is between the reference voltages of comparator 2 and comparator 1 ($0.88 < V_{FB} < 1.00$), the output voltage is considered "power not good high" and the power good pin is pulled low with a 55 Ω pulldown resistance. Finally, if the feedback voltage is greater than comparator 1 ($1.0 < V_{FB}$), the output voltage is considered "overvoltage," the Power Good pin will remain low, and the device will latch off. To clear a latch fault, input voltage must be recycled. Graphical representation of the OOV, OUV, and Power Good pin functionality is shown in Figures 25 and 26.

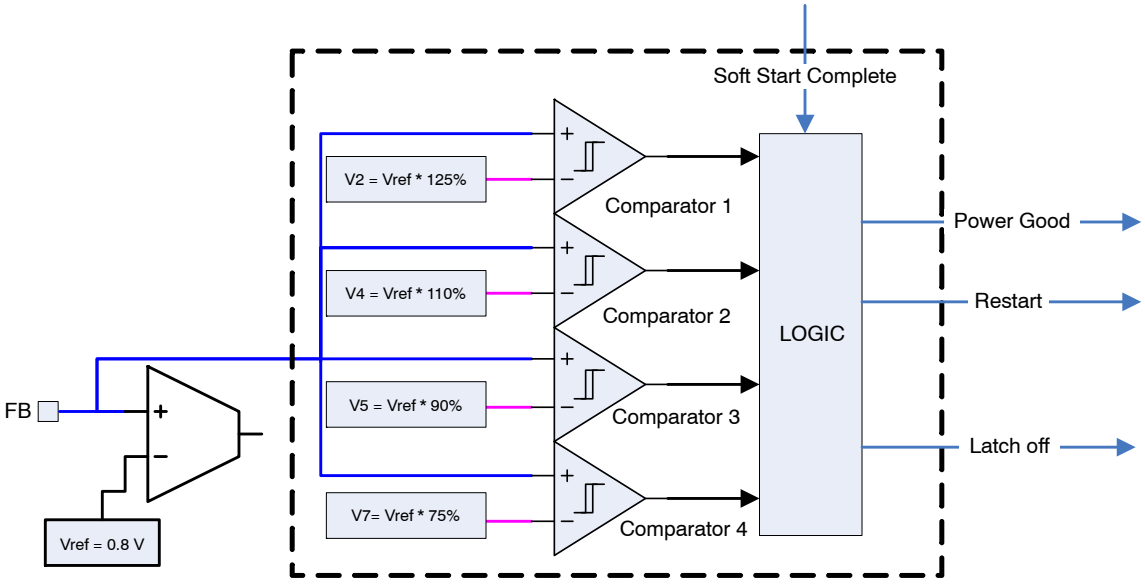



**Figure 23. OOV, OUV, and Power Good Circuit Diagram**

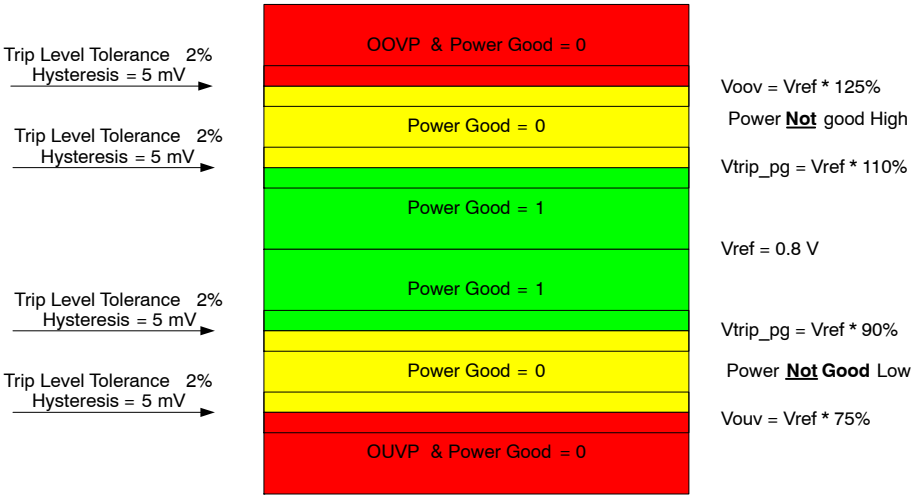



**Figure 24. OOV, OUV, and Power Good Window Diagram**

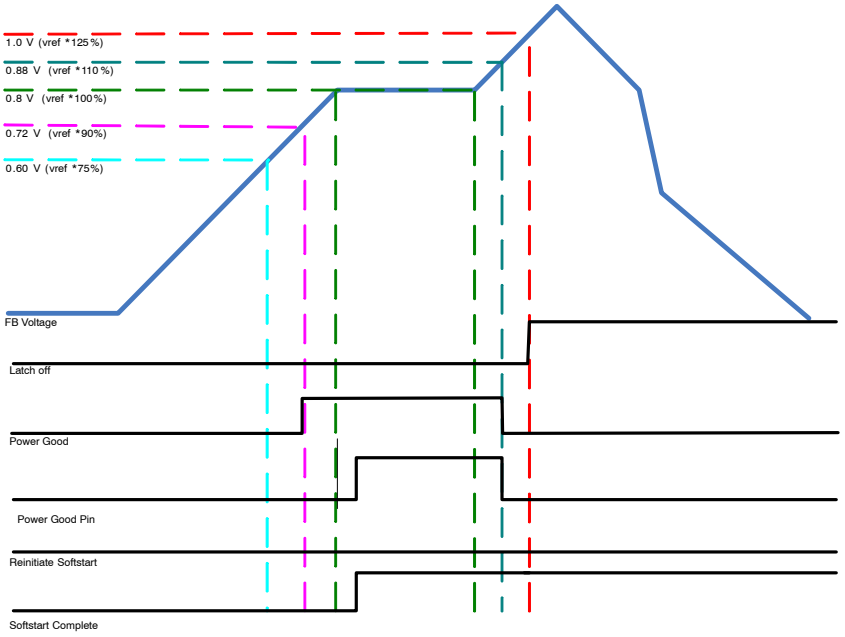



**Figure 25. Powerup Sequence and Overvoltage Latch**

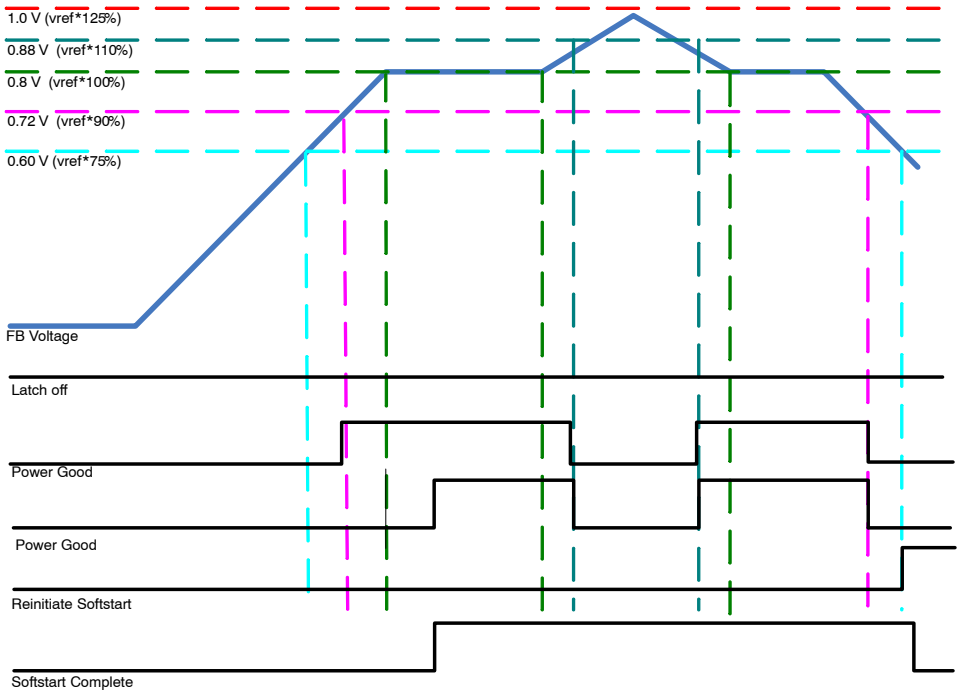



**Figure 26. Powerup Sequence and Undervoltage Soft−Start**

## CURRENT LIMIT AND CURRENT LIMIT SET

### Overview

The NCP3012 uses the voltage drop across the High Side MOSFET during the on time to sense inductor current. The $I_{Limit}$ block consists of a voltage comparator circuit which compares the differential voltage across the $V_{CC}$ Pin and the $V_{SW}$ Pin with a resistor settable voltage reference. The sense portion of the circuit is only active while the HS MOSFET is turned ON.

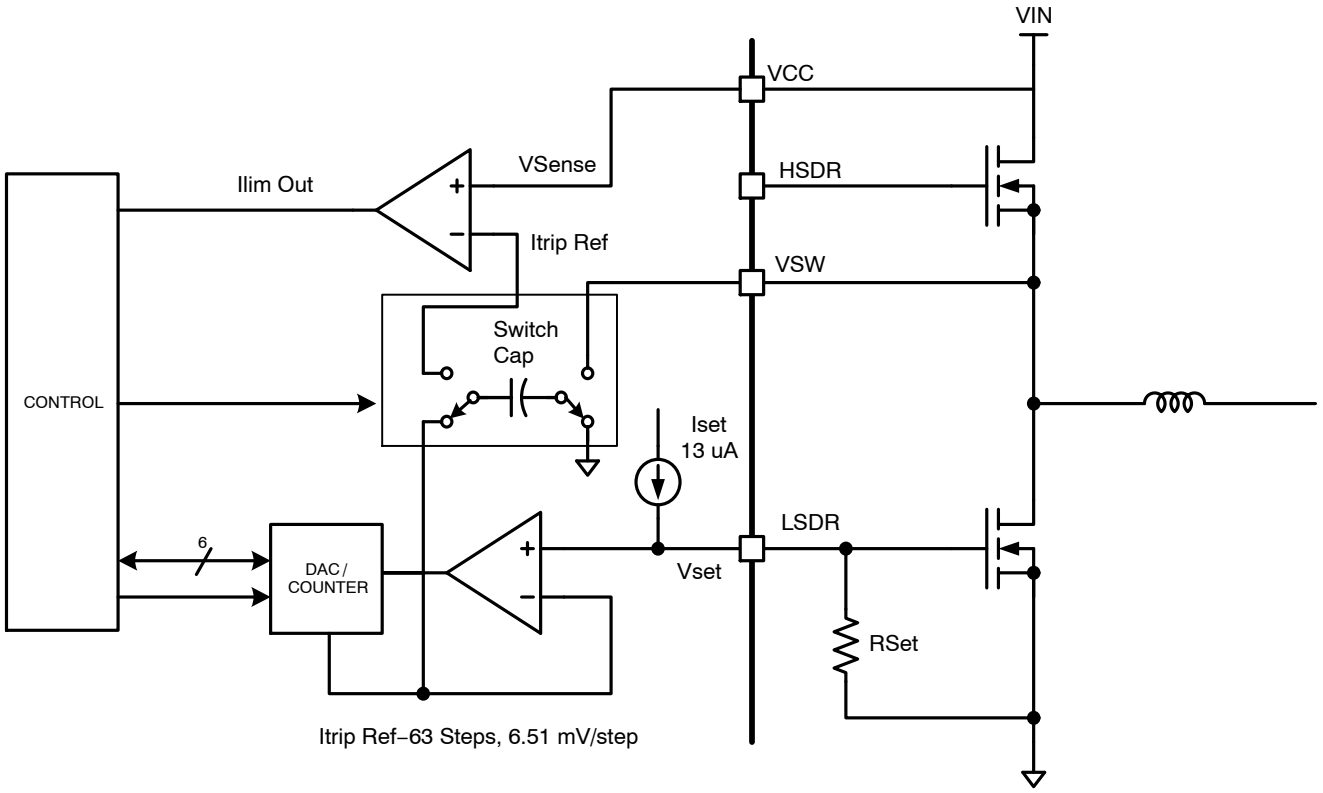



**Figure 27. $I_{set}$ / $I_{Limit}$ Block Diagram**

### Current Limit Set

The $I_{Limit}$ comparator reference is set during the startup sequence by forcing a typically 13 μA current through the low side gate drive resistor. The gate drive output will rise to a voltage level shown in the equation below:

$$V_{set} = I_{set} * R_{set} \qquad \text{(eq. 4)}$$

Where $I_{SET}$ is 13 μA and $R_{SET}$ is the gate to source resistor on the low side MOSFET.

This resistor is normally installed to prevent MOSFET leakage from causing unwanted turn on of the low side MOSFET. In this case, the resistor is also used to set the $I_{Limit}$ trip level reference through the $I_{Limit}$ DAC. The $I_{set}$ process takes approximately 350 μs to complete prior to Soft−Start stepping. The scaled voltage level across the $I_{SET}$ resistor is converted to a 6 bit digital value and stored as the trip value. The binary $I_{Limit}$ value is scaled and converted to the analog $I_{Limit}$ reference voltage through a DAC counter. The DAC has 63 steps in 6.51 mV increments equating to a maximum sense voltage of 403 mV. During the $I_{set}$ period prior to Soft−Start, the DAC counter increments the reference on the $I_{SET}$ comparator until it crosses the $V_{SET}$ voltage and holds the DAC reference output to that count value. This voltage is translated to the $I_{Limit}$ comparator during the $I_{Sense}$ portion of the switching cycle through the switch cap circuit. See Figure 27. Exceeding the maximum sense voltage results in no current limit. Steps 0 to 10 result in an effective current limit of 0 mV.

### Current Sense Cycle

Figure 28 shows how the current is sampled as it relates to the switching cycle. Current level 1 in Figure 28 represents a condition that will not cause a fault. Current level 2 represents a condition that will cause a fault. The sense circuit is allowed to operate below the 3/4 point of a given switching cycle. A given switching cycle's 3/4 $T_{on}$ time is defined by the prior cycle's $T_{on}$ and is quantized in 10 ns steps. A fault occurs if the sensed MOSFET voltage exceeds the DAC reference within the 3/4 time window of the switching cycle.

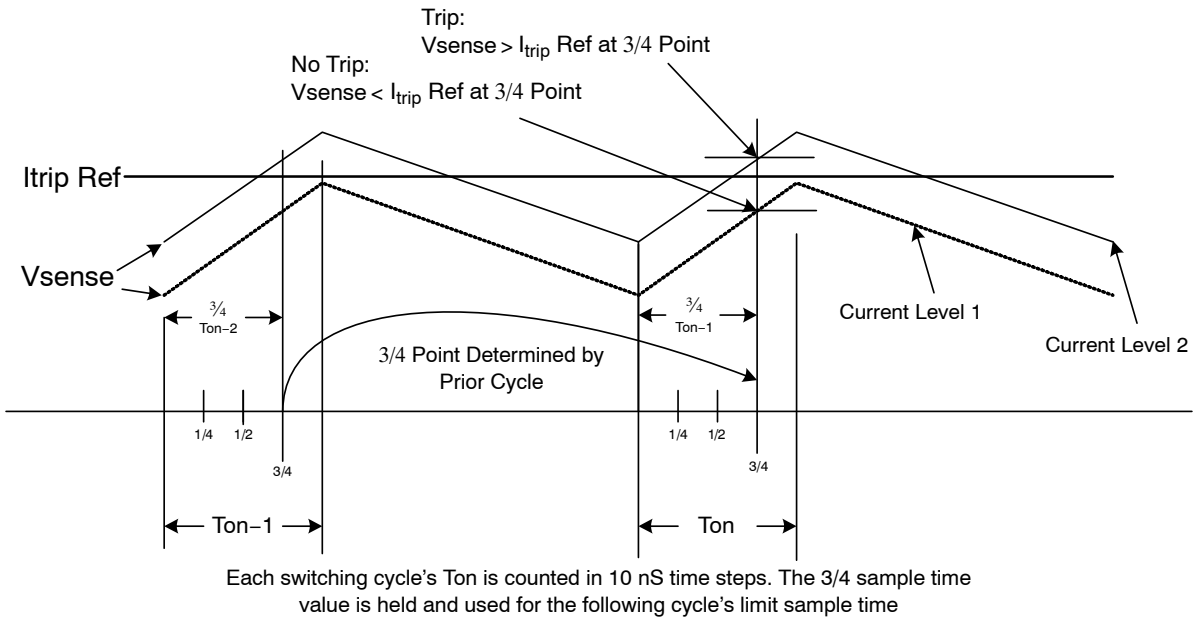



**Figure 28. $I_{Limit}$ Trip Point Description**

### Soft−Start Current limit

During soft−start the $I_{SET}$ value is doubled to allow for inrush current to charge the output capacitance. The DAC reference is set back to its normal value after soft−start has completed.

### $V_{SW}$ Ringing

The $I_{Limit}$ block can lose accuracy if there is excessive $V_{SW}$ voltage ringing that extends beyond the 1/2 point of the high−side transistor on−time. Proper snubber design and keeping the ratio of ripple current and load current in the 10−30% range can help alleviate this as well.

### Current Limit

A current limit trip results in completion of one switching cycle and subsequently half of another cycle $T_{on}$ to account for negative inductor current that might have caused negative potentials on the output. Subsequently the power MOSFETs are both turned off and a 4 soft−start time period wait passes before another soft−start cycle is attempted.

### $I_{ave}$ vs Trip Point

The average load trip current versus $R_{SET}$ value is shown the equation below:

$$I_{AveTRIP} = \frac{I_{set} \times R_{set}}{R_{DS(on)}} - \frac{1}{4}\left[\frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}\right] \quad \text{(eq. 5)}$$

Where:
L = Inductance (H)
$I_{SET}$ = 13 μA
$R_{SET}$ = Gate to Source Resistance (Ω)
$R_{DS(on)}$ = On Resistance of the HS MOSFET (Ω)
$V_{IN}$ = Input Voltage (V)
$V_{OUT}$ = Output Voltage (V)
$F_{SW}$ = Switching Frequency (Hz)

### Boost Clamp Functionality

The boost circuit requires an external capacitor connected between the BST and $V_{SW}$ pins to store charge for supplying the high and low−side gate driver voltage. This clamp circuit limits the driver voltage to typically 7.5 V when $V_{IN}$ > 9 V, otherwise this internal regulator is in dropout and typically $V_{IN}$ − 1.25 V.

The boost circuit regulates the gate driver output voltage and acts as a switching diode. A simplified diagram of the boost circuit is shown in Figure 29. While the switch node is grounded, the sampling circuit samples the voltage at the boost pin, and regulates the boost capacitor voltage. The sampling circuit stores the boost voltage while the $V_{SW}$ is high and the linear regulator output transistor is reversed biased.

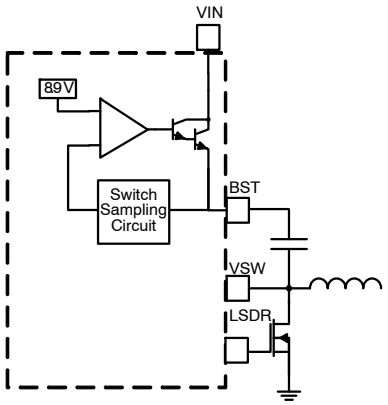



**Figure 29. Boost Circuit**

Reduced sampling time occurs at high duty cycles where the low side MOSFET is off for the majority of the switching period. Reduced sampling time causes errors in the regulated voltage on the boost pin. High duty cycle / input voltage induced sampling errors can result in increased boost ripple voltage or higher than desired DC boost voltage. Figure 30 outlines all operating regions.

The recommended operating conditions are shown in Region 1 (Green) where a 0.1 μF, 25 V ceramic capacitor can be placed on the boost pin without causing damage to the device or MOSFETS. Larger boost ripple voltage occurring over several switching cycles is shown in Region 2 (Yellow). The boost ripple frequency is dependent on the output capacitance selected. The ripple voltage will not damage the device or ±12 V gate rated MOSFETs.

Conditions where maximum boost ripple voltage could damage the device or ±12 V gate rated MOSFETs can be seen in Region 3 (Orange). Placing a boost capacitor that is no greater than 10X the input capacitance of the high side MOSFET on the boost pin limits the maximum boost voltage < 12 V. The typical drive waveforms for Regions 1, 2 and 3 (green, yellow, and orange) regions of Figure 30 are shown in Figure 31.

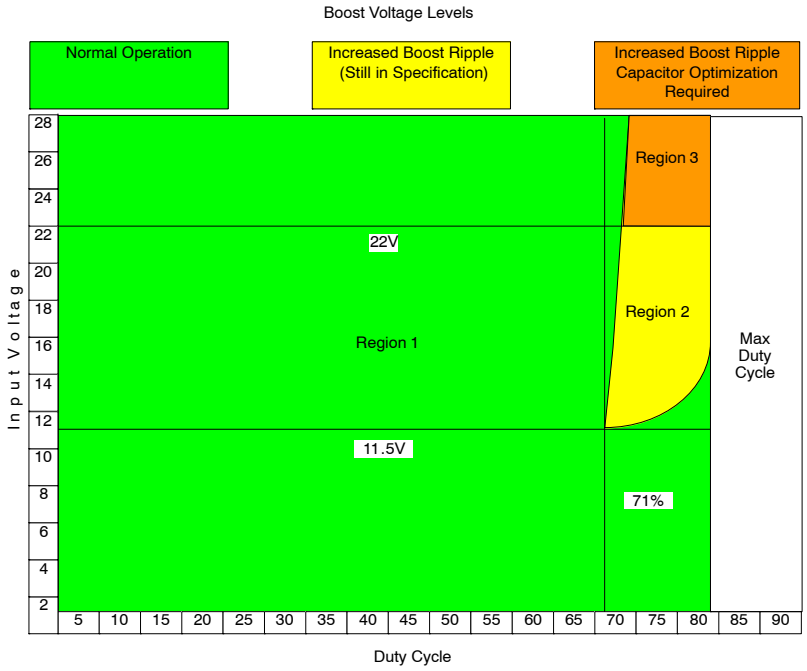



**Figure 30. Safe Operating Area for Boost Voltage with a 0.1 μF Capacitor**

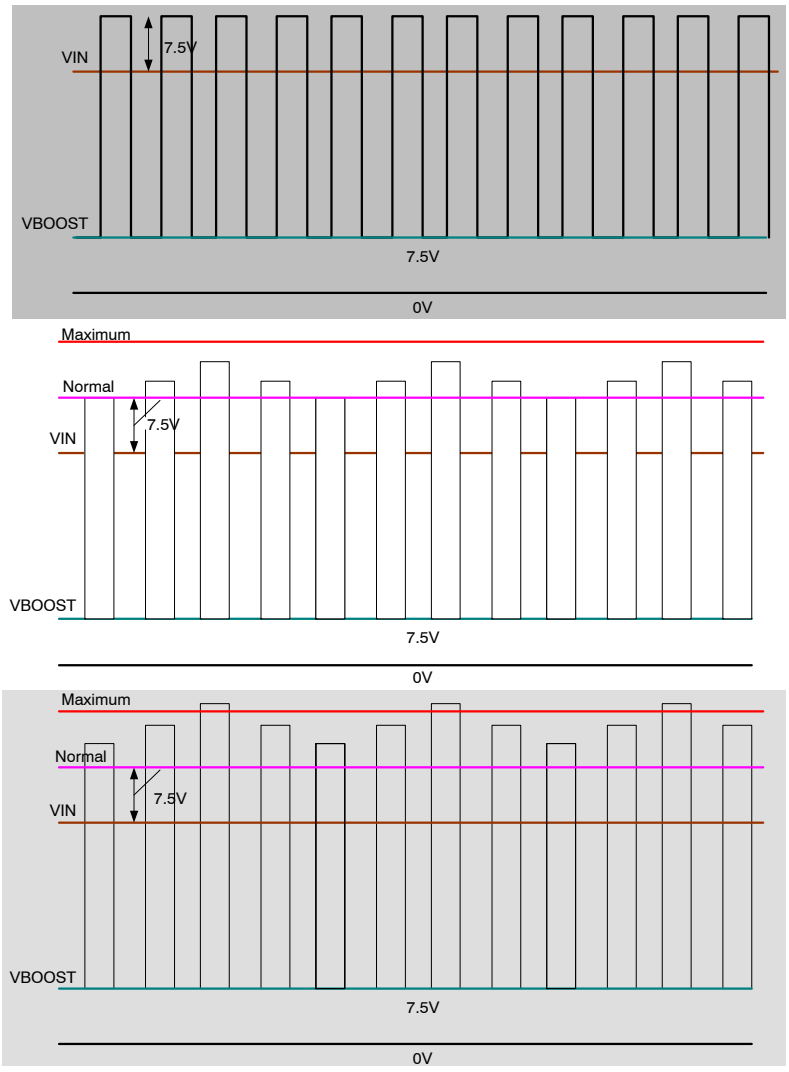
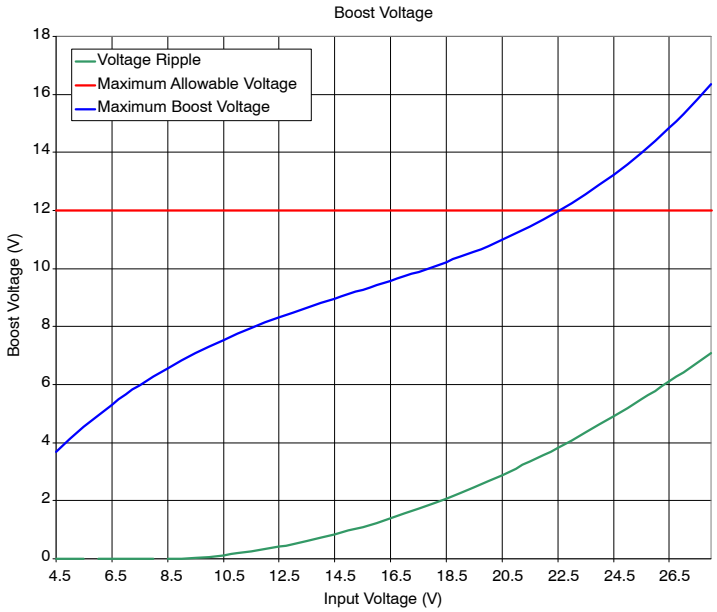



**Figure 31. Typical Waveforms for Region 1 (top), Region 2 (middle), and Region 3 (bottom)**

To illustrate, a 0.1 μF boost capacitor operating at > 80% duty cycle and > 22.5 V input voltage will exceed the specifications for the driver supply voltage. See Figure 32.




(Clarity on Boost Max and Ripple Def)

**Figure 32. Boost Voltage at 80% Duty Cycle**

### Inductor Selection

When selecting the inductor, it is important to know the input and output requirements. Some example conditions are listed below to assist in the process.

**Table 1. DESIGN PARAMETERS**

| Design Parameter | | Example Value |
|---|---|---|
| Input Voltage | ($V_{IN}$) | 9 V to 18 V |
| Nominal Input Voltage | ($V_{IN}$) | 12 V |
| Output Voltage | ($V_{OUT}$) | 3.3 V |
| Input ripple voltage | ($VIN_{RIPPLE}$) | 300 mV |
| Output ripple voltage | ($VOUT_{RIPPLE}$) | 50 mV |
| Output current rating | ($I_{OUT}$) | 8 A |
| Operating frequency | (Fsw) | 75 kHz |

A buck converter produces input voltage ($V_{IN}$) pulses that are LC filtered to produce a lower dc output voltage ($V_{OUT}$). The output voltage can be changed by modifying the on time relative to the switching period (T) or switching frequency. The ratio of high side switch on time to the switching period is called duty cycle (D). Duty cycle can also be calculated using $V_{OUT}$, $V_{IN}$, the low side switch voltage drop $V_{LSD}$, and the High side switch voltage drop $V_{HSD}$.

$$F = \frac{1}{T} \qquad \text{(eq. 6)}$$

$$D = \frac{T_{ON}}{T}(-D) = \frac{T_{OFF}}{T} \qquad \text{(eq. 7)}$$

$$D = \frac{V_{OUT} + V_{LSD}}{V_{IN} - V_{HSD} + V_{LSD}} \approx D = \frac{V_{OUT}}{V_{IN}} \qquad \text{(eq. 8)}$$

$$\rightarrow 27.5\% = \frac{3.3\ V}{12\ V}$$

The ratio of ripple current to maximum output current simplifies the equations used for inductor selection. The formula for this is given in Equation 9.

$$ra = \frac{\Delta I}{I_{OUT}} \qquad \text{(eq. 9)}$$

The designer should employ a rule of thumb where the percentage of ripple current in the inductor lies between 10% and 40%. When using ceramic output capacitors the ripple current can be greater thus a user might select a higher ripple current, but when using electrolytic capacitors a lower ripple current will result in lower output ripple. Now, acceptable values of inductance for a design can be calculated using Equation 10.

$$L = \frac{V_{OUT}}{I_{OUT} \cdot ra \cdot F_{SW}} \cdot (1 - D) \rightarrow 22\ \mu H \qquad \text{(eq. 10)}$$

$$= \frac{3.3\ V}{8\ A \cdot 25\% \cdot 75\ kHz} \cdot (1 - 27.5\%)$$

The relationship between ra and L for this design example is shown in Figure 33.

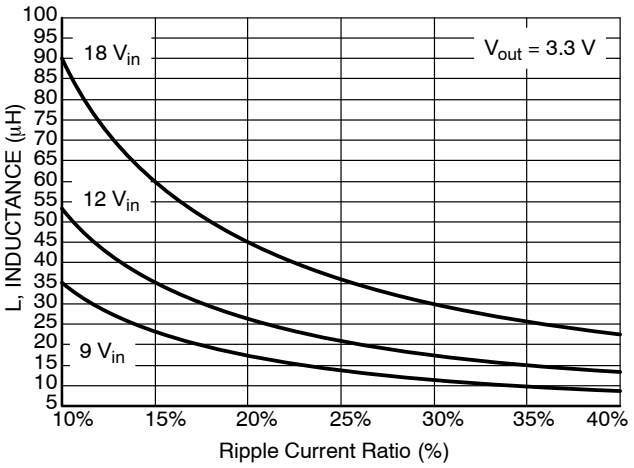



**Figure 33. Ripple Current Ratio vs. Inductance**

To keep within the bounds of the parts maximum rating, calculate the RMS current and peak current.

$$I_{RMS} = I_{OUT} \cdot \sqrt{1 + \frac{ra^2}{12}} \rightarrow 8.02\ A = 8\ A \cdot \sqrt{1 + \frac{(0.25)^2}{12}} \quad \text{(eq. 11)}$$

$$I_{PK} = I_{OUT} \cdot \left(1 + \frac{ra}{2}\right) \rightarrow 9.0\ A = 8\ A \cdot \left(1 + \frac{(0.25)}{2}\right) \quad \text{(eq. 12)}$$

An inductor for this example would be around 3.3 μH and should support an rms current of 8.02 A and a peak current of 9.0 A.

The final selection of an output inductor has both mechanical and electrical considerations. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by Equation 13.

$$SlewRate_{LOUT} = \frac{V_{IN} - V_{OUT}}{L_{OUT}} \rightarrow 0.4\frac{A}{\mu s} = \frac{12\ V - 3.3\ V}{22\ \mu H} \quad \text{(eq. 13)}$$

This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. This results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak−to−peak ripple current for the NCP3012 is given by the following equation:

$$I_{PP} = \frac{V_{OUT}(1 - D)}{L_{OUT} \cdot F_{SW}} \quad \text{(eq. 14)}$$

Ipp is the peak to peak current of the inductor. From this equation it is clear that the ripple current increases as $L_{OUT}$ decreases, emphasizing the trade−off between dynamic response and ripple current.

The power dissipation of an inductor consists of both copper and core losses. The copper losses can be further categorized into dc losses and ac losses. A good first order approximation of the inductor losses can be made using the DC resistance as they usually contribute to 90% of the losses of the inductor shown below:

$$LP_{CU} = I_{RMS}^{\ 2} \cdot DCR \quad \text{(eq. 15)}$$

The core losses and ac copper losses will depend on the geometry of the selected core, core material, and wire used. Most vendors will provide the appropriate information to make accurate calculations of the power dissipation then the total inductor losses can be capture buy the equation below:

$$LP_{tot} = LP_{CU\_DC} + LP_{CU\_AC} + LP_{Core} \quad \text{(eq. 16)}$$

### Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$Iin_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \quad \text{(eq. 17)}$$

D is the duty cycle, $Iin_{RMS}$ is the input RMS current, and $I_{OUT}$ is the load current.

The equation reaches its maximum value with D = 0.5. Loss in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \cdot \left(I_{IN-RMS}\right)^2 \quad \text{(eq. 18)}$$

$P_{CIN}$ is the power loss in the input capacitors and $ESR_{CIN}$ is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must by surge protected. Otherwise, capacitor failure could occur.

### Input Start−up Current

To calculate the input startup current, the following equation can be used.

$$I_{INRUSH} = \frac{C_{OUT} \cdot V_{OUT}}{t_{SS}} \quad \text{(eq. 19)}$$

$I_{inrush}$ is the input current during startup, $C_{OUT}$ is the total output capacitance, $V_{OUT}$ is the desired output voltage, and $t_{SS}$ is the soft start interval. If the inrush current is higher than the steady state input current during max load, then the input fuse should be rated accordingly, if one is used.

### Output Capacitor Selection

The important factors to consider when selecting an output capacitor is dc voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements.

The output capacitor must be rated to handle the ripple current at full load with proper derating. The RMS ratings given in datasheets are generally for lower switching frequency than used in switch mode power supplies but a multiplier is usually given for higher frequency operation. The RMS current for the output capacitor can be calculated below:

$$Co_{RMS} = I_O \cdot \frac{ra}{\sqrt{12}} \quad \text{(eq. 20)}$$

The maximum allowable output voltage ripple is a combination of the ripple current selected, the output capacitance selected, the equivalent series inductance (ESL) and ESR.

The main component of the ripple voltage is usually due to the ESR of the output capacitor and the capacitance selected.

$$V_{ESR\_C} = I_O \cdot ra \cdot \left( ESR_{Co} + \frac{1}{8 \cdot F_{SW} \cdot Co} \right) \quad \text{(eq. 21)}$$

The ESL of capacitors depends on the technology chosen but tends to range from 1 nH to 20 nH where ceramic capacitors have the lowest inductance and electrolytic capacitors then to have the highest. The calculated contributing voltage ripple from ESL is shown for the switch on and switch off below:

$$V_{ESLON} = \frac{ESL \cdot I_{PP} \cdot F_{SW}}{D} \quad \text{(eq. 22)}$$

$$V_{ESLOFF} = \frac{ESL \cdot I_{PP} \cdot F_{SW}}{(1 - D)} \quad \text{(eq. 23)}$$

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The controller immediately recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

During a load step transient the output voltage initially drops due to the current variation inside the capacitor and the ESR (neglecting the effect of the effective series inductance (ESL)).

$$\Delta V_{OUT-ESR} = \Delta I_{TRAN} \cdot ESR_{Co} \quad \text{(eq. 24)}$$

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is approximated by the following equation:

$$\Delta V_{OUT-DISCHG} = \frac{\left(I_{TRAN}\right)^2 \cdot L_{OUT}}{C_{OUT} \cdot \left(V_{IN} - V_{OUT}\right)} \quad \text{(eq. 25)}$$

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. It should be noted that ΔVOUT−DISCHARGE and ΔVOUT−ESR are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL).

Conversely during a load release, the output voltage can increase as the energy stored in the inductor dumps into the output capacitor. The ESR contribution from Equation 21 still applies in addition to the output capacitor charge which is approximated by the following equation:

$$\Delta V_{OUT-CHG} = \frac{\left(I_{TRAN}\right)^2 \cdot L_{OUT}}{C_{OUT} \cdot V_{OUT}} \quad \text{(eq. 26)}$$

### Power MOSFET Selection

Power dissipation, package size, and the thermal environment drive MOSFET selection. To adequately select the correct MOSFETs, the design must first predict its power dissipation. Once the dissipation is known, the thermal impedance can be calculated to prevent the specified maximum junction temperatures from being exceeded at the highest ambient temperature.

Power dissipation has two primary contributors: conduction losses and switching losses. The control or high−side MOSFET will display both switching and conduction losses. The synchronous or low−side MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non−overlap time of the gate drivers.

Starting with the high−side or control MOSFET, the power dissipation can be approximated from:

$$P_{D\_CONTROL} = P_{COND} + P_{SW\_TOT} \quad \text{(eq. 27)}$$

The first term is the conduction loss of the high−side MOSFET while it is on.

$$P_{COND} = \left(I_{RMS\_CONTROL}\right)^2 \cdot R_{DS(on)\_CONTROL} \quad \text{(eq. 28)}$$

Using the ra term from Equation 9, $I_{RMS}$ becomes:

$$I_{RMS\_CONTROL} = I_{OUT} \cdot \sqrt{D \cdot \left(1 + \left(\frac{ra^2}{12}\right)\right)} \quad \text{(eq. 29)}$$

The second term from Equation 27 is the total switching loss and can be approximated from the following equations.

$$P_{SW\_TOT} = P_{SW} + P_{DS} + P_{RR} \quad \text{(eq. 30)}$$

The first term for total switching losses from Equation 30 includes the losses associated with turning the control MOSFET on and off and the corresponding overlap in drain voltage and current.

$$P_{SW} = P_{TON} + P_{TOFF} = \frac{1}{2} \cdot \left(I_{OUT} \cdot V_{IN} \cdot f_{SW}\right) \cdot \left(t_{ON} + t_{OFF}\right) \quad \text{(eq. 31)}$$

where:

$$t_{ON} = \frac{Q_{GD}}{I_{G1}} = \frac{Q_{GD}}{(V_{BST} - V_{TH})/(R_{HSPU} + R_G)} \quad \text{(eq. 32)}$$

and:

$$t_{OFF} = \frac{Q_{GD}}{I_{G2}} = \frac{Q_{GD}}{(V_{BST} - V_{TH})/(R_{HSPD} + R_G)} \quad \text{(eq. 33)}$$

Next, the MOSFET output capacitance losses are caused by both the control and synchronous MOSFET but are dissipated only in the control MOSFET.

$$P_{DS} = \frac{1}{2} \cdot Q_{OSS} \cdot V_{IN} \cdot f_{SW} \quad \text{(eq. 34)}$$

Finally the loss due to the reverse recovery time of the body diode in the *synchronous* MOSFET is shown as follows:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{SW} \quad \text{(eq. 35)}$$

The low−side or synchronous MOSFET turns on into zero volts so switching losses are negligible. Its power dissipation only consists of conduction loss due to $R_{DS(on)}$ and body diode loss during the non−overlap periods.

$$P_{D\_SYNC} = P_{COND} + P_{BODY} \quad \text{(eq. 36)}$$

Conduction loss in the low−side or synchronous MOSFET is described as follows:

$$P_{COND} = (I_{RMS\_SYNC})^2 \cdot R_{DS(on)\_SYNC} \quad \text{(eq. 37)}$$

where:

$$I_{RMS\_SYNC} = I_{OUT} \cdot \sqrt{(1 - D) \cdot \left(1 + \left(\frac{ra^2}{12}\right)\right)} \quad \text{(eq. 38)}$$

The body diode losses can be approximated as:

$$P_{BODY} = V_{FD} \cdot I_{OUT} \cdot f_{SW} \cdot (NOL_{LH} + NOL_{HL}) \quad \text{(eq. 39)}$$

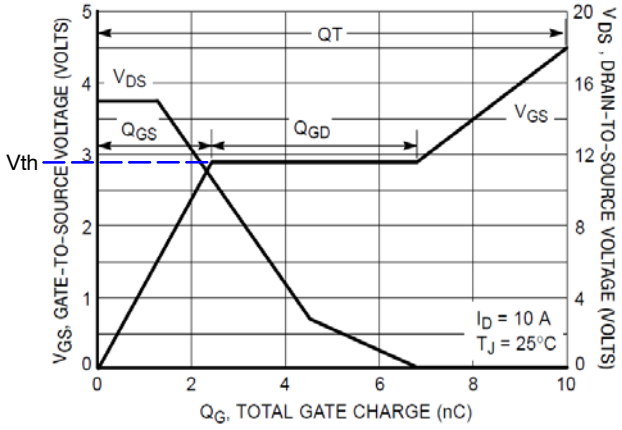



**Figure 34. MOSFET Switching Characteristics**

$I_{G1}$: output current from the high−side gate drive (HSDR)
$I_{G2}$: output current from the low−side gate drive (LSDR)
$f_{SW}$: switching frequency of the converter.
$V_{BST}$: gate drive voltage for the high−side drive, typically 7.5 V.
$Q_{GD}$: gate charge plateau region, commonly specified in the MOSFET datasheet
$V_{TH}$: gate−to−source voltage at the gate charge plateau region
$Q_{OSS}$: MOSFET output gate charge specified in the data sheet
$Q_{RR}$: reverse recovery charge of the low−side or synchronous MOSFET, specified in the datasheet
$R_{DS(on)\_CONTROL}$: on resistance of the high−side, or control, MOSFET
$R_{DS(on)\_SYNC}$: on resistance of the low−side, or synchronous, MOSFET
$NOL_{LH}$: dead time between the LSDR turning off and the HSDR turning on, typically 85 ns
$NOL_{HL}$: dead time between the HSDR turning off and the LSDR turning on, typically 75 ns

Once the MOSFET power dissipations are determined, the designer can calculate the required thermal impedance for each device to maintain a specified junction temperature at the worst case ambient temperature. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D \cdot R_{\theta JA}$$

$T_J$: Junction Temperature
$T_A$: Ambient Temperature
$P_D$: Power Dissipation of the MOSFET under analysis
$R_{\theta JA}$: Thermal Resistance Junction−to−Ambient of the MOSFET's package

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e. worst case MOSFET $R_{DS(on)}$).

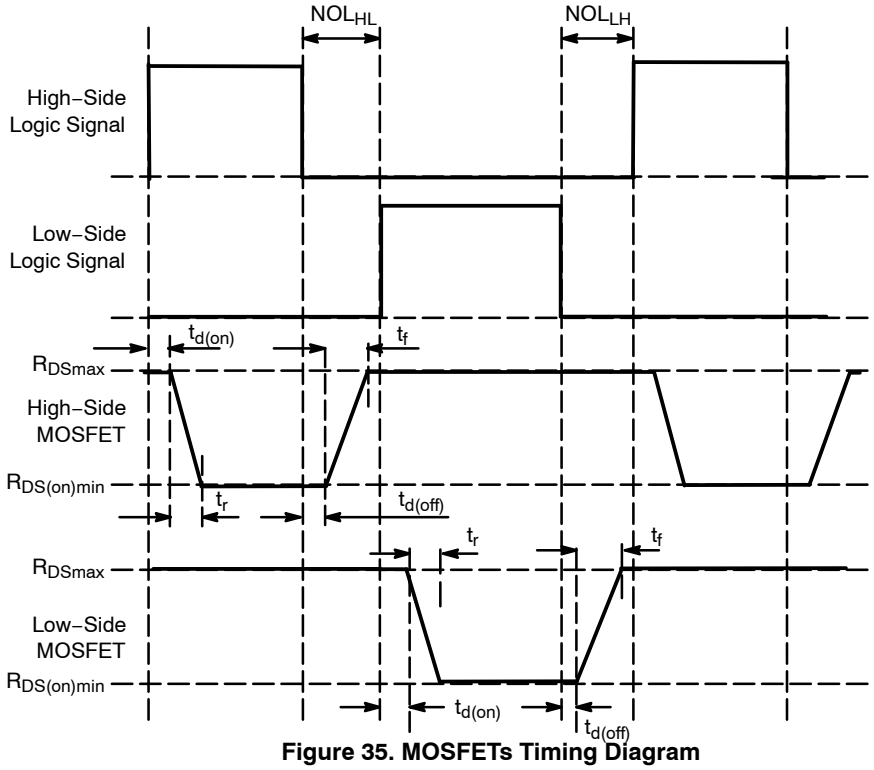



**Figure 35. MOSFETs Timing Diagram**

Another consideration during MOSFET selection is their delay times. Turn−on and turn−off times must be short enough to prevent cross conduction. If not, there will be conduction from the input through both MOSFETs to ground. Therefore, the following conditions must be met.

$$t_{d(ON)\_CONTROL} + NOL_{LH} > t_{d(OFF)\_SYNC} + t_{f\_SYNC}$$

and (eq. 40)

$$t_{(ON)\_SYNC} + NOL_{HL} > t_{d(OFF)\_CONTROL} + t_{f\_CONTROL}$$

The MOSFET parameters, $t_{d(ON)}$, $t_r$, $t_{d(OFF)}$ and $t_f$ are can be found in their appropriate datasheets for specific conditions. $NOL_{LH}$ and $NOL_{HL}$ are the dead times which were described earlier and are 85 ns and 75 ns, respectively.

### Feedback and Compensation

The NCP3012 is a voltage mode buck convertor with a transconductance error amplifier compensated by an external compensation network. Compensation is needed to achieve accurate output voltage regulation and fast transient response. The goal of the compensation circuit is to provide a loop gain function with the highest crossing frequency and adequate phase margin (minimally 45°). The transfer function of the power stage (the output LC filter) is a double pole system. The resonance frequency of this filter is expressed as follows:

$$f_{P0} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} \quad \text{(eq. 41)}$$

Parasitic Equivalent Series Resistance (ESR) of the output filter capacitor introduces a high frequency zero to the filter network. Its value can be calculated by using the following equation:

$$f_{Z0} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR} \quad \text{(eq. 42)}$$

The main loop zero crossover frequency f0 can be chosen to be 1/10 − 1/5 of the switching frequency. Table 2 shows the three methods of compensation.

**Table 2. COMPENSATION TYPES**

| Zero Crossover Frequency Condition | Compensation Type | Typical Output Capacitor Type |
|---|---|---|
| $f_{P0} < f_{Z0} < f_0 < f_S/2$ | Type II | Electrolytic, Tantalum |
| $f_{P0} < f_0 < f_{Z0} < f_S/2$ | Type III Method I | Tantalum, Ceramic |
| $f_{P0} < f_0 < f_S/2 < f_{Z0}$ | Type III Method II | Ceramic |

### Compensation Type II

This compensation is suitable for electrolytic capacitors. Components of the Type II compensation (Figure 36) network can be specified by the following equations:

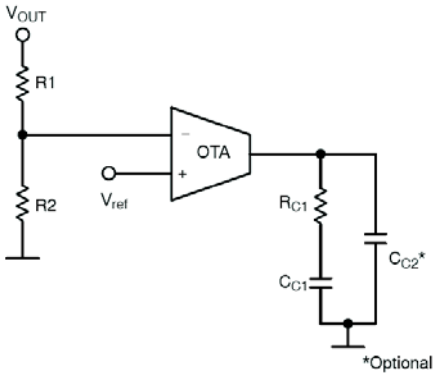



**Figure 36. Type II Compensation**

$$R_{C1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot V_{OUT}}{ESR \cdot V_{IN} \cdot V_{ref} \cdot gm} \quad \text{(eq. 43)}$$

$$C_{C1} = \frac{1}{0.75 \cdot 2 \cdot \pi \cdot f_{P0} \cdot R_{C1}} \quad \text{(eq. 44)}$$

$$C_{C2} = \frac{1}{\pi \cdot R_{C1} \cdot f_S} \quad \text{(eq. 45)}$$

$$R1 = \frac{V_{OUT} - V_{ref}}{V_{ref}} \cdot R2 \quad \text{(eq. 46)}$$

$V_{RAMP}$ is the peak−to−peak voltage of the oscillator ramp and gm is the transconductance error amplifier gain. Capacitor $C_{C2}$ is optional.

### Compensation Type III

Tantalum and ceramics capacitors have lower ESR than electrolytic, so the zero of the output LC filter goes to a higher frequency above the zero crossover frequency. This requires a Type III compensation network as shown in Figure 37.

There are two methods to select the zeros and poles of this compensation network. Method I is ideal for tantalum output capacitors, which have a higher ESR than ceramic:

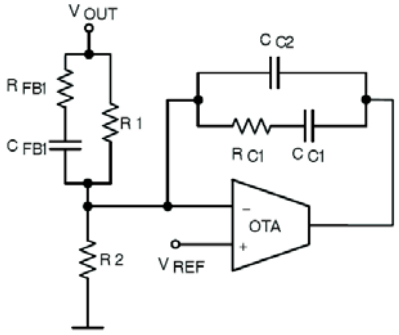



**Figure 37. Type III Compensation**

$$f_{Z1} = 0.75 \cdot f_{P0} \quad \text{(eq. 47)}$$

$$f_{Z2} = f_{P0} \quad \text{(eq. 48)}$$

$$f_{P2} = f_{Z0} \quad \text{(eq. 49)}$$

$$f_{P3} = \frac{f_S}{2} \quad \text{(eq. 50)}$$

Method II is better suited for ceramic capacitors that typically have the lowest ESR available:

$$f_{Z2} = f_0 \cdot \sqrt{\frac{1 - \sin\theta\,max}{1 + \sin\theta\,max}} \quad \text{(eq. 51)}$$

$$f_{P2} = f_0 \cdot \sqrt{\frac{1 + \sin\theta\,max}{1 - \sin\theta\,max}} \quad \text{(eq. 52)}$$

$$f_{Z1} = 0.5 \cdot f_{Z2} \quad \text{(eq. 53)}$$

$$f_{P3} = 0.5 \cdot f_S \quad \text{(eq. 54)}$$

θmax is the desired maximum phase margin at the zero crossover frequency, $f_0$. It should be 45° – 75°. Convert degrees to radians by the formula:

$$\theta\,max = \theta\,max_{degress} \cdot \left(\frac{2 \cdot \pi}{360}\right) : Units = radians \quad \text{(eq. 55)}$$

The remaining calculations are the same for both methods.

$$R_{C1} >> \frac{2}{gm} \quad \text{(eq. 56)}$$

$$C_{C1} = \frac{1}{2 \cdot \pi \cdot f_{Z1} \cdot R_{C1}} \quad \text{(eq. 57)}$$

$$C_{C2} = \frac{1}{2 \cdot \pi \cdot f_{P3} \cdot R_{C1}} \quad \text{(eq. 58)}$$

$$C_{FB1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot C_{OUT}}{V_{IN} \cdot R_{C1}} \quad \text{(eq. 59)}$$

$$R_{FB1} = \frac{1}{2\pi \cdot C_{FB1} \cdot f_{P2}} \quad \text{(eq. 60)}$$

$$R1 = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot f_{Z2}} - R_{FB1} \quad \text{(eq. 61)}$$

$$R2 = \frac{V_{ref}}{V_{OUT} - V_{ref}} \cdot R1 \quad \text{(eq. 62)}$$

If the equation in Equation 63 is not true, then a higher value of $R_{C1}$ must be selected.

$$\frac{R1 \cdot R2 \cdot R_{FB1}}{R1 \cdot R_{FB1} + R2 \cdot R_{FB1} + R1 \cdot R2} > \frac{1}{gm} \quad \text{(eq. 63)}$$

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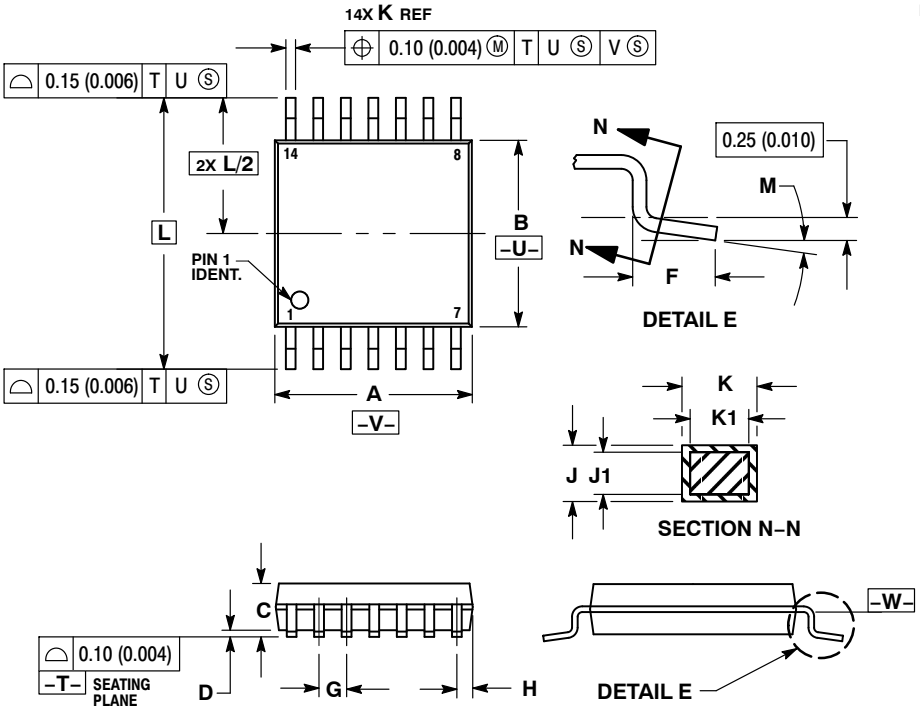


NOTES:
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3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
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6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

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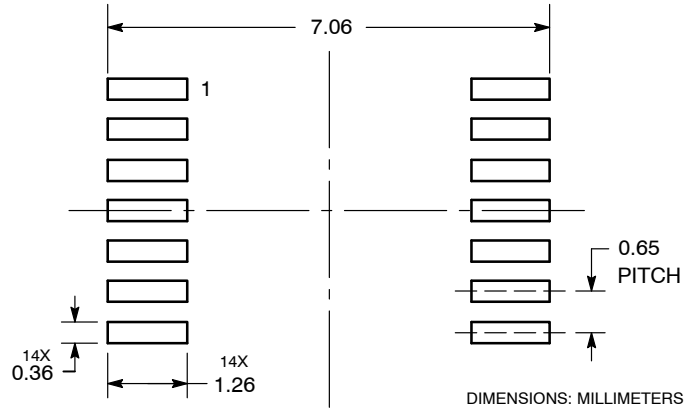


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