# THE DATASHEET OF

# NCP5399FTR2G

# NCP5399

# 2-Phase Controller for CPU Applications

The NCP5399 is a one or two−phase buck controller which combines differential voltage and current sensing, and adaptive voltage positioning to power Intel VR10.x processors. Dual−edge pulse−width modulation (PWM) combined with inductor current sensing reduces system cost by providing the fastest initial response to transient load events. Staggered phase modulation reduces total bulk and ceramic output capacitance required to satisfy transient load−line regulation.

A high performance operational error amplifier is provided which allows easy compensation of the system. The proprietary method of Dynamic Reference Injection (patented) makes the error amplifier compensation virtually independent of the system response to VID changes, eliminating tradeoffs between overshoot and Dynamic VID performance.

### Features

- Meets Intel's VR 10.x Specifications
- Dual−edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Dynamic Reference Injection (Patented)
- DAC Range from 0.8375 V to 1.6 V
- ±0.5% System Voltage Accuracy from 1.0 V to 1.6 V
- True Differential Remote Voltage Sensing Amplifier
- Phase−to−Phase Current Balancing
- "Lossless" Differential Inductor Current Sensing
- Differential Current Sense Amplifiers for each Phase
- Adaptive Voltage Positioning (AVP)
- Frequency Range: 100 KHz – 1 MHz
- Latched Over Voltage Protection (OVP)
- Threshold Sensitive Enable Pin for VTT Sensing
- Power Good Output with Internal Delays
- Programmable Soft Start Time
- This is a Pb−Free Device

### Applications

- Desktop Processors
- Gaming Applications

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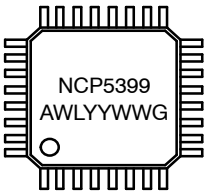
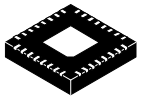
**MARKING DIAGRAMS**

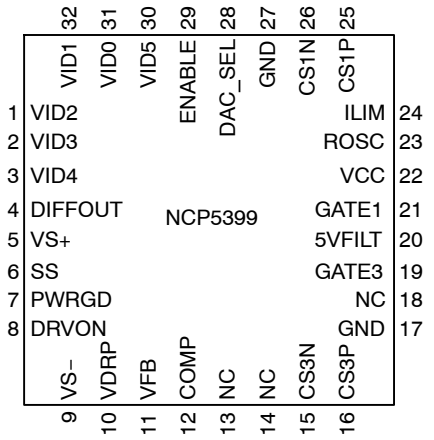
**32 PIN LQFP**
**FT SUFFIX**
**CASE 873A**



**32 PIN QFN**
**MN SUFFIX**
**CASE 485AM**


NCP5399 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package




(Top View)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCP5399FTR2G | LQFP−32 (Pb−Free) | 2000 / Tape & Reel |
| NCP5399MNR2G | QFN−32 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

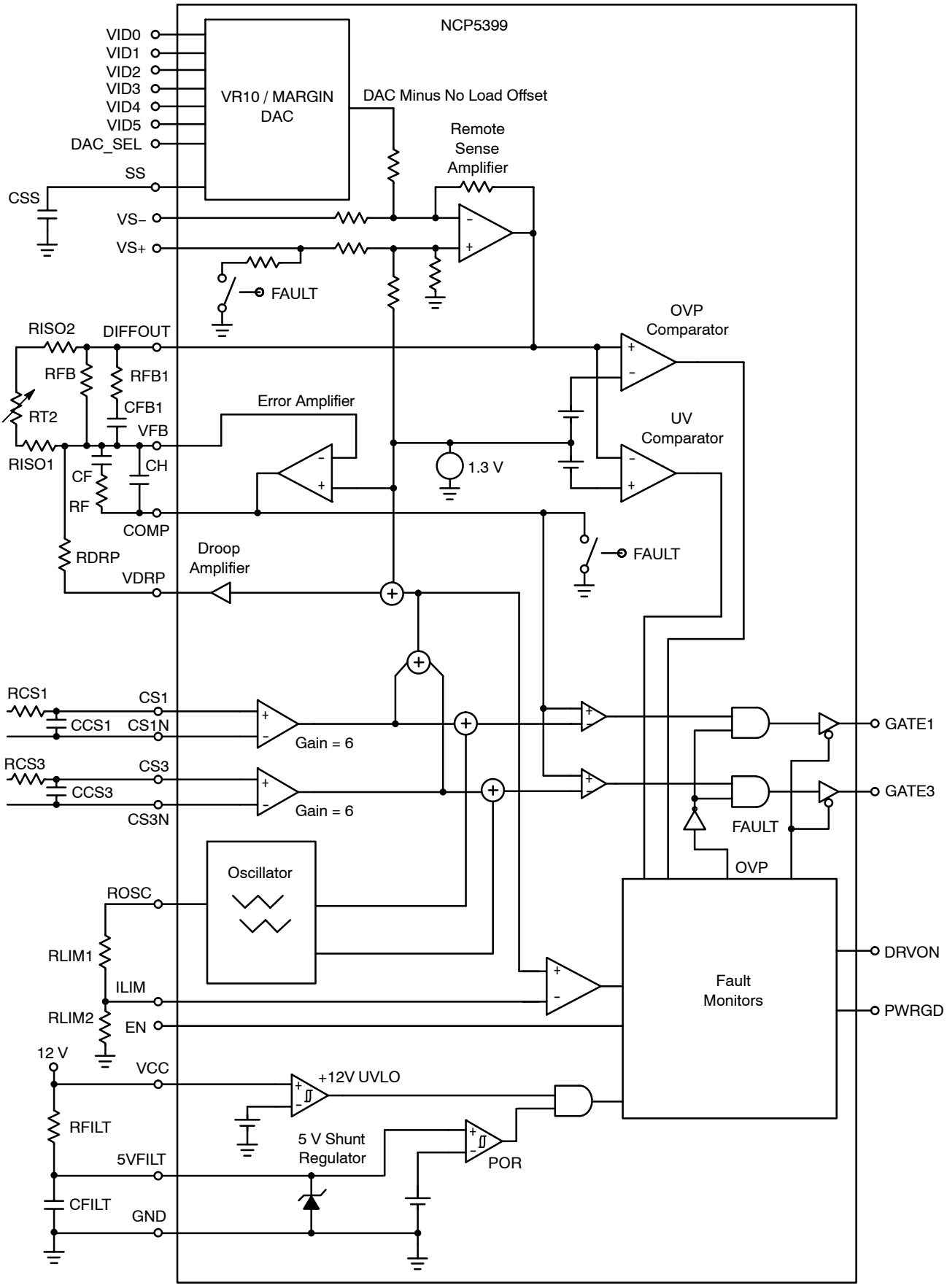



**Figure 1. Functional Block Diagram**

**PIN DESCRIPTIONS**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VID2 | Voltage ID DAC input |
| 2 | VID3 | Voltage ID DAC input |
| 3 | VID4 | Voltage ID DAC input |
| 4 | DIFFOUT | Output of the differential remote sense amplifier. |
| 5 | VS+ | Non−inverting input to the internal differential remote sense amplifier. |
| 6 | SS | A capacitor from this pin to ground programs the soft−start time. |
| 7 | PWRGD | Power Good output. Open drain type output. High indicates the output is regulating. |
| 8 | DRVON | Output to enable Gate Drivers |
| 9 | VS− | Inverting input to the internal differential remote sense amplifier. |
| 10 | VDRP | Current signal output for Adaptive Voltage Positioning (AVP). The offset of this pin above the 1.3 V internal bias voltage is proportional to the output current. Connect a resistor from this pin to VFB to set the amount of AVP current into the feedback resistor (RFB) to produce an output voltage droop. Leave this pin open for no AVP. |
| 11 | VFB | Error amplifier inverting input. Connect a resistor from this pin to DIFFOUT. The value of this resistor and the amount of current from the droop resistor (RDRP) will set the amount of output voltage droop (AVP) during load. |
| 12 | COMP | Output of the error amplifier and the non−inverting input of the PWM comparators. |
| 13 | NC | This pin can be grounded or left unconnected. |
| 14 | NC | This pin can be grounded or left unconnected. |
| 15 | CS3N | Inverting input of current sense amplifier #3 |
| 16 | CS3P | Non−inverting input of current sense amplifier #3 |
| 17 | GND | Power supply return |
| 18 | NC | Do not connect anything to this pin |
| 19 | GATE3 | PWM output to gate driver. |
| 20 | 5VFILT | Power input pin. Connect a 243 ohm resistor from this pin to $V_{CC}$, and a 2.2 μF ceramic capacitor from this pin to ground. |
| 21 | GATE1 | PWM output to gate driver. |
| 22 | VCC | 12 V input supply monitor. |
| 23 | ROSC | A resistance from this pin to ground programs the oscillator frequency. Also, this pin supplies an output voltage of 2 V which may be used to form a voltage divider to the ILIM pin for setting the over current shut-down threshold as shown in the Applications Schematics. |
| 24 | ILIM | Over current shutdown threshold. Connect this pin to the ROSC pin via a resistor divider as shown in the Applications Schematics. To disable over current protection, connect this pin directly to the ROSC pin. For correct operation, this pin should only be connected to the voltage generated by the ROSC pin − do not connect this pin to externally generated voltages. |
| 25 | CS1P | Non−inverting input of current sense amplifier #1 |
| 26 | CS1N | Inverting input of current sense amplifier #1 |
| 27 | GND | This pin must be grounded. |
| 28 | DAC_SEL | Allows selection of VR10.x or MARGIN DAC |
| 29 | ENABLE | Pull this pin high to enable controller. Pull this pin to ground to disable controller. A Low to High transition on this pin will initiate soft start. 20 MHz filtering at this pin is recommended. |
| 30 | VID5 | Voltage ID DAC input |
| 31 | VID0 | Voltage ID DAC input |
| 32 | VID1 | Voltage ID DAC input |

## MAXIMUM RATINGS

### Electrical Information

| Pin Symbol | $V_{MAX}$ (V) | $V_{MIN}$ (V) | $I_{SOURCE}$ (mA) | $I_{SINK}$ (mA) |
|---|---|---|---|---|
| COMP | 5.5 | −0.3 | 10 | 10 |
| VDRP | 5.5 | −0.3 | 5 | 5 |
| VS+ | 2.0 | GND − 300 mV | 1 | 1 |
| VS− | 2.0 | GND − 300 mV | 1 | 1 |
| DIFFOUT | 5.5 | −0.3 | 20 | 20 |
| PWRGD | 5.5 | −0.3 | N/A | 20 |
| DRVON | 5.5 | −0.3 | 1 | 2 |
| $V_{CC}$ | 15.0 | −0.3 | N/A | 1 |
| 5VFILT | 5.25 | −0.3 | N/A | 40 |
| ROSC | 5.5 | −0.3 | 1 | N/A |
| All Other Pins | 5.5 | −0.3 | | |

*All signals reference to GND (pin 17) unless otherwise noted.

### Thermal Information

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristic, LQFP Package (Note 1) | $R_{\theta JA}$ | 52 | °C/W |
| Operating Junction Temperature Range (Note 2) | $T_J$ | 0 to 125 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to 85 | °C |
| Maximum Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |
| Moisture Sensitivity Level, LQFP Package | MSL | 3 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*The maximum package power dissipation must be observed.

1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

**ELECTRICAL CHARACTERISTICS**
(Unless otherwise stated: 0°C < $T_A$ < 85°C; 4.75 V < 5VFILT < 5.25 V; All DAC Codes; $C_{5VFILT}$ = 1.0 μF)

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Error Amplifier** | | | | | |
| Input Bias Current (Note 3) | | −20 | – | 20 | nA |
| Input Offset Voltage (Note 3) | | −1.0 | – | 1.0 | mV |
| Open Loop DC Gain (Note 3) | CL = 60 pF to GND, RL = 10 KΩ to GND | – | 100 | – | dB |
| Open Loop Unity Gain Bandwidth (Note 3) | CL = 60 pF to GND, RL = 10 KΩ to GND | – | 15 | – | MHz |
| Open Loop Phase Margin (Note 3) | CL = 60 pF to GND, RL = 10 KΩ to GND | – | 70 | – | deg |
| Slew Rate (Note 3) | ΔVin = 100 mV, G = −10 V/V,<br>COMP between 1.5 V and 2.5 V,<br>CL = 60 pF to GND,<br>DC Load = ±125 μA | – | 5 | – | V/μs |
| Maximum Output Voltage | 10 mV of overdrive, $I_{SOURCE}$ = 2.0 mA | 2.2 | 5VFILT− 20 mV | – | V |
| Minimum Output Voltage | 10 mV of overdrive, $I_{SINK}$ = 2.0 mA | – | 0.01 | 0.5 | V |
| Output source current (Note 3) | 10 mV input overdrive, COMP = 2.0 V | 2.0 | – | – | mA |
| Output sink current (Note 3) | 10 mV input overdrive, COMP = 1.0 V | 2.0 | – | – | mA |
| **Differential Summing Amplifier** | | | | | |
| VS+ Input Resistance | DRVON = low<br>DRVON = high | –<br>– | 1.5<br>17 | –<br>– | kΩ |
| VS+ Input Bias Voltage | DRVON = low<br>DRVON = high | –<br>– | 0.05<br>0.65 | –<br>– | V |
| VS− Bias Current | VS− = 0 V | – | 33 | – | μA |
| VS+ Input Voltage Range | 0.95 ≤ ΔDIFFOUT/ΔVS+ ≤ 1.05<br>0.5 V ≤ DIFFOUT ≤ 2.0 V | −0.3 | – | 2.0 | V |
| VS− Input Voltage Range | 0.95 ≤ ΔDIFFOUT/ΔVS− ≤ 1.05<br>0.5 V ≤ DIFFOUT ≤ 2.0 V | −0.3 | – | 0.3 | V |
| DC Gain VS+ to DIFFOUT | 0 V < DAC − VS+ < 0.3 V | 0.98 | 1.0 | 1.025 | V/V |
| DAC Accuracy (measured at VS+) | Closed loop measurement including error amplifier. | | | | |
| | 1.0 ≤ DAC ≤ 1.6 | −0.5 | – | 0.5 | % |
| | 0.8 ≤ DAC ≤ 1.0 | −5 | – | 5 | mV |
| −3 dB Bandwidth (Note 3) | CL = 80 pF to GND,<br>RL = 10 KΩ to GND | – | 10 | – | MHz |
| Slew Rate (Note 3) | VS+ − VS− step = ±100 mV;<br>DIFFOUT between 1.3 V and 1.2 V | – | ±5 | – | V/μs |
| Maximum Output Voltage | VS+ minus DAC = 0.8 V<br>$I_{SOURCE}$ = 2.0 mA | 2.0 | 3.0 | – | V |
| Minimum Output Voltage | VS+ minus DAC = −0.8 V<br>$I_{SINK}$ = 2.0 mA | – | 0.01 | 0.5 | V |
| Output source current (Note 3) | VS+ minus DAC = 0.8 V<br>DIFFOUT = 2.0 V | 2.0 | – | – | mA |
| Output sink current (Note 3) | VS+ minus DAC = −0.8 V<br>DIFFOUT = 1.0 V | 2.0 | – | – | mA |

3. Guaranteed by design. Not tested in production.
4. This is the maximum current used by the internal circuits of the NCP5399 with no current flowing into the internal 5 V shunt regulator.

**ELECTRICAL CHARACTERISTICS**
(Unless otherwise stated: 0°C < $T_A$ < 85°C; 4.75 V < 5VFILT < 5.25 V; All DAC Codes; $C_{5VFILT}$ = 1.0 μF)

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Internal Bias Voltage** | | | | | |
| The VDRP pin offset voltage & the voltage at the Error Amp (+) input | | – | 1.30 | – | V |
| **VRDP Adaptive Voltage Positioning Amplifier** | | | | | |
| Current Sense Input to VDRP Gain | −60 mV < (CSxP − CSxN) < 60 mV (each CS input independently) | 5.64 | 5.8 | 5.95 | V/V |
| Current Sense Input to VDRP −3 dB Bandwidth (Note 3) | $C_L$ = 30 pF to GND, $R_L$ = 10 KΩ to GND | – | 4 | – | MHz |
| VDRP Output Slew Rate (Note 3) | ΔVin = 25 mV, VDRP between 1.3 V and 1.9 V, $C_L$ = 330 pF to GND, $R_L$ between 1 k and 10 k to 1.3 V | 2.5 | – | – | V/μs |
| VDRP Output Voltage Offset from Internal Bias Voltage | CSxP = CSNx = 1.3 V | −15.0 | – | +15.0 | mV |
| Maximum VDRP Output Voltage | CSxP − CSxN = 0.1 V (all phases), Isource = 1.0 mA | 2.6 | 3.0 | – | V |
| Minimum VDRP Output Voltage | CSxP − CSxN = −0.033 V (all phases) Isink = 1.0 mA | – | 0.1 | 0.5 | V |
| Output source current (Note 3) | VDRP = 2.0 V | – | 1.3 | – | mA |
| Output sink current (Note 3) | VDRP = 1.0 V | – | 25 | – | mA |
| **Current Sense Amplifiers** | | | | | |
| Input Bias Current (Note 3) | CSxP = CSxN = 1.4 V | −20 | – | 20 | nA |
| Common Mode Input Voltage Range | | −0.3 | – | 2.0 | V |
| Differential Mode Input Voltage Range | | −120 | – | 120 | mV |
| Input Referred Offset Voltage (Note 3) | CSxP = CSxN = 1.000 V | −1.0 | – | 1.0 | mV |
| Current Sense Input to PWM Gain | 0 V < CSxP−CSxN < 0.1 V | – | 6.0 | – | V/V |
| **Oscillator** | | | | | |
| Switching Frequency Range (Note 3) | | 100 | – | 1000 | kHz |
| Switching Frequency Accuracy | ROSC = 50 kΩ<br>ROSC = 25 kΩ<br>ROSC = 10 kΩ | –<br>–<br>950 | 235<br>450<br>1000 | –<br>–<br>1050 | kHz<br>kHz<br>kHz |
| Switching Frequency Tolerance (Note 3) | 100 KHz < Fsw < 1 MHz | – | 15 | – | % |
| ROSC Output Voltage | 20 μA = $I_{ROSC}$ = 250 μA | 1.95 | 2.0 | 2.065 | V |
| **Modulators (PWM Comparators)** | | | | | |
| Minimum Pulse Width (Note 3) | Fs = 1000 KHz | – | 30 | 40 | ns |
| Propagation Delay (Note 3) | ±20 mV of overdrive | – | 20 | – | ns |
| Magnitude of the PWM Ramp | | – | 1 | – | V |
| 0% Duty Cycle | COMP voltage when the PWM outputs remain LOW | – | 1.3 | – | V |
| 100% Duty Cycle | COMP voltage when the PWM outputs remain HIGH | – | 2.3 | – | V |
| PWM Linear Duty Cycle (Note 3) | | – | 90 | – | % |

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**ELECTRICAL CHARACTERISTICS**
(Unless otherwise stated: 0°C < $T_A$ < 85°C; 4.75 V < 5VFILT < 5.25 V; All DAC Codes; $C_{5VFILT}$ = 1.0 μF)

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Modulators (PWM Comparators)** | | | | | |
| PWM Phase Angle Error | | −15 | – | 15 | deg |
| **Power Good Output (PWRGD)** | | | | | |
| PWRGD Output Saturation Voltage | $I_{PWRGD}$ = 10 mA | – | – | 0.4 | V |
| PWRGD Rise Time | External pull−up of 680 Ω to 1.25 V, $C_L$ = 45 pF, ΔVo = 10% to 90% | – | – | 150 | ns |
| PWRGD High − Output Leakage Current | PWRGD = 5.0 V | – | – | 1 | μA |
| PWRGD Upper Threshold Voltage | VCORE increasing, DAC = 1.3 V | – | 300 | – | mV below DAC |
| PWRGD Lower Threshold Voltage | VCORE decreasing, DAC = 1.3 V | – | 350 | – | mV below DAC |
| PWRGD Rising Delay | VCORE increasing | – | – | 3 | ms |
| PWRGD Falling Delay | VCORE decreasing | – | – | 250 | μs |
| **PWM Outputs** | | | | | |
| Output High Voltage | Sourcing 500 μA | 3.0 | – | $V_{5VFILT}$ | V |
| Output Low Voltage | Sinking 500 μA | – | – | 0.15 | V |
| Rise Time | $C_L$ = 20 pF, ΔVo = 0.3 to 2.0 V | – | 7 | 25 | ns |
| Fall Time | $C_L$ = 20 pF, ΔVo = 2.0 V to 0.3 V | – | 9 | 25 | ns |
| Output Impedance − Sourcing | Resistance to 5VFILT | – | 100 | – | Ω |
| Output Impedance − Sinking | Resistance to GND | – | 100 | – | Ω |
| **DRVON** | | | | | |
| Output High Voltage | Sourcing 500 μA | 3.0 | – | – | V |
| Output Low Voltage | Sinking 500 μA | – | – | 0.7 | V |
| Rise Time | $C_L$ = 20 pF, ΔVo = 10% to 90% | – | 24 | 30 | ns |
| Fall Time | $C_L$ = 20 pF, ΔVo = 90% to 10% | – | 11 | 20 | ns |
| Internal Pull Down Resistance | | – | 70 | – | KΩ |
| **Soft−Start** | | | | | |
| Soft−Start Pin Source Current | Voltage on SS pin < DAC | 3.75 | 5.0 | 6.25 | μA |
| Soft−Start Pin Ramp Time | Css = 0.01 μF; Time to 1.05 V | – | 2.2 | – | ms |
| Soft−Start Pin Discharge Voltage | DRVON pin LO (Fault) | – | – | 25 | mV |
| **Enable Input** | | | | | |
| Enable High Input Leakage Current | EN = 3.3 V | – | – | 1.0 | μA |
| Rising Threshold | $V_{UPPER}$ | 0.800 | – | 0.920 | V |
| Falling Threshold | $V_{LOWER}$ | 0.670 | – | 0.830 | V |
| Total Hysteresis | $V_{UPPER} - V_{LOWER}$ | – | 130 | – | mV |
| Enable Delay Time | Time from Enable transitioning HI to initiation of Soft−start | 1.0 | – | 5.0 | ms |
| Disable Delay Time | Time from Enable transitioning LO to DRVON LO | – | 150 | 200 | ns |

3. Guaranteed by design. Not tested in production.
4. This is the maximum current used by the internal circuits of the NCP5399 with no current flowing into the internal 5 V shunt regulator.

**ELECTRICAL CHARACTERISTICS**
(Unless otherwise stated: 0°C < $T_A$ < 85°C; 4.75 V < 5VFILT < 5.25 V; All DAC Codes; $C_{5VFILT}$ = 1.0 μF)

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Current Limit** | | | | | |
| Current Sense Amp to ILIM Gain | 20 mV < (CSx−CSxN) < 60 mV (each CS Input independently) | 5.7 | 5.95 | 6.2 | V/V |
| ILIM Pin Input Bias Current | ILIM = 2.0 V | – | – | 1.0 | μA |
| ILIM Pin Working Voltage Range (Note 3) | | 0.2 | – | 2.0 | V |
| ILIM offset voltage | Offset extrapolated to CSx − CSxN = 0 V and referred to the ILIM pin. | −33 | 17 | 67 | mV |
| Delay (Note 3) | | – | 300 | – | ns |
| **Overvoltage Protection** | | | | | |
| Overvoltage Threshold | | DAC+ 160 | – | DAC+ 200 | mV |
| Delay | | – | 100 | – | ns |
| **Undervoltage Protection** | | | | | |
| $V_{CC}$ UVLO Start Threshold | | – | 9.25 | 9.5 | V |
| $V_{CC}$ UVLO Stop Threshold | | 8.25 | 8.5 | – | V |
| $V_{CC}$ UVLO Hysteresis | | – | 0.75 | – | V |
| **VID Inputs** | | | | | |
| Upper Threshold | $V_{UPPER}$ | – | – | 800 | mV |
| Lower Threshold | $V_{LOWER}$ | 300 | – | – | mV |
| Input Bias Current | | – | – | 500 | nA |
| Delay before Latching VID Change (VID De−Skewing) (Note 3) | Measured from the edge of the 1st VID change | 500 | – | 800 | ns |
| **Internal DAC Slew Rate Limiter** | | | | | |
| Positive Slew Rate Limit | VID step range of +500 mV | – | 6.3 | – | mV/μs |
| Negative Slew Rate Limit | VID step range of −500 mV | – | −6.3 | – | mV/μs |
| **Shunt Regulator** | | | | | |
| Recommended Operating Current | Not Enabled; 243 Ω to 12 V | – | 30 | – | mA |
| Minimum Operating Current | Operating at 1 MHz (Note 4) | 16.5 | – | – | mA |
| Regulated Voltage | EN Low, No PWM; 243 Ω to 12 V, 1.0 μF to GND | – | 5.0 | – | V |
| **DAC Voltage** | | | | | |
| System Voltage Accuracy | 1.0 V < DAC < 1.6 V<br>0. 8375 V < DAC < 1.0 V | – | – | ±0.5<br>±5 | %<br>mV |
| DAC = VR10.x DAC | | – | – | 0.6 | V |
| DAC = MARGIN DAC | | 0.6 | – | 2.0 | V |

3. Guaranteed by design. Not tested in production.
4. This is the maximum current used by the internal circuits of the NCP5399 with no current flowing into the internal 5 V shunt regulator.

| VID4<br>400 mV | VID3<br>200 mV | VID2<br>100 mV | VID1<br>50 mV | VID0<br>25 mV | VID5<br>12.5 mV | VR10.x<br>Voltage (V) | MARGIN<br>Voltage (V) |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 1.6000 | 0.55000 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.5875 | 0.74375 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1.5750 | 0.54375 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1.5625 | 0.73750 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1.5500 | 0.53750 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1.5375 | 0.73125 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1.5250 | 0.53125 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1.5125 | 0.72500 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1.5000 | 0.52500 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1.4875 | 0.71875 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1.4750 | 0.51875 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1.4625 | 0.71250 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1.4500 | 0.51250 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1.4375 | 0.70625 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1.4250 | 0.50625 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1.4125 | 0.70000 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1.4000 | 0.50000 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1.3875 | 0.69375 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1.3750 | OFF |
| 1 | 0 | 1 | 0 | 0 | 0 | 1.3625 | 0.68750 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1.3500 | OFF |
| 1 | 0 | 1 | 0 | 1 | 0 | 1.3375 | 0.68125 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1.3250 | OFF |
| 1 | 0 | 1 | 1 | 0 | 0 | 1.3125 | 0.67500 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1.3000 | OFF |
| 1 | 0 | 1 | 1 | 1 | 0 | 1.2875 | 0.66875 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1.2750 | OFF |
| 1 | 1 | 0 | 0 | 0 | 0 | 1.2625 | 0.66250 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1.2500 | OFF |
| 1 | 1 | 0 | 0 | 1 | 0 | 1.2375 | 0.65625 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1.2250 | OFF |
| 1 | 1 | 0 | 1 | 0 | 0 | 1.2125 | 0.65000 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1.2000 | OFF |
| 1 | 1 | 0 | 1 | 1 | 0 | 1.1875 | 0.64375 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1.1750 | OFF |
| 1 | 1 | 1 | 0 | 0 | 0 | 1.1625 | 0.63750 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1.1500 | OFF |
| 1 | 1 | 1 | 0 | 1 | 0 | 1.1375 | 0.63125 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1.1250 | OFF |
| 1 | 1 | 1 | 1 | 0 | 0 | 1.1125 | 0.62500 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1.1000 | OFF |
| 1 | 1 | 1 | 1 | 1 | 0 | OFF | 0.61875 |

| VID4<br>400 mV | VID3<br>200 mV | VID2<br>100 mV | VID1<br>50 mV | VID0<br>25 mV | VID5<br>12.5 mV | VR10.x<br>Voltage (V) | MARGIN<br>Voltage (V) |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | OFF | OFF |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.0875 | 0.81250 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.0750 | 0.61250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.0625 | 0.80625 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.0500 | 0.60625 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.0375 | 0.80000 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.0250 | 0.60000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.0125 | 0.79375 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.0000 | 0.59375 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0.9875 | 0.78750 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0.9750 | 0.58750 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0.9625 | 0.78125 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0.9500 | 0.58125 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0.9375 | 0.77500 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0.9250 | 0.57500 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0.9125 | 0.76875 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0.9000 | 0.56875 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0.8875 | 0.76250 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0.8750 | 0.56250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0.8625 | 0.75625 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0.8500 | 0.55625 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0.8375 | 0.75000 |

## TYPICAL CHARACTERISTICS

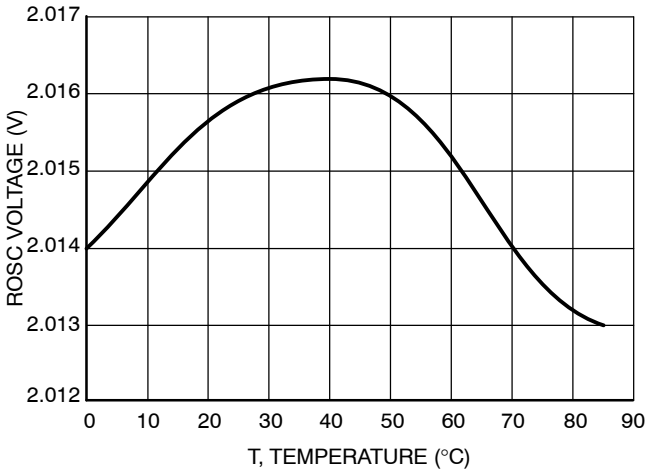



**Figure 2. ROSC Voltage vs. Temperature**

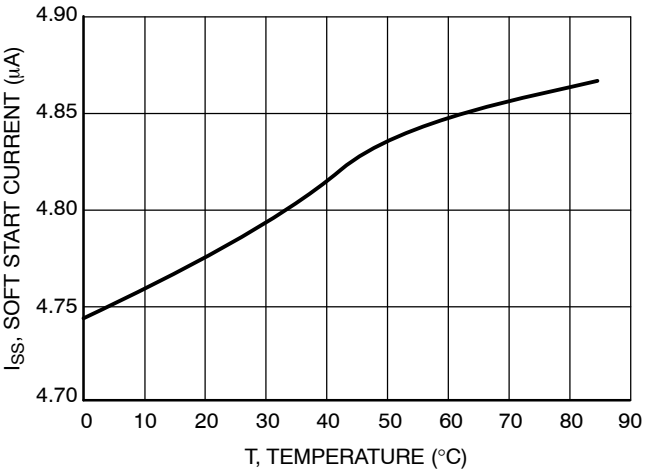



**Figure 3. Soft−Start Current vs. Temperature**

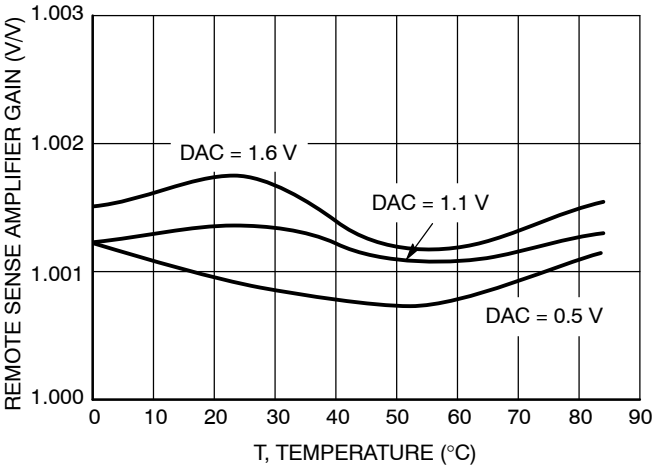



**Figure 4. Remote Sense Amplifier Gain vs. Temperature**

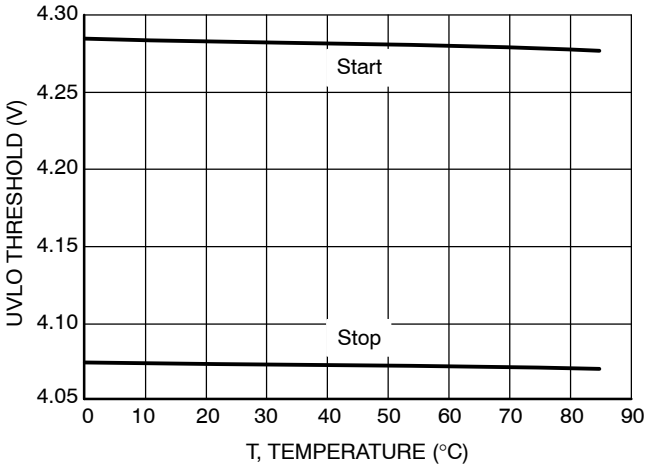



**Figure 5. UVLO Threshold vs. Temperature**

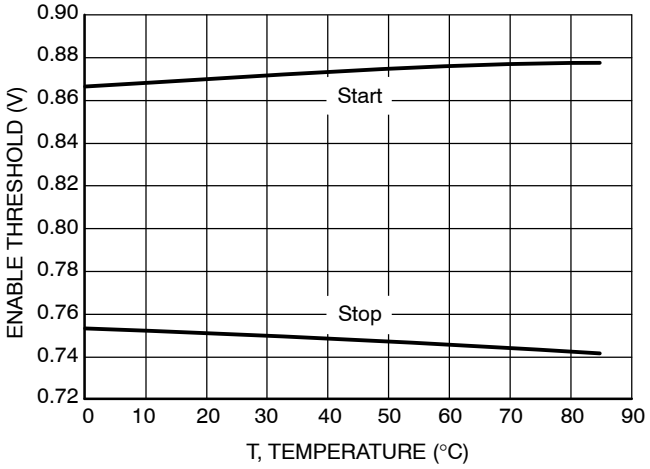



**Figure 6. Enable Threshold vs. Temperature**

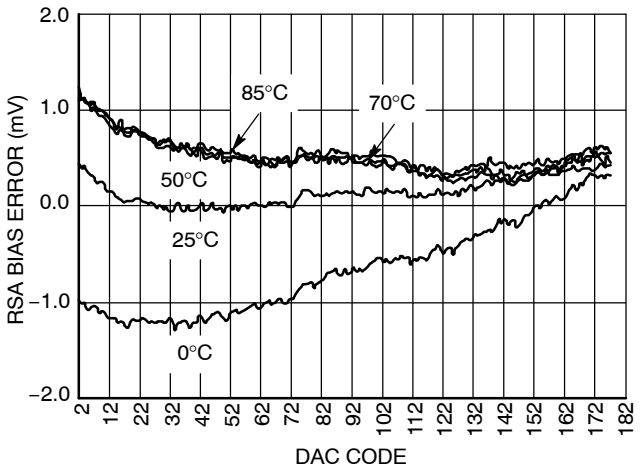



**Figure 7. Remote Sense Amplifier Bias Error vs. DAC Code**

## TYPICAL CHARACTERISTICS

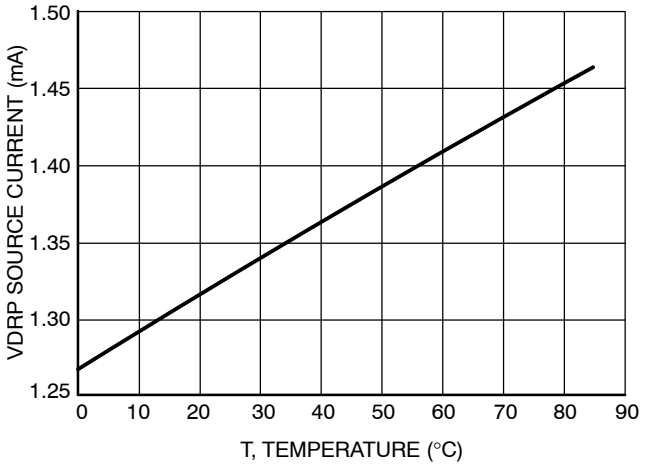



**Figure 8. VDRP Source Current vs. Temperature**

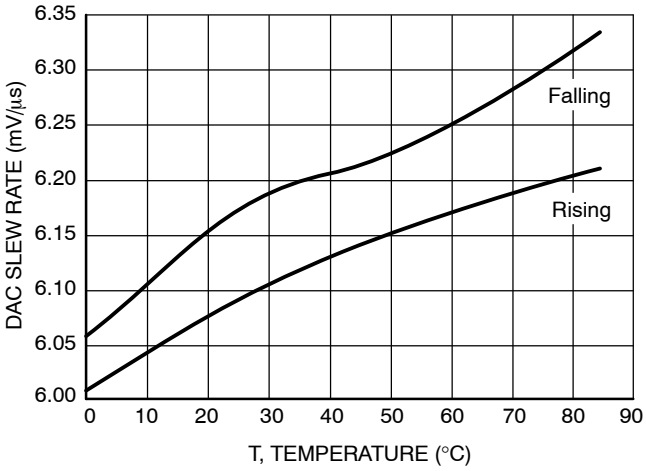



**Figure 9. DAC Slew Rate vs. Temperature**

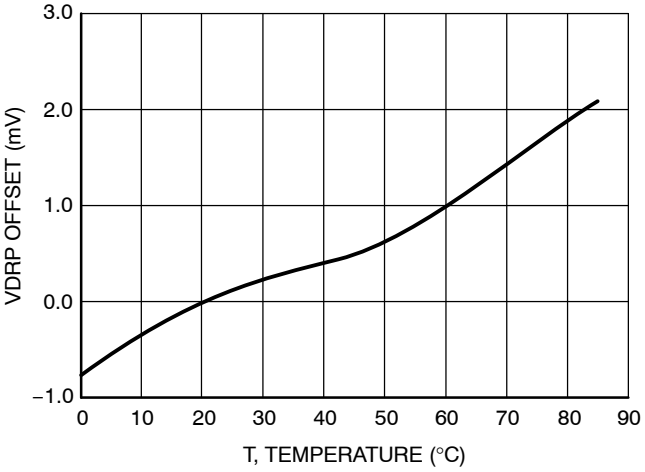



**Figure 10. VDRP Offset vs. Temperature**

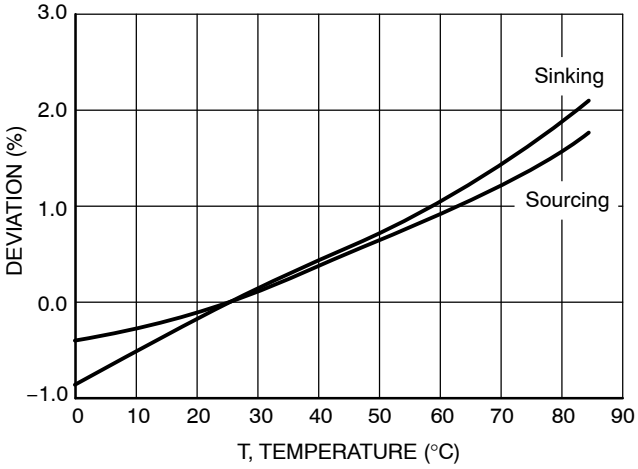



**Figure 11. PWM Output Resistance Deviation vs. Temperature**

## FUNCTIONAL DESCRIPTION

### General

The NCP5399 dual edge modulated multiphase PWM controller is specifically designed with the necessary features for a high current VR10 CPU power system. The IC consists of the following blocks: Precision Programmable DAC, Differential Remote Voltage Sense Amplifier, High Performance Voltage Error Amplifier, Differential Current Feedback Amplifiers, Precision Oscillator and Triangle Wave Generators, and PWM Comparators. Protection features include Undervoltage Lockout, Soft−Start, Overcurrent Protection, Overvoltage Protection, and Power Good Monitor.

### Remote Output Sensing Amplifier (RSA)

A true differential amplifier allows the NCP5399 to measure the Vcore voltage referenced to ground at the point of load. This configuration allows the regulator to cancel out voltage drops in the Vcore ground return path. The RSA also subtracts the DAC (minus VID offset) voltage, thereby producing an unamplified output error voltage at the DIFFOUT pin. This output has a 1.3 volt bias to allow for positive and negative error voltages.

### Precision Programmable DAC

A precision programmable DAC with 2 options is provided. These DAC's have 0.5% accuracy over the entire operating temperature range of the part. The DAC is selected by the voltage applied to pin28 − DAC_SEL. The DAC table can be changed dynamically either before or after ENABLE.

### High Performance Voltage Error Amplifier

The error amplifier is designed to provide high slew rate and bandwidth. Although not required when operating as the controller of a voltage regulator, a capacitor from COMP to VFB is required for stable unity gain test configurations.

### GATE Outputs

The part can be configured to run in single−phase or 2−phase mode. In 2−phase mode, both PWM outputs GATE1 and GATE3 drive external gate drivers as shown in the 2−phase Applications Schematic. In single−phase mode, either GATE output can be used.

### Differential Current Sense Amplifiers

Two differential amplifiers are provided to sense the output current of each phase. The inputs of each current sense amplifier must be connected across the current sensing element of the phase controlled by the corresponding gate output (GATE1 or GATE3). If a phase is unused, the Current Sense inputs of the unused channel should be connected in parallel with the corresponding Current Sense inputs of the other channel. In this way, the CS to VDRP, and the CS to ILIM gains are double the values given in the specifications above, which improves accuracy. A voltage is generated across the current sense element (such as an inductor or sense resistor) by the current flowing in that phase. The outputs of the current sense amplifiers are used to control three functions. First, the outputs control the adaptive voltage positioning, where the output voltage is actively controlled according to the total output current. In this function, current sense outputs are summed so that the total output current is used. This summed output signal is also fed to the current limit circuit. Finally, the individual phase currents are connected to the respective PWM comparators. In this way current balance is accomplished.

### Oscillator and Triangle Wave Generator

A programmable precision oscillator is provided. The oscillator 's frequency is programmed by the resistance connected from the ROSC pin to ground. The user will usually form this resistance from two resistors in order to create a voltage divider that uses the ROSC output voltage as the reference for creating the current limit setpoint voltage. The oscillator frequency range is 100 kHz/phase to 1.0 MHz/phase. The oscillator generates 2 triangle waveforms (symmetrical rising and falling slopes) between 1.3 V and 2.3 V. The triangle waves have a 180 degree phase delay between them.

### PWM Comparators with Hysteresis

Both PWM comparators receive the error amplifier output signal at their noninverting input. Each comparator receives one of the triangle waves offset by 1.3 V at it's inverting input. The output of the comparators generate the PWM outputs GATE1 and GATE3. During steady state operation, the duty cycle will center on the valley of the triangle waveform, with steady state duty cycle calculated by $V_{out}/V_{in}$. During a transient event, both high and low comparator output transitions shift phase to the points where the error amplifier output intersects the down and up ramp of the triangle wave.

## Protection Features

### Undervoltage Lockout

An undervoltage lockout (UVLO) senses the voltage at the $V_{CC}$ input. During powerup, the $V_{CC}$ input voltage to the controller is monitored, and the PWM outputs and the soft−start circuit are disabled until the input voltage exceeds the threshold voltage of the UVLO comparator. The UVLO comparator incorporates hysteresis to avoid chattering, since $V_{CC}$ is likely to decrease as soon as the converter initiates soft−start.

### Overcurrent Shutdown

The NCP5399 incorporates a programmable overcurrent function. A comparator and latch make up this function. The inverting input of the comparator is connected to the ILIM pin. The voltage at this pin sets the maximum output current the converter can produce. The ROSC pin provides a convenient and accurate reference voltage from which a resistor divider can create the overcurrent setpoint voltage. Although not actually disabled, tying the ILIM pin directly to the ROSC pin sets the limit above useful levels – effectively disabling overcurrent shutdown. The comparator noninverting input is the summed current information from the current sense amplifiers. The overcurrent latch is set when the current information exceeds the voltage at the ILIM pin. The outputs are immediately disabled, the PWRGD and DRVON pins are pulled low, and the soft−start is pulled low. The outputs will remain disabled until the $V_{CC}$ voltage is removed and re−applied, or the ENABLE input is brought low and then high.

### Overvoltage Protection and Power Good Monitor

An output voltage monitor is incorporated. During normal operation, if the voltage at the DIFFOUT pin exceeds 1.5 V, the PWRGD pin goes low, the DRVON signal remains high, the PWM outputs are set low. The outputs will remain disabled until the VCC voltage is removed and reapplied. During normal operation, if the output voltage falls more than 350 mV below the DAC setting, the PWRGD pin will be set low until the output rises.

### Soft−Start

The NCP5399 incorporates an externally programmable soft−start. The soft−start circuit works by controlling the ramp−up of the DAC voltage during powerup. The initial soft−start pin voltage is 0 V. The soft−start circuitry clamps the DAC input of the Remote Sense Amplifier to the SS pin voltage until the SS pin voltage exceeds the DAC setting (minus VID offset). Thereafter, the clamp on the DAC voltage is removed and the soft−start pin is pulled to 0 V.

### Shunt Regulator

An internal shunt regulator connected to the 5VFILT pin is provided to convert the 12 V present at the VCC pin to the 5 V required to power the NCP5399 circuitry. A 220 to 250 ohm resistor rated for at least 0.25 Watt dissipation must be connected between the VCC and 5VFILT pins, in order to limit the current drawn from the 12 V source. A 1.0 μF ceramic capacitor must be connected from the 5VFILT pin to ground as close to the pins as possible.

### Programming the Switching Frequency

The switching frequency of the NCP5399 is controlled by the current flowing out of the Rosc pin. Since the voltage on the Rosc pin is fixed at 2 V, the current out of the pin, and the operating frequency is a function of the sum of the resistance of RLIM1 and RLIM2. The frequency can be determined with the following formula:

$$Freq = 7750\ Rosc^{-0.8887} \quad \text{(eq. 1)}$$

$$Rosc = \frac{23790}{Freq^{1.1252}}$$

Where Freq is the switching frequency (per phase) in kHz, and Rosc is the sum of the resistance RLIM1 and RLIM2 in kohm.

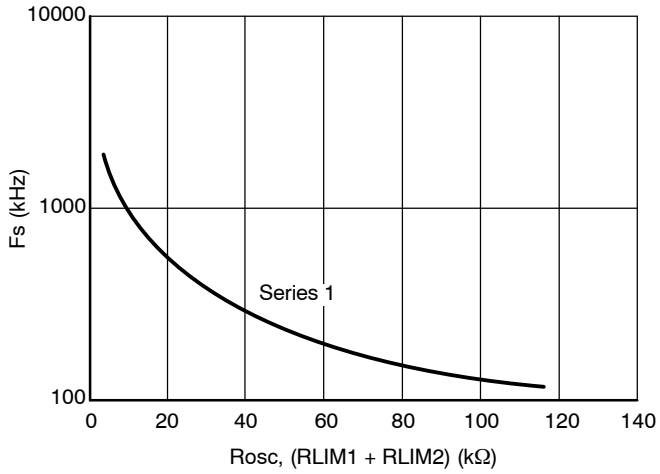



**Figure 12.**

The current limit function is based on the total sensed current of all phases multiplied by a gain of 6. DCR sensed inductor current is function of the winding temperature. The best approach is to set the maximum current limit based on the expected average maximum temperature of the inductor windings.

$$DCR_{Tmax} = DCR_{25C} \cdot (1 + 0.00393\ (T_{max} - 25)) \quad \text{(eq. 2)}$$

Calculate the current limit voltage:

$$V_{ILIMIT} \cong 6 \cdot \left( I_{MIN\_OCP} \cdot DCR_{Tmax} + \frac{DCR_{Tmax} \cdot Vout}{2 \cdot Vin \cdot F_{sw}} \cdot \left( \frac{Vin - Vout}{L} - (N-1) \cdot \frac{Vout}{L} \right) \right) \quad \text{(eq. 3)}$$

Solve for the individual resistors:

$$RLIM2 = \frac{V_{ILIMIT} \cdot R_{TOTAL}}{2 \cdot V} \quad \text{(eq. 4)}$$

$$RLIM1 = R_{TOTAL} - R_{LIM2} \quad \text{(eq. 5)}$$

#### Final Equation for the Current Limit Threshold

$$I_{LIMIT}(T_{inductor}) \cong \frac{\left( \frac{2 \cdot V \cdot RLIM2}{RLIM1 + RLIM2} \right)}{6 \cdot (DCR_{25C} \cdot (1 + 0.00393(T_{Inductor} - 25)))} - \frac{Vout}{2 \cdot Vin \cdot F_{sw}} \cdot \left( \frac{Vin - Vout}{L} - (N-1) \cdot \frac{Vout}{L} \right) \quad \text{(eq. 6)}$$

### Inductor Selection

When using inductor current sensing it is recommended that the inductor does not saturate by more than 10% at maximum load. The inductor also must not go into hard saturation before current limit trips. The demo board includes a two phase output filter using the T50–8 core from Micrometals with 4turns and a DCR target of 0.75 mΩ @ 25°C. Smaller DCR values can be used, however, current sharing accuracy and droop accuracy decrease as DCR decreases.

## Inductor Current Sense Compensation

The NCP5399 uses the inductor current sensing method. This method uses an RC filter to cancel out the inductance of the inductor and recover the voltage that is the result of the current flowing through the inductor's DCR. This is done by matching the RC time constant of the current sense filter to the L/DCR time constant. The first cut approach is to use a 0.1 μF capacitor for C and then solve for R.

$$Rsense(T) = \frac{L}{0.1 \cdot \mu F \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot (T-25))} \quad \text{(eq. 7)}$$

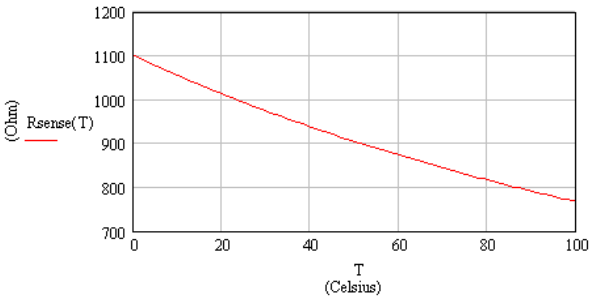



**Figure 13.**

Because the inductor value is a function of load and inductor temperature final selection of R is best done experimentally on the bench by monitoring the Vdroop pin and performing a step load test on the actual solution.

## Simple Average PSPICE Model

A simple state average model shown in Figure 14 can be used to determine a stable solution and provide insight into the control system.

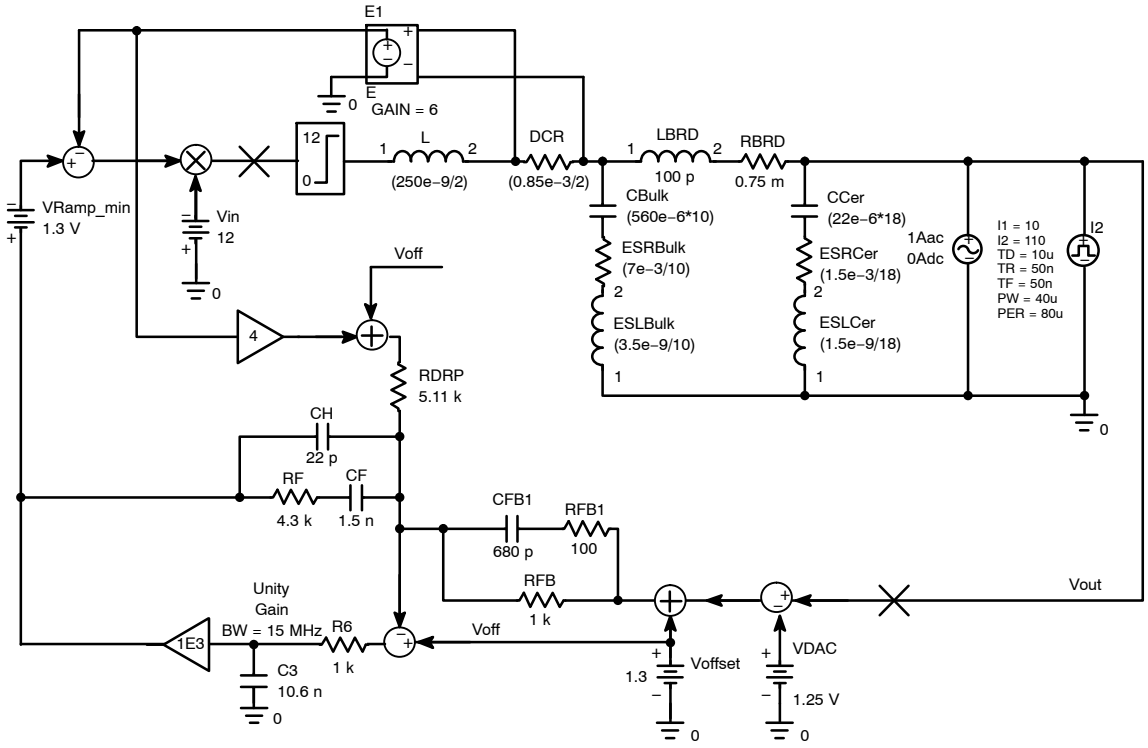



**Figure 14.**

## Compensation and Output Filter Design

The values shown on the demo board are a good place to start for any similar output filter solution. The dynamic performance can then be adjusted by swapping out various individual components.

If the required output filter and switching frequency are significantly different, it's best to use the available PSPICE models to design the compensation and output filter from scratch.

The design target for this demo board was 1.0 mΩ out to 2.0 MHz. The phase switching frequency is currently set to 330 kHz. It can easily be seen that the board impedance of 0.75 mΩ between the load and the bulk capacitance has a large effect on the output filter. In this case the ten 560 μF bulk capacitors have an ESR of 7.0 mΩ. Thus the bulk ESR plus the board impedance is 0.7 mΩ + 0.75 mΩ or 1.45 mΩ. The actual output filter impedance does not drop to 1.0 mΩ until the ceramic breaks in at over 375 kHz. The

controller must provide some loop gain slightly less than one out to a frequency in excess 300 kHz. At frequencies below where the bulk capacitance ESR breaks with the bulk capacitance, the DC−DC converter must have sufficiently high gain to control the output impedance completely. Standard Type−3 compensation works well with the NCP5399. RFB1 should be kept above 50 Ω to ensure compensator stability.

The goal is to compensate the system such that the resulting gain generates constant output impedance from DC up to the frequency where the ceramic takes over holding the impedance below 1.0 mΩ. See the example of the locations of the poles and zeros that were set to optimize the model above.

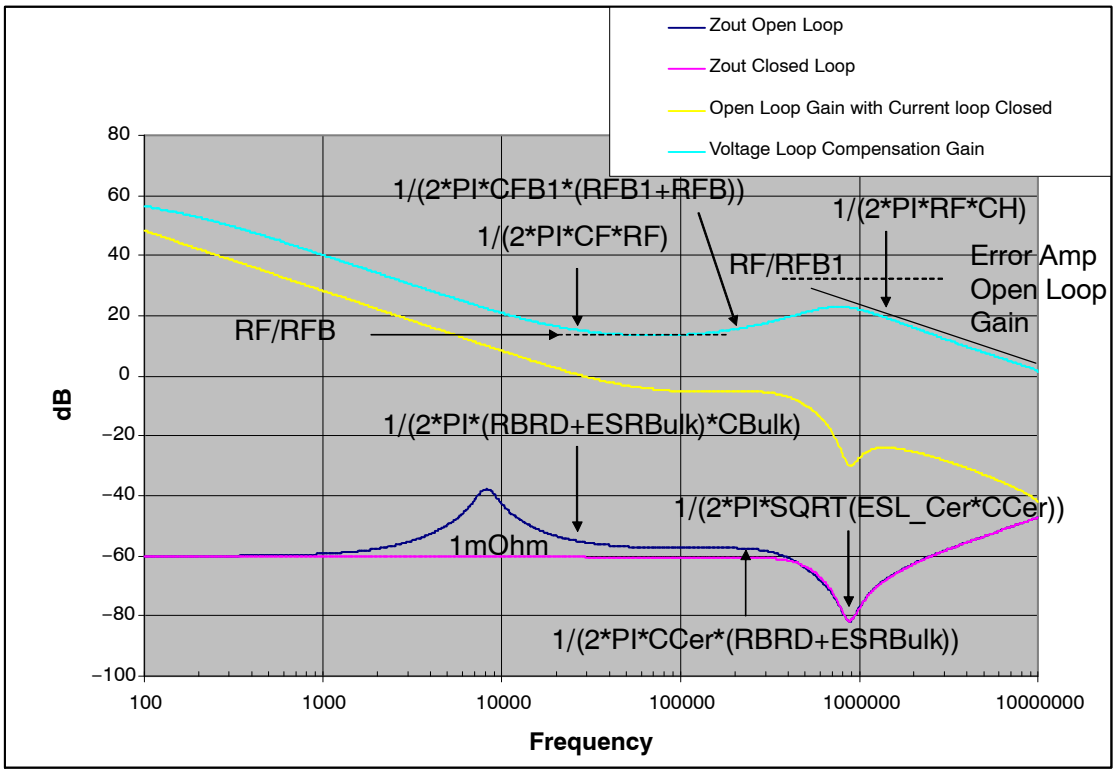



**Figure 15.**

By matching the following equations a good set of starting compensation values can be found for a typical mixed bulk and ceramic capacitor type output filter.

$$\frac{1}{2\pi \cdot CF \cdot RF} = \frac{1}{2\pi \cdot (RBRD + ESRBulk) \cdot CBulk}$$
$$\frac{1}{2\pi \cdot CFBI \cdot (RFBI + RFB)} = \frac{1}{2\pi \cdot CCer * (RBRD + ESRBulk)} \quad \text{(eq. 8)}$$

RFB should be set to provide optimal thermal compensation in conjunction with thermistor RT2, RISO1 and RISO2. With RFB set to 1.0 kΩ, RFB1 is usually set to 100 Ω for maximum phase boost, and the value of RF is typically set to 4.0 kΩ.

## Droop Injection and Thermal Compensation

The VDRP signal is generated by summing the sensed output currents for each phase and applying a gain of approximately six. VDRP is externally summed into the feedback network by the resistor RDRP. This introduces an offset which is proportional to the output current thereby forcing a controlled, resistive output impedance.

RRDP determines the target output impedance by the basic equation:

$$\frac{Vout}{Iout} = Zout = \frac{RFB \cdot DCR \cdot 6}{RDRP} \qquad RDRP = \frac{RFB \cdot DCR \cdot 6}{Zout} \qquad \text{(eq. 9)}$$

The value of the inductor's DCR varies with temperature according to the following equation 11:

$$DCR(T) = DCR_{25C} \cdot (1 + 0.00393(T-25)) \qquad \text{(eq. 10)}$$

The system can be thermally compensated to cancel this effect to a great degree by adding an NTC (negative temperature coefficient resistor) in parallel with RFB to reduce the droop gain as the temperature increases. The NTC device is nonlinear. Putting a resistor in series with the NTC helps make the device appear more linear with temperature. The series resistor is split and inserted on both sides of the NTC to reduce noise injection into the feedback loop. The recommended total value for RISO1 plus RISO2 is approximately 1.0 kΩ.

The output impedance varies with inductor temperature by the equation:

$$\vdash Zout(T) = \frac{RFB \cdot DCR_{25C} \cdot (1 + 0.00393(T-25)) \cdot 6}{Rdroop} \qquad \text{(eq. 11)}$$

By including the NTC RT2 and the series isolation resistors the new equation becomes:

$$Zout(T) = \frac{\frac{RFB \cdot (RISO1 + RT2(T) + RISO2)}{RFB + RISO1 + RT2(T) + RISO2} \cdot DCR_{25C} \cdot (1 + 0.00393(T-25)) \cdot 6}{Rdroop} \qquad \text{(eq. 12)}$$

The typical equation of a NTC is based on a curve fit equation 14.

$$RT2(T) = RT2_{25C} \cdot e^{\beta\left[\left(\frac{1}{273+T}\right) - \left(\frac{1}{298}\right)\right]} \qquad \text{(eq. 13)}$$

The demo board is populated with a 10 kΩ NTC with a Beta of 4300. Figure 16 shows the uncompensated and compensated output impedance versus temperature.

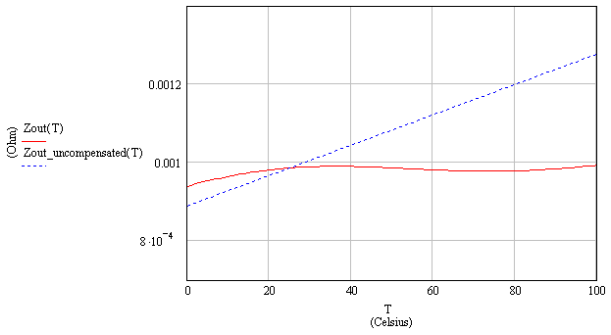



**Figure 16. Uncompensated and Compensated Output Impedance vs. Temperature**

ON Semiconductor provides an excel spreadsheet to help with the selection of the NTC. The actual selection of the NTC will be effected by the location of the output inductor with respect to the NTC and airflow, and should be verified with an actual system thermal solution.

## OVP

The overvoltage protection threshold is not adjustable. OVP protection is enabled as soon as soft−start begins and is disabled when the part is disabled. When OVP is tripped, the controller commands all four gate drivers to enable their low side MOSFETs, and VR_RDY transitions low. In order to recover from an OVP condition, $V_{CC}$ must fall below the UVLO threshold. See the state diagram for further details. The OVP circuit monitors the output of DIFFOUT. If the DIFFOUT signal reaches 180 mV above the nominal 1.3 V offset the OVP will trip. The DIFFOUT signal is the difference between the output voltage and the DAC voltage plus the 1.3 V internal offset. This results in the OVP tracking the DAC voltage even during a dynamic change in the VID setting during operation.

## Gate Driver and MOSFET Selection

ON Semiconductor provides the NCP3418B as a companion gate driver IC. The NCP3418B driver is optimized to work with a range of MOSFETs commonly used in CPU applications. The NCP3418B provides special functionality and is required for the high performance dynamic VID operation of the part. Contact your local ON Semiconductor applications engineer for MOSFET recommendations.

## Board Stack−Up

The demo board follows the recommended Intel Stack−up and copper thickness as shown.

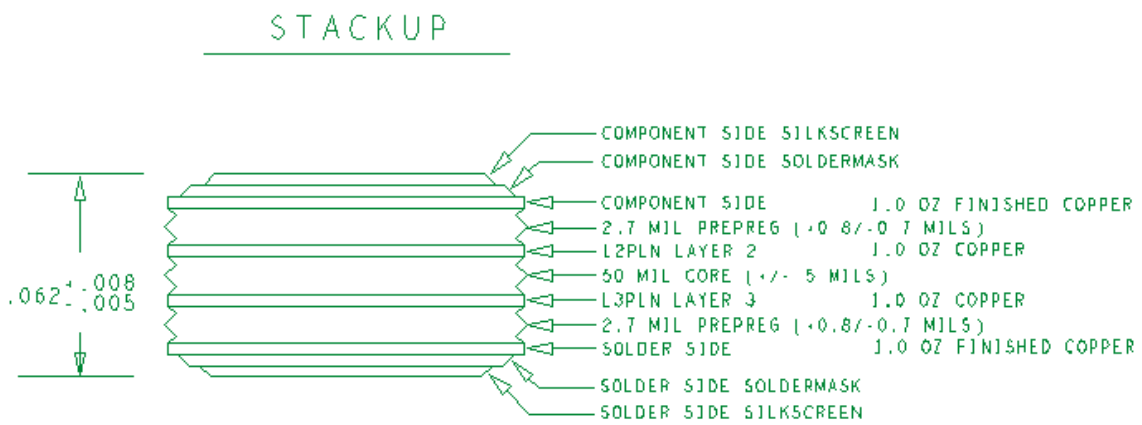



**Figure 17.**

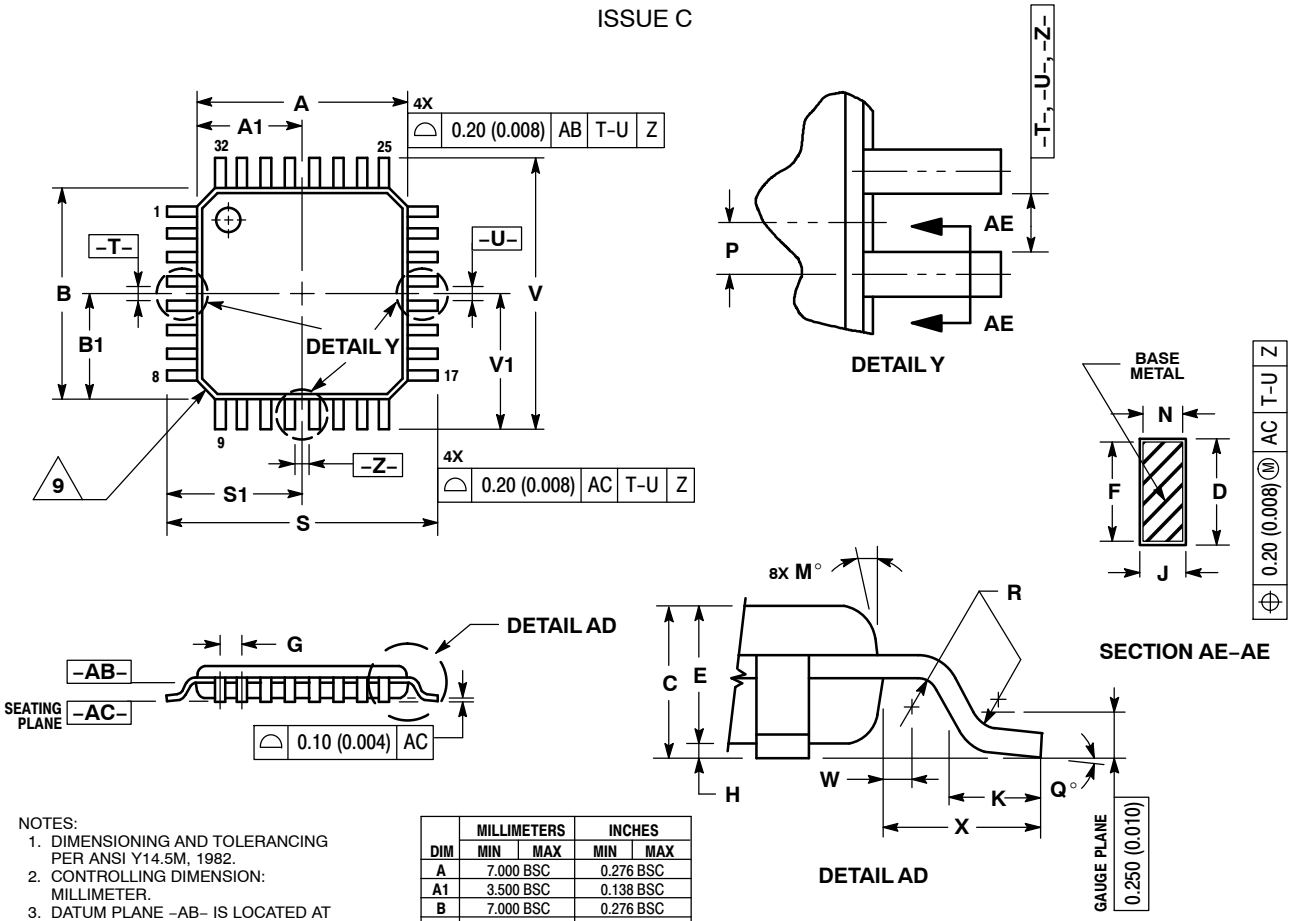
## Board Layout

A complete Allegro ATX and BTX demo board layout file and schematics are available by request at www.onsemi.com and can be viewed using the Allegro Free Physical Viewer 15.x from the Cadence website http://www.cadence.com/.

Close attention should be paid to the routing of the sense traces and control lines that propagate away from the controller IC. Routing should follow the demo board example. For further information or layout review contact ON Semiconductor.

## PACKAGE DIMENSIONS

**32 LEAD LQFP**
CASE 873A–02
ISSUE C

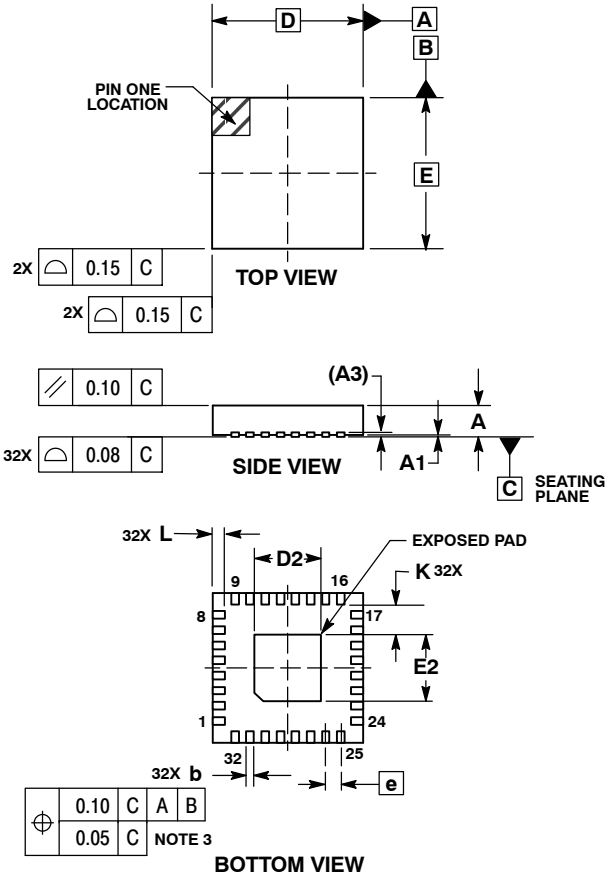



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.000 BSC | | 0.276 BSC | |
| A1 | 3.500 BSC | | 0.138 BSC | |
| B | 7.000 BSC | | 0.276 BSC | |
| B1 | 3.500 BSC | | 0.138 BSC | |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC | | 0.031 BSC | |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.450 | 0.750 | 0.018 | 0.030 |
| M | 12° REF | | 12° REF | |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC | | 0.016 BSC | |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC | | 0.354 BSC | |
| S1 | 4.500 BSC | | 0.177 BSC | |
| V | 9.000 BSC | | 0.354 BSC | |
| V1 | 4.500 BSC | | 0.177 BSC | |
| W | 0.200 REF | | 0.008 REF | |
| X | 1.000 REF | | 0.039 REF | |

## PACKAGE DIMENSIONS

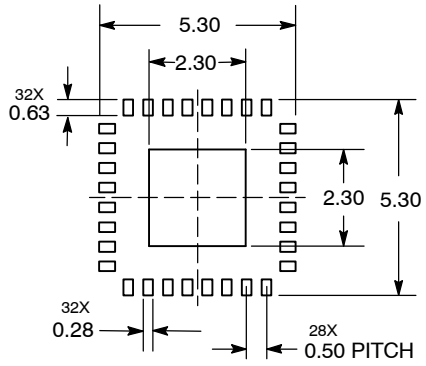
**QFN32 5x5, 0.5P**
CASE 485AM−01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.800 | 0.900 | 1.000 |
| A1 | 0.000 | 0.025 | 0.050 |
| A3 | | 0.200 REF | |
| b | 0.180 | 0.250 | 0.300 |
| D | | 5.00 BSC | |
| D2 | 2.100 | 2.200 | 2.300 |
| E | | 5.00 BSC | |
| E2 | 2.100 | 2.200 | 2.300 |
| e | | 0.500 BSC | |
| K | | 1.000 REF | |
| L | 0.300 | 0.400 | 0.500 |

### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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