



**THE DATASHEET OF  
NCV8402ASTT3G**



# Self-Protected Low Side Driver with Temperature and Current Limit

## NCV8402, NCV8402A

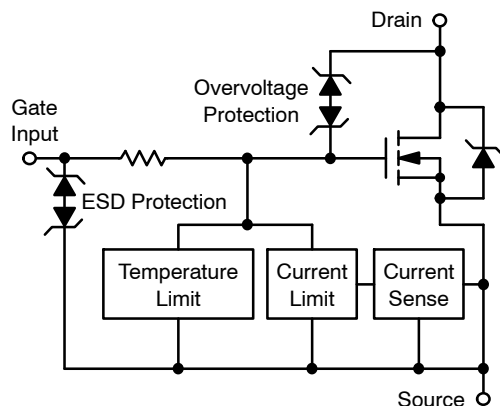
NCV8402/A is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

### Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- NCV8402AMNWT1G – Wettable Flanks Product
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

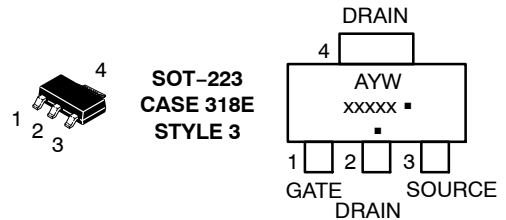
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial



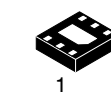
$V_{(BR)DSS}$ (Clamped)	$R_{DS(ON)}$ TYP	$I_D$ MAX
42 V	165 mΩ @ 10 V	2.0 A*

\*Max current limit value is dependent on input condition.

### MARKING DIAGRAMS



SOT-223  
CASE 318E  
STYLE 3



DFN6  
CASE 506AX

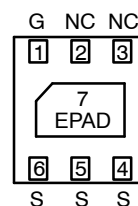


DFN6 (WF)  
CASE 506DK

A = Assembly Location  
Y = Year  
W or WW = Work Week  
xxxxx = V8402 or 8402A  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### DFN6 PACKAGE PIN DESCRIPTION



Pin #	Symbol	Description
1	G	Gate Input
2	NC	No Connect
3	NC	No Connect
4	S*	Source
5	S*	Source
6	S*	Source
7	EPAD	Drain

\*Pins 4, 5, 6 are internally shorted together. It is recommended to short these pins externally.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

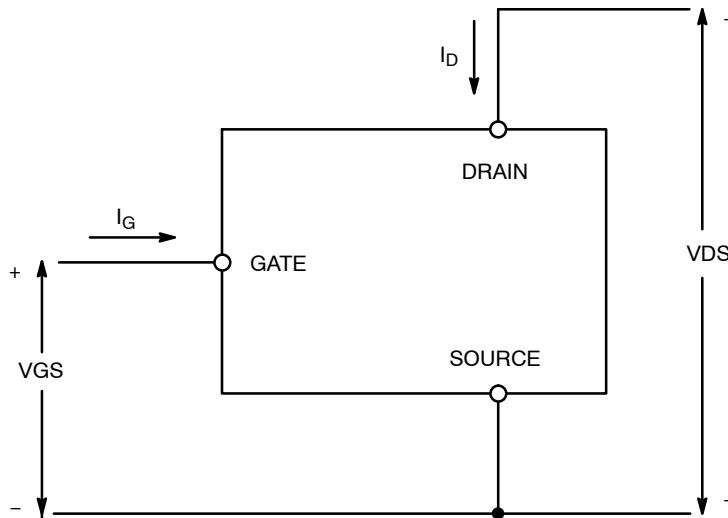
# NCV8402, NCV8402A

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	42	V
Drain-to-Gate Voltage Internally Clamped ( $R_G = 1.0\text{ M}\Omega$ )	$V_{DGR}$	42	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 14$	V
Continuous Drain Current	$I_D$	Internally Limited	
Total Power Dissipation – SOT-223 Version @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2) @ $T_S = 25^\circ\text{C}$	$P_D$	1.1 1.74 8.9	W
Total Power Dissipation – DFN Version @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2) @ $T_S = 25^\circ\text{C}$	$P_D$	0.76 1.78 8.9	W
Maximum Continuous Drain Current – SOT-223 Version @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2) @ $T_S = 25^\circ\text{C}$	$I_D$	1.54 1.94 6.75	A
Maximum Continuous Drain Current – DFN Version @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2) @ $T_S = 25^\circ\text{C}$	$I_D$	1.28 1.97 6.75	A
Thermal Resistance SOT223 Junction-to-Ambient Steady State (Note 1) SOT223 Junction-to-Ambient Steady State (Note 2) SOT223 Junction-to-Soldering Point Steady State  DFN Junction-to-Ambient Steady State (Note 1) DFN Junction-to-Ambient Steady State (Note 2) DFN Junction-to-Soldering Point Steady State	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$  $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	114 72 14  163 70 14	$^\circ\text{C/W}$
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 32\text{ V}$ , $V_G = 5.0\text{ V}$ , $I_{PK} = 1.0\text{ A}$ , $L = 300\text{ mH}$ , $R_{G(ext)} = 25\ \Omega$ )	$E_{AS}$	150	mJ
Load Dump Voltage ( $V_{GS} = 0$ and $10\text{ V}$ , $R_I = 2.0\ \Omega$ , $R_L = 9.0\ \Omega$ , $t_d = 400\text{ ms}$ )	$V_{LD}$	55	V
Operating Junction Temperature	$T_J$	-40 to 150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06" thick).
- Surface-mounted onto 2" sq. FR4 board (1" sq., 1 oz. Cu, 0.06" thick).



**Figure 1. Voltage and Current Convention**

# NCV8402, NCV8402A

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage (Note 3)	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 25°C	V <sub>(BR)DSS</sub>	42	46	55	V
	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 150°C (Note 5)		40	45	55	
Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V, T <sub>J</sub> = 25°C	I <sub>DSS</sub>		0.25	4.0	μA
Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V, T <sub>J</sub> = 150°C (Note 5)	I <sub>DSS</sub>		1.1	20	μA
Gate Input Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 5.0 V	I <sub>GSSF</sub>		50	100	μA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 150 μA	V <sub>GS(th)</sub>	1.3	1.8	2.2	V
Gate Threshold Temperature Coefficient		V <sub>GS(th)</sub> /T <sub>J</sub>		4.0		-mV/°C
Static Drain-to-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.7 A, T <sub>J</sub> = 25°C	R <sub>DS(on)</sub>		165	200	mΩ
	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.7 A, T <sub>J</sub> = 150°C (Note 5)			305	400	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 1.7 A, T <sub>J</sub> = 25°C			195	230	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 1.7 A, T <sub>J</sub> = 150°C (Note 5)			360	460	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 25°C			190	230	
	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 150°C (Note 5)			350	460	
Source-Drain Forward On Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.0 A	V <sub>SD</sub>		1.0		V

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Time (10% V <sub>IN</sub> to 90% I <sub>D</sub> )	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 12 V, I <sub>D</sub> = 2.5 A, R <sub>L</sub> = 4.7 Ω	t <sub>on</sub>		25	30	μs
Turn-Off Time (90% V <sub>IN</sub> to 10% I <sub>D</sub> )		t <sub>off</sub>		120	200	μs
Turn-On Rise Time (10% I <sub>D</sub> to 90% I <sub>D</sub> )		t <sub>rise</sub>		20	25	μs
Turn-Off Fall Time (90% I <sub>D</sub> to 10% I <sub>D</sub> )		t <sub>fall</sub>		50	70	μs
Slew-Rate ON (70% to 50% V <sub>DD</sub> )		-dV <sub>DS</sub> /dt <sub>ON</sub>		0.8	1.2	V/μs
Slew-Rate OFF (50% to 70% V <sub>DD</sub> )		dV <sub>DS</sub> /dt <sub>OFF</sub>		0.3	0.5	V/μs

## SELF PROTECTION CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (Note 4)

Current Limit	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5.0 V, T <sub>J</sub> = 25°C (Note 6)	I <sub>LIM</sub>	3.7	4.3	5.0	A
	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5.0 V, T <sub>J</sub> = 150°C (Notes 5, 6)		2.3	3.0	3.7	
	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 25°C (Note 6)		4.2	4.8	5.4	
	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 150°C (Notes 5, 6)		2.7	3.6	4.5	
Temperature Limit (Turn-off)	V <sub>GS</sub> = 5.0 V (Notes 5, 6)	T <sub>LIM(off)</sub>	150	175	200	°C
Thermal Hysteresis	V <sub>GS</sub> = 5.0 V	ΔT <sub>LIM(on)</sub>		15		
Temperature Limit (Turn-off)	V <sub>GS</sub> = 10 V (Notes 5, 6)	T <sub>LIM(off)</sub>	150	165	185	
Thermal Hysteresis	V <sub>GS</sub> = 10 V	ΔT <sub>LIM(on)</sub>		15		

## GATE INPUT CHARACTERISTICS (Note 5)

Device ON Gate Input Current	V <sub>GS</sub> = 5 V I <sub>D</sub> = 1.0 A	I <sub>GON</sub>		50		μA
	V <sub>GS</sub> = 10 V I <sub>D</sub> = 1.0 A			400		

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Fault conditions are viewed as beyond the normal operating range of the part.

5. Not subject to production testing.

6. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

# NCV8402, NCV8402A

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
-----------	----------------	--------	-----	-----	-----	------

### GATE INPUT CHARACTERISTICS (Note 5)

Current Limit Gate Input Current	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$	$I_{GCL}$		0.05		mA
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$			0.4		
Thermal Limit Fault Gate Input Current	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$	$I_{GTL}$		0.15		mA
	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$			0.7		

### ESD ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 5)

Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000			V
	Machine Model (MM)		400			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.
6. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

TYPICAL PERFORMANCE CURVES

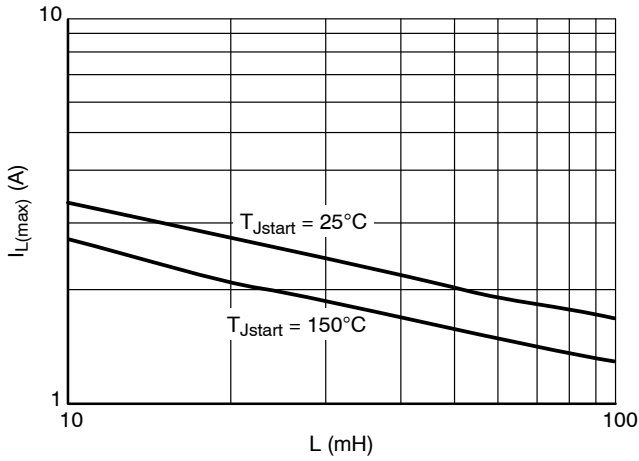


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

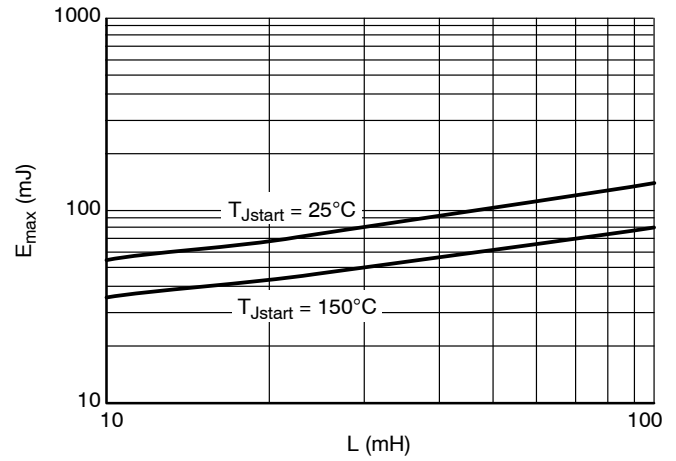


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

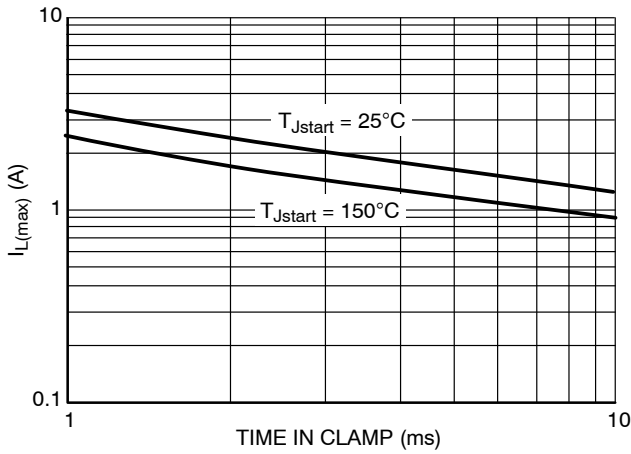


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

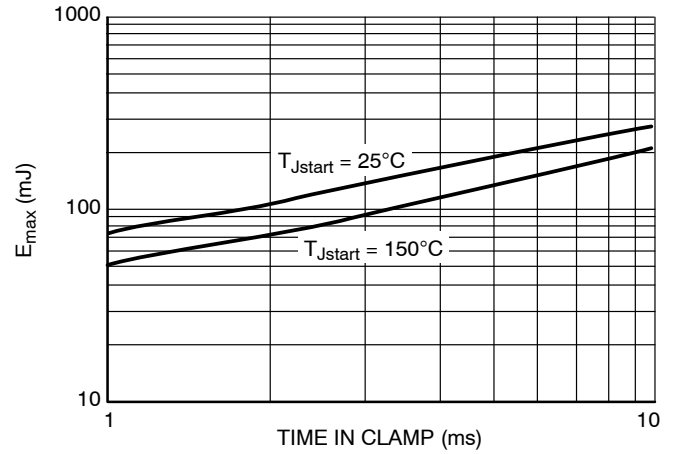


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

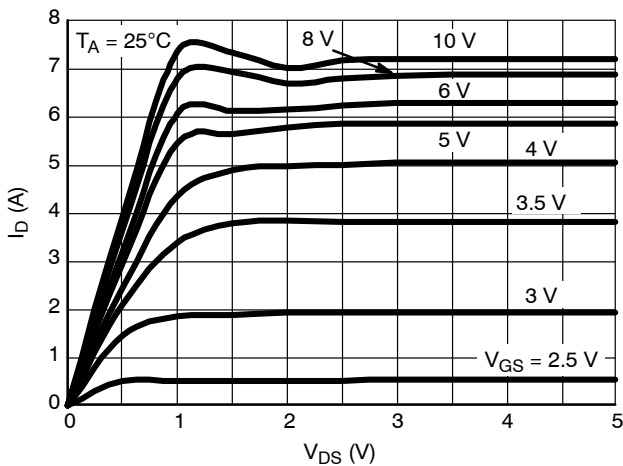


Figure 6. On-state Output Characteristics

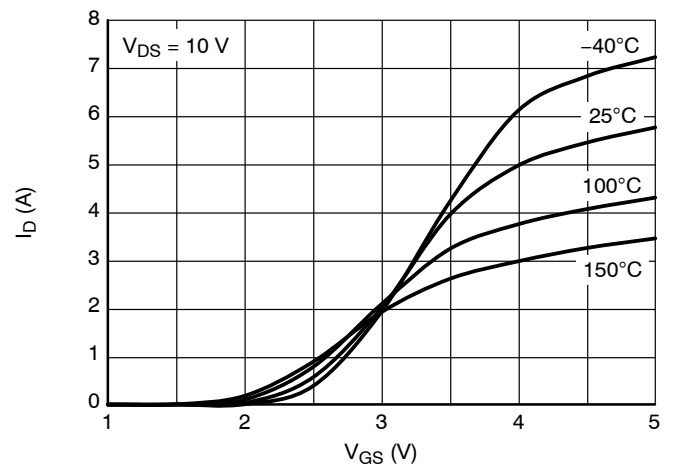


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

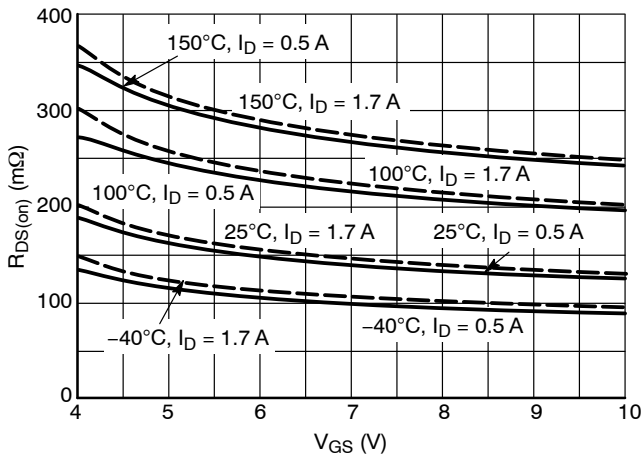


Figure 8.  $R_{DS(on)}$  vs. Gate-Source Voltage

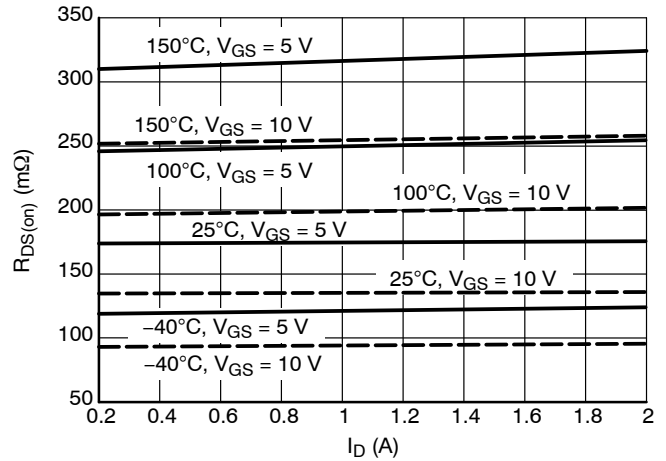


Figure 9.  $R_{DS(on)}$  vs. Drain Current

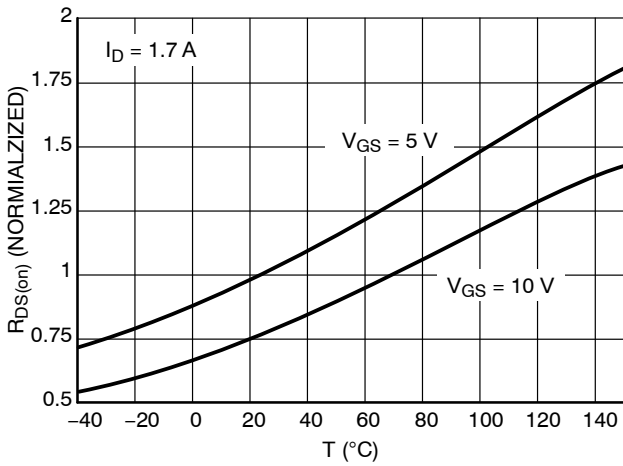


Figure 10. Normalized  $R_{DS(on)}$  vs. Temperature

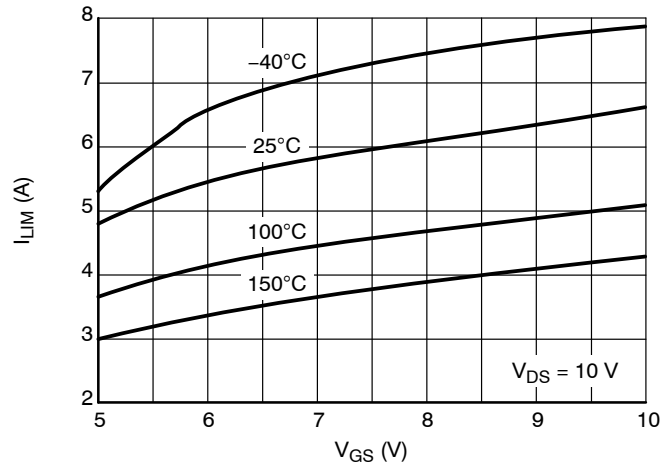


Figure 11. Current Limit vs. Gate-Source Voltage

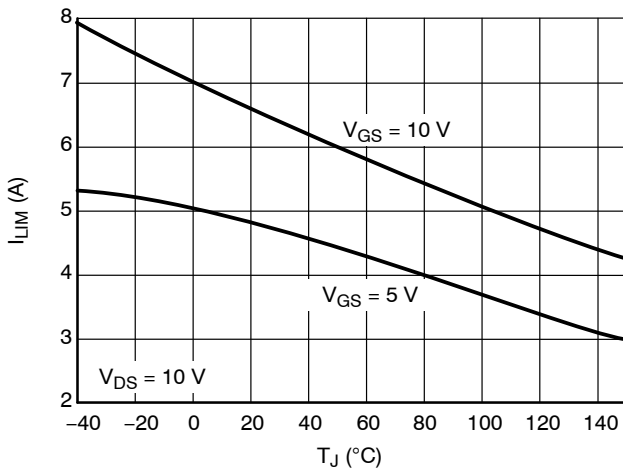


Figure 12. Current Limit vs. Junction Temperature

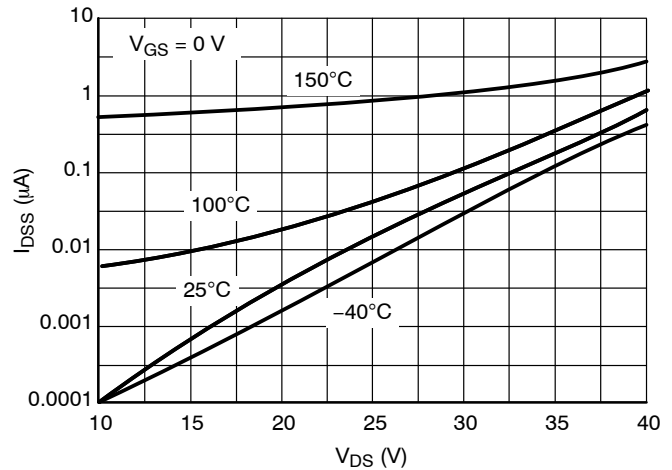


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

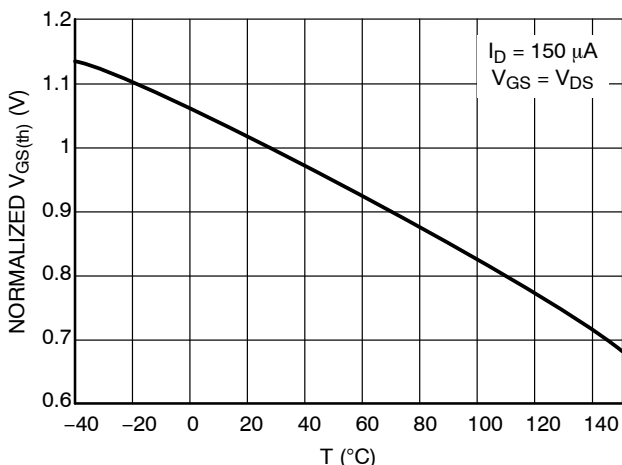


Figure 14. Normalized Threshold Voltage vs. Temperature

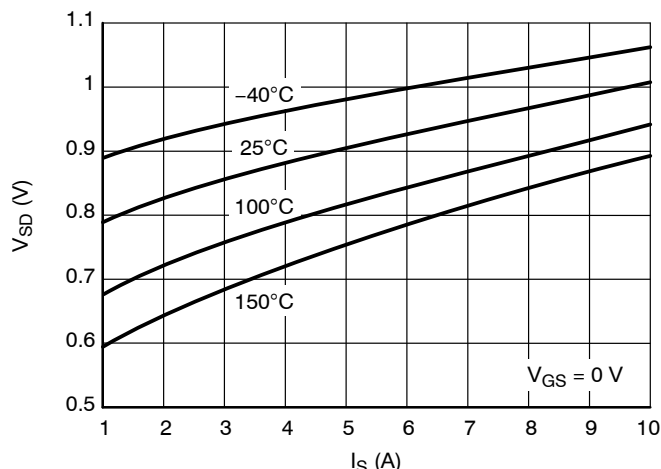


Figure 15. Source-Drain Diode Forward Characteristics

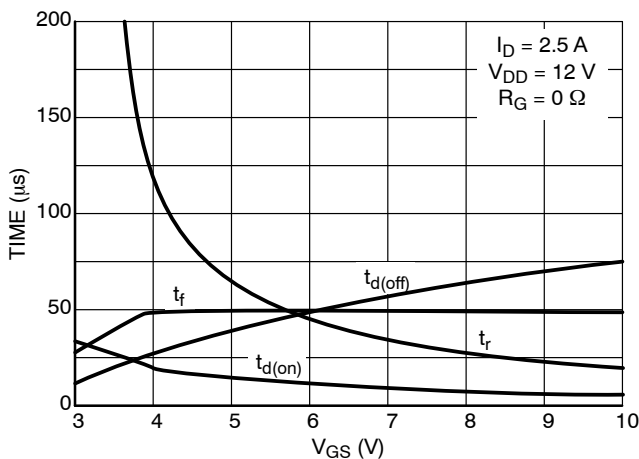


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

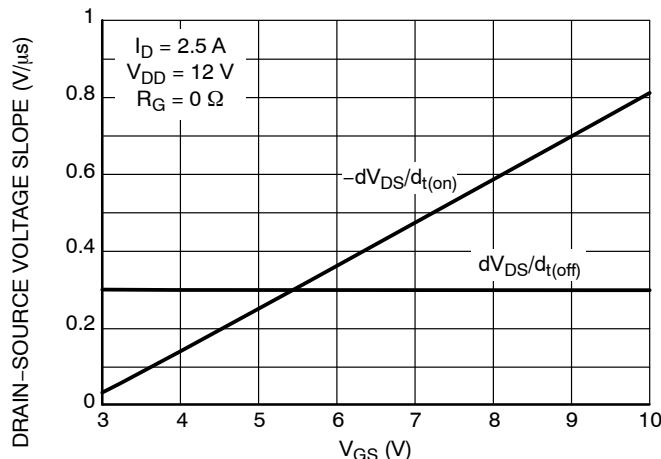


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

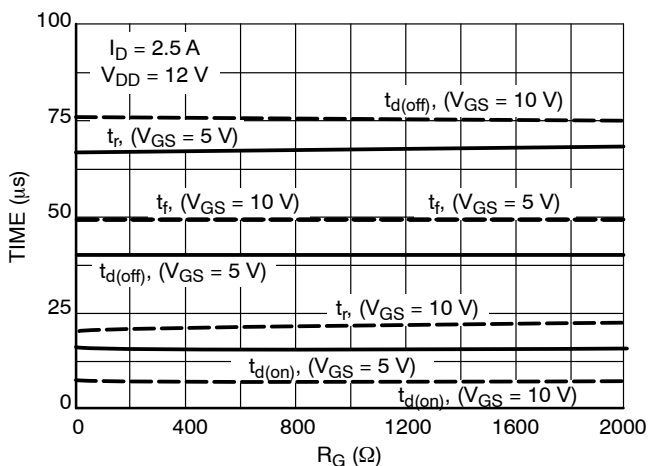


Figure 18. Resistive Load Switching Time vs. Gate Resistance

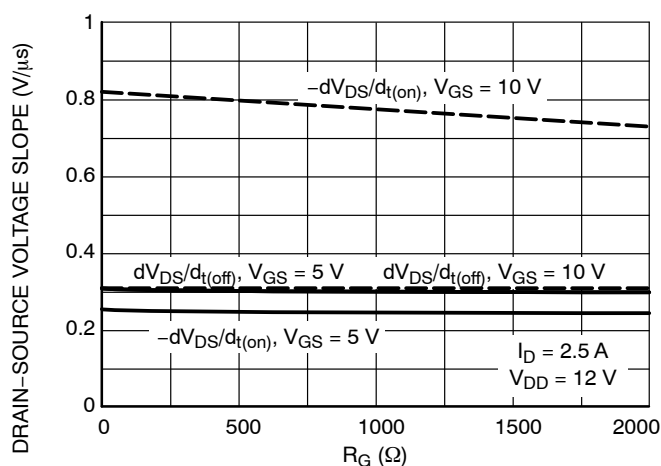


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

# NCV8402, NCV8402A

## TYPICAL PERFORMANCE CURVES

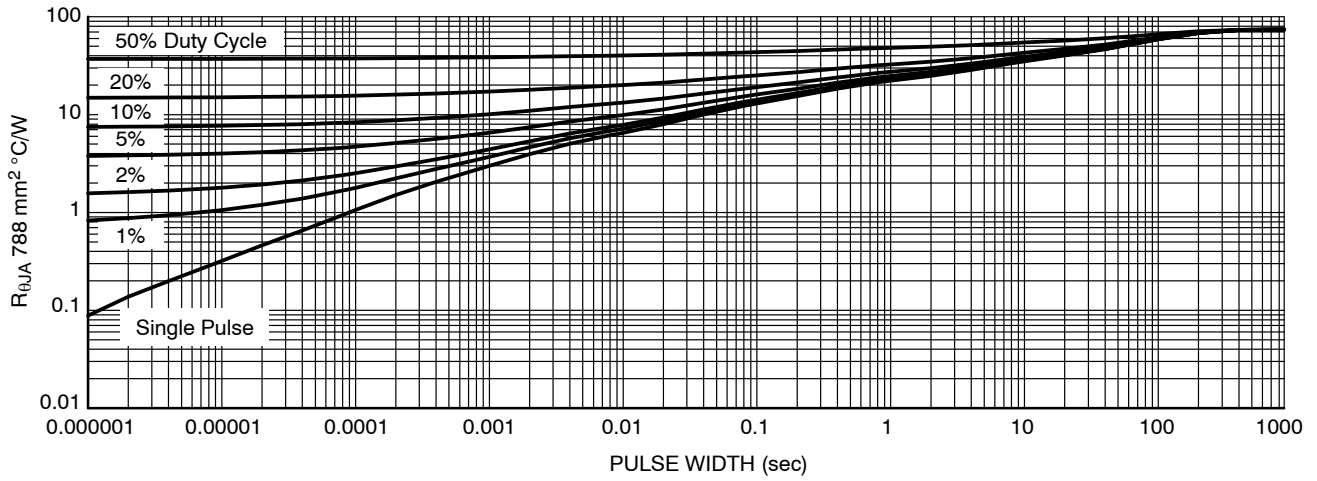


Figure 20. Transient Thermal Resistance – SOT-223 Package

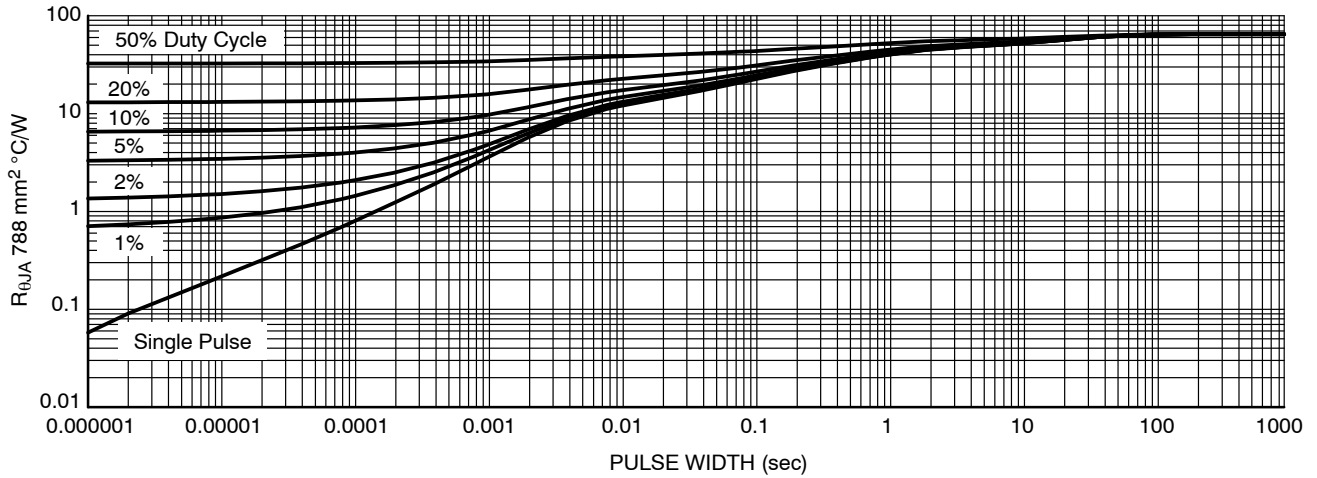


Figure 21. Transient Thermal Resistance – DFN Package

# NCV8402, NCV8402A

## TEST CIRCUITS AND WAVEFORMS

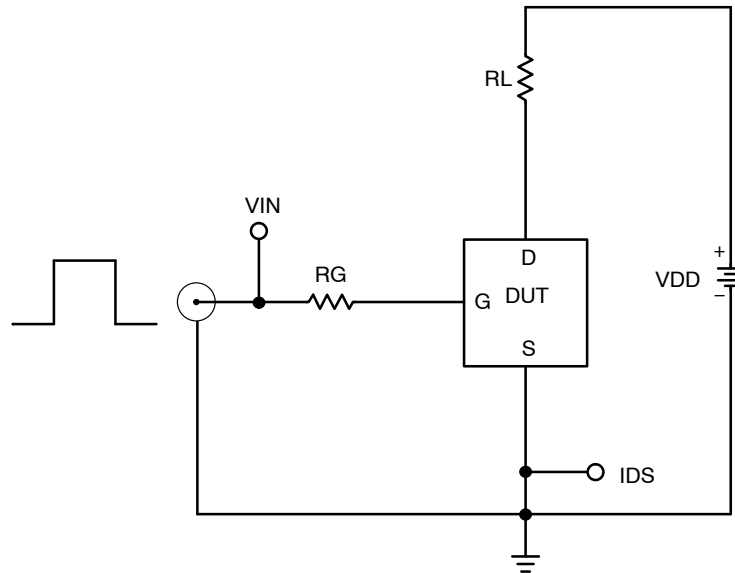


Figure 22. Resistive Load Switching Test Circuit

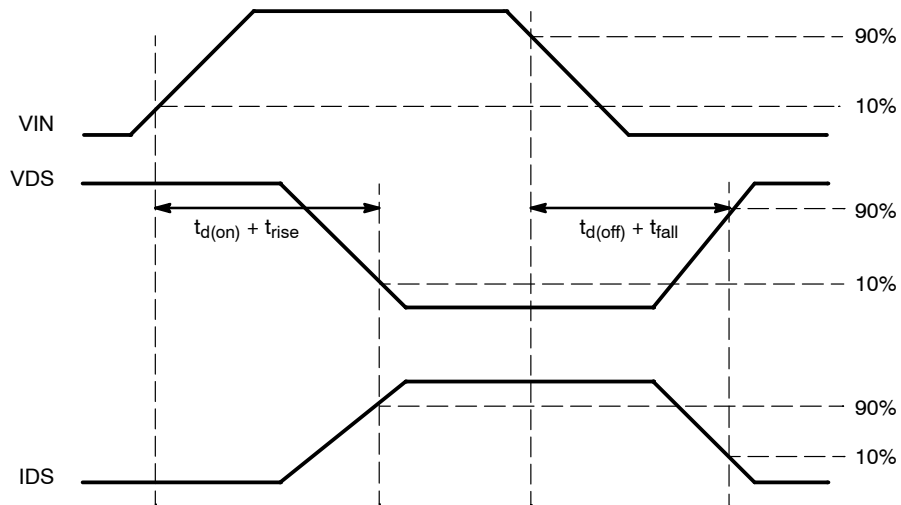


Figure 23. Resistive Load Switching Waveforms

# NCV8402, NCV8402A

## TEST CIRCUITS AND WAVEFORMS

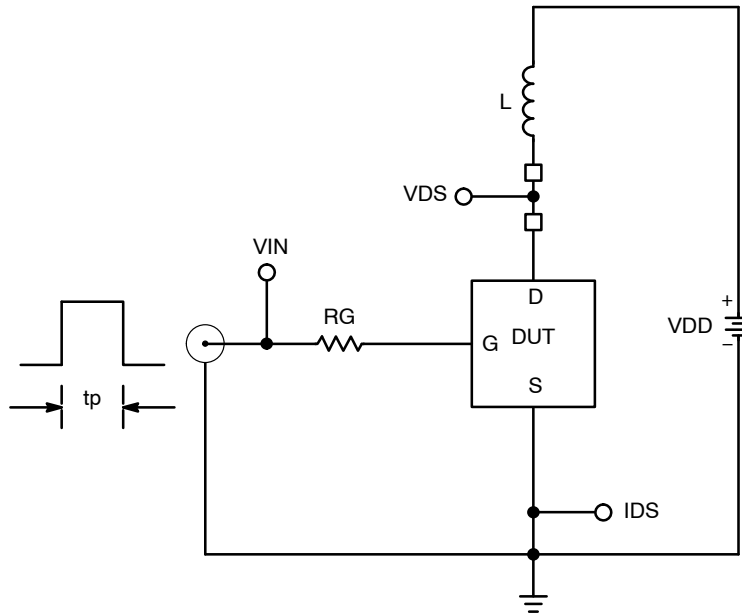


Figure 24. Inductive Load Switching Test Circuit

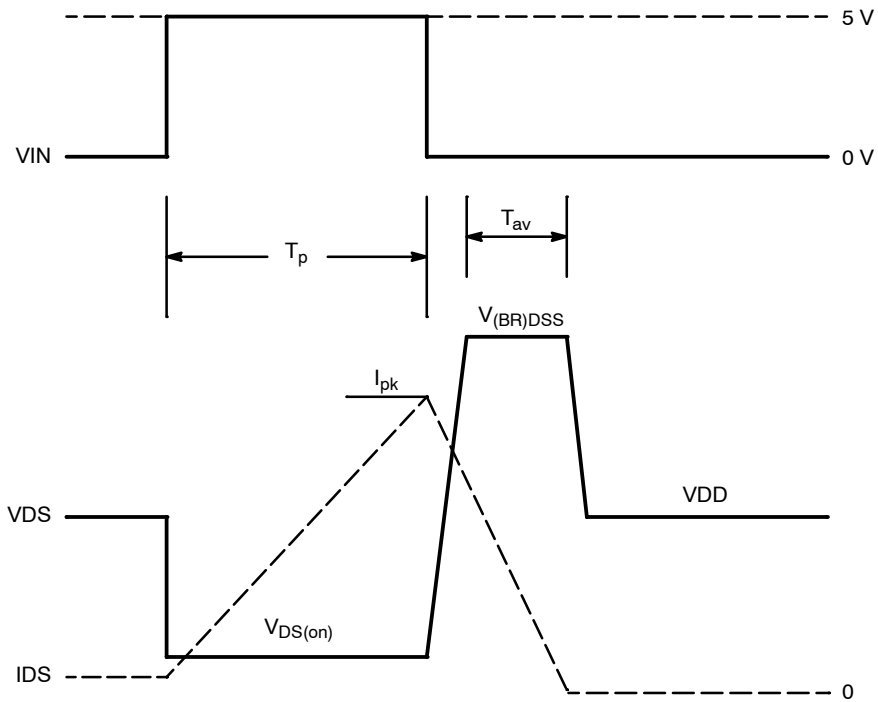


Figure 25. Inductive Load Switching Waveforms

## NCV8402, NCV8402A

### ORDERING INFORMATION

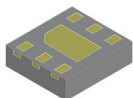
Device*	Package	Shipping†
NCV8402STT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NCV8402ASTT1G		
NCV8402STT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV8402ASTT3G		
NCV8402AMNT2G	DFN6 (Pb-Free)	2000 / Tape & Reel
NCV8402AMNWT1G	DFN6 (Pb-Free, Wettable Flank)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

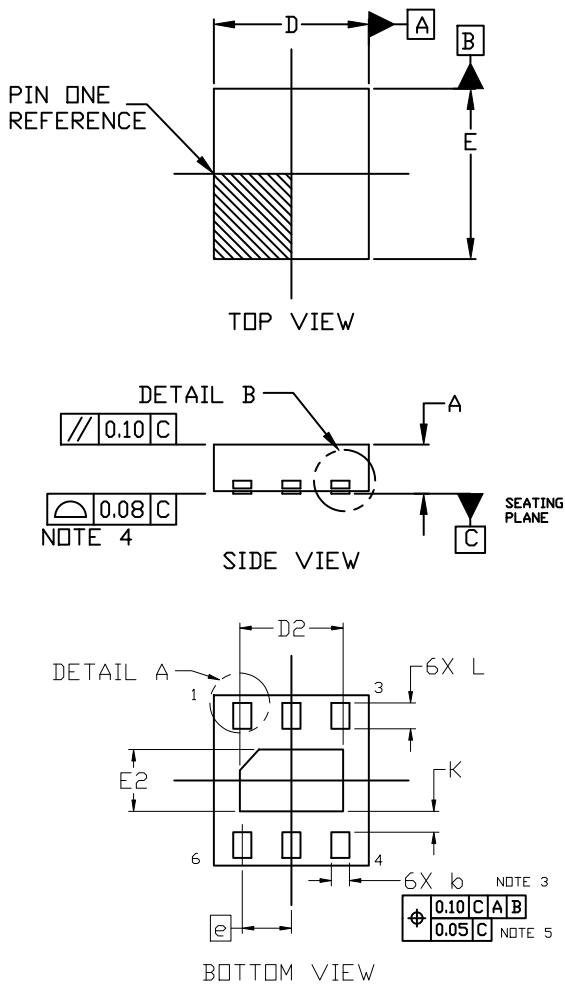
# NCV8402, NCV8402A

## PACKAGE DIMENSIONS



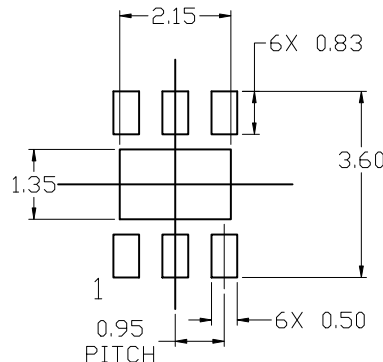
**DFN6 3.0x3.3, 0.95P**  
CASE 506AX  
ISSUE A

DATE 22 SEP 2020

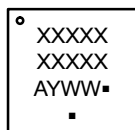


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. DIMENSION *b* APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
  5. POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
<i>b</i>	0.30	0.35	0.40
D	2.90	3.00	3.10
D2	1.90	2.00	2.10
E	3.20	3.30	3.40
E2	1.10	1.20	1.30
<i>e</i>	0.95 BSC		
K	0.40 REF		
L	0.40	0.50	0.60
L1	0.00	---	0.15



### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\* For additional information on our Pb-Free strategy and soldering details, please download the IN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/T.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

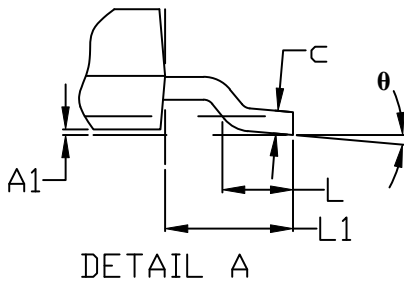
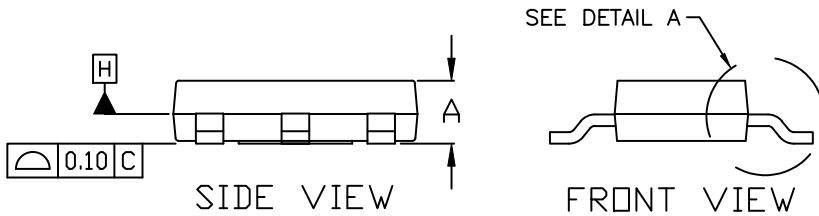
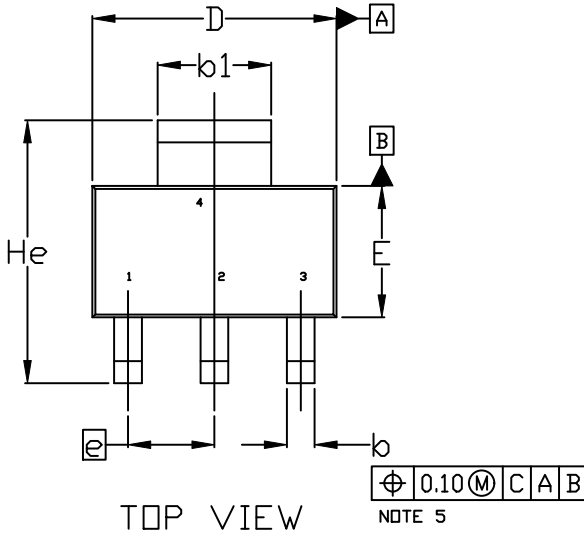
ON Semiconductor®



SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

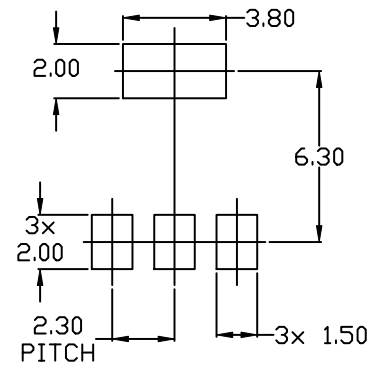
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
$\theta$	0°	---	10°



DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

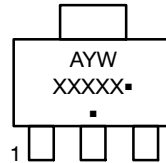
ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***




- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98ASB42680B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOT-223 (TO-261)</b>	<b>PAGE 2 OF 2</b>

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

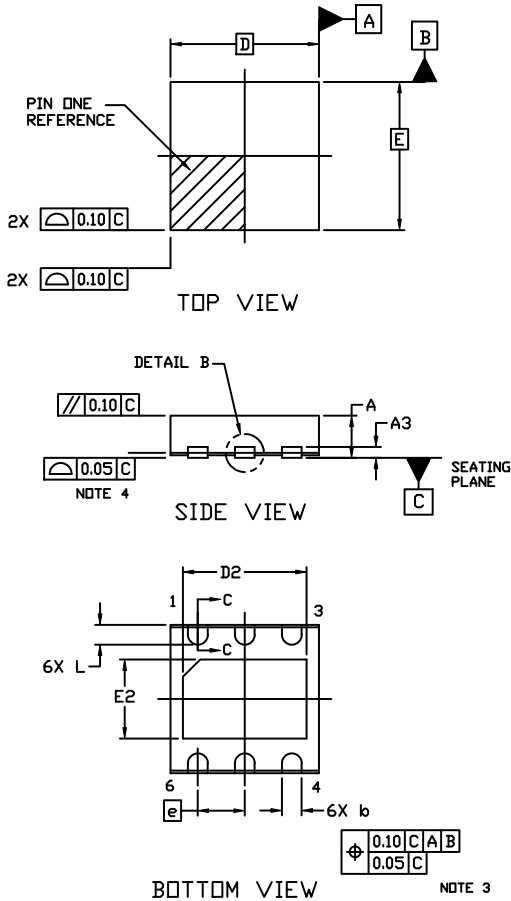
ON Semiconductor®



SCALE 2:1

DFNW6 3x3, 0.95P  
CASE 506DK  
ISSUE A

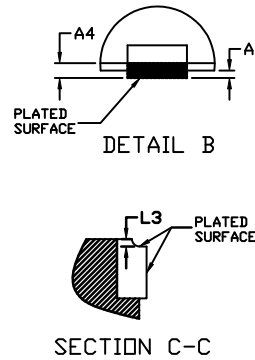
DATE 07 MAY 2021



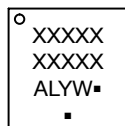
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
4. PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	MAX.	MAX.
A	0.75	0.85	0.95
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.35	0.40	0.45
D	3.00 BSC		
D2	2.40	2.50	2.60
E	3.00 BSC		
E2	1.50	1.60	1.70
e	0.95 BSC		
L	0.30	0.40	0.50
L3	0.00	0.05	0.10



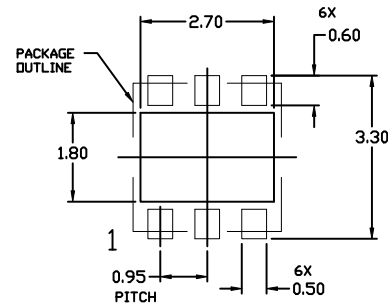
**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON12549G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DFNW6 3X3, 0.95P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View NCV8402ASTT3G on WIN SOURCE](#)
- ⊖ [ON Semiconductor Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management