



**THE DATASHEET OF
NCV8518PDR2G**



NCV8518

Low Dropout Linear Regulator with Watchdog, Wake Up, RESET, and ENABLE

The NCV8518 device is a precision micropower voltage regulator. It has a fixed output voltage of 5.0 V and regulates within $\pm 2\%$. It is suitable for use in all automotive environments and contains all the required functions to control a microprocessor. This device has low dropout voltage and low quiescent current. It includes a watchdog timer, adjustable reset, wake up and enable function. Also encompassed in this device are safety features such as thermal shutdown and short circuit protection. It is capable of handling up to 45 V transients.

Features

- Output Voltage of 5.0 V
- $\pm 2\%$ Output Voltage Tolerance
- Output Current up to 250 mA
- Micropower Compatible Control Functions:
 - ENABLE
 - Watchdog
 - RESET
 - Wake Up
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- Low Dropout Voltage
- Low Quiescent Current of 100 μA
- Protection Features:
 - Thermal Shutdown
 - Short Circuit
- Low Sleep Mode Current less than 1.0 μA
- AEC Qualified
- PPAP Capable
- These are Pb-Free Devices

Applications

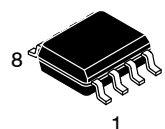
- Tire Pressure Monitor
- Battery Powered Consumer Electronics



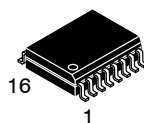
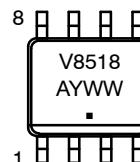
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<http://onsemi.com>

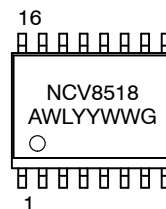
MARKING DIAGRAMS



SOIC-8
EXPOSED PAD
CASE 751AC



SOIC-16 LEAD
WIDE BODY
EXPOSED PAD
CASE 751AG



A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
▪, or G = Pb-Free Package

ORDERING INFORMATION

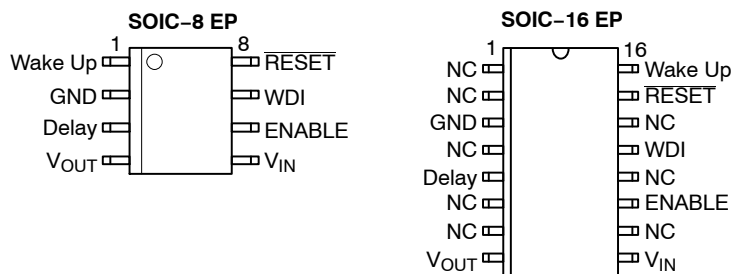
Device	Package	Shipping†
NCV8518PDG	SOIC-8*	98 Units / Rail
NCV8518PDR2G	SOIC-8*	2500 / Tape & Reel
NCV8518PWG	SOIC-16*	47 Units / Rail
NCV8518PWR2G	SOIC-16*	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*These packages are inherently Pb-Free.

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PIN CONNECTIONS



PIN FUNCTION DESCRIPTION

Pin		Symbol	Description
SOIC-8 EP	SOIC-16 E PAD		
4	8	V _{OUT}	Regulated output voltage.
5	9	V _{IN}	Input supply voltage.
7	13	WDI	CMOS compatible Watchdog input. The watchdog function monitors the falling edge of the incoming signal.
2	3	GND	Ground connection.
6	11	ENABLE	ENABLE control for the IC. Positive logic.
8	15	RESET	CMOS compatible output RESET goes low whenever V _{OUT} drops by more than 7.0% from nominal, or during the absence of a correct watchdog signal.
3	5	Delay	Buffered reference voltage used to create timing current for RESET and Watchdog threshold frequency from R _{Delay} .
-	1, 2, 4, 6, 7, 10, 12, 14	NC	No Connection.
1	16	Wake Up	Continuously generated signal that interrupts the microprocessor from sleep mode.
EPAD	EPAD	EPAD	Connect to Ground potential or leave unconnected.

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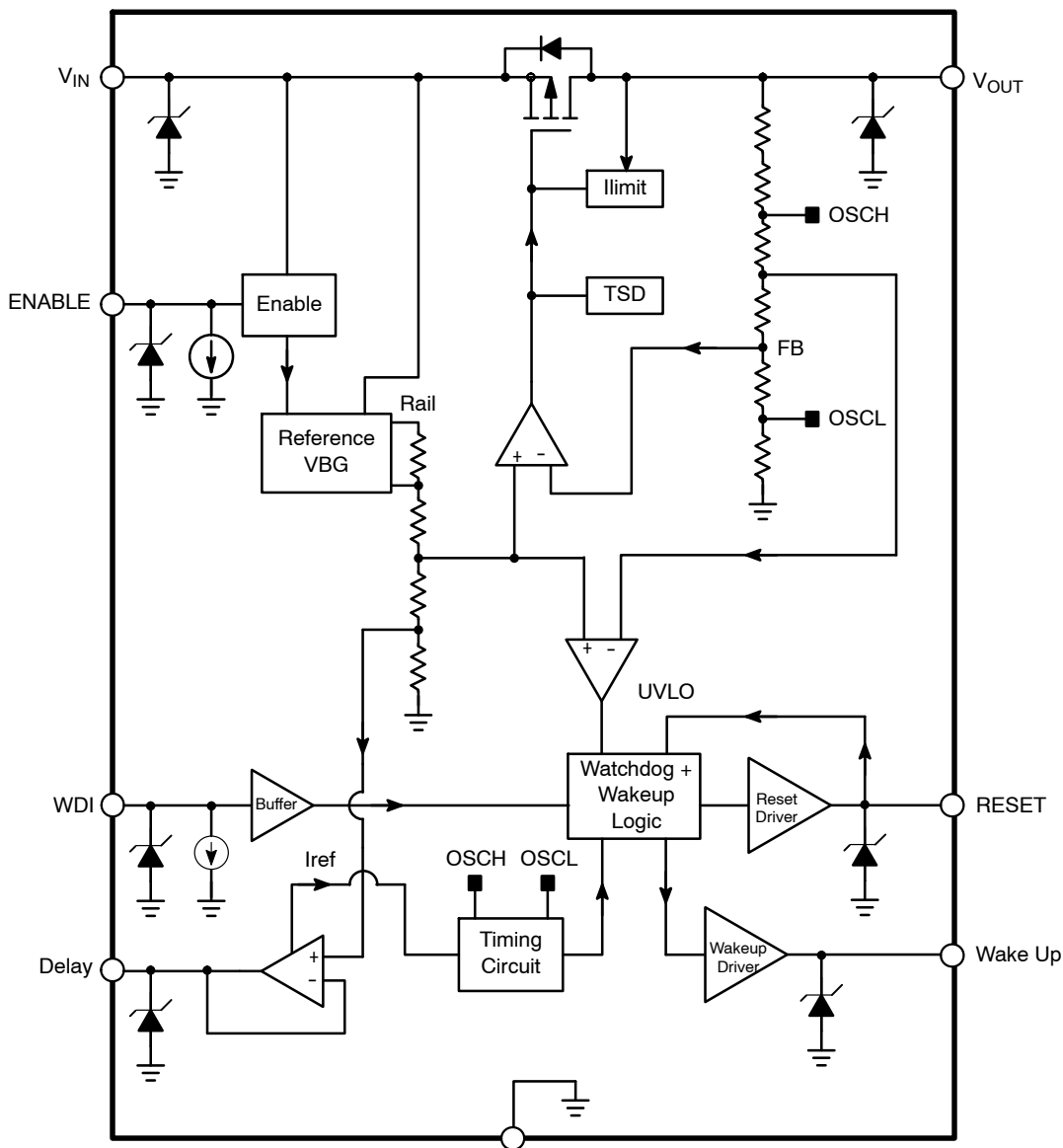


Figure 1. Block Diagram

NCV8518

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	$V_{IN, ENABLE}$	-0.3 to 45	V
Output Voltage	V_{OUT}	-0.3 to +7.0	V
RESET Voltage	V_{RESET}	0 V to V_{OUT}	V
RESET Current (RESET may be incidentally shorted either to V_{OUT} or to GND without damage)	I_{RESET}	Internally Limited	mA
ESD Susceptibility (Human Body Model)	-	2.0	kV
Logic Inputs/Outputs (Reset, WDI, Wake Up, Delay)	-	-0.3 to +7.0	V
Operating Junction Temperature	T_J	-40 to 150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Moisture Sensitivity Level SOIC-16 EP (Case 751R) SOIC-8 EP (Case 751AC)	MSL	1 2	
Lead Temperature Soldering: Reflow Leaded Part 60-150 sec above 183°C, 30 sec max at peak Lead-Free Part 60-150 sec above 217°C, 40 sec max at peak	- -	240 peak 265 peak	°C °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Board/Mounting Conditions Typical Value		Unit
SO-8 Exposed Pad Package			
	100 sq. mm spreader board (Note 1)	1 sq. inch spreader board (Note 2)	
Junction to case top (Ψ_{JT})	14	14	°C/W
Junction to lead1 (Ψ_{JL1})	36	26	°C/W
Junction to board (Ψ_{JB}) (Note 3)	15	14	°C/W
Junction to ambient (θ_{JA})	126	80	°C/W
SO-16 Exposed Pad Package			
	100 sq. mm spreader board (Note 1)	1 sq. inch spreader board (Note 2)	
Junction to case top (Ψ_{JT})	20	20	°C/W
Junction to lead1 (Ψ_{JL1})	41	26	°C/W
Junction to board (Ψ_{JB}) (Note 3)	12	12	°C/W
Junction to ambient (θ_{JA})	113	70	°C/W

Specific notes on thermal characterization conditions:

All boards are 0.062" thick FR4, 3" square, with varying amounts of copper heat spreader, in still air (free convection) conditions. Numerical values are derived from an axisymmetric finite-element model where active die area, total die area, flag area, pad area, and board area are equated to the actual corresponding areas.


- 1 oz copper, 100 mm² (0.155 in²) spreader area (includes exposed pad).
- 1 oz copper, 645 mm² (1 in²) spreader area (includes exposed pad).
- "board" is defined as center of exposed pad soldered to board; this is the recommended number to be used for thermal calculations, as it best represents the primary heat flow path and is least sensitive to board and ambient properties.

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
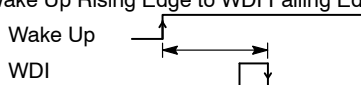
ELECTRICAL CHARACTERISTICS ($-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$; $6.0\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$, $100\ \mu\text{A} \leq I_{\text{OUT}} \leq 150\text{ mA}$, $C_2 = 1.0\ \mu\text{F}$, $R_{\text{Delay}} = 60\text{ k}$; unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output					
Output Voltage	V_{OUT}	4.9 -2%	5.00	5.10 +2%	V
Dropout Voltage ($V_{\text{IN}} - V_{\text{OUT}}$, $I_{\text{OUT}} = 150\text{ mA}$) (Note 4)	V_{DO}	-	425	750	mV
Load Regulation ($V_{\text{IN}} = 13.5\text{ V}$, $100\ \mu\text{A} \leq I_{\text{OUT}} \leq 150\text{ mA}$)	Reg_{load}	-	5.0	30	mV
Line Regulation ($6.0\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$, $I_{\text{OUT}} = 5.0\text{ mA}$)	Reg_{line}	-	5.0	20	mV
Current Limit	I_{lim}	255	400	-	mA
Thermal Shutdown (Guaranteed by Design)	T_{Jmax}	150	180	210	$^{\circ}\text{C}$
Quiescent Current ($V_{\text{IN}} = 13.5\text{ V}$, $I_{\text{OUT}} = 100\ \mu\text{A}$, 150 mA , $\text{ENABLE} = 2.0\text{ V}$) ($\text{ENABLE} = 0\text{ V}$)	I_{Q}	- -	100 -	150 1.0	μA

RESET

Threshold Voltage 	-	4.50	4.65	4.75	V
Output Low ($R_{\text{LOAD}} = 10\text{ k}$ to V_{OUT} , $V_{\text{OUT}} = 1.0\text{ V}$)	-	-	0.2	0.4	V
Output High ($R_{\text{LOAD}} = 10\text{ k}$ to GND)	-	$V_{\text{OUT}} - 0.4$	$V_{\text{OUT}} - 0.2$	-	V
Power On Reset Delay Time ($V_{\text{IN}} = 13.5\text{ V}$, $R_{\text{Delay}} = 60\text{ k}$, $I_{\text{OUT}} = 5.0\text{ mA}$) ($V_{\text{IN}} = 13.5\text{ V}$, $R_{\text{Delay}} = 120\text{ k}$, $I_{\text{OUT}} = 5.0\text{ mA}$) ($V_{\text{IN}} = 13.5\text{ V}$, $R_{\text{Delay}} = 500\text{ k}$, $I_{\text{OUT}} = 5.0\text{ mA}$)	t_{D}	2.0 - -	3.0 6.0 25	4.0 - -	ms

Watchdog Input

Threshold	WDI_{high}	30	50	70	$\%V_{\text{OUT}}$
Hysteresis 	WDI_{hys}	25	100	-	mV
Input Current ($\text{WDI} = 6.0\text{ V}$)	-	-	0.1	2.0	μA
Wake Up Rising Edge to WDI Falling Edge Delay 	-	5.0	-	-	μs

ENABLE (Note 5)

Input Threshold Logic Low Logic High	$V_{\text{th(EN)}}$	- 2.0	- -	0.8 -	V
Input Current ($\text{ENABLE} = 2.0\text{ V}$)	-	-	3.0	10	μA

4. Measured when the output voltage has dropped 2% from the nominal value.
5. If ENABLE is connected to V_{IN} , a $20\text{ k}\Omega$ resistor must be placed in series.

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ELECTRICAL CHARACTERISTICS (continued) ($-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$; $6.0\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$, $100\ \mu\text{A} \leq I_{\text{OUT}} \leq 150\text{ mA}$, $C_2 = 1.0\ \mu\text{F}$, $R_{\text{Delay}} = 60\text{ k}$; unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Wake Up Output ($V_{\text{IN}} = 14\text{ V}$, $I_{\text{OUT}} = 5.0\text{ mA}$)					
Wake Up Period ($R_{\text{DELAY}} = 60\text{ k}$) ($R_{\text{DELAY}} = 120\text{ k}$) ($R_{\text{DELAY}} = 500\text{ k}$)	-	18 - -	25 50 208	32 - -	ms
Wake Up Duty Cycle Nominal	-	45	50	55	%
RESET HIGH to Wake Up Rising Delay Time ($R_{\text{DELAY}} = 60\text{ k}$) 50% RESET Rising Edge to 50% Wake Up Edge ($R_{\text{DELAY}} = 120\text{ k}$) ($R_{\text{DELAY}} = 500\text{ k}$)	-	9.0 - -	12.5 25 104	16 - -	ms
Wake Up Response to Watchdog Input 50% WDI Falling Edge to 50% Wake Up Falling Edge	-	-	0.1	5.0	μs
Wake Up Response to RESET 50% RESET Falling Edge to 50% Wake Up Falling Edge ($V_{\text{OUT}} = 5.0\text{ V} \rightarrow 4.5\text{ V}$)	-	-	0.1	5.0	μs
Output Low ($R_{\text{LOAD}} = 10\text{ k}$)	-	-	0.2	0.4	V
Output High ($R_{\text{LOAD}} = 10\text{ k}$)	-	$V_{\text{OUT}} - 0.5$	$V_{\text{OUT}} - 0.25$	-	V
Delay					
Output Voltage ($R_{\text{DELAY}} = 60\text{ k}, 120\text{ k}, 500\text{ k}$)	-	-	0.48	-	V

DEFINITION OF TERMS

Dropout Voltage: The input-to-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current with no load.

Current Limit: Peak current that can be delivered to the output.

TIMING DIAGRAMS

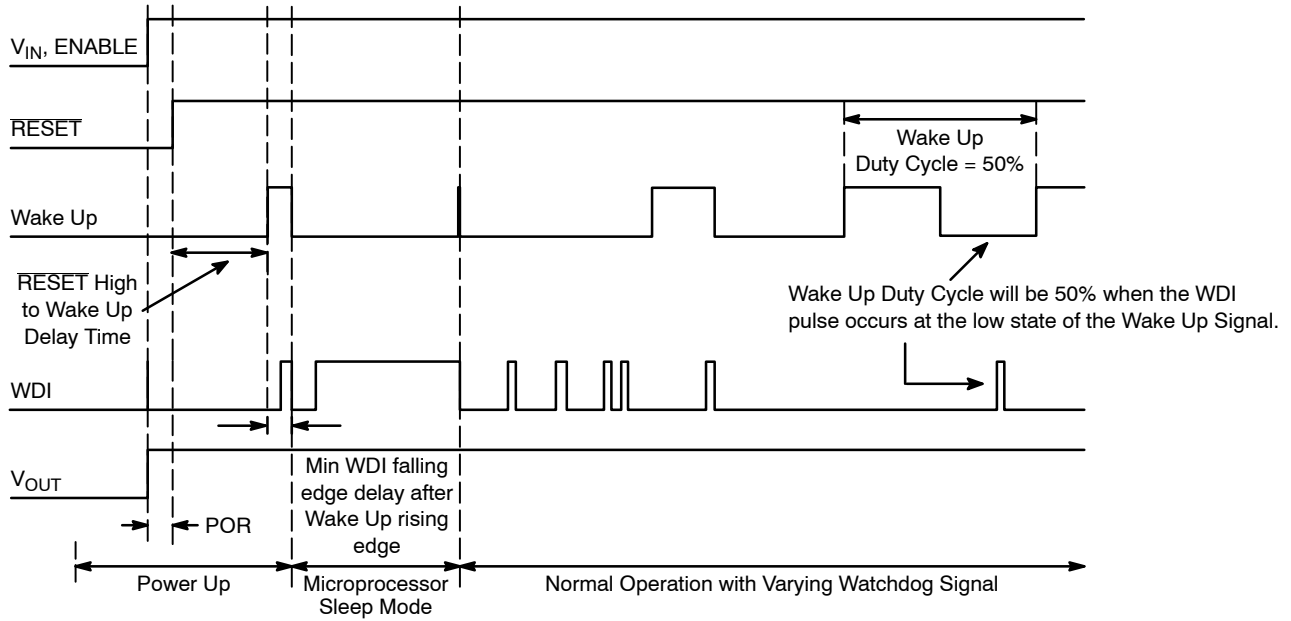


Figure 2. Power Up, Sleep Mode and Normal Operation

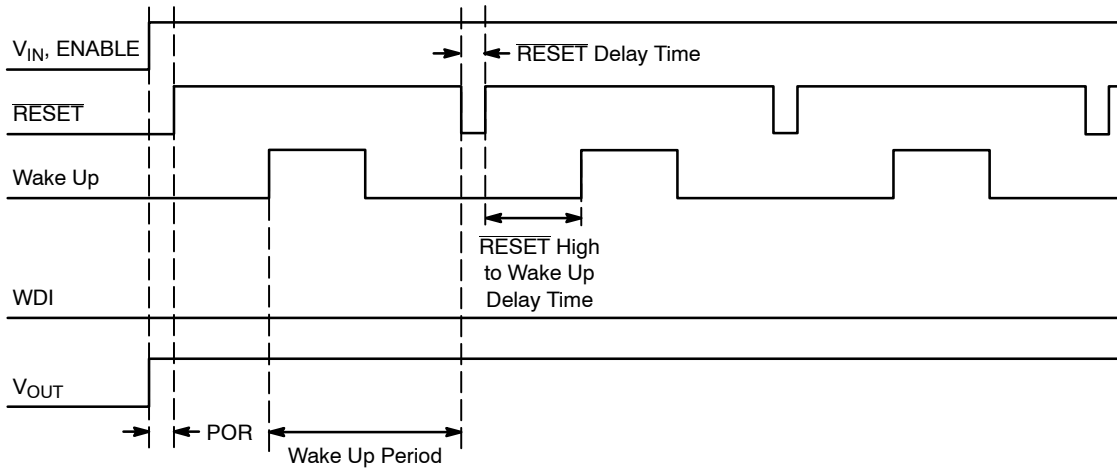


Figure 3. Error Condition: Watchdog Remains Low and a \overline{RESET} is Issued

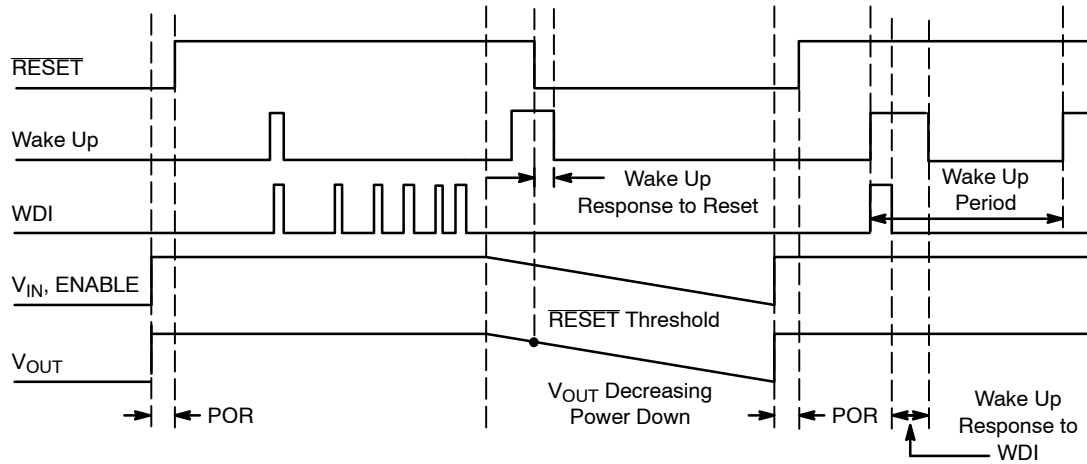


Figure 4. Power Down, Restart Sequence, and Wake Up Response to WDI

TYPICAL PERFORMANCE CHARACTERISTICS

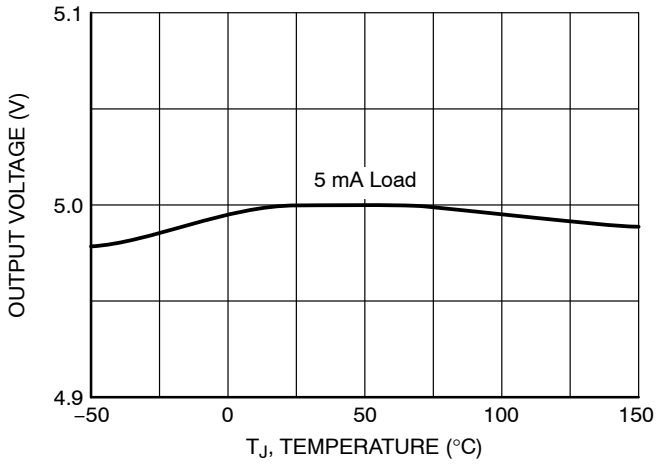


Figure 5. Output Voltage vs. Temperature

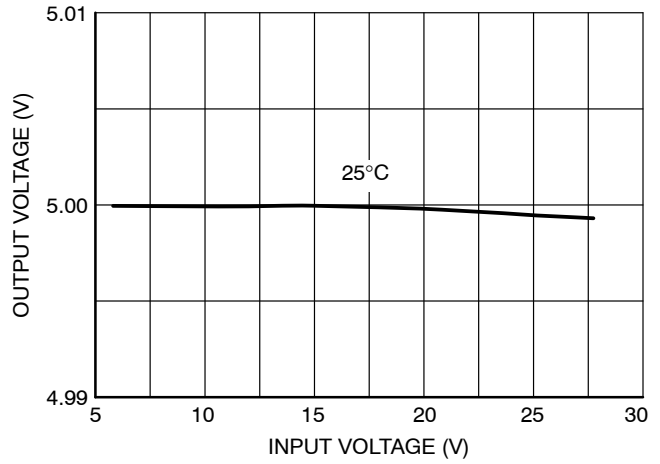


Figure 6. Output Voltage vs. Input Voltage

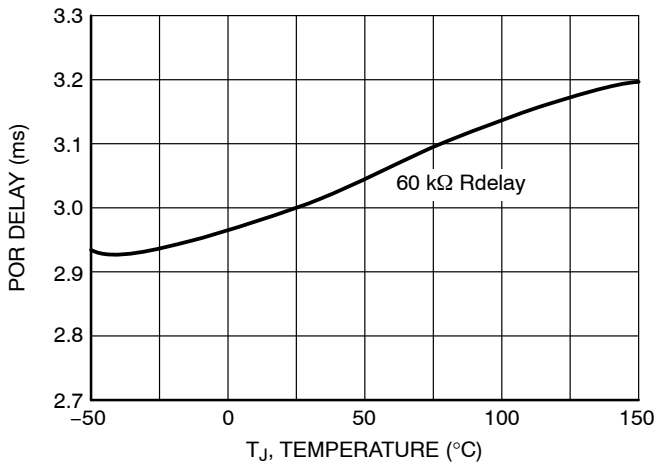


Figure 7. POR Delay vs. Temperature, 60 kΩ Rdelay

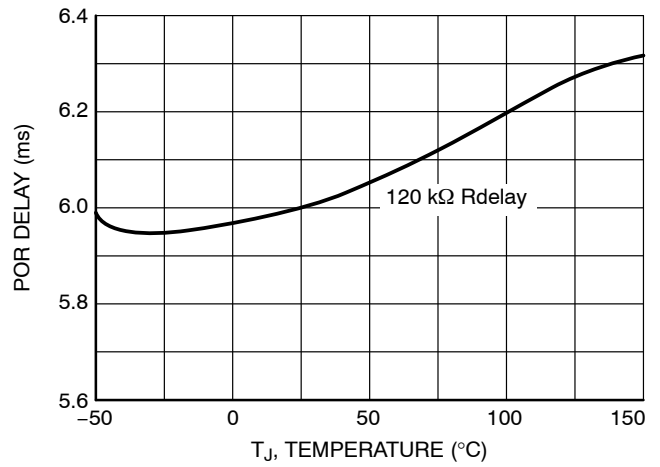


Figure 8. POR Delay vs. Temperature, 120 kΩ Rdelay

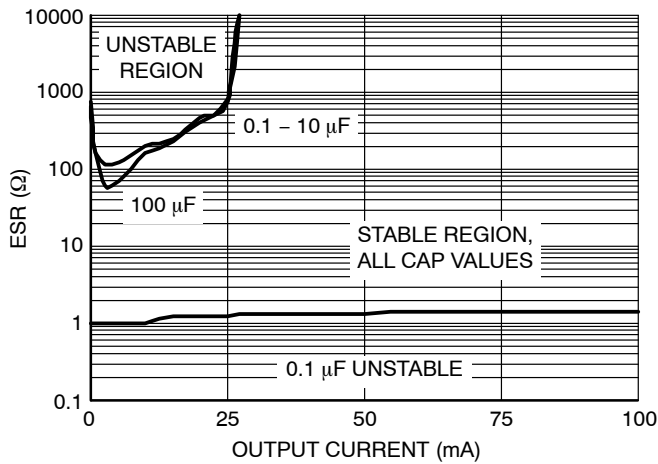


Figure 9. Stability Region of Capacitive ESR vs. Output Current

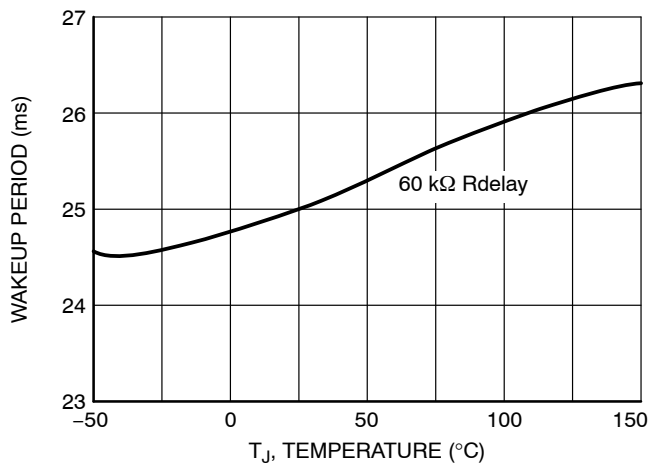


Figure 10. Wakeup Period vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

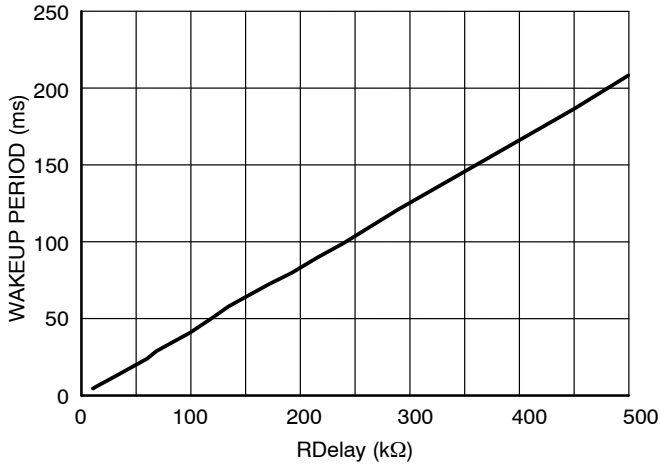


Figure 11. Wakeup Period vs. RDelay

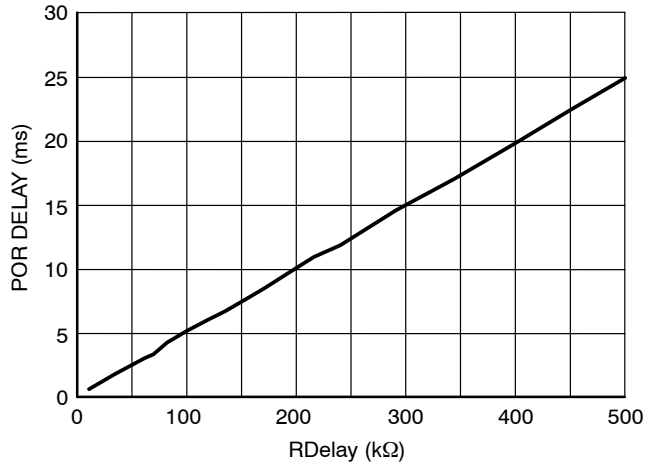


Figure 12. POR Delay vs. RDelay

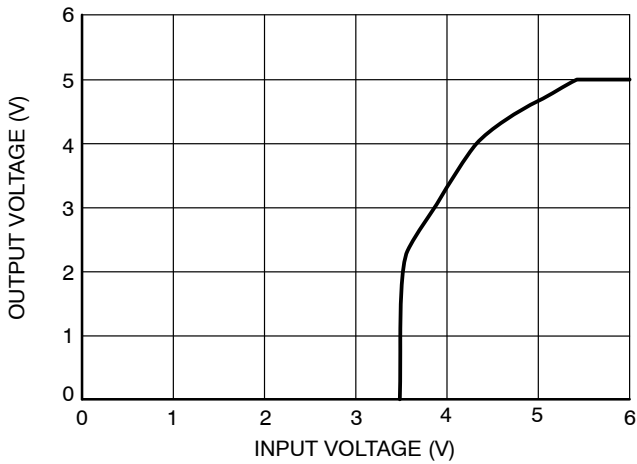


Figure 13. Output Voltage vs. Input Voltage, 5 mA Load

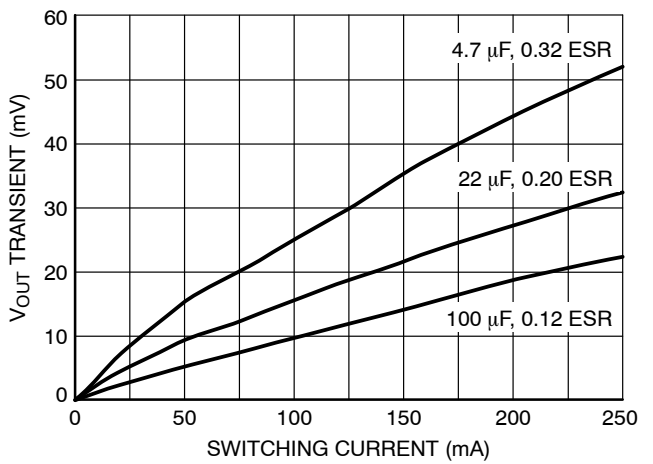


Figure 14. Load Transient Response

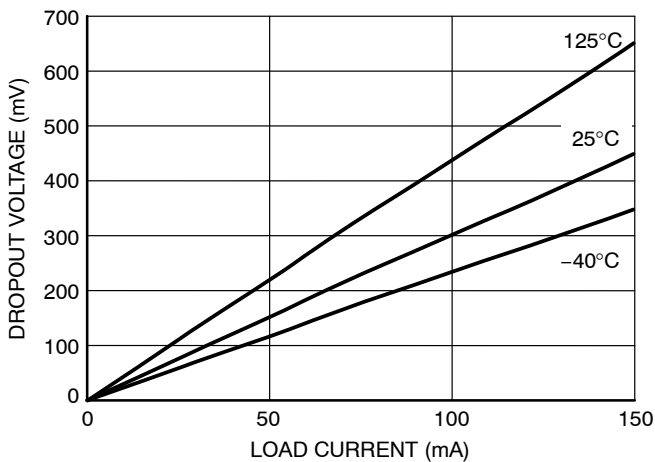


Figure 15. Dropout Voltage vs. Output Current

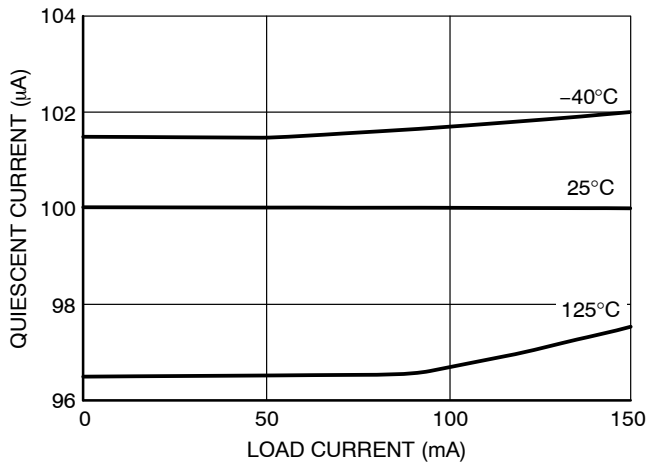
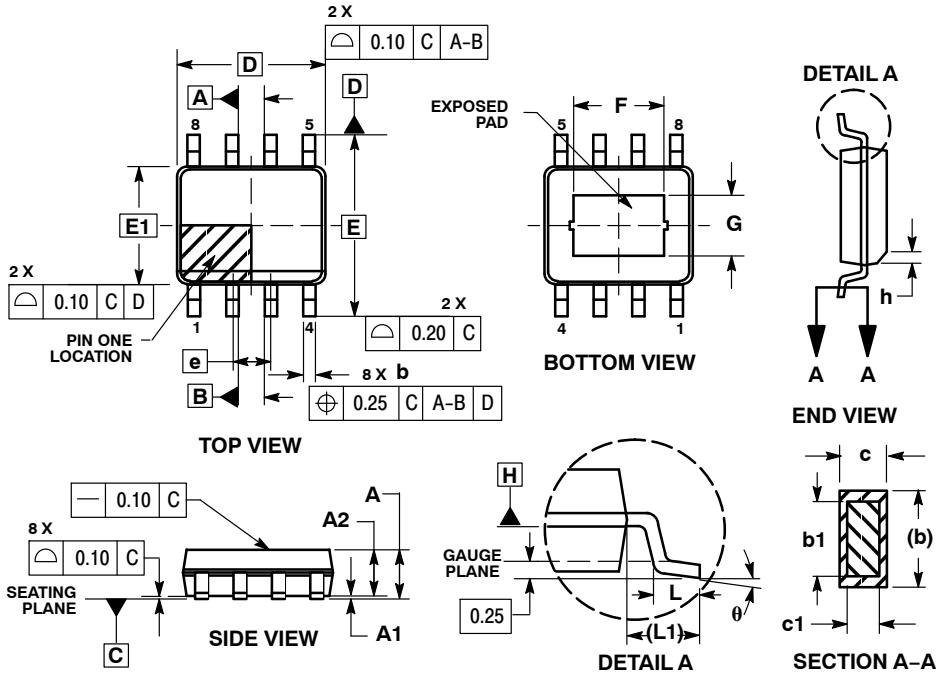


Figure 16. Quiescent Current vs. Output Current

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PACKAGE DIMENSIONS

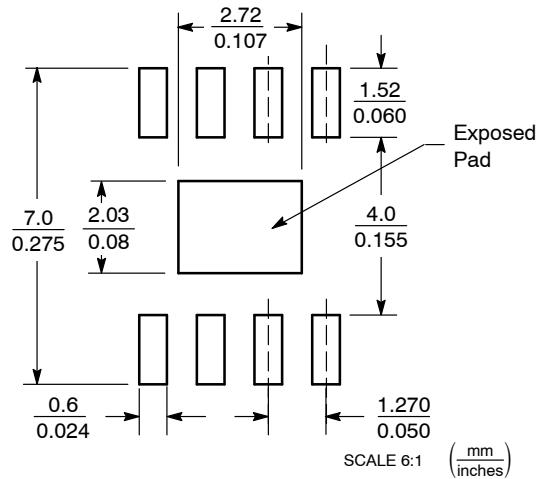
SOIC-8 EP
D SUFFIX
CASE 751AC-01
ISSUE B



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
 4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

MILLIMETERS		
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0°	8°

SOLDERING FOOTPRINT*

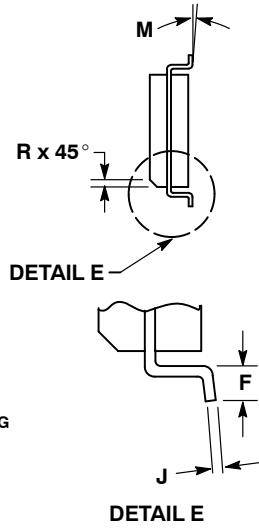
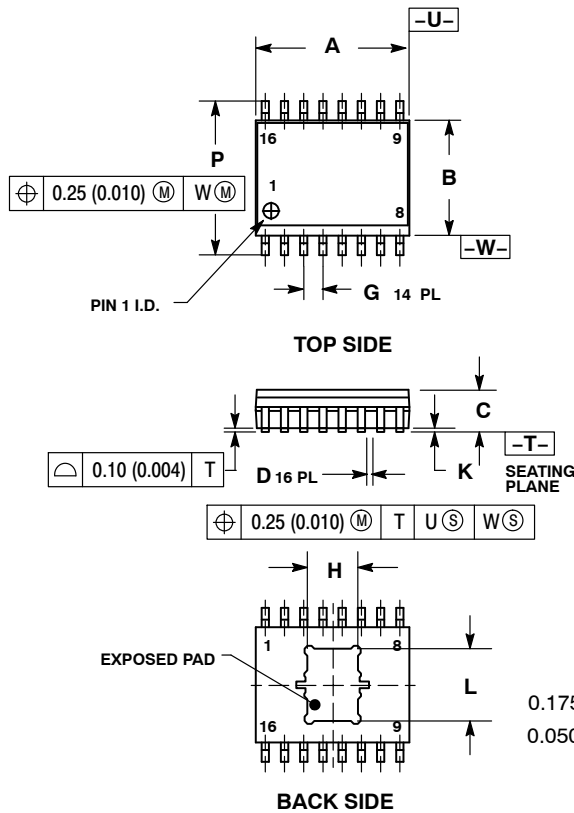


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCV8518

PACKAGE DIMENSIONS

SOIC-16 LEAD WIDE BODY, EXPOSED PAD PDW SUFFIX CASE 751AG-01 ISSUE A

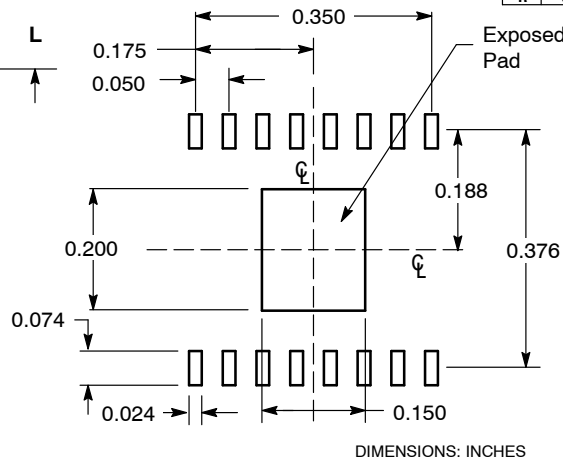


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R-01 OBSOLETE, NEW STANDARD 751R-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.45	3.66	0.136	0.144
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.72	4.93	0.186	0.194
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management