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## NDT014

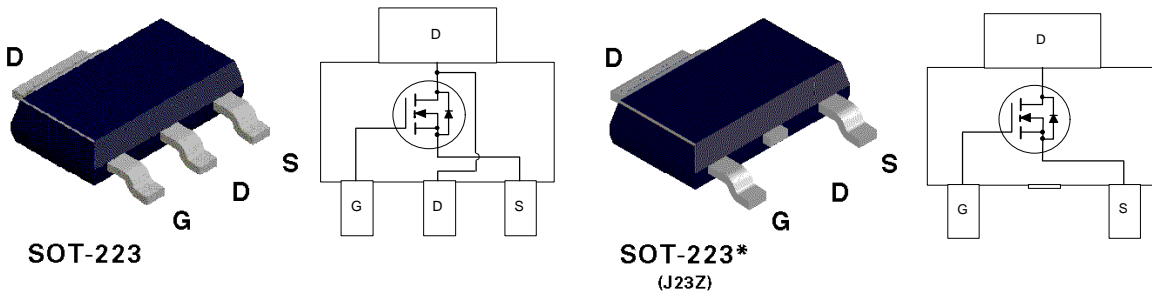
### N-Channel Enhancement Mode Field Effect Transistor

#### General Description

Power SOT N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

#### Features

- 2.7A, 60V.  $R_{DS(ON)} = 0.2\Omega @ V_{GS} = 10V$ .
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.



#### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDT014	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	$\pm 2.7$	A
	- Pulsed	$\pm 10$	
$P_D$	Maximum Power Dissipation (Note 1a)	3	W
		1.3 (Note 1b)	
		1.1 (Note 1c)	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

\* Order option J23Z for cropped center drain lead.

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			25	$\mu\text{A}$
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			250	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.6\text{ A}$		0.18	0.2	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 1.6\text{ A}$		2		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		155		pF
$C_{oss}$	Output Capacitance			60		pF
$C_{rss}$	Reverse Transfer Capacitance			15		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 30\text{ V}, I_D = 10\text{ A},$ $V_{GEN} = 10\text{ V}, R_{GEN} = 24\ \Omega$		10	20	ns
$t_r$	Turn - On Rise Time			64	100	ns
$t_{D(off)}$	Turn - Off Delay Time			10	20	ns
$t_f$	Turn - Off Fall Time			10	20	ns
$Q_g$	Total Gate Charge	$V_{DS} = 48\text{ V},$ $I_D = 10\text{ A}, V_{GS} = 10\text{ V}$		5	11	nC
$Q_{gs}$	Gate-Source Charge			1.2	3.1	nC
$Q_{gd}$	Gate-Drain Charge			2	5.8	nC

### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				2.7	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current				22	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.7\text{ A}$ (Note 2)		0.95	1.6	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}$ , $I_F = 10\text{ A}$ , $di_F/dt = 100\text{ A}/\mu\text{s}$			140	ns

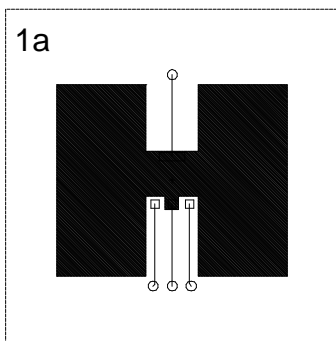
Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

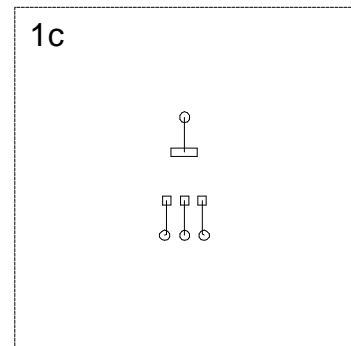
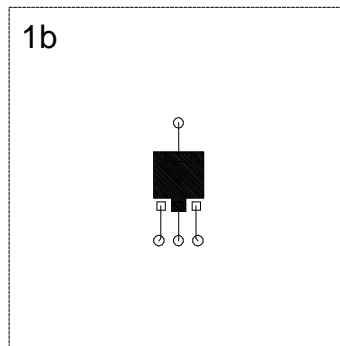
$$P_D(t) = \frac{T_J - T_A}{R_{\theta J A}(t)} = \frac{T_J - T_A}{R_{\theta J C} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical  $R_{\theta JA}$  using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 42°C/W when mounted on a 1 in<sup>2</sup> pad of 2oz copper.
- 95°C/W when mounted on a 0.066 in<sup>2</sup> pad of 2oz copper.
- 110°C/W when mounted on a 0.0123 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper



- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

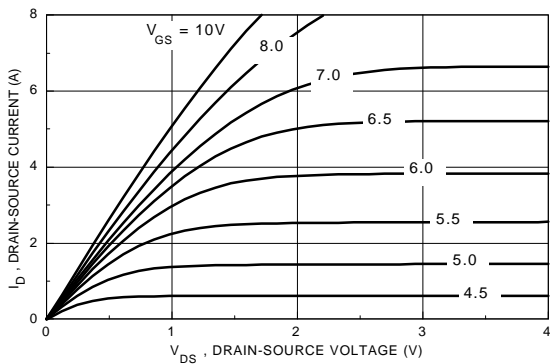


Figure 1. On-Region Characteristics.

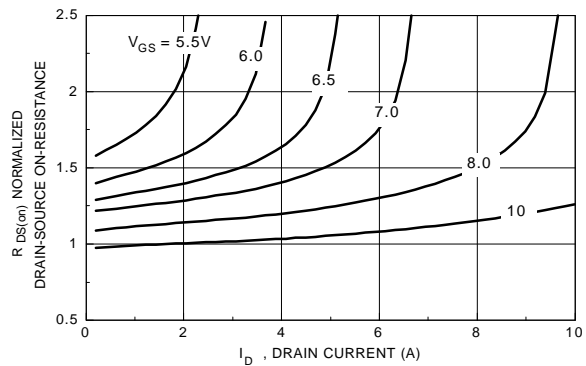


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

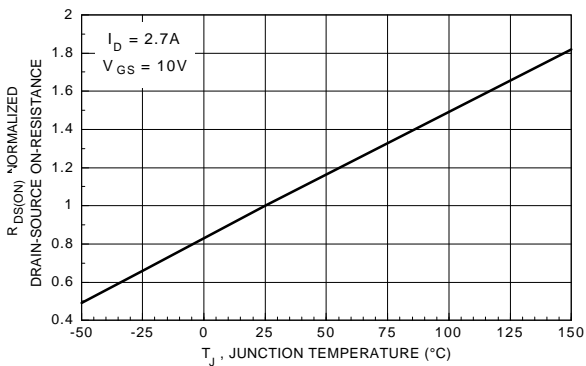


Figure 3. On-Resistance Variation with Temperature.

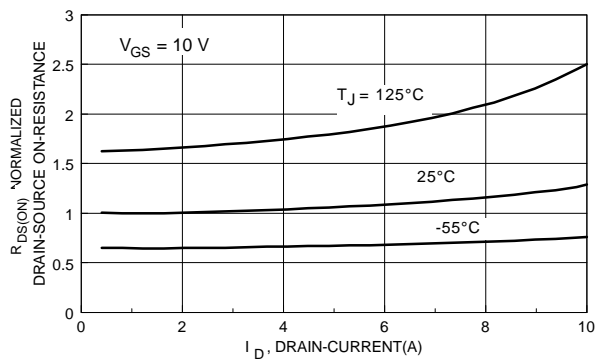


Figure 4. On-Resistance Variation with Drain Current and Temperature.

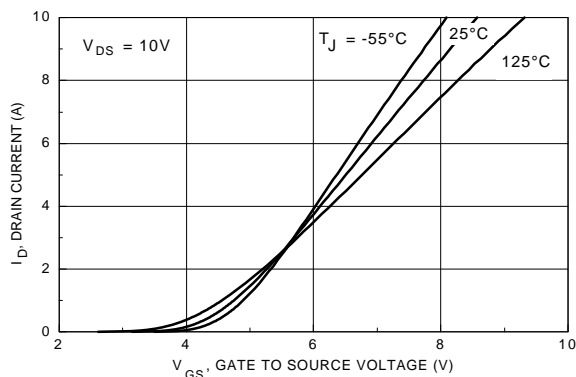


Figure 5. Transfer Characteristics.

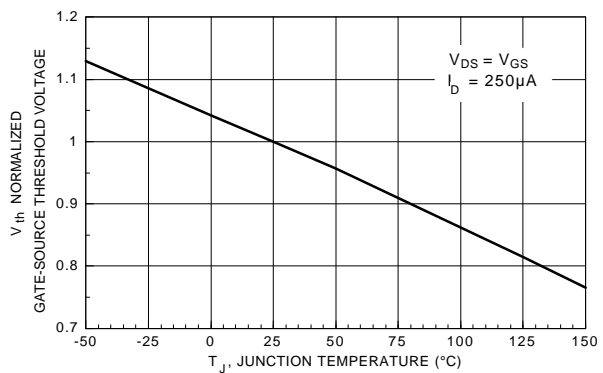


Figure 6. Gate Threshold Variation with Temperature.

## Typical Electrical Characteristics (continued)

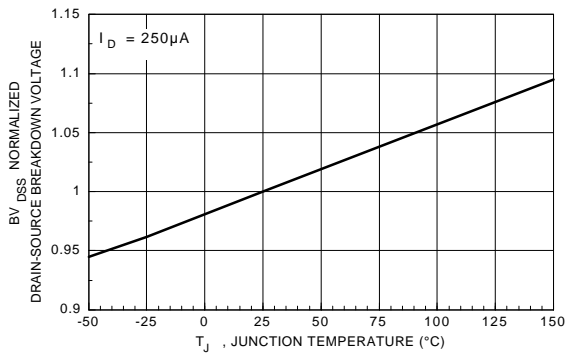


Figure 7. Breakdown Voltage Variation with Temperature.

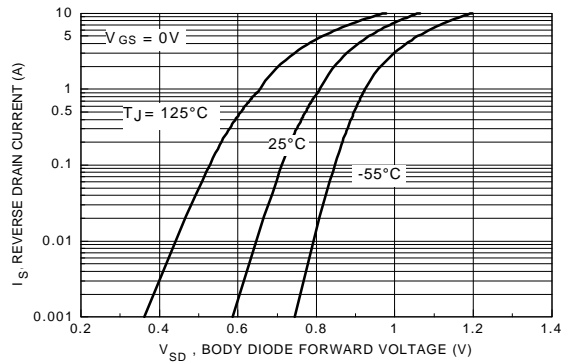


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

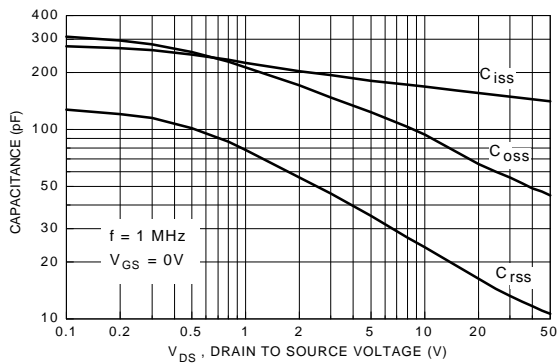


Figure 9. Capacitance Characteristics.

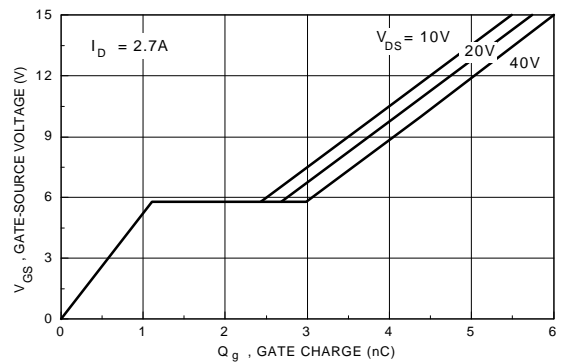


Figure 10. Gate Charge Characteristics.

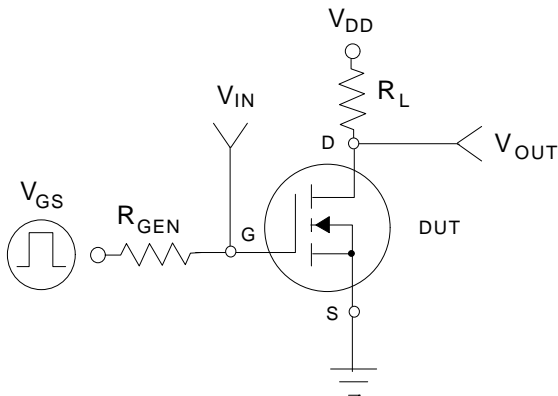


Figure 11. Switching Test Circuit.

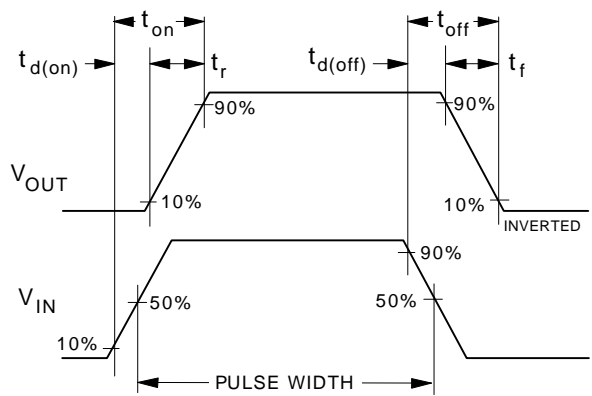


Figure 12. Switching Waveforms.

### Typical Electrical Characteristics (continued)

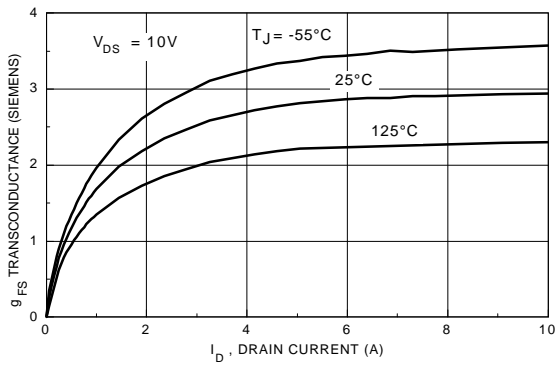


Figure 13. Transconductance Variation with Drain Current and Temperature.

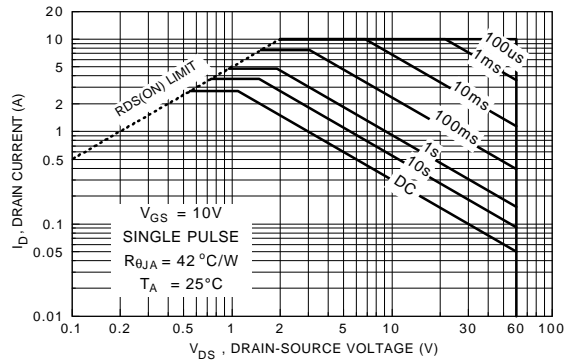


Figure 14. Maximum Safe Operating Area.

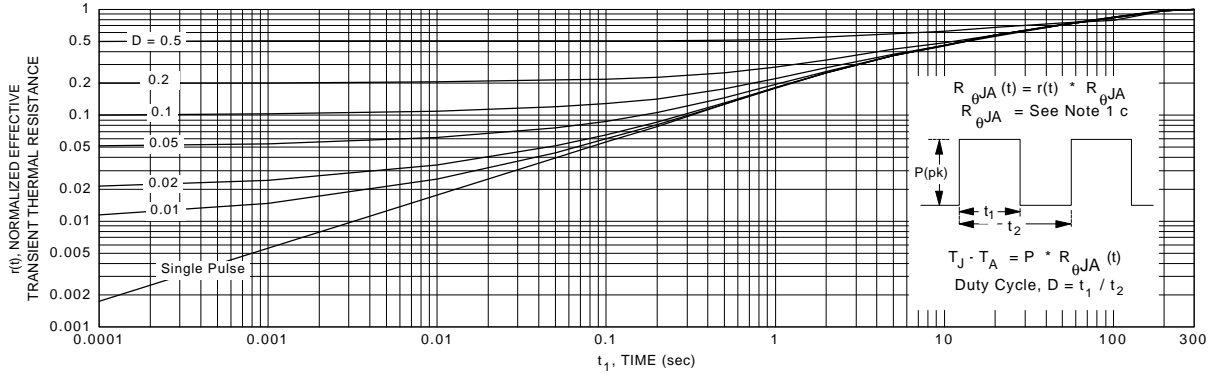
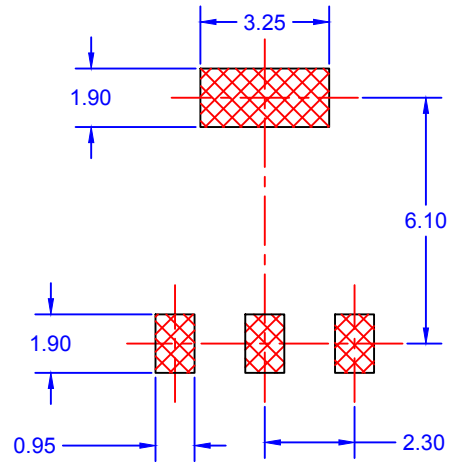
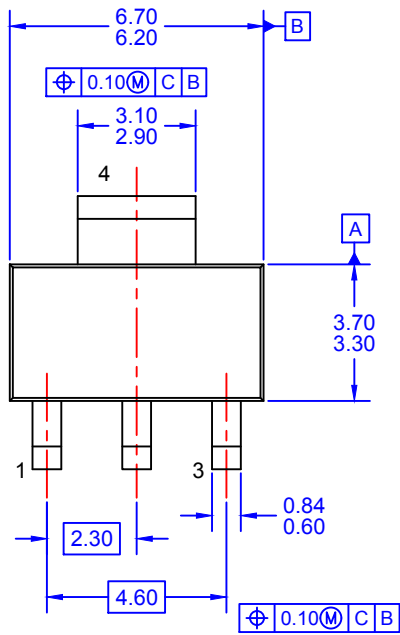
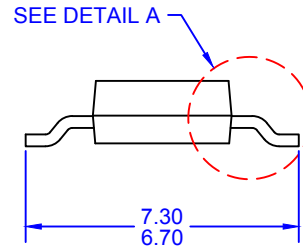
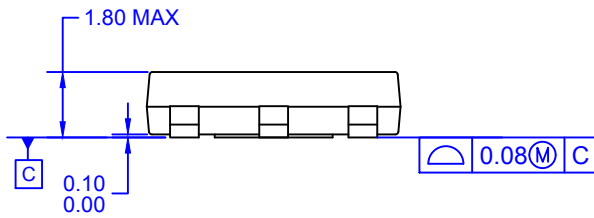


Figure 15. Transient Thermal Response Curve.

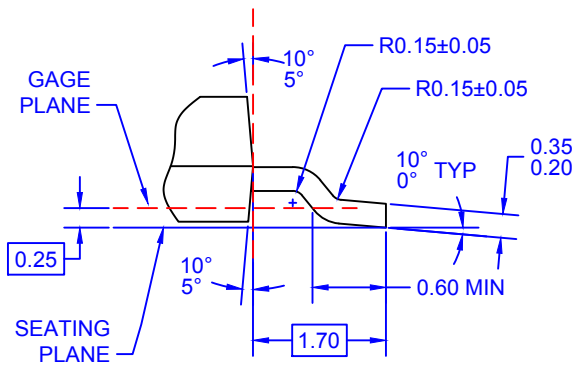
Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.



LAND PATTERN RECOMMENDATION



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 A) DRAWING BASED ON JEDEC REGISTRATION TO-261C, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
 D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.  
 E) LANDPATTERN NAME: SOT230P700X180-4BN  
 F) DRAWING FILENAME: MKT-MA04AREV3



DETAIL A  
SCALE: 2:1



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