

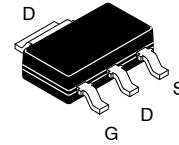


# THE DATASHEET OF NDT014L



# N-Channel Logic Level Enhancement Mode Field Effect Transistor

## NDT014L



SOT-223  
CASE 318H

### General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC-DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- 2.8 A, 60 V.  $R_{DS(ON)} = 0.2 \Omega @ V_{GS} = 4.5 V$   
 $R_{DS(ON)} = 0.16 \Omega @ V_{GS} = 10 V$
- High Density Cell Design For Extremely Low  $R_{DS(ON)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- This Device is Pb-Free

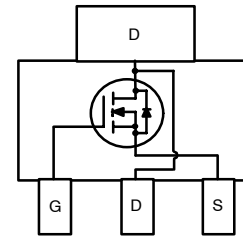
### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ , unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	$\pm 2.8$	A
		$\pm 10$	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b) (Note 1c)	3	W
		1.3	
		1.1	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 150	$^\circ C$

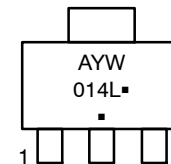
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS Values are at $T_A = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ C/W$



### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- 014L = Specific Device Code
- = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NDT014L	SOT-223	4000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NDT014L

**ELECTRICAL CHARACTERISTICS** Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
--------	-----------	------------	-----	-----	-----	------

## OFF CHARACTERISTICS

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60	–	–	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$	–	–	25 250	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA

## ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	1 0.8	1.5 1.1	3 2	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.8\text{ A}$ $T_J = 125^\circ\text{C}$	–	0.17 0.22	0.2 0.36	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 3.4\text{ A}$	–	0.12	0.16	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	5	–	–	A
		$V_{DS} = 10\text{ V}, V_{DS} = 5\text{ V}$	10	–	–	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2.8\text{ A}$	–	4.2	–	S

## DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	–	214	–	pF
$C_{oss}$	Output Capacitance		–	70	–	pF
$C_{rss}$	Reverse Transfer Capacitance		–	27	–	pF

## SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 30\text{ V}, I_D = 3\text{ A},$ $V_{GEN} = 10\text{ V}, R_{GEN} = 12\ \Omega$	–	6	12	ns
$t_r$	Turn–On Rise Time		–	14	25	ns
$t_{d(off)}$	Turn–Off Delay Time		–	15	28	ns
$t_f$	Turn–Off Fall Time		–	10	18	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 2.8\text{ A},$ $V_{GS} = 4.5\text{ V}$	–	36	5	nC
$Q_{gs}$	Gate–Source Charge		–	0.8	–	nC
$Q_{gd}$	Gate–Drain Charge		–	1.4	–	nC

## DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

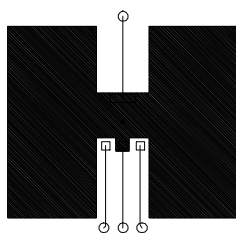
$I_S$	Maximum Continuous Drain–Source Diode Forward Current	–	–	2.3	A	
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ (Note 2)	–	0.85	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 2.3\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	–	–	140	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$  is the sum of the junction–to–case and case–to–ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user’s board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)@T_J}$$

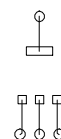
Applications on 4.5"x5" FR-4 PCB under still air environment, typical  $R_{\theta JA}$  is found to be:



a.  $42^\circ\text{C}/\text{W}$  with  $1\text{ in}^2$  of 2 oz copper mounting pad.



b.  $95^\circ\text{C}/\text{W}$  with  $0.066\text{ in}^2$  of 2 oz copper mounting pad.



c.  $110^\circ\text{C}/\text{W}$  with  $0.0123\text{ in}^2$  of 2 oz copper mounting pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

TYPICAL CHARACTERISTICS

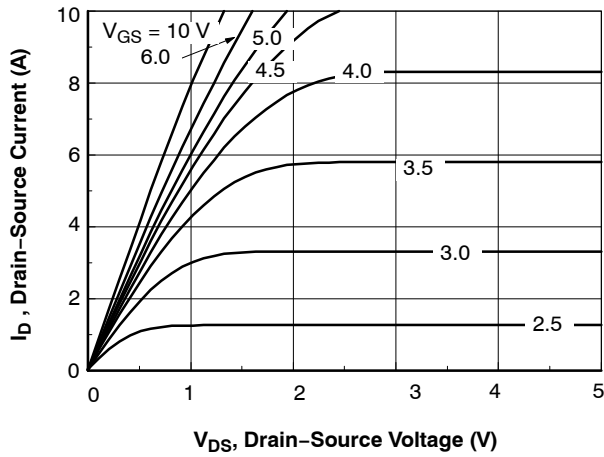


Figure 1. On-Region Characteristics

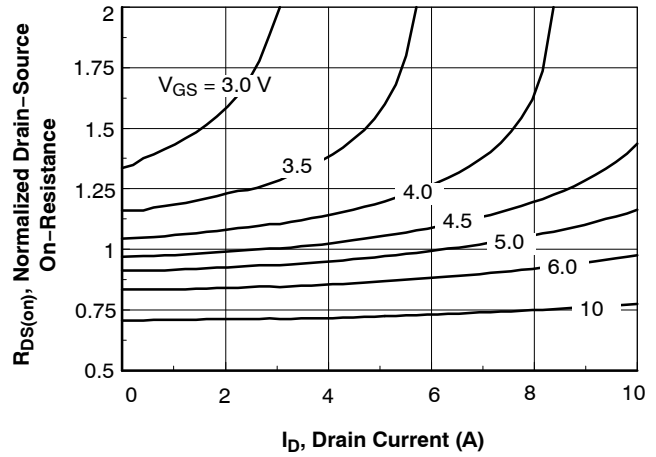


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

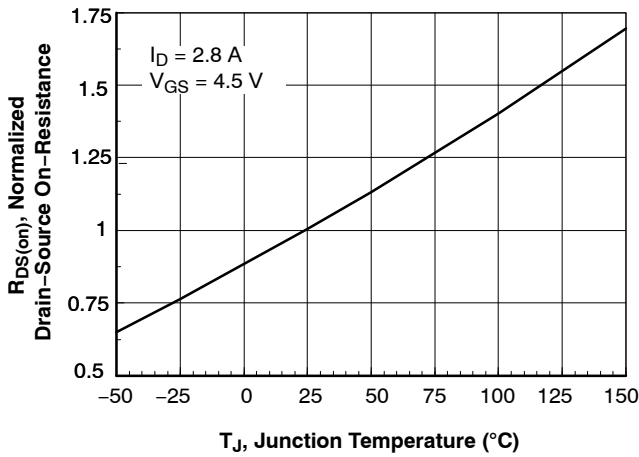


Figure 3. On-Resistance Variation with Temperature

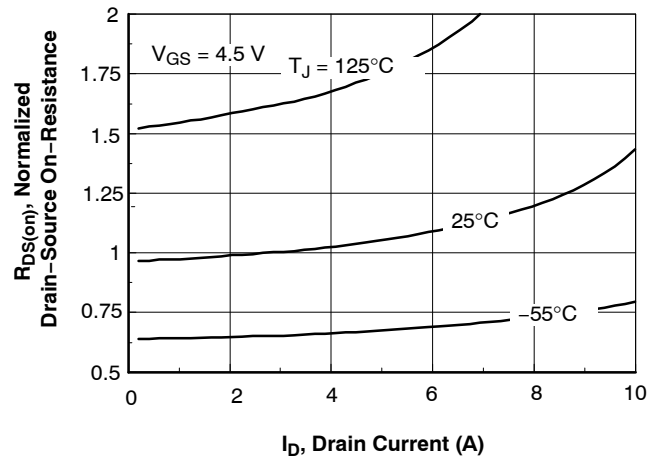


Figure 4. On-Resistance Variation with Drain Current and Temperature

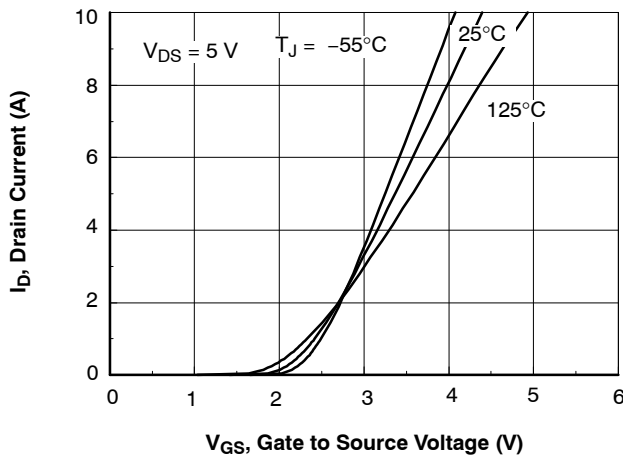


Figure 5. Transfer Characteristics

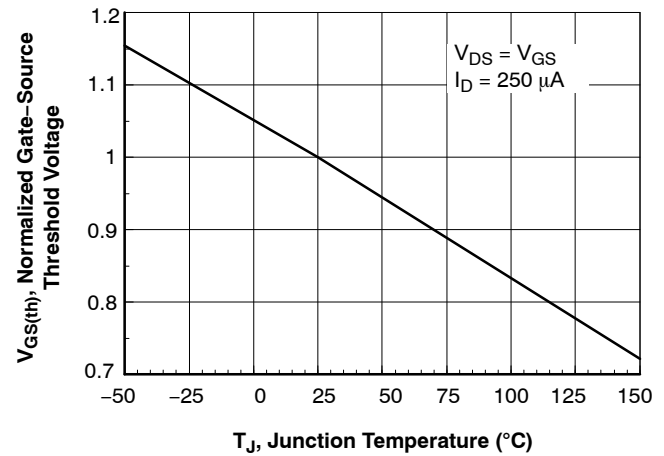


Figure 6. Gate Threshold Variation with Temperature

TYPICAL CHARACTERISTICS (continued)

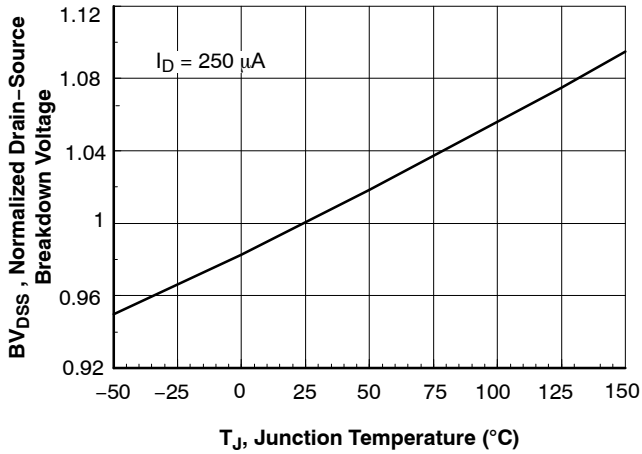


Figure 7. Breakdown Voltage Variation with Temperature

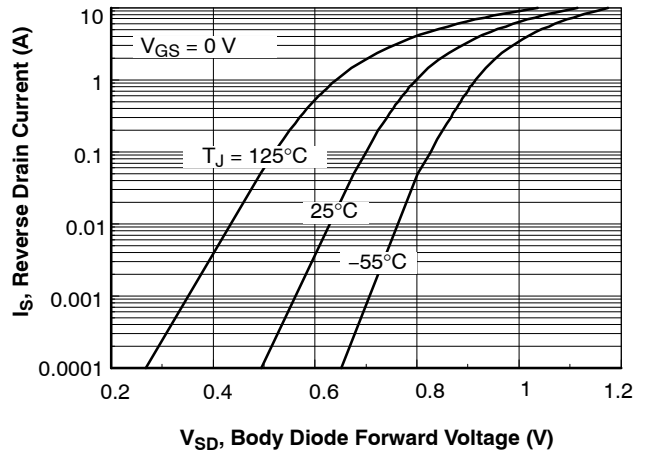


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

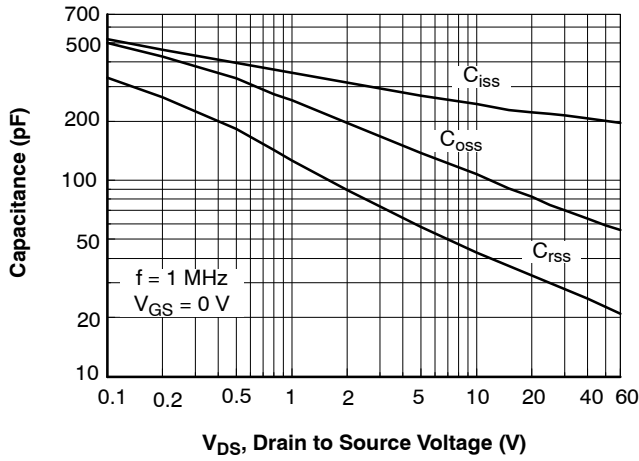


Figure 9. Capacitance Characteristics

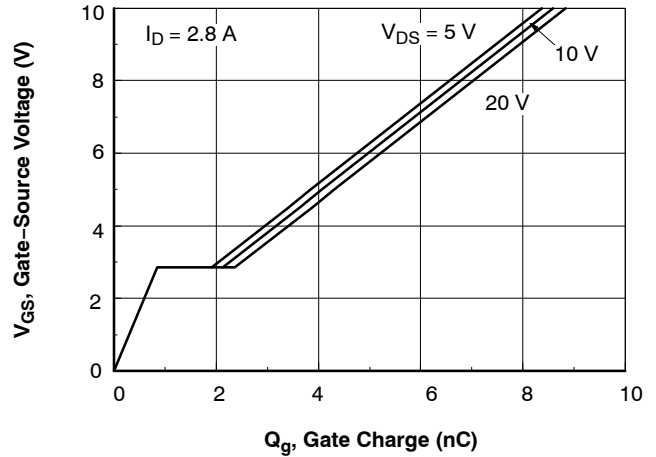


Figure 10. Gate Charge Characteristics

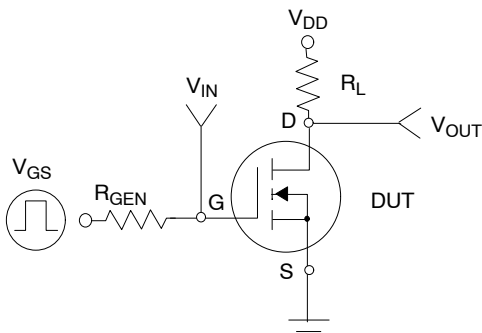


Figure 11. Switching Test Circuit

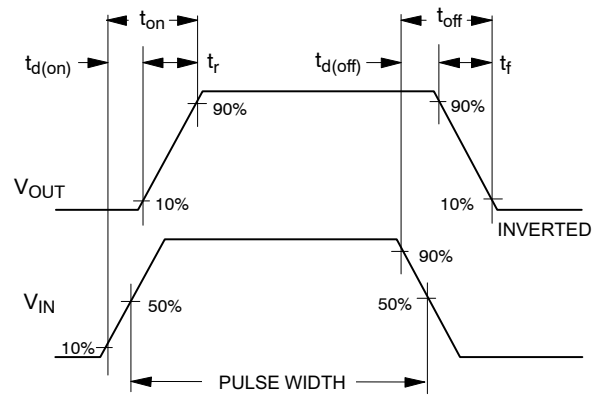


Figure 12. Switching Waveforms

TYPICAL CHARACTERISTICS (continued)

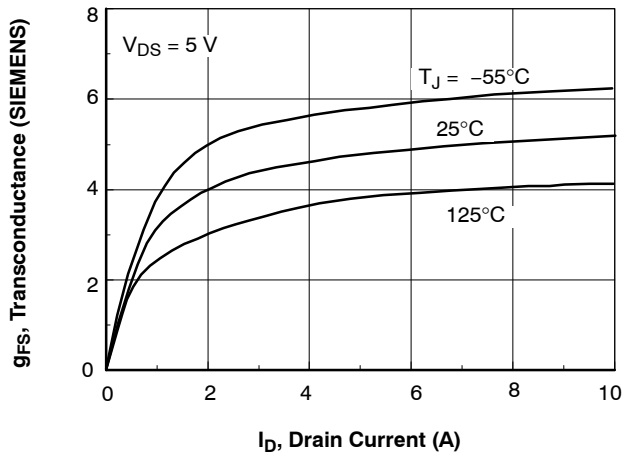


Figure 13. Transconductance Variation with Drain Current and Temperature

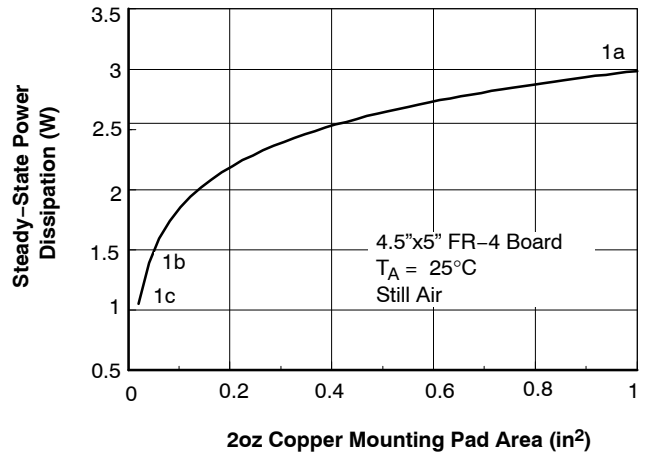


Figure 14. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area

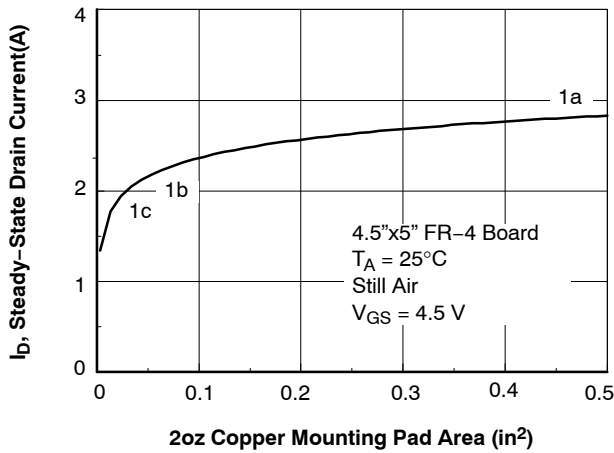


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

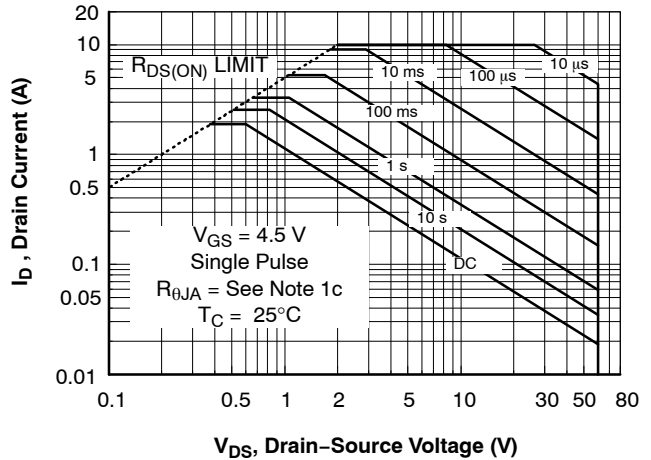


Figure 16. Maximum Safe Operating Area

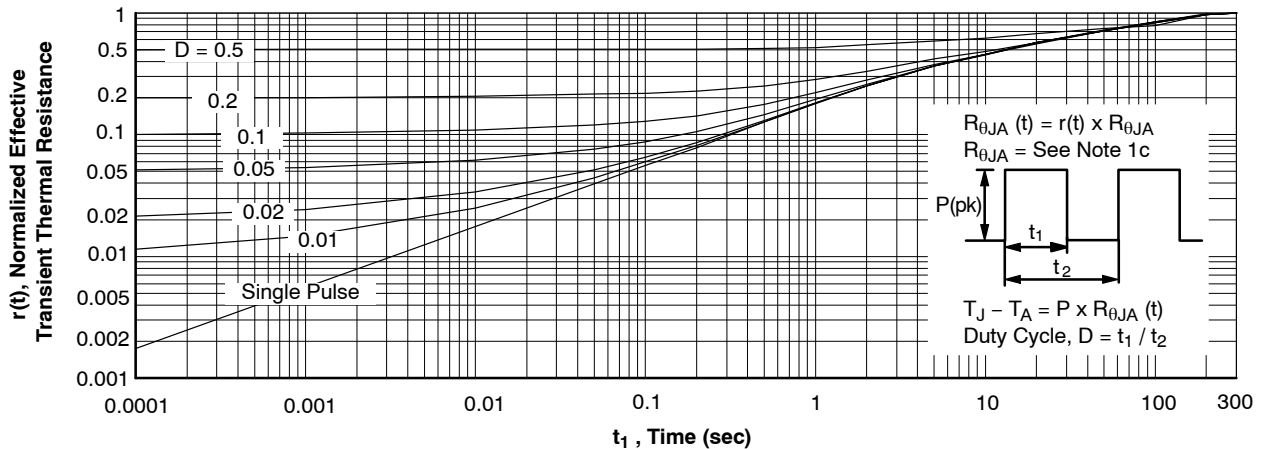


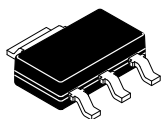
Figure 17. Typical Transient Thermal Impedance Curve

Thermal characterization performed under the conditions of Note 1c. Should better thermal design employs,  $R_{\theta JA}$  will be lower and reach thermal equivalent sooner.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

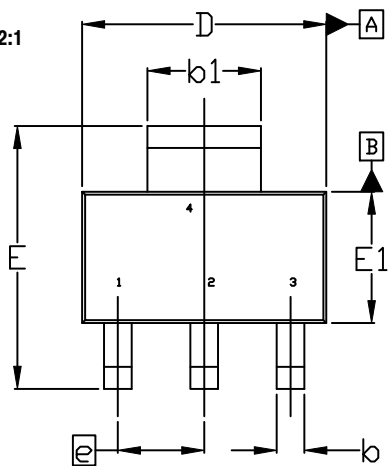
ON Semiconductor®



**SOT-223**  
CASE 318H  
ISSUE B

DATE 13 MAY 2020

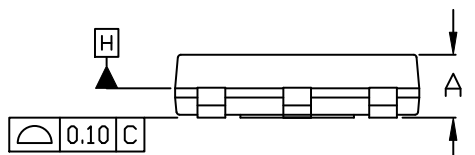
SCALE 2:1



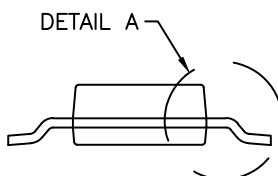
TOP VIEW

$\Phi 0.10 \text{ (M)}$  C A B

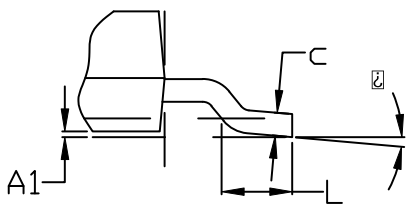
NOTE 7



SIDE VIEW



END VIEW

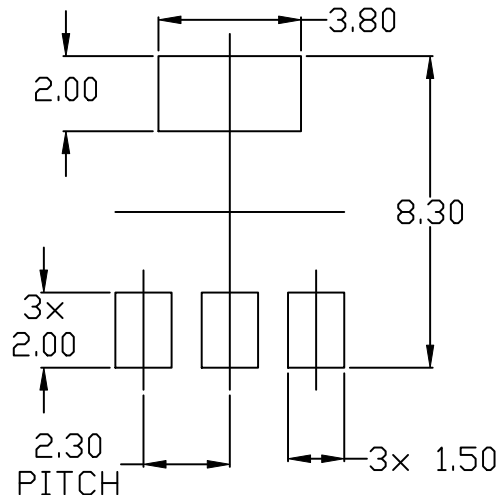


DETAIL A

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

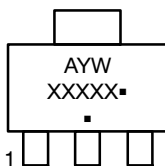
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
$\square$	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98ASH70634A</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOT-223</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)


### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)



## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View NDT014L on WIN SOURCE](#)
-  [Fairchild/ON Semiconductor Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management