



**THE DATASHEET OF
NLSF3T125MNR2G**



NLSF3T125

Quad Bus Buffer

with 3-State Control Inputs

The NLSF3T125 is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The NLSF3T125 requires the 3-state control input (\overline{OE}) to be set High to place the output into the high impedance state.

The T125 inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The NLSF3T125 input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: $t_{PD} = 3.8$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 4.0$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model; > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

FUNCTION TABLE

NLSF3T125		
Inputs		Output
A	\overline{OE}	Y
H	L	H
L	L	L
X	H	Z



ON Semiconductor®

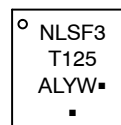
<http://onsemi.com>



1

QFN-16
CASE 485G

MARKING DIAGRAM



NLSF3T125 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NLSF3T125MNR2G	QFN-16 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLSF3T125

Active-Low Output Enables

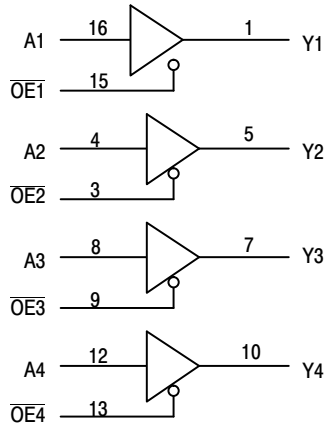


Figure 1. Logic Diagram

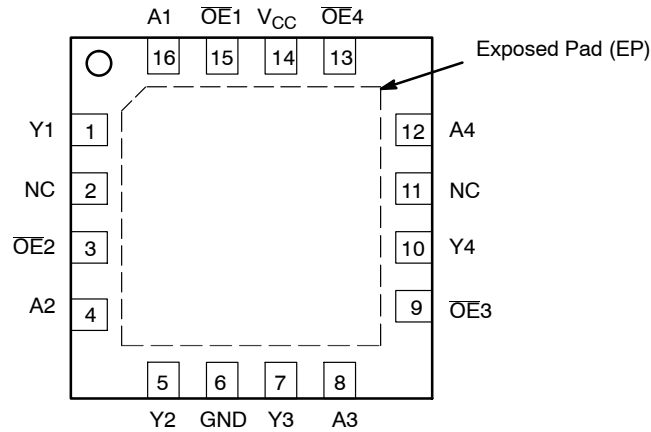


Figure 2. QFN – 16 Pinout (Top View)

MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{in}	DC Input Voltage	-0.5 to +7.0	V
V_{out}	DC Output Voltage Output in 3-State High or Low State	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current ($V_{OUT} < GND$; $V_{OUT} > V_{CC}$)	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air QFN Packages	500	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

NLSF3T125

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage Output in 3-State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature	-40	+85	°C
t_r, t_f	Input Rise and Fall Time $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Units		
				Min	Typ	Max	Min	Max	Min	Max			
V_{IH}	Minimum High-Level Input Voltage	$2.3 \text{ V} \pm 0.3 \text{ V}$ $3.3 \text{ V} \pm 0.3 \text{ V}$ $5.0 \text{ V} \pm 0.5 \text{ V}$		$0.5 V_{CC}$ $0.4 V_{CC}$ $0.44 V_{CC}$			$0.5 V_{CC}$ $0.4 V_{CC}$ $0.44 V_{CC}$		$0.5 V_{CC}$ $0.4 V_{CC}$ $0.44 V_{CC}$		V		
V_{IL}	Maximum Low-Level Input Voltage	$2.3 \text{ V} \pm 0.3 \text{ V}$ $3.3 \text{ V} \pm 0.3 \text{ V}$ $5.0 \text{ V} \pm 0.5 \text{ V}$				$0.3 V_{CC}$ $0.18 V_{CC}$ $0.18 V_{CC}$		$0.3 V_{CC}$ $0.18 V_{CC}$ $0.18 V_{CC}$		$0.3 V_{CC}$ $0.18 V_{CC}$ $0.18 V_{CC}$		V	
V_{OH}	Minimum High-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{OL} @ I_{OL}, 50 \text{ mA}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0			1.9		1.9		V	
			3.0	2.9	3.0			2.9		2.9			
			4.5	4.4	4.5			4.4		4.4			
V_{OL}	Maximum Low-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{OL} @ I_{OL}, 50 \text{ mA}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu\text{A}$	2.0		0.0	0.1			0.1		0.1		V
			3.0		0.0	0.1			0.1		0.1		
			4.5		0.0	0.1			0.1		0.1		
V_{OL}	Maximum Low-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 2.0 \text{ mA}$ $I_{OL} = 4.0 \text{ mA}$ $I_{OL} = 8.0 \text{ mA}$	2.0			0.36			0.44		0.52		V
			3.0			0.36			0.44		0.52		
			4.5			0.36			0.44		0.52		
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5 \text{ V}$ or GND	0 to 5.5			± 0.1		± 1.0		± 1.0		μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40		μA	
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4 \text{ V}$	5.5			1.35		1.50		1.65		mA	
I_{OZ}	Maximum 3-State Leakage Current	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5			± 0.25		± 2.5		± 2.5		μA	
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5 \text{ V}$	0.0			0.5		5.0		10		μA	

NLSF3T125

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	1.0	14.5	16.9	1.0	18.1	1.0	19.2	ns
		$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF	1.0 1.0	5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	12.0 16.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF	1.0 1.0	3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5	1.0 1.0	8.5 10.5	ns
t_{PZL} , t_{PZH}	Maximum Output Enable Time, OE to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	1.0	14.8	16.2	1.0	17.4	1.0	19.3	ns
		$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $R_L = 1.0$ k Ω $C_L = 50$ pF	1.0 1.0	5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	11.5 15.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1.0$ k Ω $C_L = 50$ pF	1.0 1.0	3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0	1.0 1.0	7.5 9.5	ns
t_{PLZ} , t_{PHZ}	Maximum Output Disable Time, OE to Y	$V_{CC} = 2.3 \pm 0.3$ V $C_L = 15$ pF	1.0	15.4	18.0	1.0	19.8	1.0	22.0	ns
		$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF $R_L = 1.0$ k Ω	1.0	9.5	13.2	1.0	15.0	1.0	18.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1.0$ k Ω	1.0	6.1	8.8	1.0	10.0	1.0	12.0	ns
t_{OSLH} , t_{OSHL}	Output-to-Output Skew	$V_{CC} = 3.3 \pm 0.3$ V $C_L = 50$ pF (Note 1)			1.5		1.5		2.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 1)			1.0		1.0		1.5	ns
C_{in}	Maximum Input Capacitance			4	10		10		10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)			6						pF
			Typical @ 25°C, $V_{CC} = 5.0$ V							
C_{PD}	Power Dissipation Capacitance (Note 2)		15							pF

- Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Units
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

NLSF3T125

SWITCHING WAVEFORMS

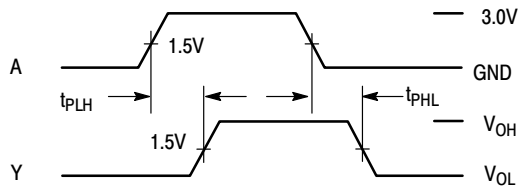


Figure 3.

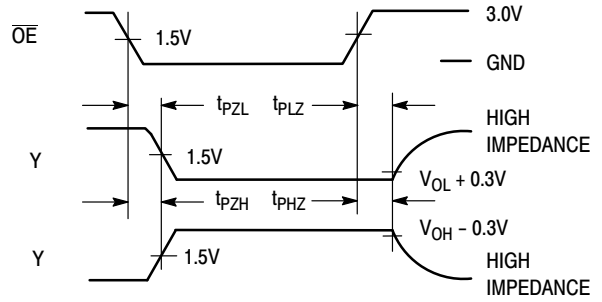
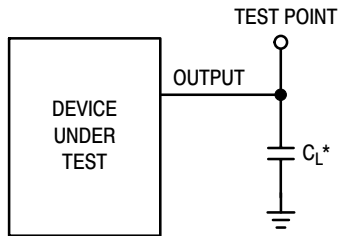
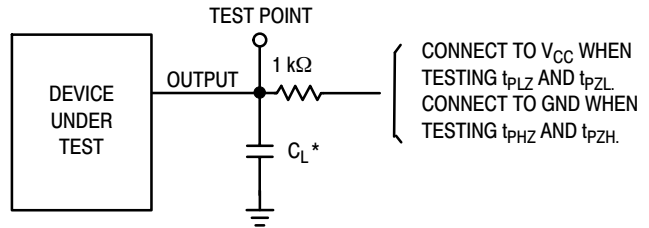


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit



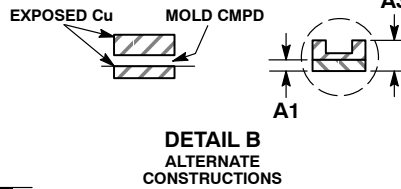
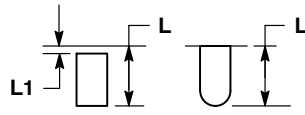
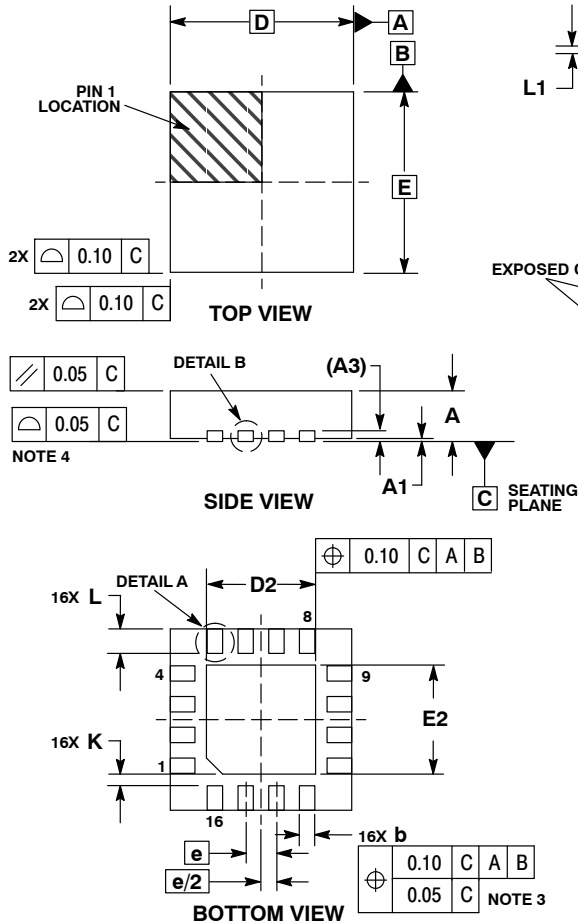
*Includes all probe and jig capacitance

Figure 6. Test Circuit

NLSF3T125

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G-01
ISSUE F

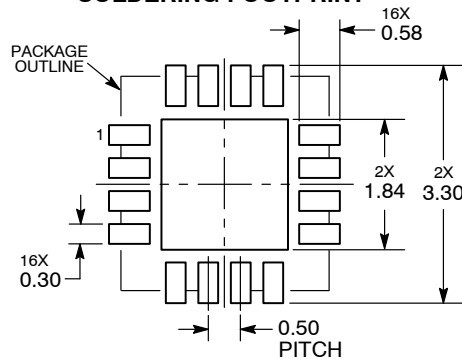


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View NLSF3T125MNR2G on WIN SOURCE](#)
- ⊖ [ON Semiconductor Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management