



**THE DATASHEET OF  
NP180N04TUK-E1-AY**



# NP180N04TUK

R07DS0542EJ0100

Rev.1.00

Sep 23, 2011

## MOS FIELD EFFECT TRANSISTOR

### Description

The NP180N04TUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

### Features

- Super low on-state resistance  
 $R_{DS(on)} = 1.05 \text{ m}\Omega \text{ MAX. ( } V_{GS} = 10 \text{ V, } I_D = 90 \text{ A )}$
- Low  $C_{iss}$ :  $C_{iss} = 10500 \text{ pF TYP. ( } V_{DS} = 25 \text{ V )}$
- Designed for automotive application and AEC-Q101 qualified

### Ordering Information

Part No.	Lead Plating	Packing		Package
NP180N04TUK-E1-AY <sup>*1</sup>	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263-7pin (MP-25ZT)
NP180N04TUK-E2-AY <sup>*1</sup>			Taping (E2 type)	

Note: <sup>\*1</sup>. Pb-free (This product does not contain Pb in the external electrode.)

### Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±180	A
Drain Current (pulse) <sup>*1</sup>	I <sub>D(pulse)</sub>	±720	A
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	348	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current <sup>*2</sup>	I <sub>AR</sub>	72	A
Repetitive Avalanche Energy <sup>*2</sup>	E <sub>AR</sub>	518	mJ

### Thermal Resistance

Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub>	0.43	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	83.3	°C/W

Notes: <sup>\*1</sup>. T<sub>C</sub> = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%

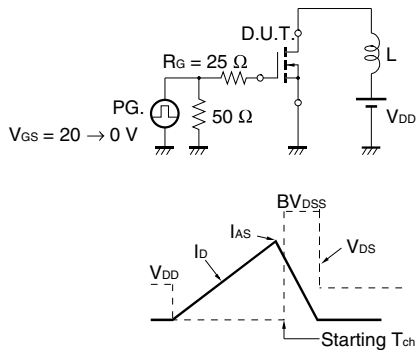
<sup>\*2</sup>. R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 → 0 V

Electrical Characteristics (T<sub>A</sub> = 25°C)

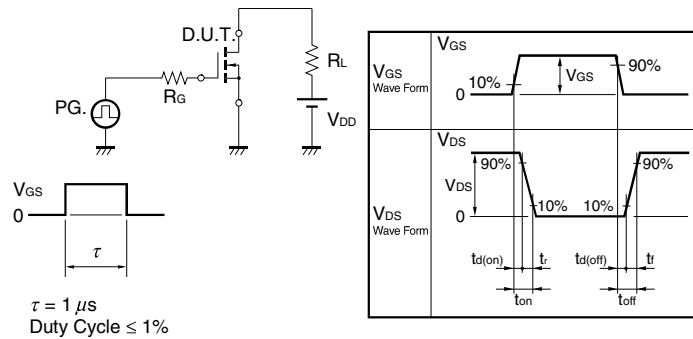
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	2.0	3.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	75	150		S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 90 A
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>		0.85	1.05	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 90 A
Input Capacitance	C <sub>iss</sub>		10500	15750	pF	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz
Output Capacitance	C <sub>oss</sub>		1600	2400	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		540	980	pF	
Turn-on Delay Time	t <sub>d(on)</sub>		38	90	ns	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 90 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 0 Ω
Rise Time	t <sub>r</sub>		22	60	ns	
Turn-off Delay Time	t <sub>d(off)</sub>		140	280	ns	V <sub>DD</sub> = 32 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 180 A
Fall Time	t <sub>f</sub>		20	50	ns	
Total Gate Charge	Q <sub>G</sub>		198	297	nC	I <sub>F</sub> = 180 A, V <sub>GS</sub> = 0 V
Gate to Source Charge	Q <sub>GS</sub>		50		nC	
Gate to Drain Charge	Q <sub>GD</sub>		48		nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.9	1.5	V	I <sub>F</sub> = 180 A, V <sub>GS</sub> = 0 V, di/dt = 100 A/μs
Reverse Recovery Time	t <sub>rr</sub>		83		ns	
Reverse Recovery Charge	Q <sub>rr</sub>		130		nC	

Note: \*1. Pulsed test

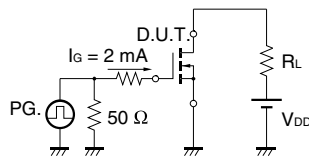
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

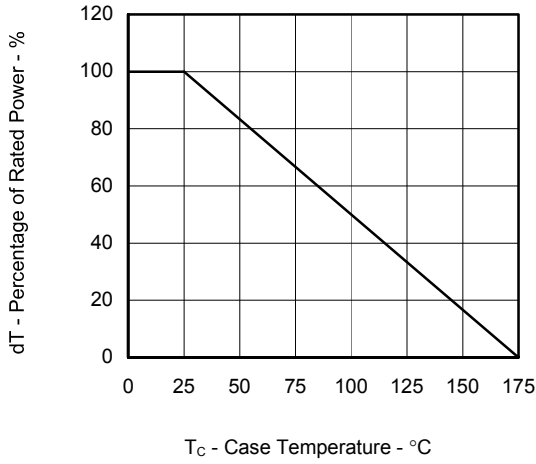


TEST CIRCUIT 3 GATE CHARGE

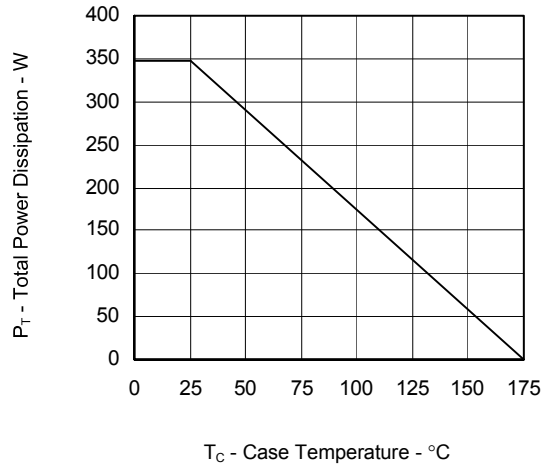


Typical Characteristics ( $T_A = 25^\circ\text{C}$ )

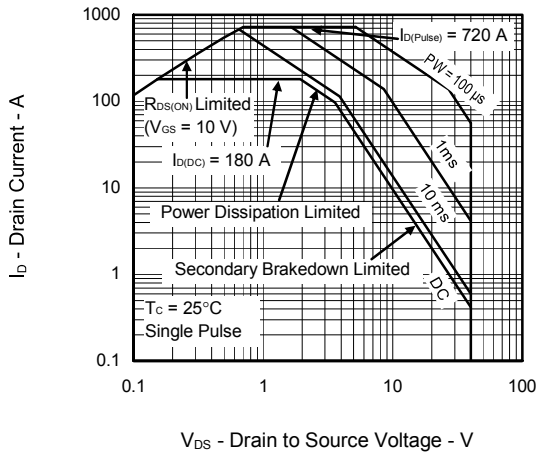
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



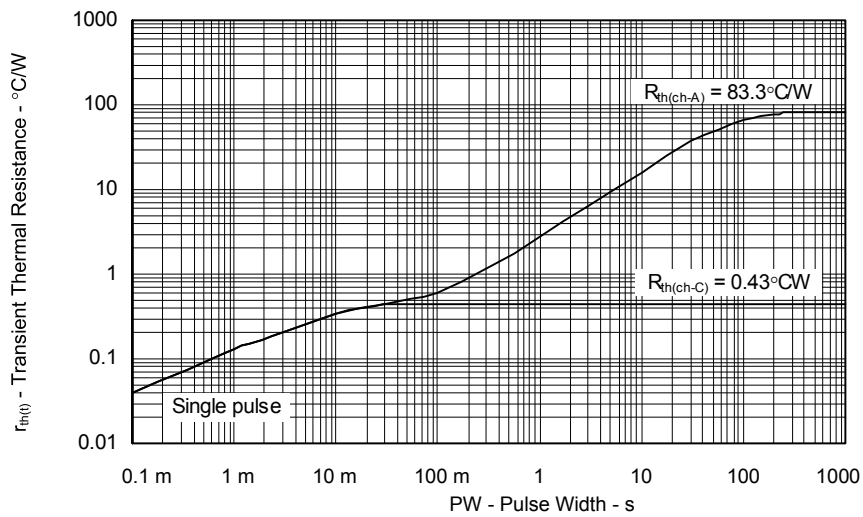
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



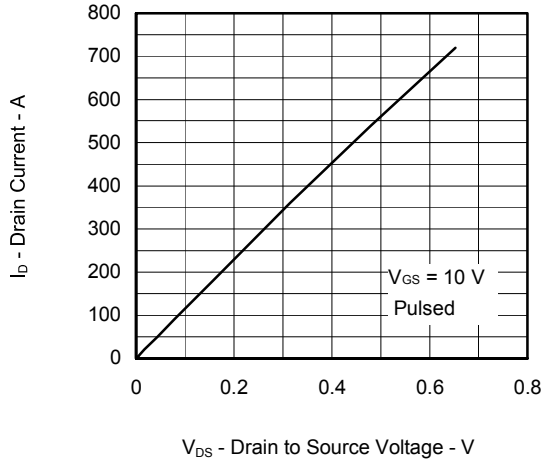
FORWARD BIAS SAFE OPERATING AREA



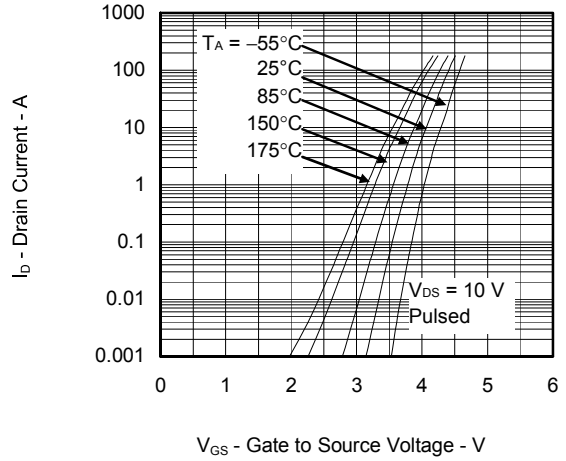
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



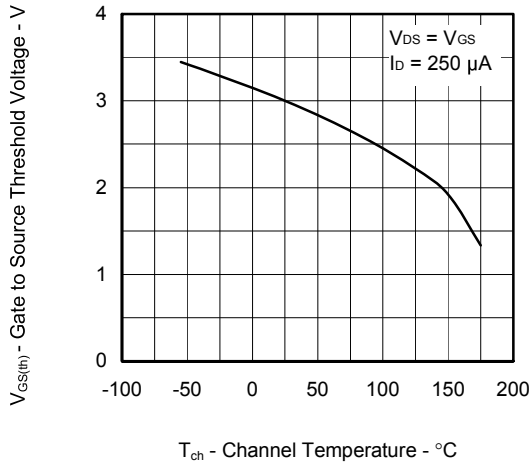
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



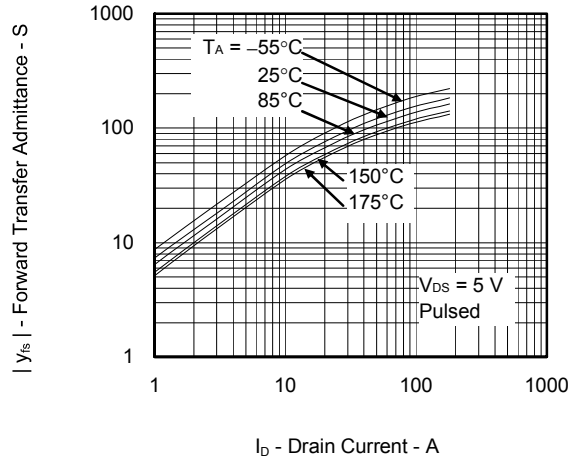
FORWARD TRANSFER CHARACTERISTICS



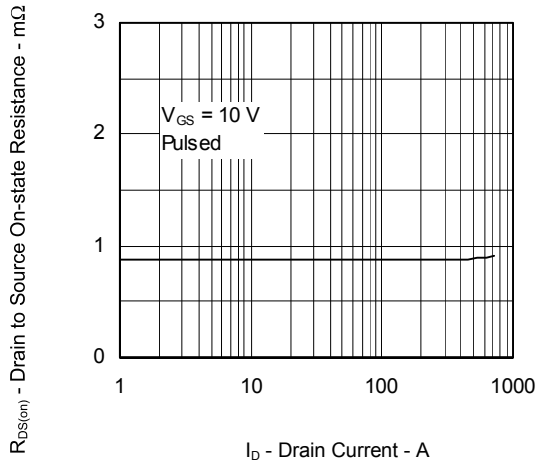
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



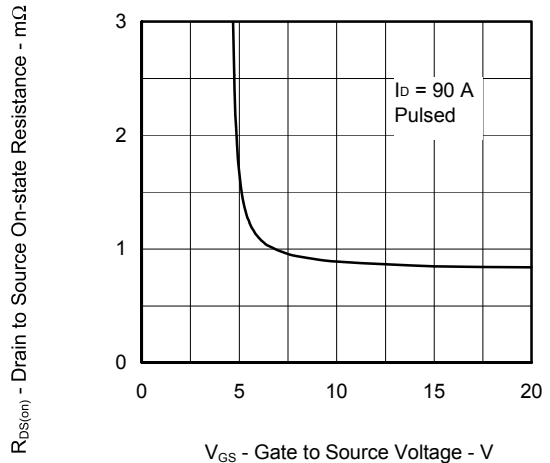
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



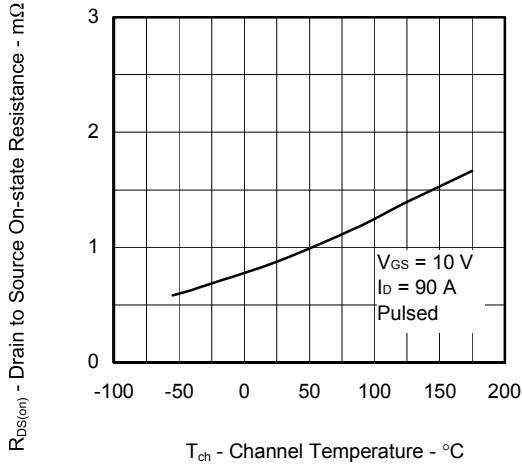
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



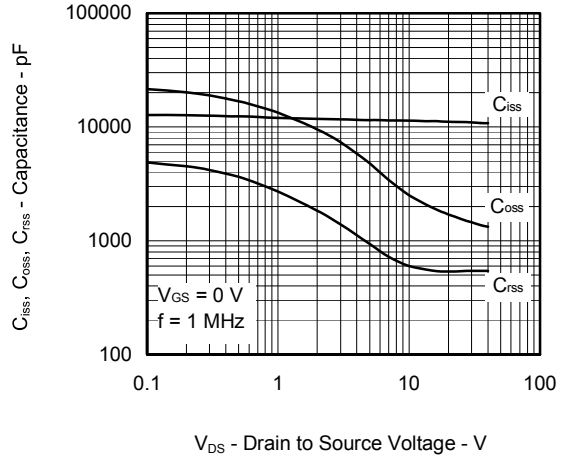
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



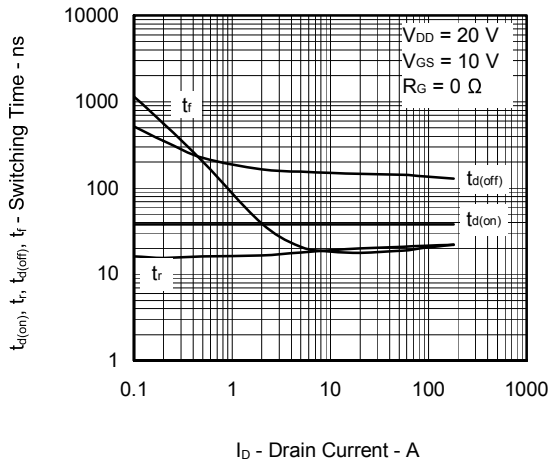
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



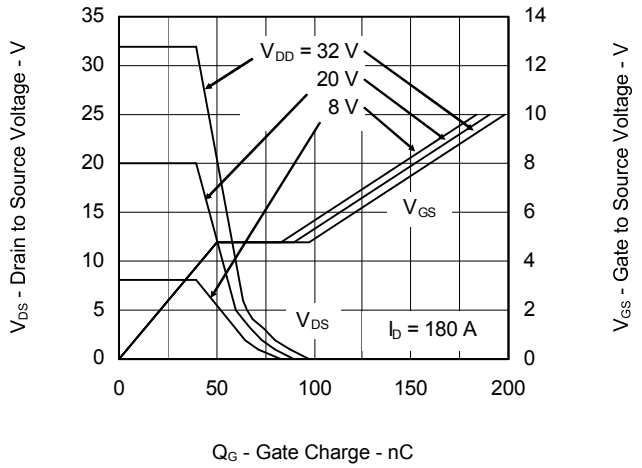
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



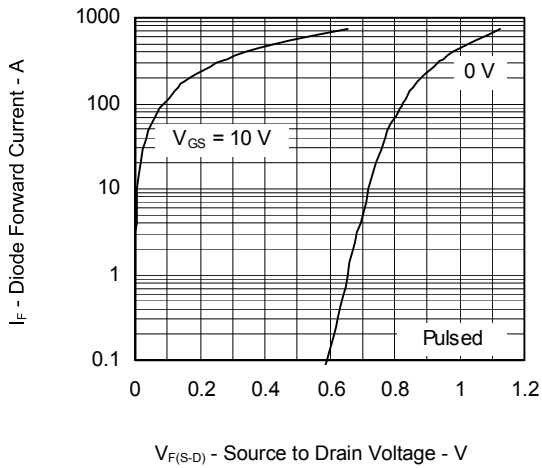
SWITCHING CHARACTERISTICS



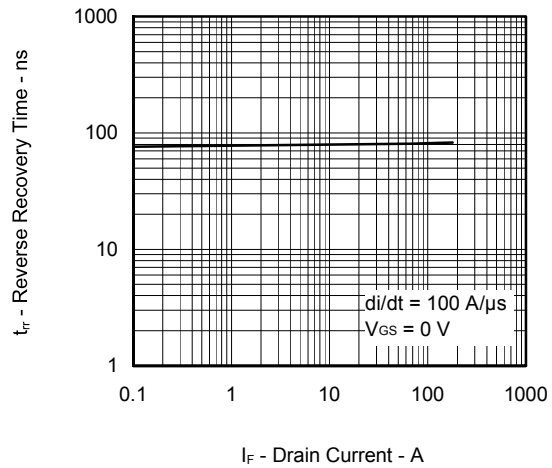
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT



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<b>Revision History</b>	<b>NP180N04TUK Data Sheet</b>
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<b>Rev.</b>	<b>Date</b>	<b>Description</b>	
		<b>Page</b>	<b>Summary</b>
1.00	Sep 23, 2011	-	First Edition Issued

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