

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The NP55N055SUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance
 $R_{DS(on)} = 10 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 28 \text{ A)}$
- Low C_{iss} : $C_{iss} = 3500 \text{ pF TYP.}$

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	55	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 55	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 220	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	77	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current ^{Note2}	I_{AR}	27	A
Repetitive Avalanche Energy ^{Note2}	E_{AR}	73	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. $T_{ch} < 150^\circ\text{C}$, $V_{DD} = 28 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

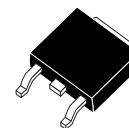
THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.95	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP55N055SUG	TO-252 (MP-3ZK)

(TO-252)



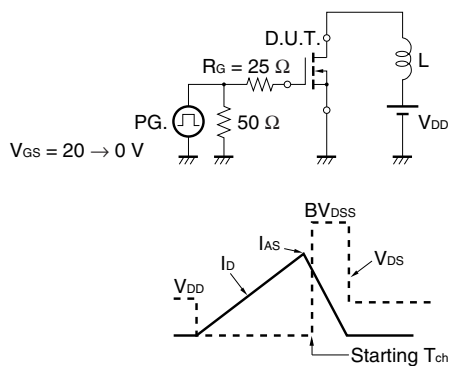
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

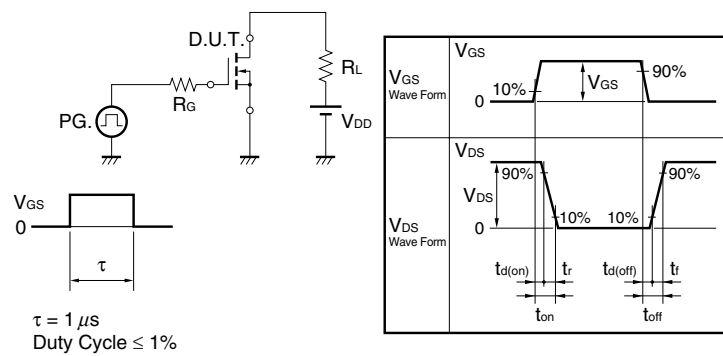
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55 V, V _{GS} = 0 V			1.0	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 28 A	11	22		S
Drain to Source On-state Resistance Note	R _{DS(on)}	V _{GS} = 10 V, I _D = 28 A		7.7	10	mΩ
Input Capacitance	C _{iss}	V _{DS} = 25 V		3500	5250	pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		260	390	pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		160	290	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 28 V, I _D = 28 A		24	53	ns
Rise Time	t _r	V _{GS} = 10 V		18	45	ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		60	120	ns
Fall Time	t _f			8	20	ns
Total Gate Charge	Q _G	V _{DD} = 44 V		60	90	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		15		nC
Gate to Drain Charge	Q _{GD}	I _D = 55 A		21		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 55 A, V _{GS} = 0 V		0.95	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 55 A, V _{GS} = 0 V		38		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		45		nC

Note Pulsed

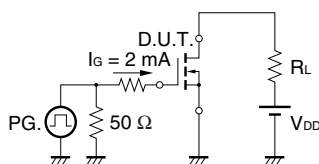
TEST CIRCUIT 1 AVALANCHE CAPABILITY



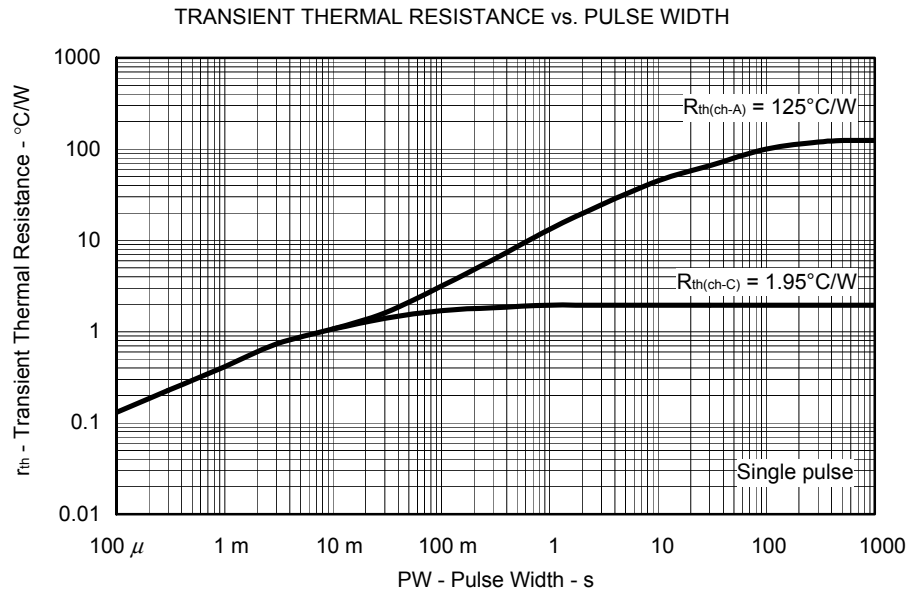
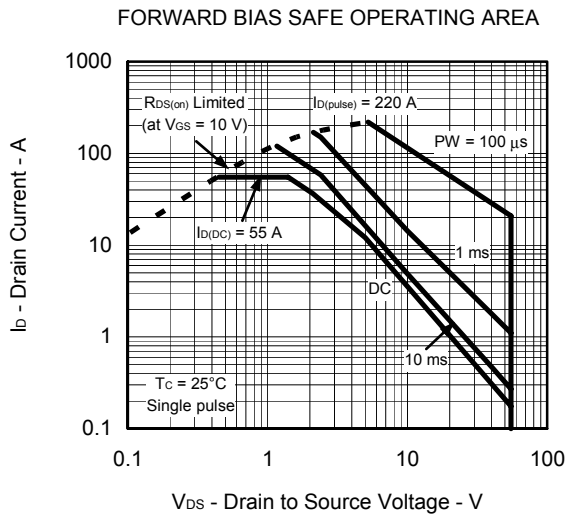
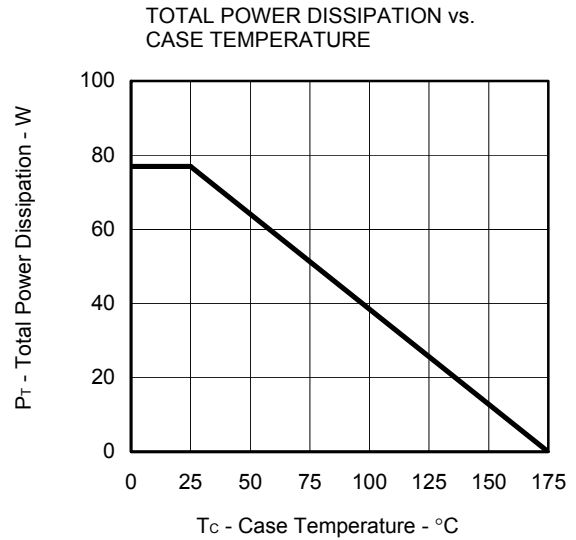
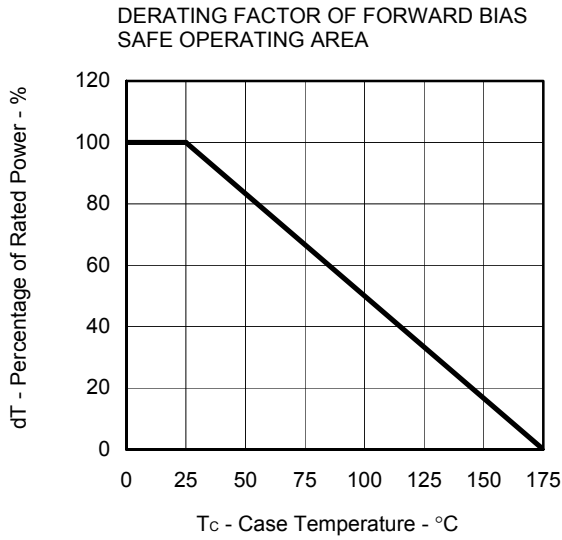
TEST CIRCUIT 2 SWITCHING TIME



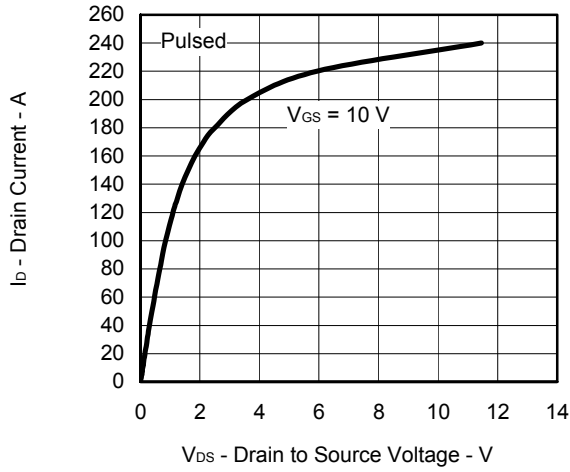
TEST CIRCUIT 3 GATE CHARGE



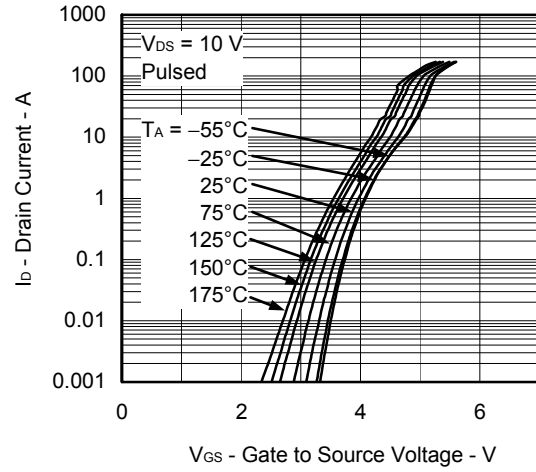
TYPICAL CHARACTERISTICS (T_A = 25°C)



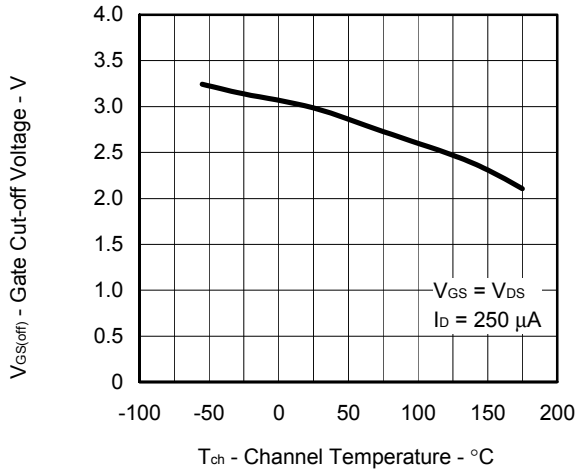
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



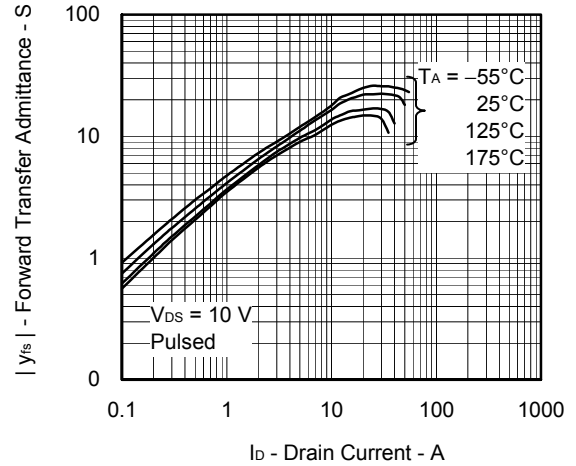
FORWARD TRANSFER CHARACTERISTICS



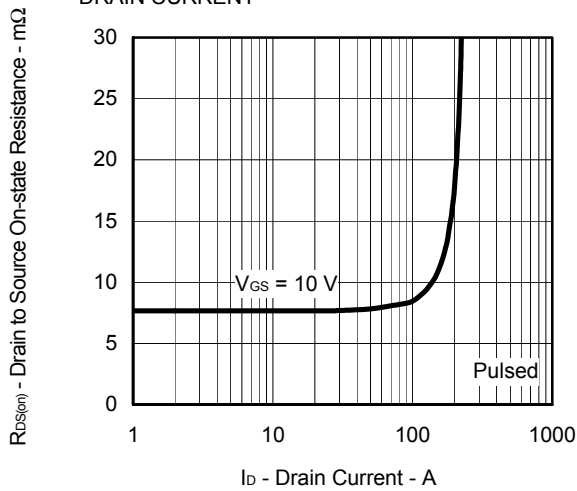
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



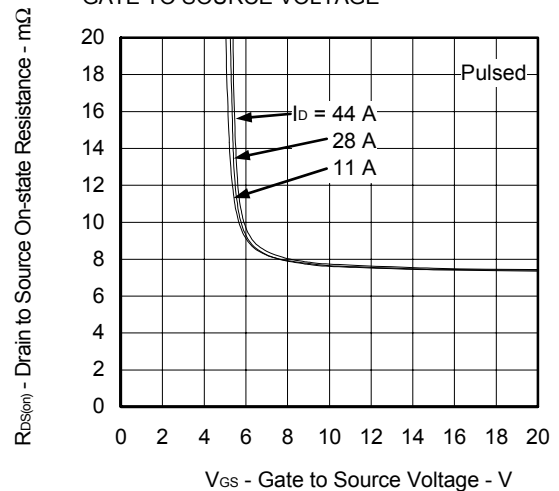
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



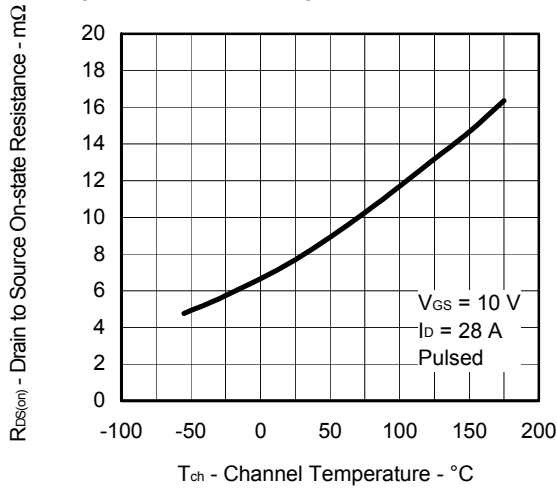
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



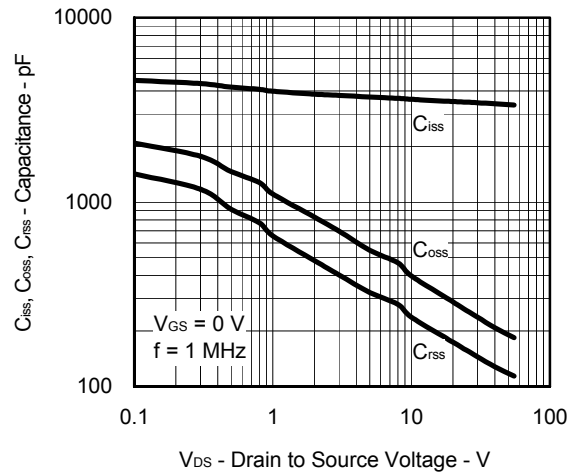
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



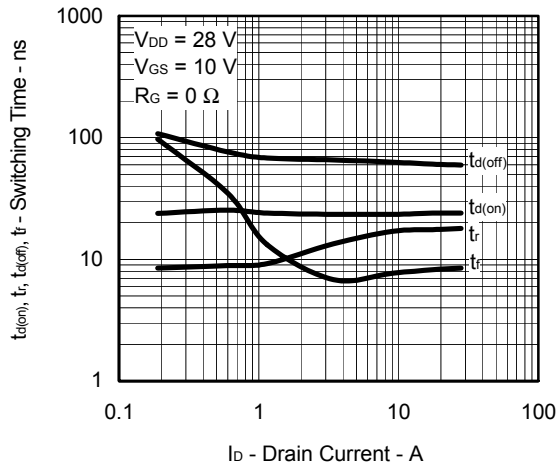
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



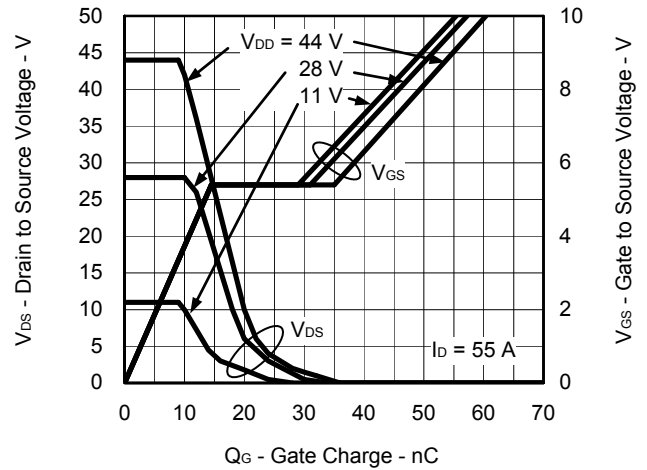
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



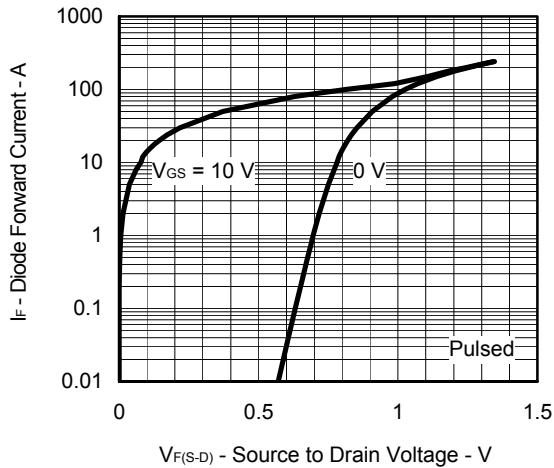
SWITCHING CHARACTERISTICS



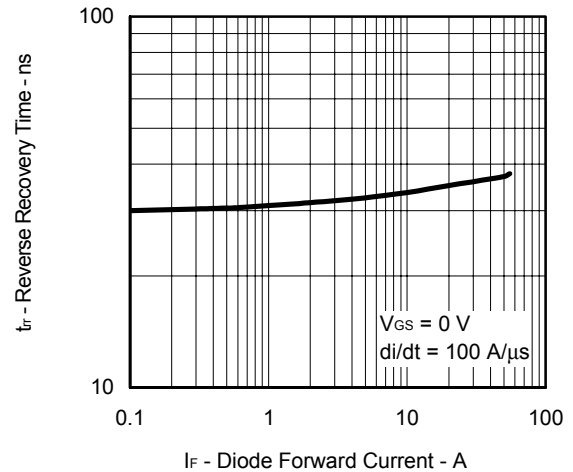
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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