



**THE DATASHEET OF
NSS35200CF8T1G**



NSS35200CF8T1G

35 V, 7 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- This is a Pb-Free Device

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

| Rating | Symbol | Max | Unit |
|--------------------------------|-----------|---------------------------|------|
| Collector-Emitter Voltage | V_{CEO} | -35 | Vdc |
| Collector-Base Voltage | V_{CBO} | -55 | Vdc |
| Emitter-Base Voltage | V_{EBO} | -5.0 | Vdc |
| Collector Current - Continuous | I_C | -2.0 | Adc |
| Collector Current - Peak | I_{CM} | -7.0 | A |
| Electrostatic Discharge | ESD | HBM Class 3 MM Class C | |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---------------------------------------|----------------|----------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D (Note 1) | 635 5.1 | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ (Note 1) | 200 | $^\circ\text{C}/\text{W}$ |
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D (Note 2) | 1.35 11 | W mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ (Note 2) | 90 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Lead #1 | $R_{\theta JL}$ | 15 | $^\circ\text{C}/\text{W}$ |
| Total Device Dissipation (Single Pulse < 10 sec) | $P_{D\text{single}}$ (Notes 2 & 3) | 2.75 | W |
| Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-4 @ 100 mm², 1 oz copper traces.
2. FR-4 @ 500 mm², 1 oz copper traces.
3. Thermal response.

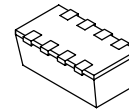
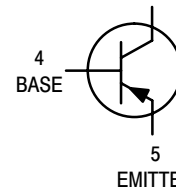


ON Semiconductor®

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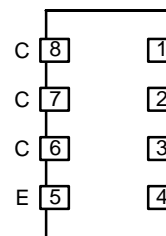
35 VOLTS
7.0 AMPS
PNP LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 78 m Ω

COLLECTOR
1, 2, 3, 6, 7, 8

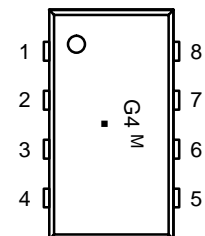


ChipFET™
CASE 1206A
STYLE 4

PIN CONNECTIONS



MARKING DIAGRAM



G4 = Specific Device Code
M = Month Code
▪ = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|----------------------|----------------------|
| NSS35200CF8T1G | ChipFET (Pb-Free) | 3000/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSS35200CF8T1G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typical | Max | Unit |
|--|----------------------|-------------------|-------------------|-------------------------|------------------|
| OFF CHARACTERISTICS | | | | | |
| Collector–Emitter Breakdown Voltage (I _C = -10 mA _{dc} , I _B = 0) | V _{(BR)CEO} | -35 | -45 | - | V _{dc} |
| Collector–Base Breakdown Voltage (I _C = -0.1 mA _{dc} , I _E = 0) | V _{(BR)CBO} | -55 | -65 | - | V _{dc} |
| Emitter–Base Breakdown Voltage (I _E = -0.1 mA _{dc} , I _C = 0) | V _{(BR)EBO} | -5.0 | -7.0 | - | V _{dc} |
| Collector Cutoff Current (V _{CB} = -35 V _{dc} , I _E = 0) | I _{CBO} | - | -0.03 | -0.1 | μA _{dc} |
| Collector–Emitter Cutoff Current (V _{CES} = -35 V _{dc}) | I _{CES} | - | -0.03 | -0.1 | μA _{dc} |
| Emitter Cutoff Current (V _{EB} = -6.0 V _{dc}) | I _{EBO} | - | -0.01 | -0.1 | μA _{dc} |
| ON CHARACTERISTICS | | | | | |
| DC Current Gain (Note 4) (I _C = -1.0 A, V _{CE} = -2.0 V) (I _C = -1.5 A, V _{CE} = -2.0 V) (I _C = -2.0 A, V _{CE} = -2.0 V) | h _{FE} | 100 100 100 | 200 200 200 | - 400 - | |
| Collector–Emitter Saturation Voltage (Note 4) (I _C = -0.1 A, I _B = -0.010 A) (I _C = -1.0 A, I _B = -0.010 A) (I _C = -2.0 A, I _B = -0.02 A) | V _{CE(sat)} | - - - | - - - | -0.10 -0.15 -0.30 | V |
| Base–Emitter Saturation Voltage (Note 4) (I _C = -1.0 A, I _B = -0.01 A) | V _{BE(sat)} | - | -0.68 | -0.85 | V |
| Base–Emitter Turn-on Voltage (Note 4) (I _C = -2.0 A, V _{CE} = -3.0 V) | V _{BE(on)} | - | -0.81 | -0.875 | V |
| Cutoff Frequency (I _C = -100 mA, V _{CE} = -5.0 V, f = 100 MHz) | f _T | 100 | - | - | MHz |
| Input Capacitance (V _{EB} = -0.5 V, f = 1.0 MHz) | C _{ibo} | - | 600 | 650 | pF |
| Output Capacitance (V _{CB} = -3.0 V, f = 1.0 MHz) | C _{obo} | - | 85 | 100 | pF |
| Turn-on Time (V _{CC} = -10 V, I _{B1} = -100 mA, I _C = -1 A, R _L = 3 Ω) | t _{on} | - | 35 | - | nS |
| Turn-off Time (V _{CC} = -10 V, I _{B1} = I _{B2} = -100 mA, I _C = 1 A, R _L = 3 Ω) | t _{off} | - | 225 | - | nS |

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

NSS35200CF8T1G

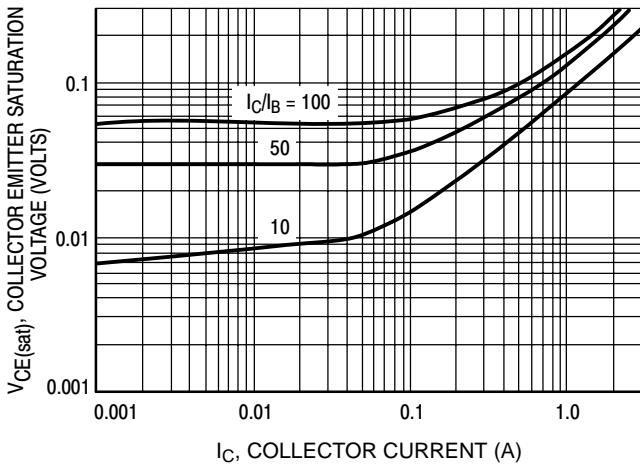


Figure 1. Collector Emitter Saturation Voltage versus Collector Current

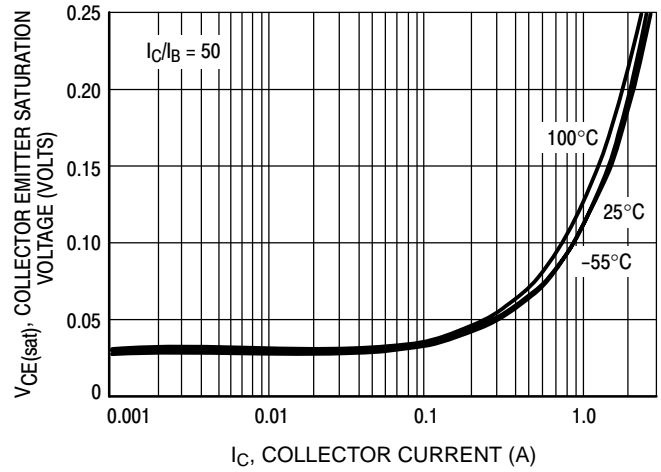


Figure 2. Collector Emitter Saturation Voltage versus Collector Current

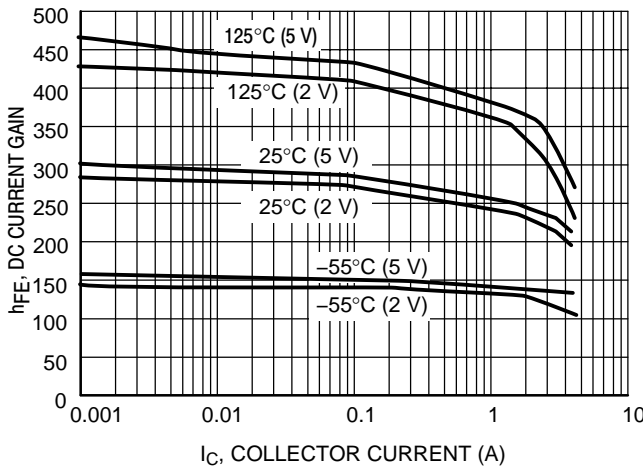


Figure 3. DC Current Gain versus Collector Current

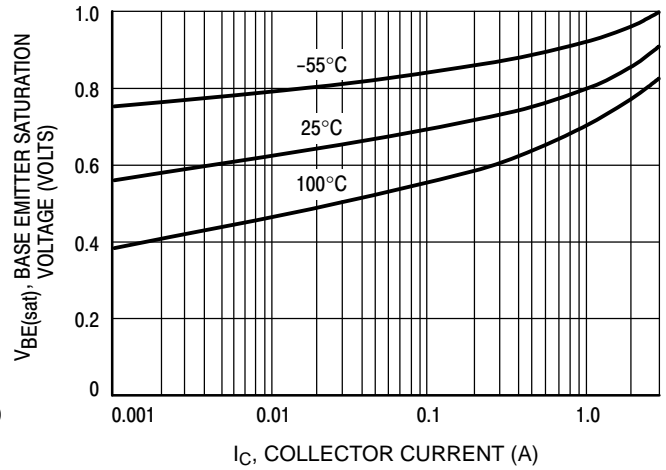


Figure 4. Base Emitter Saturation Voltage versus Collector Current

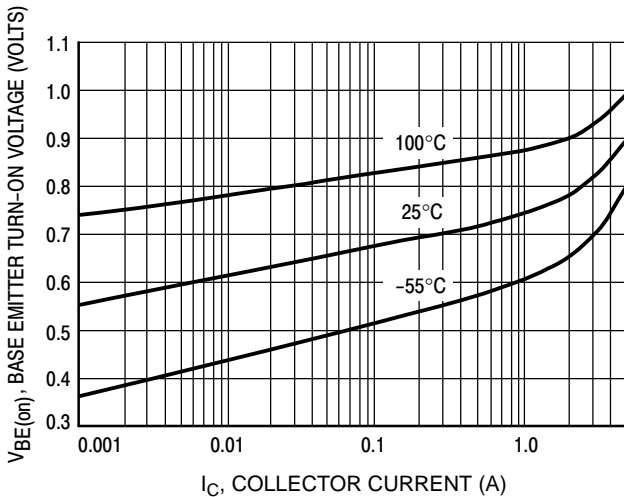


Figure 5. Base Emitter Turn-On Voltage versus Collector Current

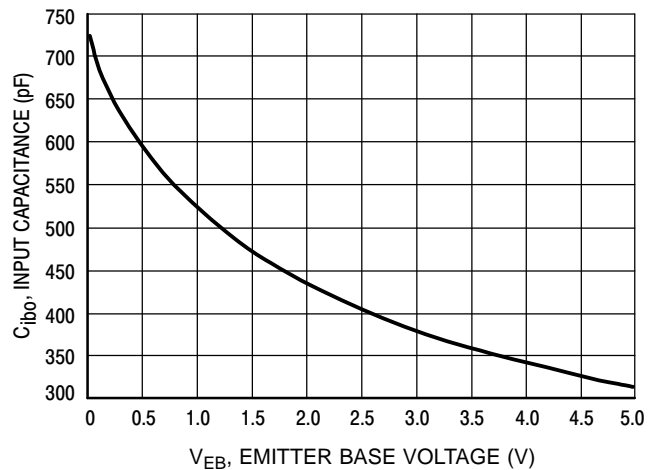


Figure 6. Input Capacitance

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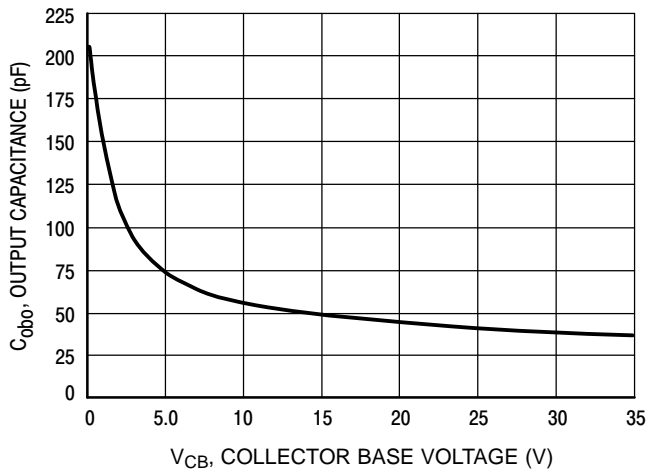


Figure 7. Output Capacitance

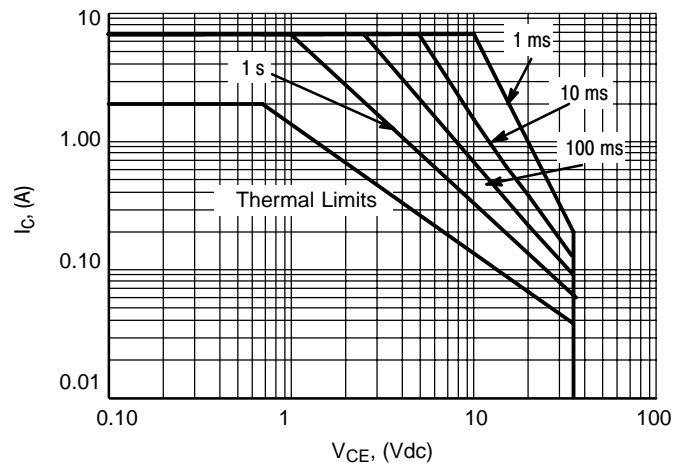


Figure 8. Safe Operating Area

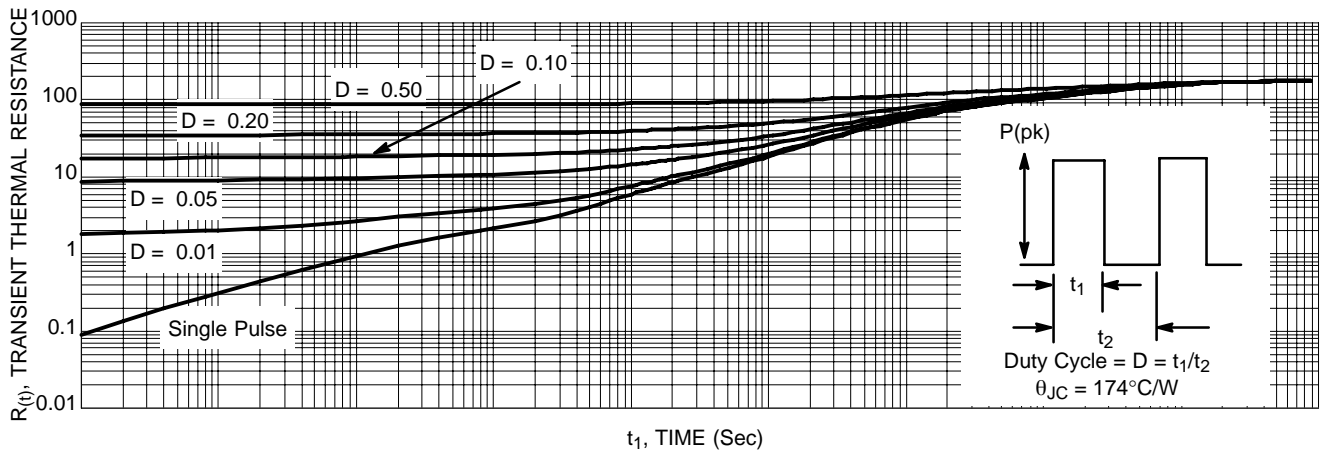
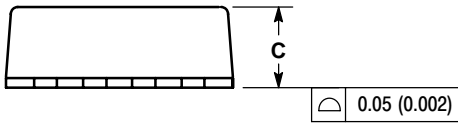
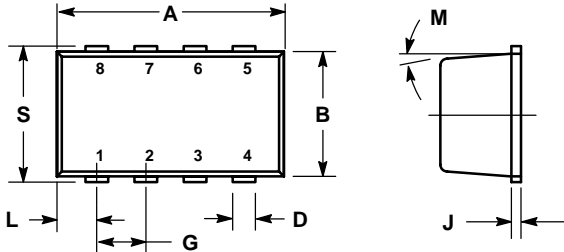


Figure 9. Normalized Thermal Response

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PACKAGE DIMENSIONS

ChipFET
CASE 1206A-03
ISSUE PRELIMINARY



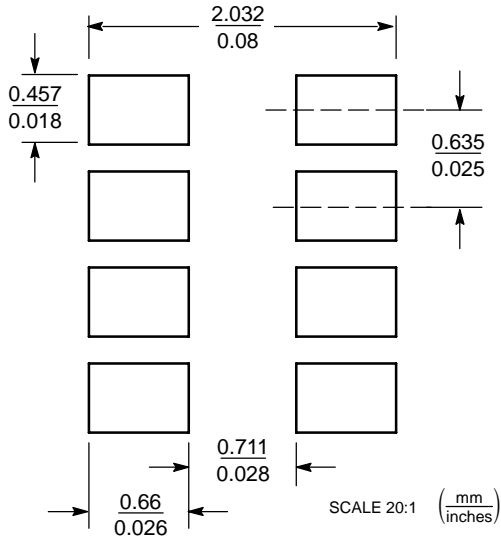
STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

NOTES:

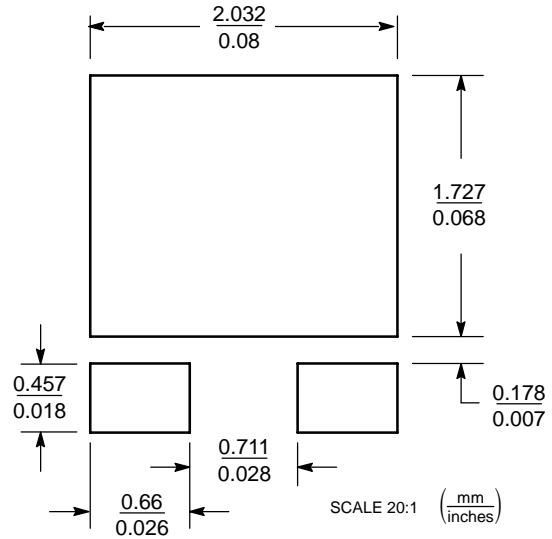
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.95 | 3.10 | 0.116 | 0.122 |
| B | 1.55 | 1.70 | 0.061 | 0.067 |
| C | 1.00 | 1.10 | 0.039 | 0.043 |
| D | 0.25 | 0.35 | 0.010 | 0.014 |
| G | 0.65 BSC | | 0.025 BSC | |
| J | 0.10 | 0.20 | 0.004 | 0.008 |
| K | 0.28 | 0.42 | 0.011 | 0.017 |
| L | 0.55 BSC | | 0.022 BSC | |
| M | 5° NOM | | 5° NOM | |
| S | 1.80 | 2.00 | 0.072 | 0.080 |

SOLDERING FOOTPRINT*



Basic



Style 4

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NSS35200CF8T1G

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