



**THE DATASHEET OF  
NSVMUN5332DW1T1G**



# MUN5332DW1, NSBC143EPDXV6, NSBC143EPDP6



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

## Complementary Bias Resistor Transistors R1 = 4.7 kΩ, R2 = 4.7 kΩ

### NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable\*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C both polarities Q<sub>1</sub> (PNP) & Q<sub>2</sub> (NPN), unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V <sub>CB0</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current – Continuous	I <sub>C</sub>	100	mAdc
Input Forward Voltage	V <sub>IN(fwd)</sub>	30	Vdc
Input Reverse Voltage	V <sub>IN(rev)</sub>	10	Vdc

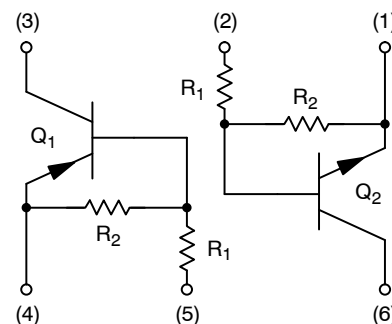
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### ORDERING INFORMATION

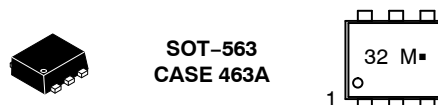
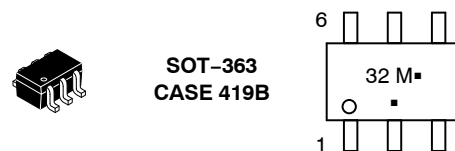
Device	Package	Shipping†
MUN5332DW1T1G, NSVMUN5332DW1T1G*	SOT-363	3,000/Tape & Reel
NSVMUN5332DW1T3G*	SOT-363	10,000/Tape & Reel
NSBC143EPDXV6T1G	SOT-563	4,000/Tape & Reel
NSBC143EPDP6T5G	SOT-963	8,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PIN CONNECTIONS



#### MARKING DIAGRAMS



32/V = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

# MUN5332DW1, NSBC143EPDXV6, NSBC143EPDP6

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
<b>MUN5332DW1 (SOT-363) ONE JUNCTION HEATED</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 31) (Note 32) Derate above $25^\circ\text{C}$ (Note 31) (Note 32)	$P_D$	187 256 1.5 2.0	mW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 31) (Note 32)	$R_{\theta JA}$	670 490	$^\circ\text{C/W}$
<b>MUN5332DW1 (SOT-363) BOTH JUNCTION HEATED (Note 33)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 31) (Note 32) Derate above $25^\circ\text{C}$ (Note 31) (Note 32)	$P_D$	250 385 2.0 3.0	mW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 31) (Note 32)	$R_{\theta JA}$	493 325	$^\circ\text{C/W}$
Thermal Resistance, Junction to Lead (Note 31) (Note 32)	$R_{\theta JL}$	188 208	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>NSBC143EPDXV6 (SOT-563) ONE JUNCTION HEATED</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 31) Derate above $25^\circ\text{C}$ (Note 31)	$P_D$	357 2.9	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 31)	$R_{\theta JA}$	350	$^\circ\text{C/W}$
<b>NSBC143EPDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 33)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 31) Derate above $25^\circ\text{C}$ (Note 31)	$P_D$	500 4.0	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 31)	$R_{\theta JA}$	250	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
<b>NSBC143EPDP6 (SOT-963) ONE JUNCTION HEATED</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 34) (Note 35) Derate above $25^\circ\text{C}$ (Note 34) (Note 35)	$P_D$	231 269 1.9 2.2	MW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 34) (Note 35)	$R_{\theta JA}$	540 464	$^\circ\text{C/W}$
<b>NSBC143EPDP6 (SOT-963) BOTH JUNCTION HEATED (Note 33)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 34) (Note 35) Derate above $25^\circ\text{C}$ (Note 34) (Note 35)	$P_D$	339 408 2.7 3.3	MW  mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 34) (Note 35)	$R_{\theta JA}$	369 306	$^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

31. FR-4 @ Minimum Pad.

32. FR-4 @ 1.0 x 1.0 Inch Pad.

33. Both junction heated values assume total power is sum of two equally powered channels.

34. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.

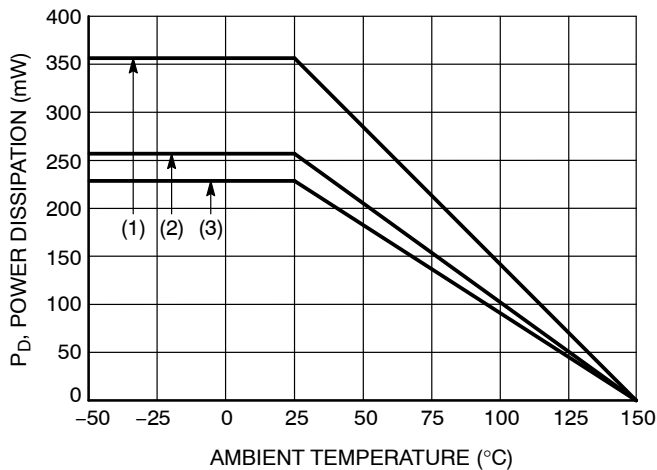
35. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces, still air.

# MUN5332DW1, NSBC143EPDXV6, NSBC143EPDP6

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ both polarities $Q_1$ (PNP) & $Q_2$ (NPN), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	-	-	100	nAdc
Collector-Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	-	-	500	nAdc
Emitter-Base Cutoff Current ( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	-	-	1.5	mAdc
Collector-Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 36) ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	-	-	Vdc
<b>ON CHARACTERISTICS</b>					
DC Current Gain (Note 36) ( $I_C = 5.0\text{ mA}$ , $V_{CE} = 10\text{ V}$ )	$h_{FE}$	15	30	-	
Collector-Emitter Saturation Voltage (Note 36) ( $I_C = 10\text{ mA}$ , $I_B = 1.0\text{ mA}$ )	$V_{CE(sat)}$	-	-	0.25	V
Input Voltage (Off) ( $V_{CE} = 5.0\text{ V}$ , $I_C = 100\ \mu\text{A}$ ) (NPN) ( $V_{CE} = 5.0\text{ V}$ , $I_C = 100\ \mu\text{A}$ ) (PNP)	$V_{i(off)}$	-	1.2	-	Vdc
Input Voltage (On) ( $V_{CE} = 0.2\text{ V}$ , $I_C = 20\text{ mA}$ ) (NPN) ( $V_{CE} = 0.2\text{ V}$ , $I_C = 20\text{ mA}$ ) (PNP)	$V_{i(on)}$	-	2.4	-	Vdc
Output Voltage (On) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OL}$	-	-	0.2	Vdc
Output Voltage (Off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.25\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OH}$	4.9	-	-	Vdc
Input Resistor	$R_1$	3.3	4.7	6.1	$\text{k}\Omega$
Resistor Ratio	$R_1/R_2$	0.8	1.0	1.2	

36. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle  $\leq$  2%.



- (1) SOT-363; 1.0 × 1.0 Inch Pad
- (2) SOT-563; Minimum Pad
- (3) SOT-963; 100 mm<sup>2</sup>, 1 oz. Copper Trace

Figure 77. Derating Curve

TYPICAL CHARACTERISTICS – NPN TRANSISTOR  
MUN5332DW1, NSBC143EPDXV6

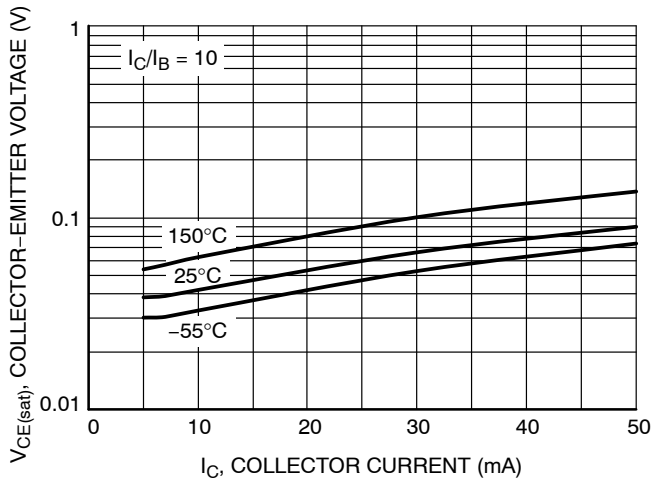


Figure 78.  $V_{CE(sat)}$ , vs.  $I_C$

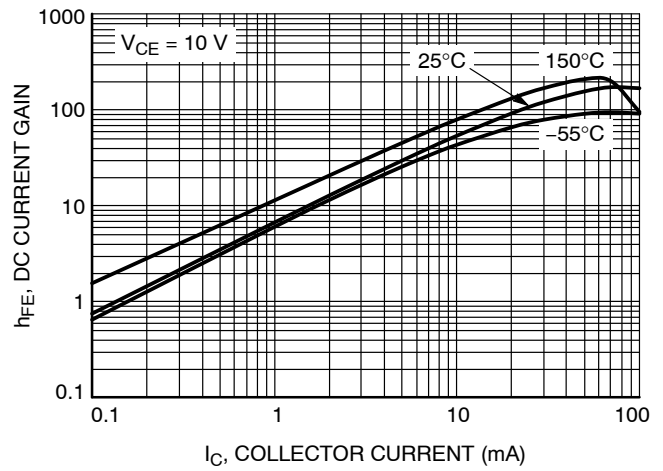


Figure 79. DC Current Gain

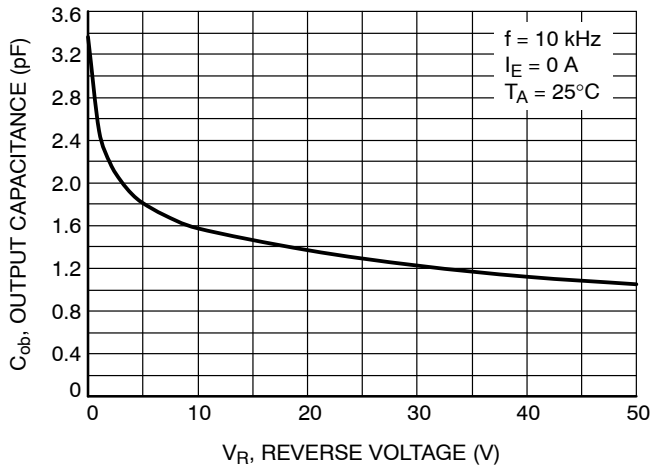


Figure 80. Output Capacitance

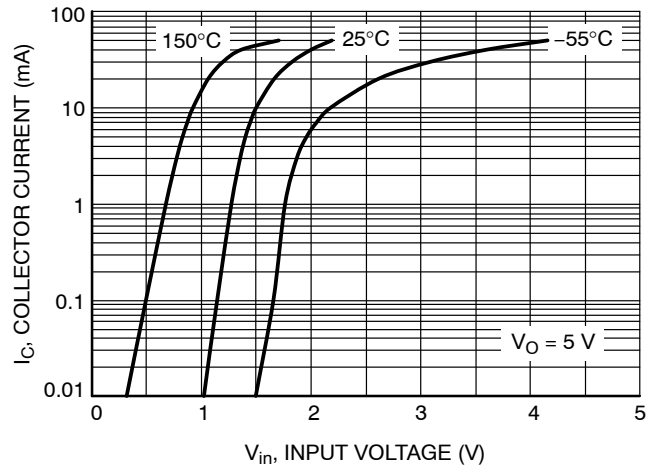


Figure 81. Output Current vs. Input Voltage

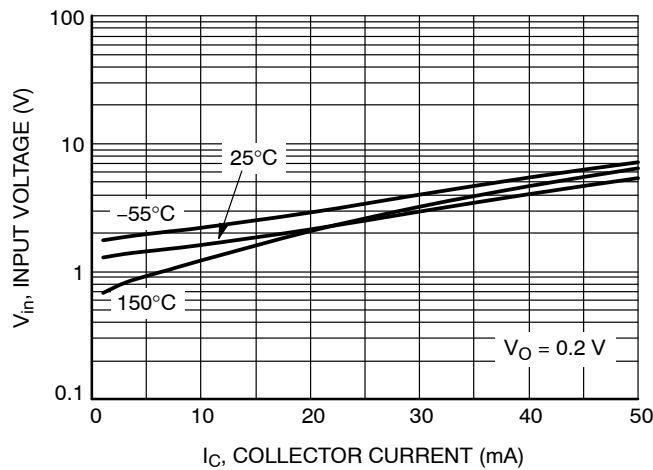


Figure 82. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR  
MUN5332DW1, NSBC143EPDXV6

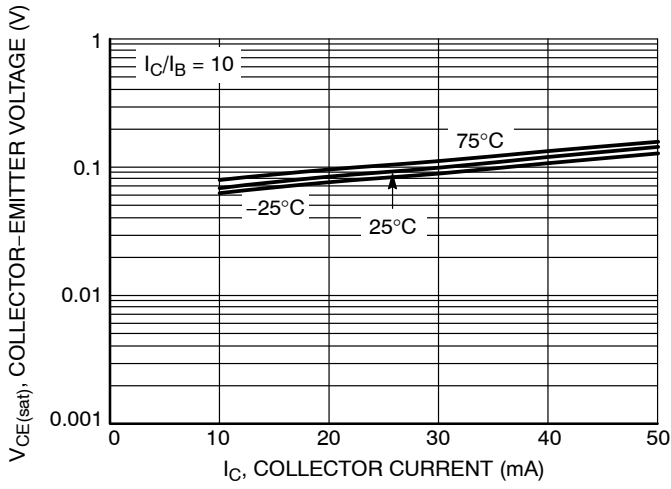


Figure 83.  $V_{CE(sat)}$  vs.  $I_C$

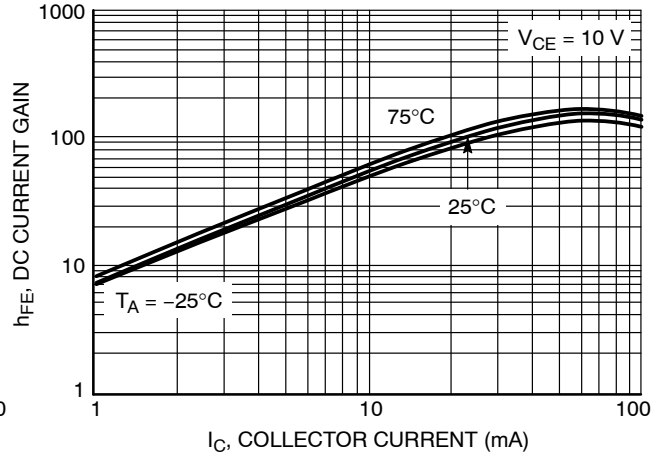


Figure 84. DC Current Gain

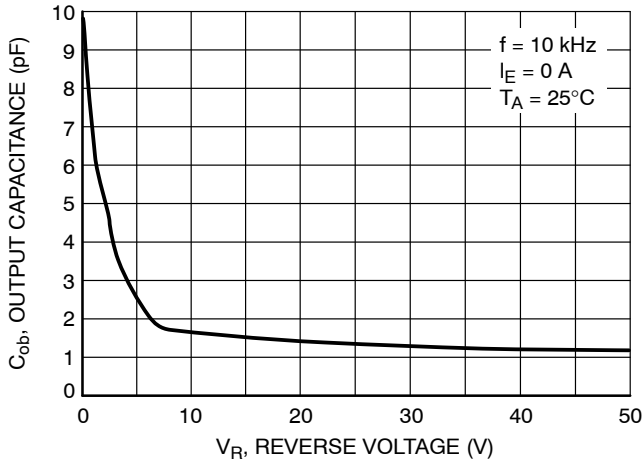


Figure 85. Output Capacitance

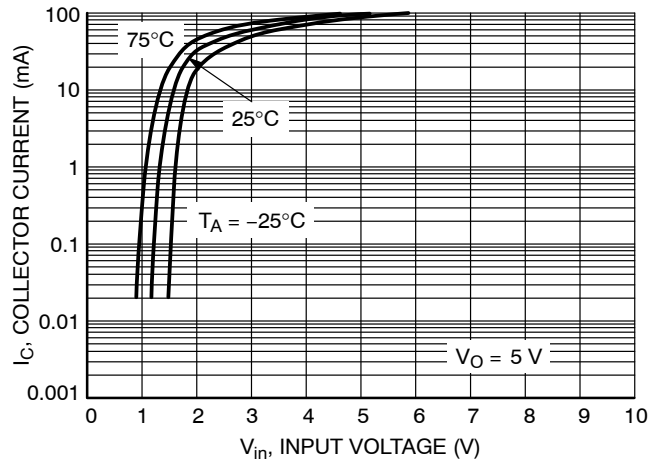


Figure 86. Output Current vs. Input Voltage

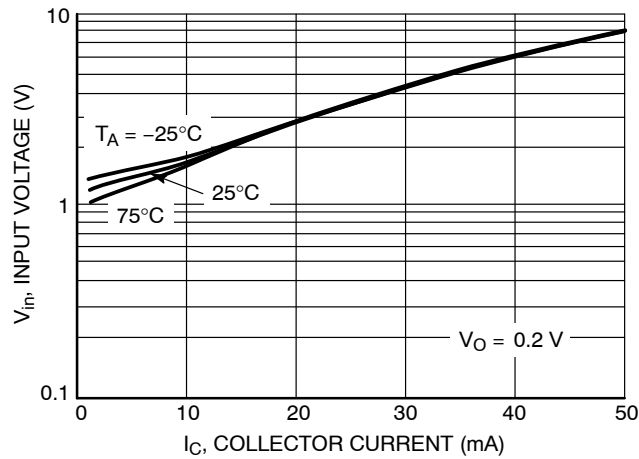


Figure 87. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – NPN TRANSISTOR  
NSBC143EPDP6

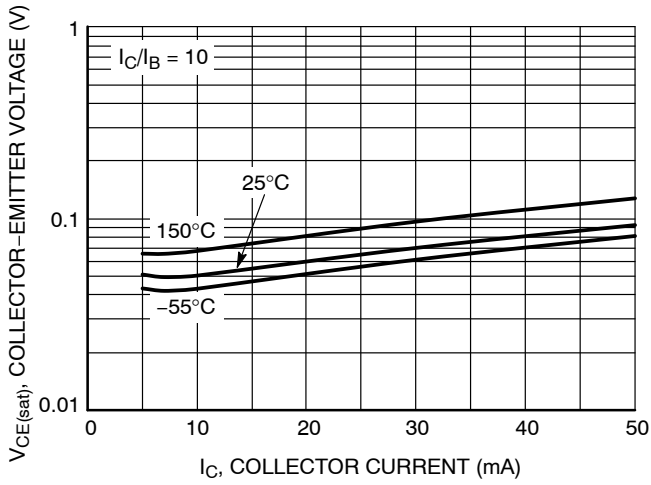


Figure 88.  $V_{CE(sat)}$ , vs.  $I_C$

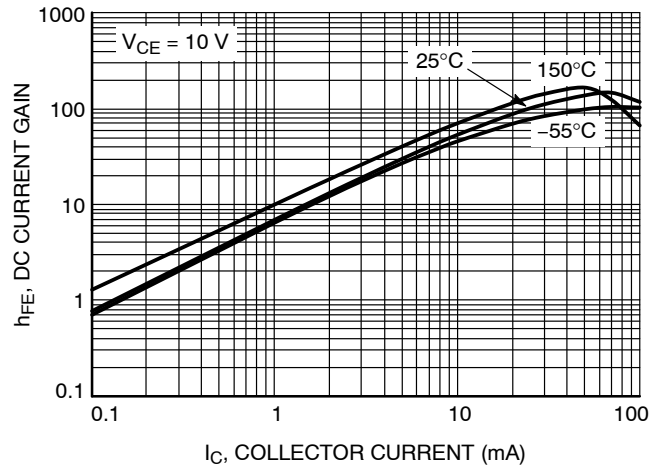


Figure 89. DC Current Gain

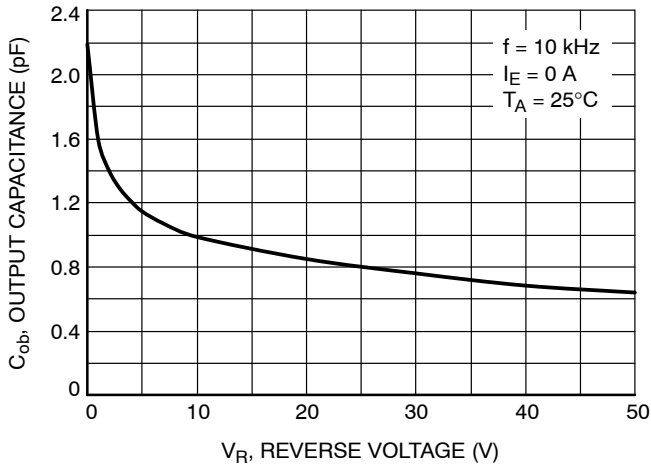


Figure 90. Output Capacitance

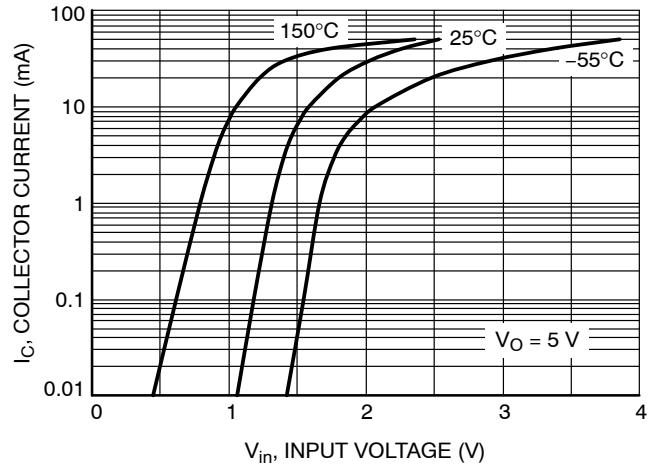


Figure 91. Output Current vs. Input Voltage

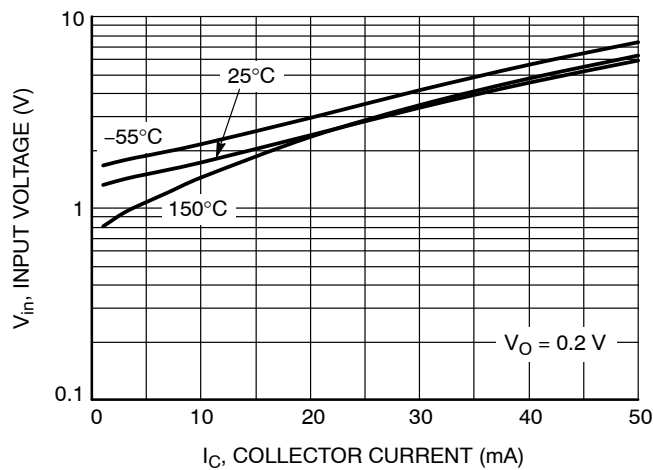


Figure 92. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR  
NSBC143EPDP6

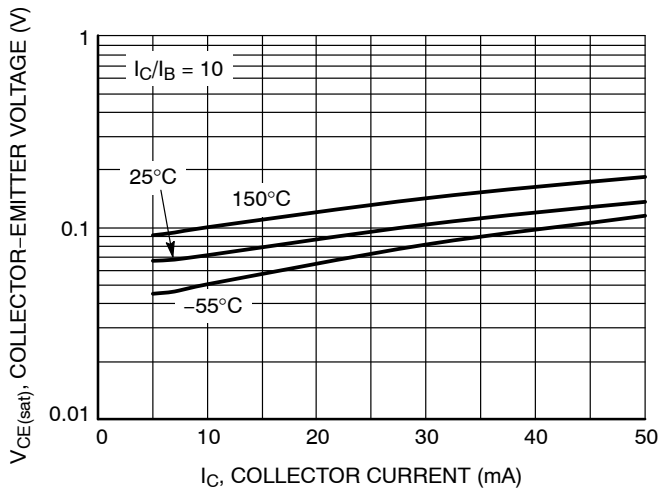


Figure 93.  $V_{CE(sat)}$  vs.  $I_C$

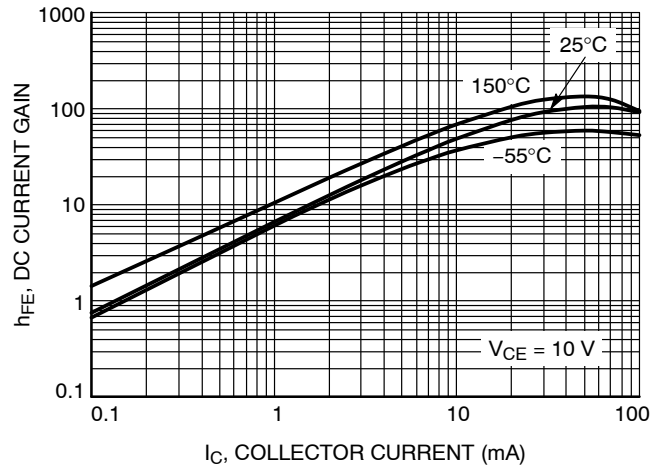


Figure 94. DC Current Gain

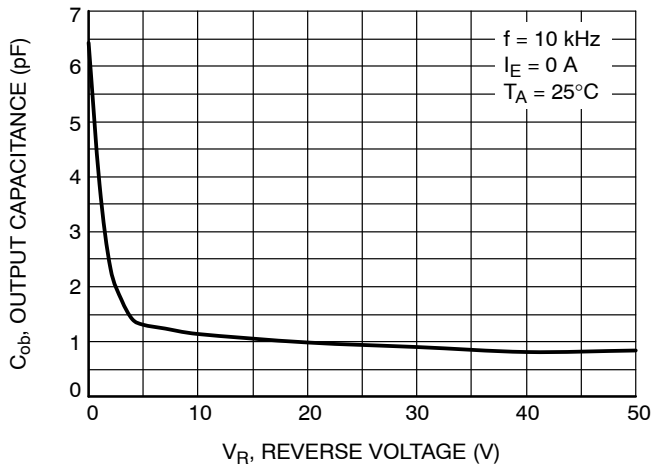


Figure 95. Output Capacitance

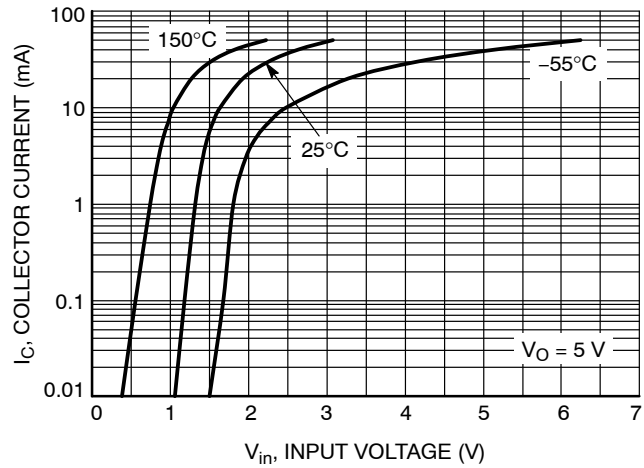


Figure 96. Output Current vs. Input Voltage

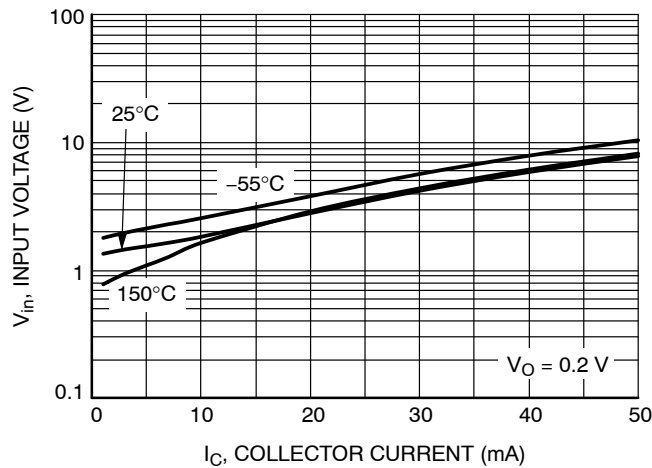
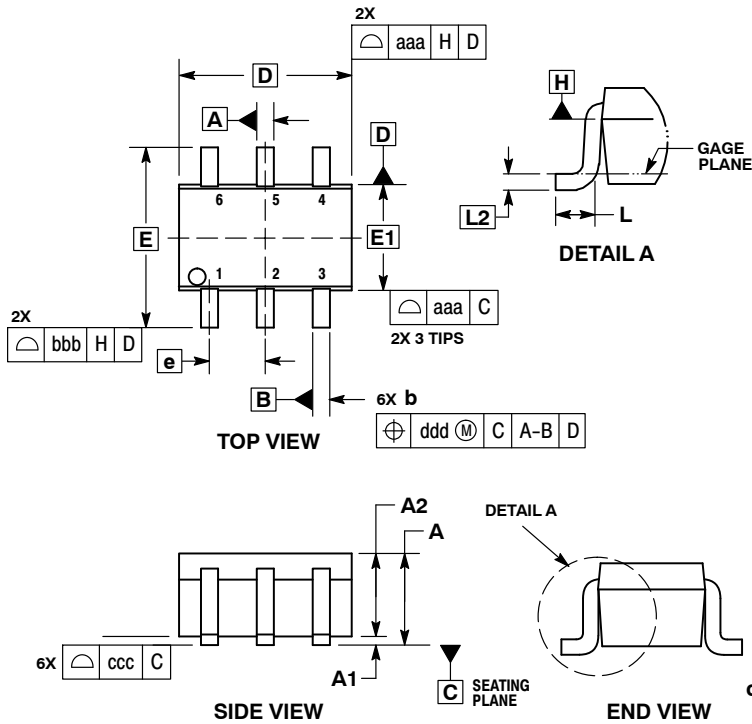


Figure 97. Input Voltage vs. Output Current

PACKAGE DIMENSIONS

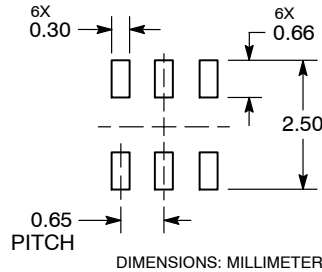
SC-88/SC70-6/SOT-363  
CASE 419B-02  
ISSUE Y



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

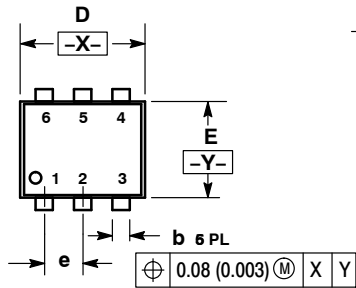
RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT-563, 6 LEAD  
CASE 463A  
ISSUE G

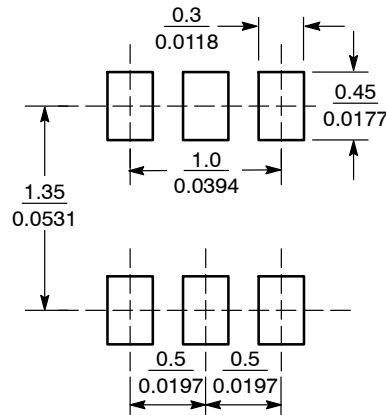


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H <sub>E</sub>	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT\*



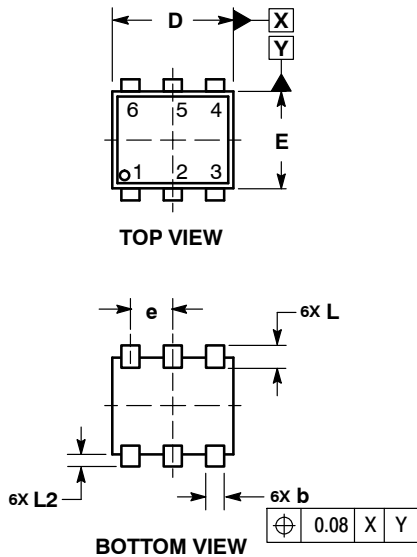
SCALE 20:1 ( $\frac{\text{mm}}{\text{inches}}$ )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MUN5332DW1, NSBC143EPDXV6, NSBC143EPDP6

## PACKAGE DIMENSIONS

**SOT-963**  
CASE 527AD  
ISSUE E

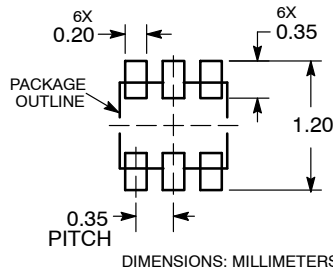


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
He	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

### RECOMMENDED MOUNTING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management