



THE DATASHEET OF
NTB125N02RT4



NTB125N02R, NTP125N02R

Power MOSFET 125 A, 24 V N-Channel TO-220, D²PAK

Features

- Planar HD3e Process for Fast Switching Performance
- Body Diode for Low t_{rr} and Q_{rr} and Optimized for Synchronous Operation
- Low C_{iss} to Minimize Driver Loss
- Optimized Q_{gd} and $R_{DS(on)}$ for Shoot-through Protection
- Low Gate Charge
- Pb-Free Packages are Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	24	V_{dc}
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V_{dc}
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	113.6	W
Drain Current –			
Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	125	A
Continuous @ $T_C = 25^\circ\text{C}$, Limited by Package	I_D	120.5	A
Continuous @ $T_A = 25^\circ\text{C}$, Limited by Wires	I_D	95	A
Single Pulse ($t_p = 10 \mu\text{s}$)	I_D	250	A
Thermal Resistance –			
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	46	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.72	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	18.6	A
Thermal Resistance –			
Junction-to-Ambient (Note 2)	$R_{\theta JA}$	63	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.98	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	15.9	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 V_{dc}$, $V_{GS} = 10 V_{dc}$, $I_L = 15.5 A_{pk}$, $L = 1 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	120	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1 inch pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).

PIN ASSIGNMENT

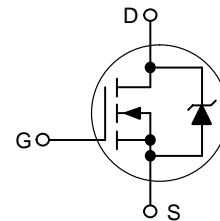
PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain



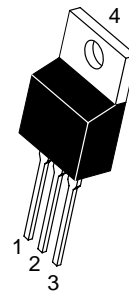
ON Semiconductor®

<http://onsemi.com>

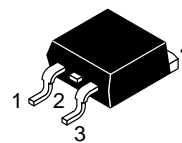
125 AMPERES, 24 VOLTS
 $R_{DS(on)} = 3.7 \text{ m}\Omega$ (Typ)



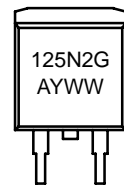
MARKING DIAGRAMS



TO-220AB
CASE 221A
STYLE 5



D²PAK
CASE 418AA
STYLE 2



125N2x = Device Code

x = R

A = Assembly Location

Y = Year

WW = Work Week

G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NTB125N02R, NTP125N02R

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 V _{dc} , I _D = 250 μA _{dc}) Temperature Coefficient (Positive)	V _{(BR)DSS}	25 –	28 15	– –	V _{dc} mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc}) (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc} , T _J = 125°C)	I _{DSS}	– –	– –	1.5 10	μA _{dc}
Gate-Body Leakage Current (V _{GS} = ±20 V _{dc} , V _{DS} = 0 V _{dc})	I _{GSS}	–	–	±100	nA _{dc}

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μA _{dc}) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.5 5.0	2.0 –	V _{dc} mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 V _{dc} , I _D = 110 A _{dc}) (V _{GS} = 4.5 V _{dc} , I _D = 55 A _{dc}) (V _{GS} = 10 V _{dc} , I _D = 20 A _{dc}) (V _{GS} = 4.5 V _{dc} , I _D = 20 A _{dc})	R _{DS(on)}	– – – –	3.7 4.9 3.7 4.7	– – 4.6 6.2	mΩ
Forward Transconductance (Note 3) (V _{DS} = 10 V _{dc} , I _D = 15 A _{dc})	g _{FS}	–	44	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 V _{dc} , V _{GS} = 0 V, f = 1 MHz)	C _{iss}	–	2710	3440	pF
Output Capacitance		C _{oss}	–	1105	1670	
Transfer Capacitance		C _{rss}	–	227	640	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 10 V _{dc} , V _{DD} = 10 V _{dc} , I _D = 40 A _{dc} , R _G = 3 Ω)	t _{d(on)}	–	11	22	ns
Rise Time		t _r	–	39	80	
Turn-Off Delay Time		t _{d(off)}	–	27	40	
Fall Time		t _f	–	21	40	
Gate Charge	(V _{GS} = 4.5 V _{dc} , I _D = 40 A _{dc} , V _{DS} = 10 V _{dc}) (Note 3)	Q _T	–	23.6	28	nC
		Q ₁	–	5.1	–	
		Q ₂	–	11	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 A _{dc} , V _{GS} = 0 V _{dc}) (Note 3) (I _S = 55 A _{dc} , V _{GS} = 0 V _{dc}) (I _S = 20 A _{dc} , V _{GS} = 0 V _{dc} , T _J = 125°C)	V _{SD}	– – –	0.82 0.99 0.65	1.2 – –	V _{dc}
Reverse Recovery Time	(I _S = 30 A _{dc} , V _{GS} = 0 V _{dc} , di _S /dt = 100 A/μs) (Note 3)	t _{rr}	–	36.5	–	ns
		t _a	–	17.7	–	
		t _b	–	18.8	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.024	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTP125N02R	TO-220AB	50 Units / Rail
NTP125N02RG	TO-220AB (Pb-Free)	50 Units / Rail
NTB125N02R	D ² PAK	50 Units / Rail
NTB125N02RG	D ² PAK (Pb-Free)	50 Units / Rail
NTB125N02RT4	D ² PAK	800 Units / Tape & Reel
NTB125N02RT4G	D ² PAK (Pb-Free)	800 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTB125N02R, NTP125N02R

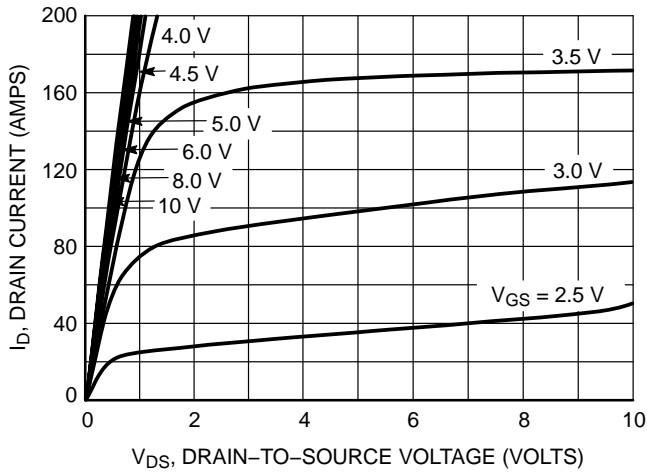


Figure 1. On-Region Characteristics

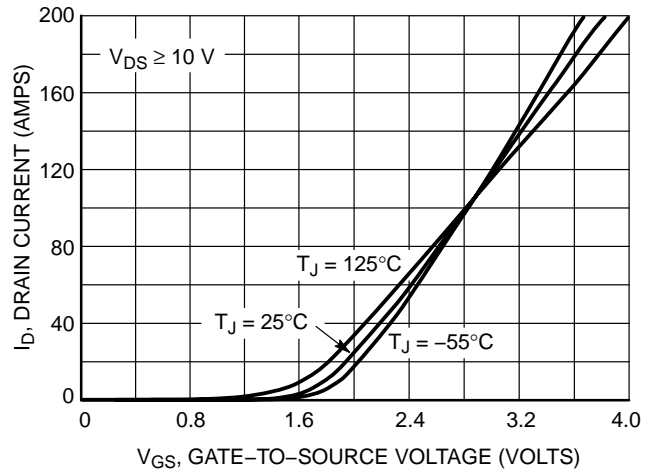


Figure 2. Transfer Characteristics

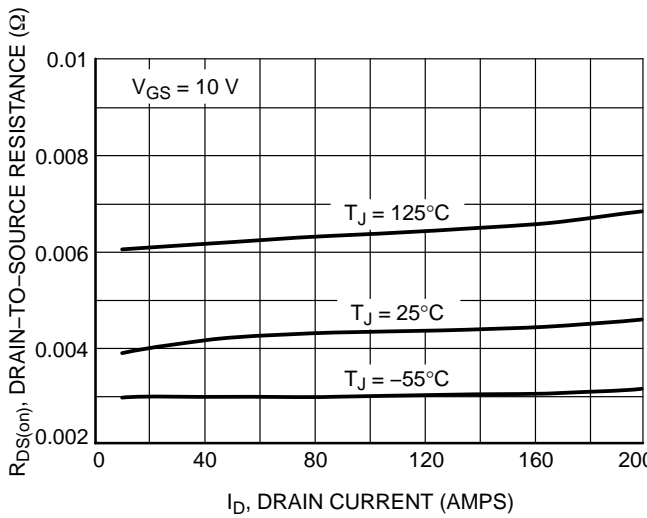


Figure 3. On-Resistance versus Drain Current and Temperature

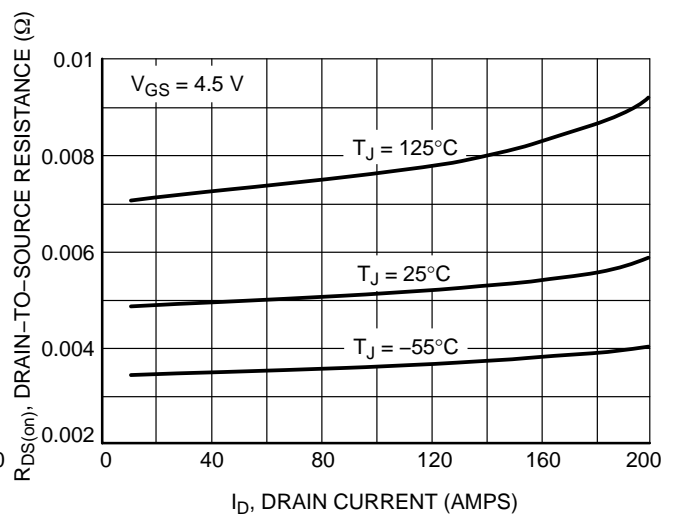


Figure 4. On-Resistance versus Drain Current and Temperature

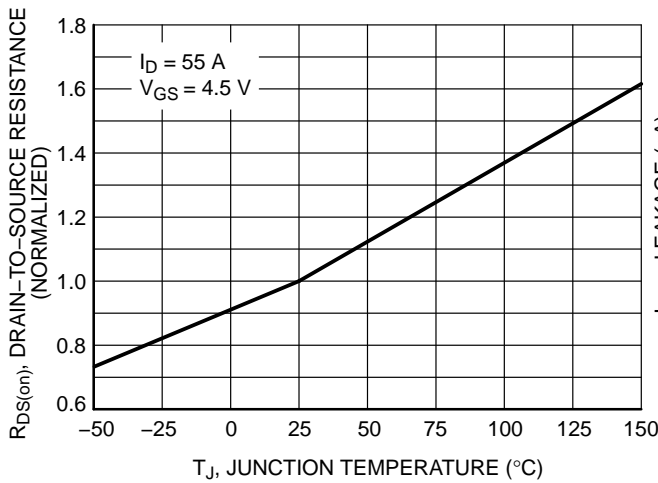


Figure 5. On-Resistance Variation with Temperature

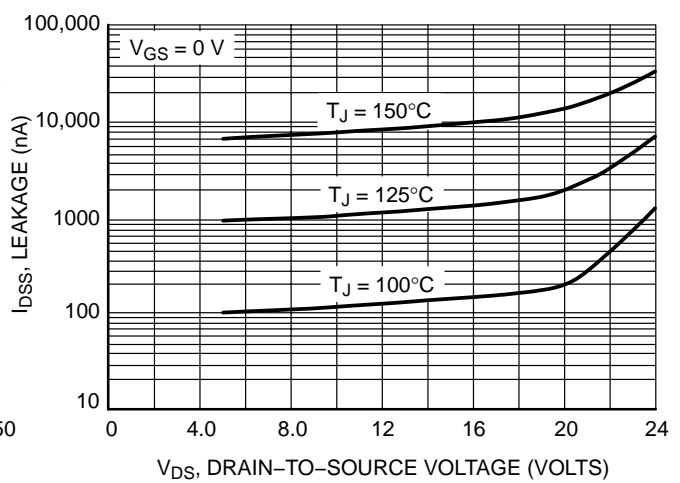


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTB125N02R, NTP125N02R

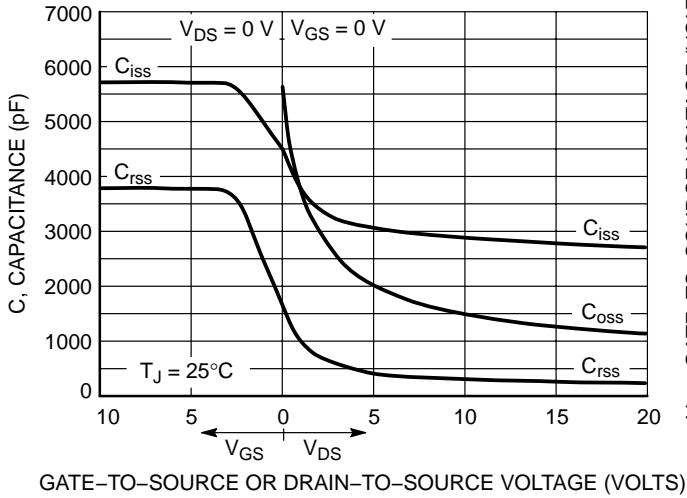


Figure 7. Capacitance Variation

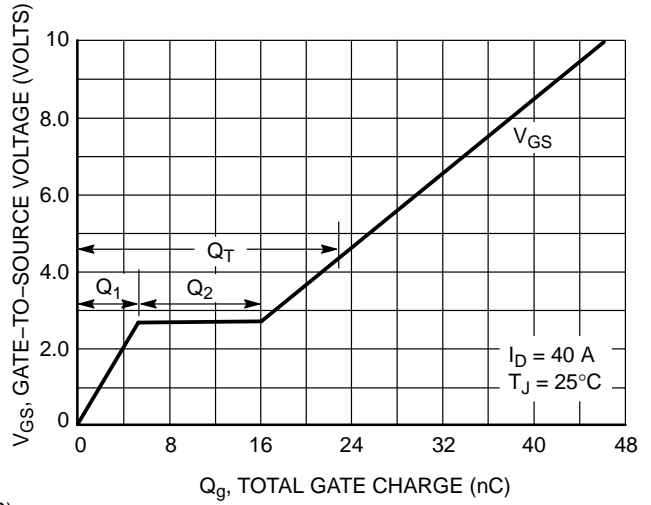


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

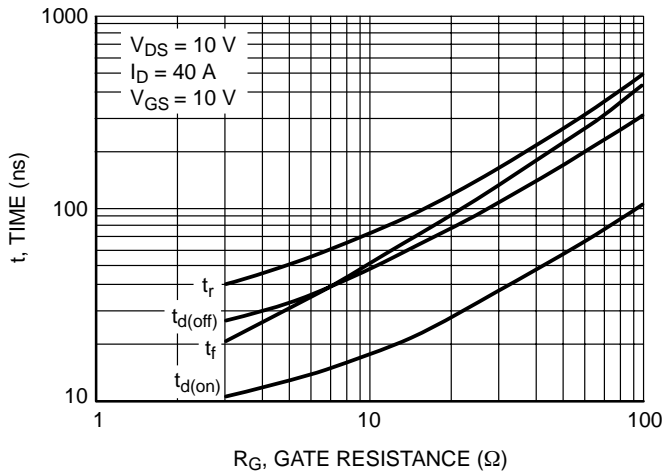


Figure 9. Resistive Switching Time Variation versus Gate Resistance

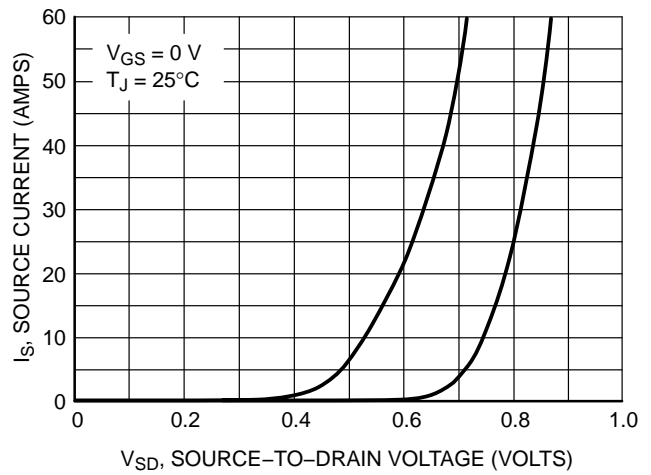


Figure 10. Diode Forward Voltage versus Current

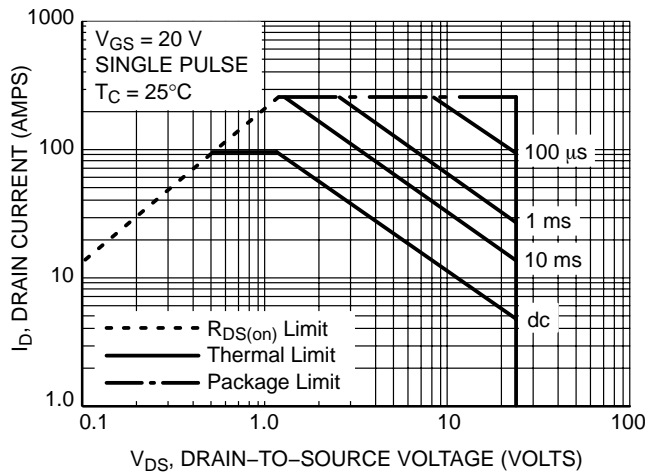


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTB125N02R, NTP125N02R

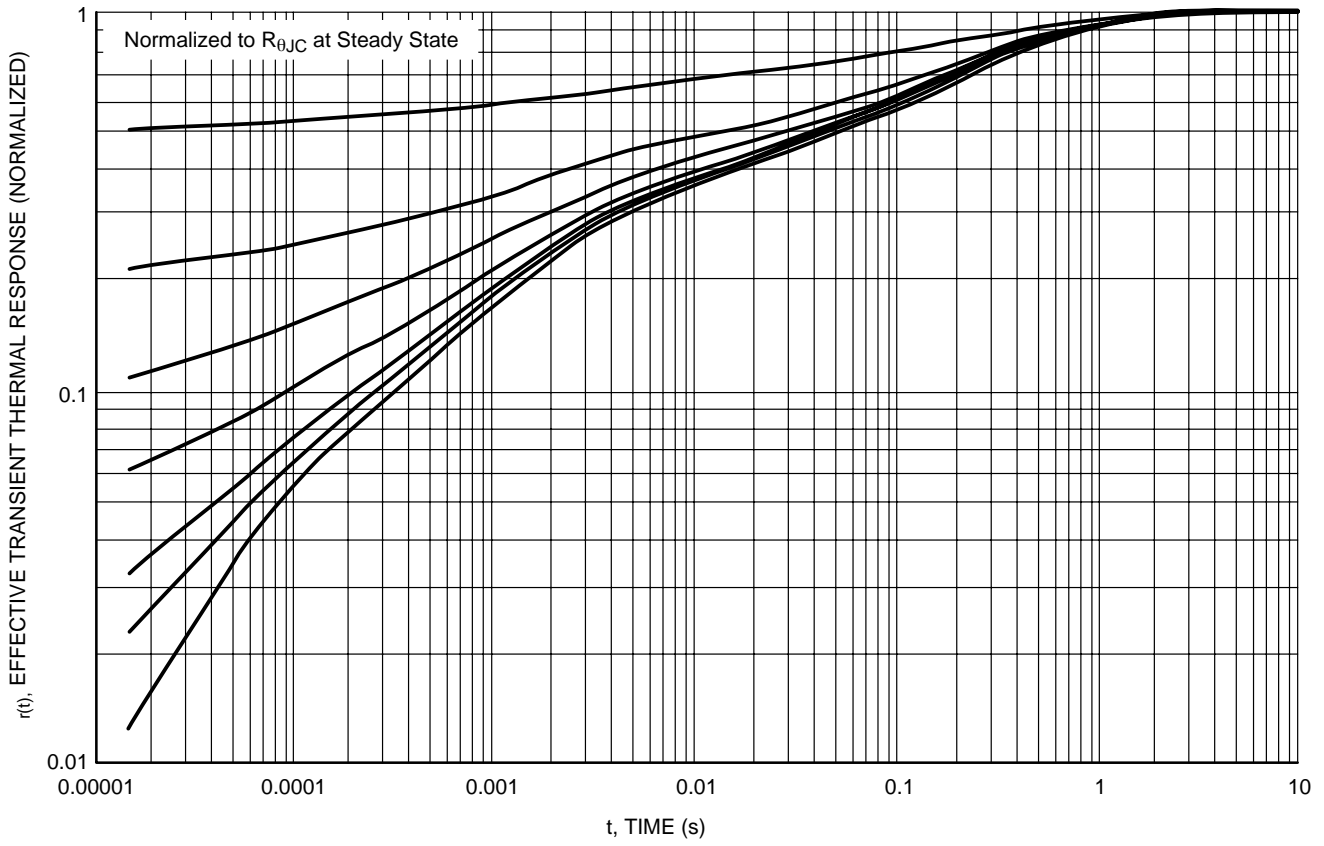
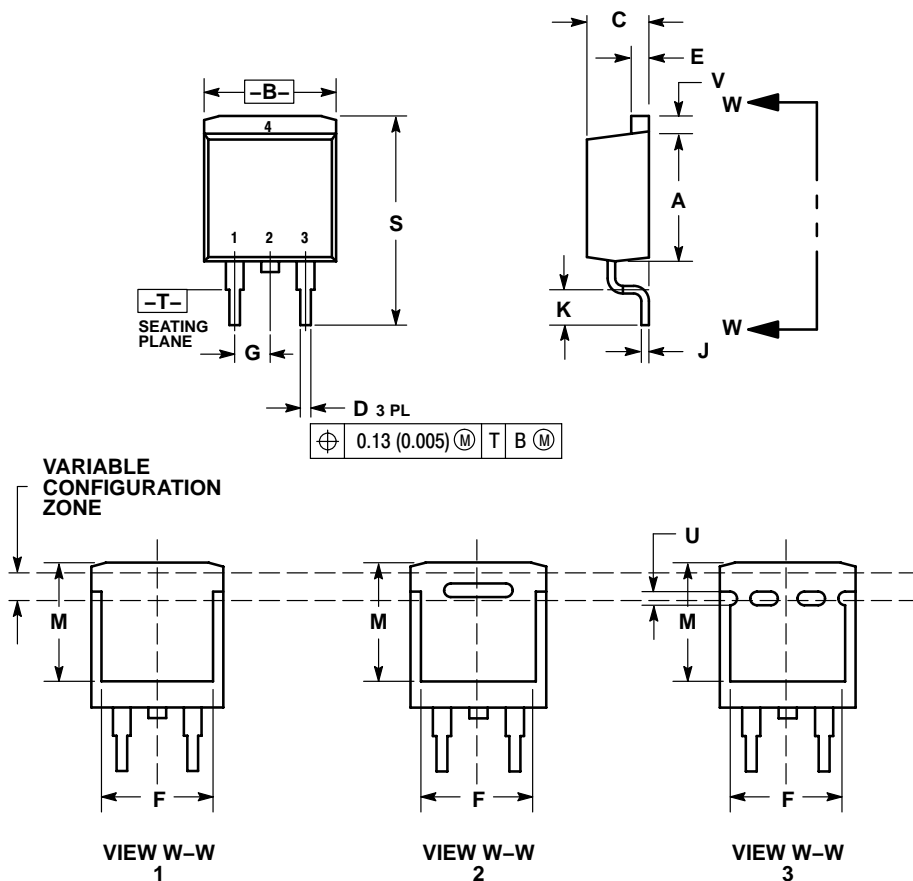


Figure 12. Thermal Response

NTB125N02R, NTP125N02R

PACKAGE DIMENSIONS

D²PAK
CASE 418AA-01
ISSUE O

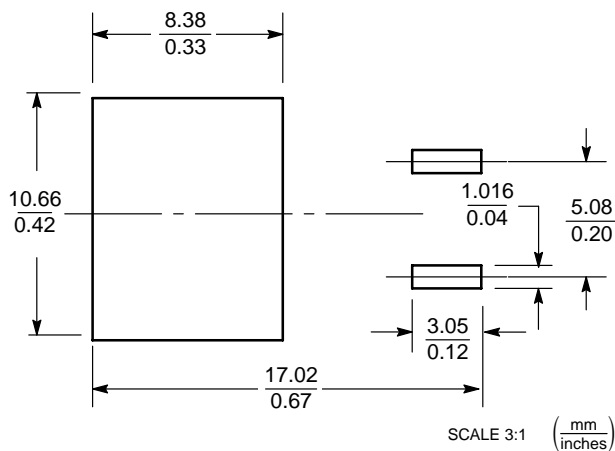


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	---	7.87	---
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	---	7.11	---
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*

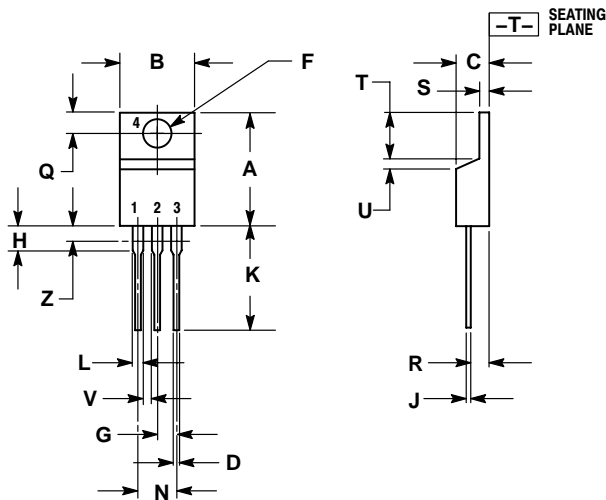


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTB125N02R, NTP125N02R

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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