



**THE DATASHEET OF
NTB65N02RT4**



NTB65N02R, NTP65N02R

Power MOSFET 65 A, 24 V N-Channel TO-220, D²PAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Pb-Free Packages are Available*

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	25	V_{dc}
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V_{dc}
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	2.0	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	62.5	W
Drain Current –			
Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	65	A
Continuous @ $T_C = 25^\circ\text{C}$, Limited by Package	I_D	58	A
Single Pulse ($t_p = 10 \mu\text{s}$)	I_{DM}	160	A
Thermal Resistance –			
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	67	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.86	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	10	A
Thermal Resistance –			
Junction-to-Ambient (Note 2)	$R_{\theta JA}$	120	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.04	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	7.6	A
Operating and Storage Temperature Range	T_J and T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 V_{dc}$, $V_{GS} = 10 V_{dc}$, $I_L = 11 A_{pk}$, $L = 1 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	60	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in. pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).

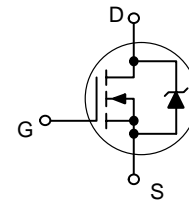
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



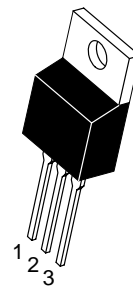
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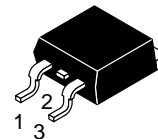
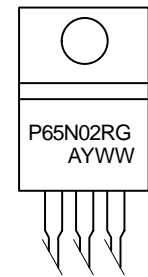
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	8.4 m Ω @ 10 V	65 A



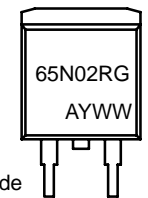
MARKING DIAGRAMS



TO-220AB
CASE 221A
STYLE 5



D²PAK
CASE 418AA
STYLE 2



65N02R = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

PIN ASSIGNMENT

PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 V _{dc} , I _D = 250 μA _{dc}) Temperature Coefficient (Positive)	V _{(BR)DSS}	24 –	27.5 25.5	– –	V _{dc} mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc}) (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc} , T _J = 150°C)	I _{DSS}	– –	– –	1.5 10	μA _{dc}
Gate-Body Leakage Current (V _{GS} = ±20 V _{dc} , V _{DS} = 0 V _{dc})	I _{GSS}	–	–	±100	nA _{dc}

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μA _{dc}) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.5 4.1	2.0 –	V _{dc} mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 4.5 V _{dc} , I _D = 15 A _{dc}) (V _{GS} = 10 V _{dc} , I _D = 20 A _{dc}) (V _{GS} = 10 V _{dc} , I _D = 30 A _{dc})	R _{DS(on)}	– – –	11.2 8.4 8.2	12.5 10.5 –	mΩ
Forward Transconductance (Note 3) (V _{DS} = 10 V _{dc} , I _D = 15 A _{dc})	g _{FS}	–	27	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 V _{dc} , V _{GS} = 0 V, f = 1 MHz)	C _{ISS}	–	948	1330	pF
Output Capacitance		C _{OSS}	–	456	640	
Transfer Capacitance		C _{rSS}	–	160	225	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 10 V _{dc} , V _{DD} = 10 V _{dc} , I _D = 30 A _{dc} , R _G = 3 Ω)	t _{d(on)}	–	7.0	–	ns
Rise Time		t _r	–	53	–	
Turn-Off Delay Time		t _{d(off)}	–	14	–	
Fall Time		t _f	–	10	–	
Gate Charge	(V _{GS} = 4.5 V _{dc} , I _D = 30 A _{dc} , V _{DS} = 10 V _{dc}) (Note 3)	Q _T	–	9.5	–	nC
		Q ₁	–	3.0	–	
		Q ₂	–	4.4	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 A _{dc} , V _{GS} = 0 V _{dc}) (Note 3) (I _S = 30 A _{dc} , V _{GS} = 0 V _{dc}) (I _S = 15 A _{dc} , V _{GS} = 0 V _{dc} , T _J = 125°C)	V _{SD}	– – –	0.88 1.10 0.80	1.2 – –	V _{dc}
Reverse Recovery Time	(I _S = 30 A _{dc} , V _{GS} = 0 V _{dc} , dI _S /dt = 100 A/μs) (Note 3)	t _{rr}	–	29.1	–	ns
		t _a	–	13.6	–	
		t _b	–	15.5	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.02	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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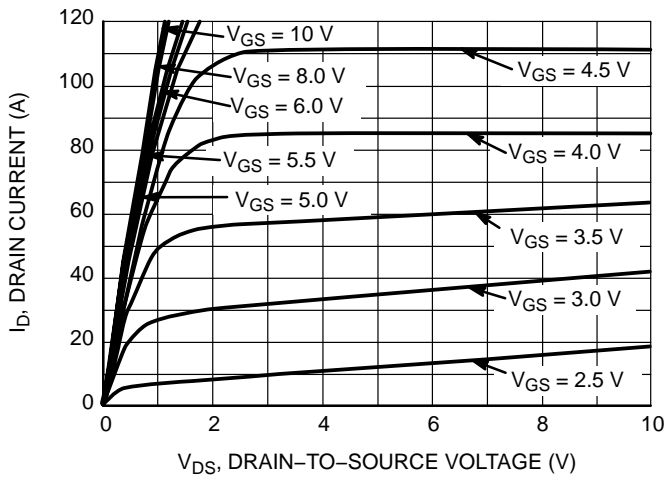


Figure 1. On-Region Characteristics

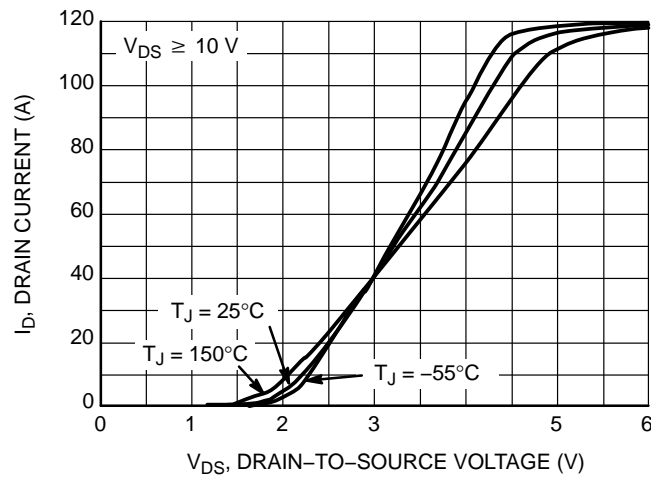


Figure 2. Transfer Characteristics

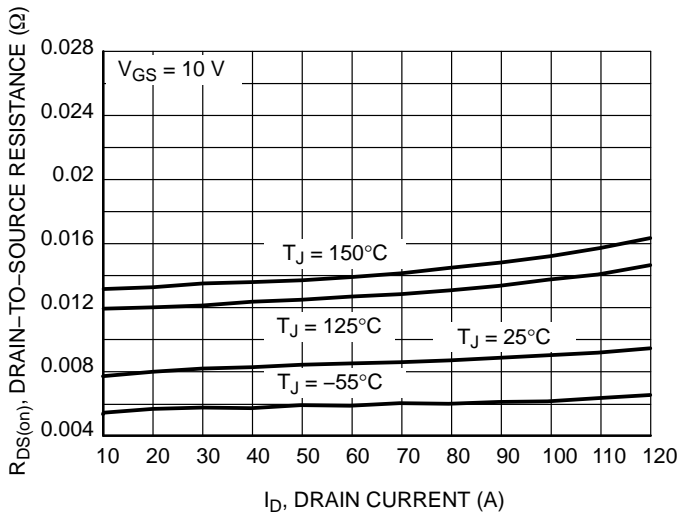


Figure 3. On-Resistance versus Drain Current and Temperature

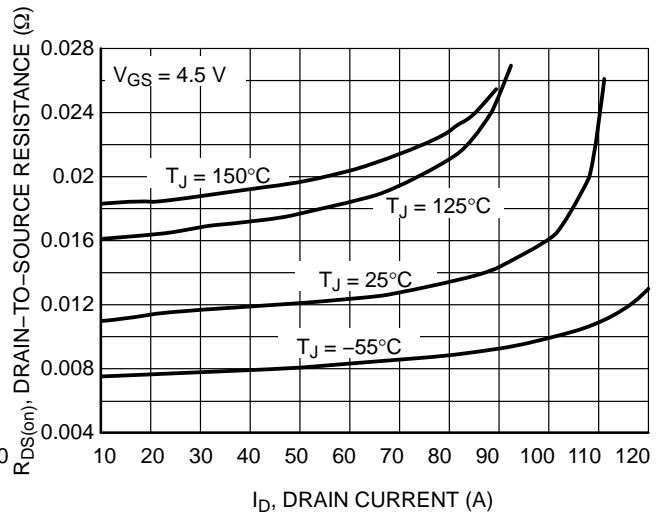


Figure 4. On-Resistance versus Drain Current and Temperature

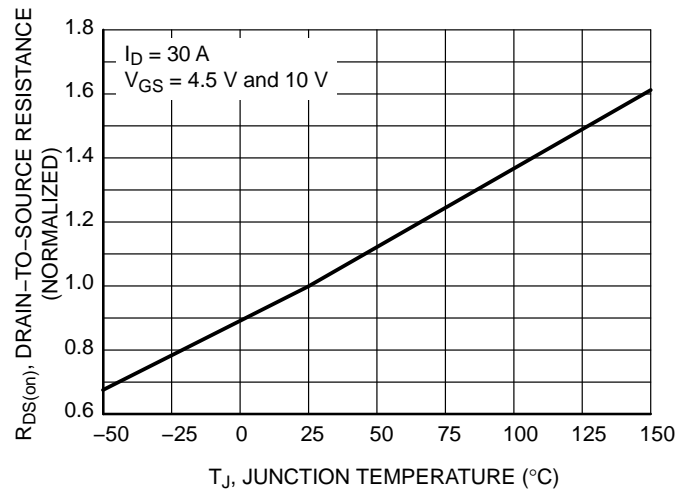


Figure 5. On-Resistance Variation with Temperature

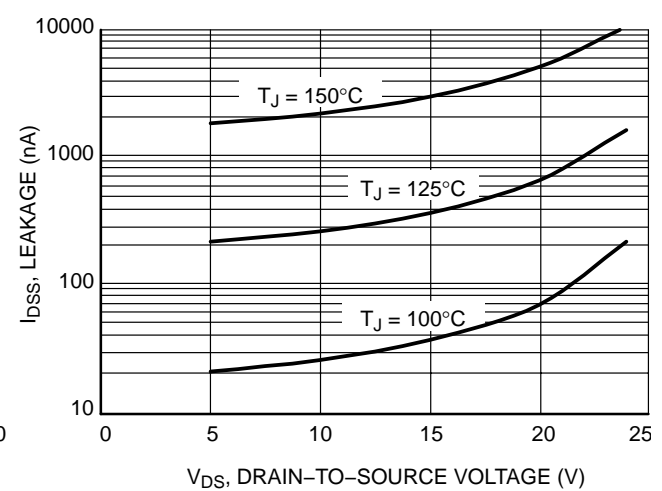


Figure 6. Drain-to-Source Leakage Current versus Voltage

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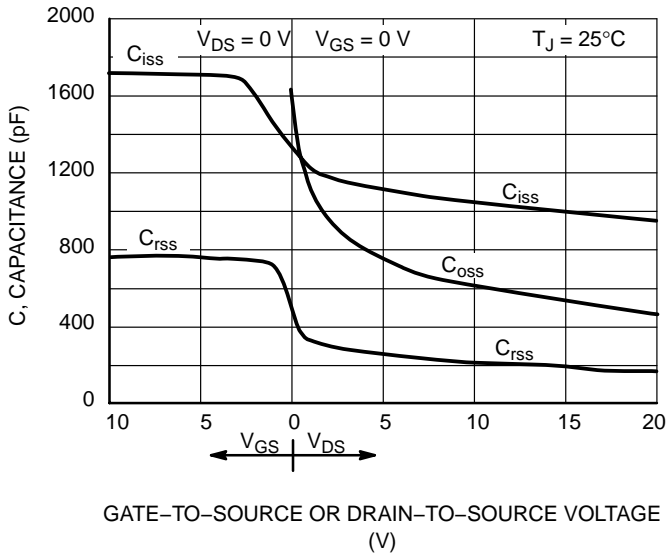


Figure 7. Capacitance Variation

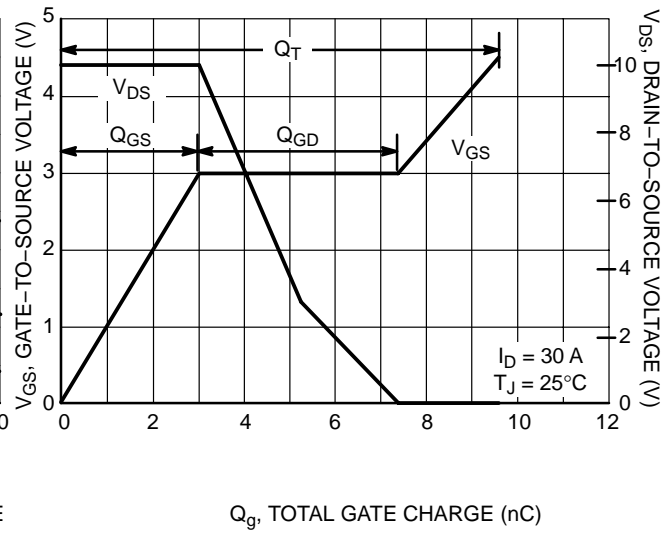


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

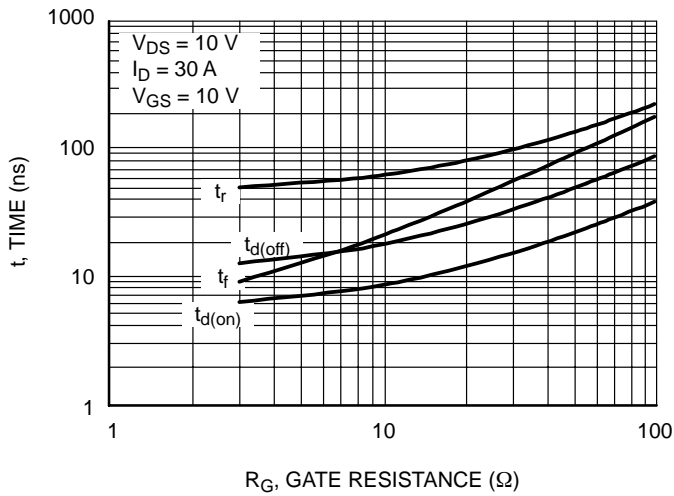


Figure 9. Resistive Switching Time Variation versus Gate Resistance

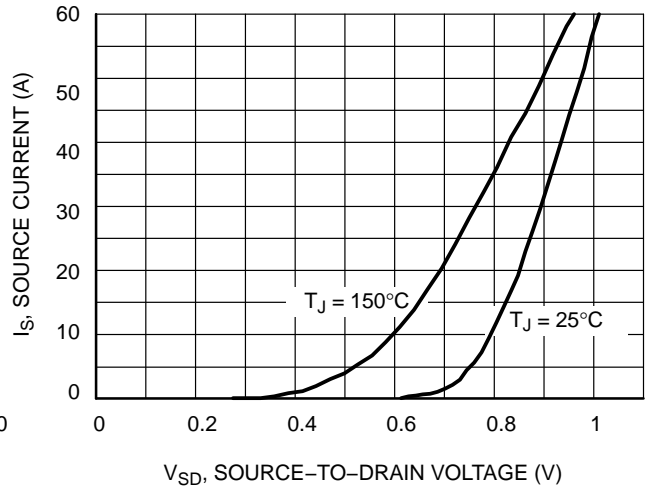


Figure 10. Diode Forward Voltage versus Current

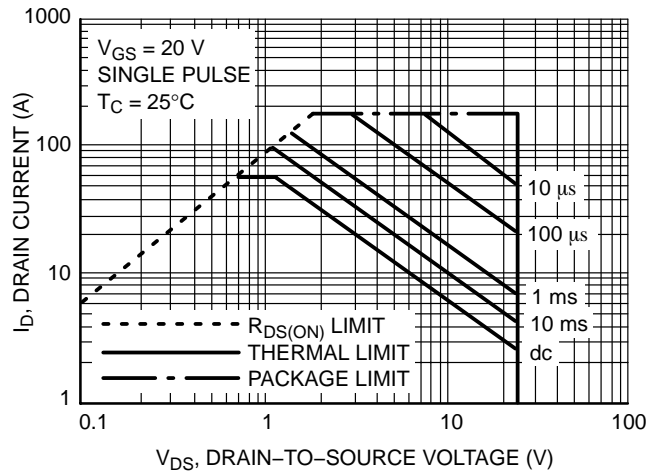


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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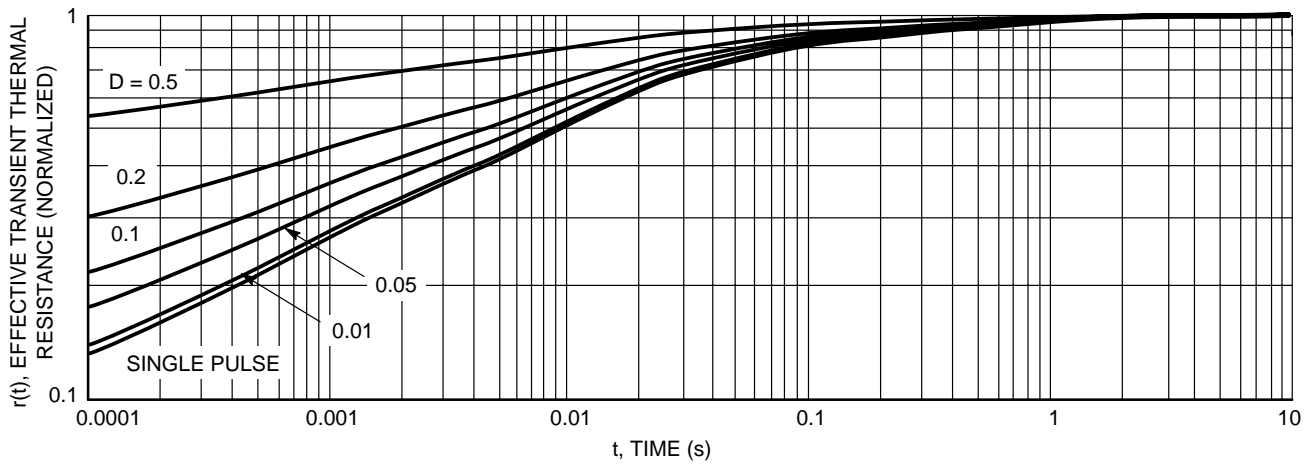


Figure 12. Thermal Response

ORDERING INFORMATION

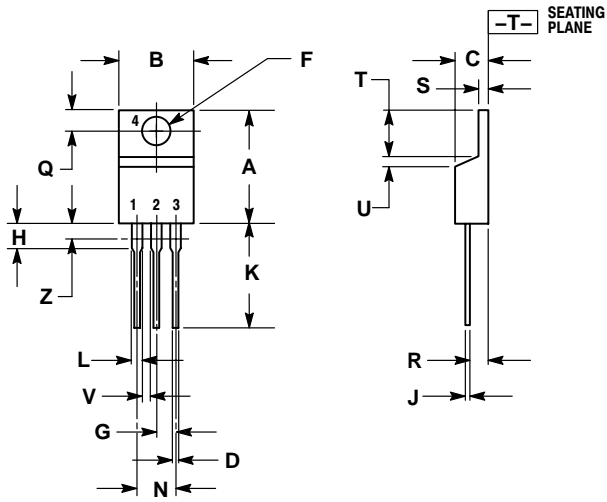
Device	Package	Shipping†
NTB65N02R	D ² PAK	50 Units / Rail
NTB65N02RG	D ² PAK (Pb-Free)	50 Units / Rail
NTB65N02RT4	D ² PAK	800 / Tape & Reel
NTB65N02RT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NTP65N02R	TO-220AB	50 Units / Rail
NTP65N02RG	TO-220AB (Pb-Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTB65N02R, NTP65N02R

PACKAGE DIMENSIONS

TO-220AB
CASE 221A-09
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

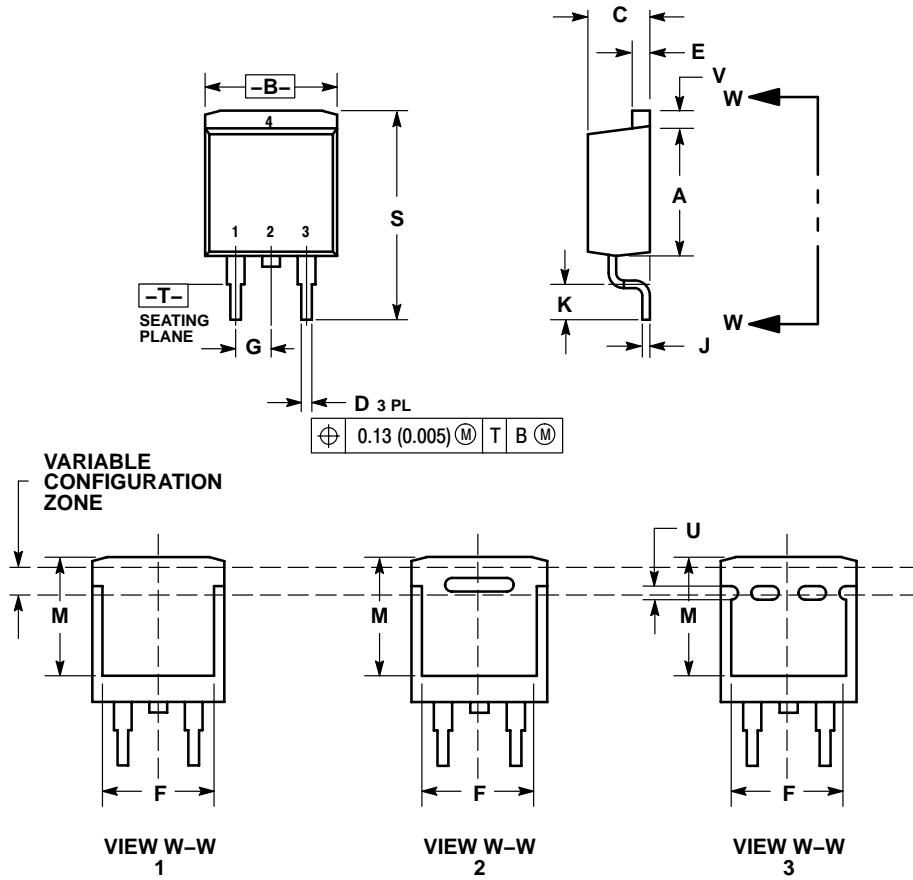
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NTB65N02R, NTP65N02R

PACKAGE DIMENSIONS

D²PAK
CASE 418AA-01
ISSUE O

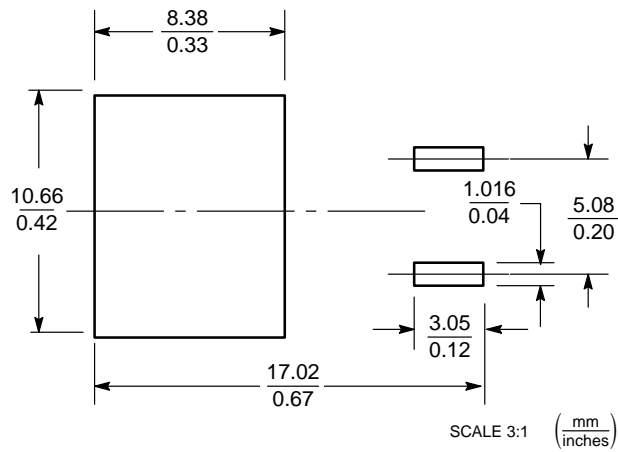


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	---	7.87	---
G	0.100 BSC	---	2.54 BSC	---
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	---	7.11	---
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40


- STYLE 2:
1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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