



**THE DATASHEET OF
NTD60N02R-035**



NTD60N02R

Power MOSFET

62 A, 25 V, N-Channel, DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- Pb-Free Packages are Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	25	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	2.6	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	58	W
Drain Current	I_D	62	A
Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	50	A
Continuous @ $T_C = 25^\circ\text{C}$, Limited by Package	I_D	32	A
Continuous @ $T_A = 25^\circ\text{C}$, Limited by Wires	I_D	32	A
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.87	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	10.5	A
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	120	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	8.5	A
Operating and Storage Temperature	T_J , and T_{stg}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50$ Vdc, $V_{GS} = 10.0$ Vdc, $I_L = 11$ Apk, $L = 1.0$ mH, $R_G = 25$ Ω)	E_{AS}	60	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

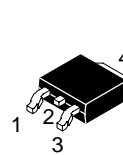
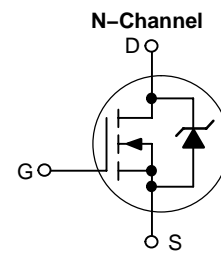
1. When surface mounted to an FR4 board using 0.5 in sq drain pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.



ON Semiconductor®

<http://onsemi.com>

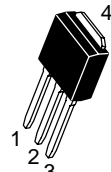
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	8.4 m Ω @ 10 V	62 A



CASE 369AA
DPAK
(Surface Mount)
STYLE 2

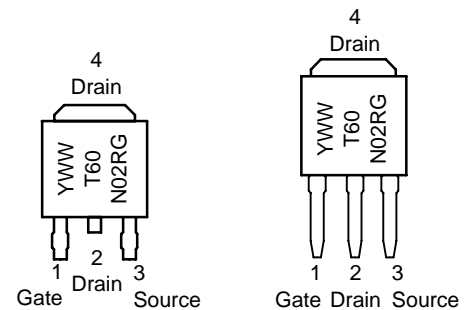


CASE 369AC
3 IPAK
(Straight Lead)
STYLE 2



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



Y = Year
WW = Work Week
T60N02R = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD60N02R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	25 –	27.5 25.5	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.5 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.5 4.1	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 4.5 Vdc, I _D = 15 Adc) (V _{GS} = 10 Vdc, I _D = 20 Adc) (V _{GS} = 10 Vdc, I _D = 31 Adc)	R _{DS(on)}	– – –	11.2 8.4 8.2	12.5 10.5 –	mΩ
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 15 Adc) (Note 3)	g _{FS}	–	27	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	1000	1330	pF
Output Capacitance		C _{oss}	–	480	640	
Transfer Capacitance		C _{rss}	–	180	225	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 10 Vdc, V _{DD} = 10 Vdc, I _D = 31 Adc, R _G = 3.0 Ω)	t _{d(on)}	–	7.0	–	ns
Rise Time		t _r	–	33	–	
Turn-Off Delay Time		t _{d(off)}	–	19	–	
Fall Time		t _f	–	9.0	–	
Gate Charge	(V _{GS} = 4.5 Vdc, I _D = 31 Adc, V _{DS} = 10 Vdc) (Note 3)	Q _T	–	9.5	14	nC
		Q _{GS}	–	2.2	–	
		Q _{GD}	–	5.0	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 31 Adc, V _{GS} = 0 Vdc) (I _S = 15 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	– – –	0.88 1.15 0.80	1.2 – –	Vdc
Reverse Recovery Time	(I _S = 31 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 3)	t _{rr}	–	29.1	–	ns
		t _a	–	13.6	–	
		t _b	–	15.5	–	
Reverse Recovery Stored Charge		Q _{rr}	–	0.02	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTD60N02R

TYPICAL CHARACTERISTICS

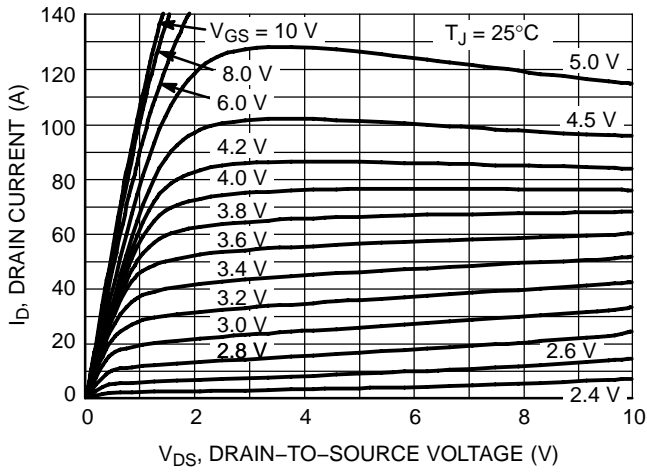


Figure 1. On-Region Characteristics

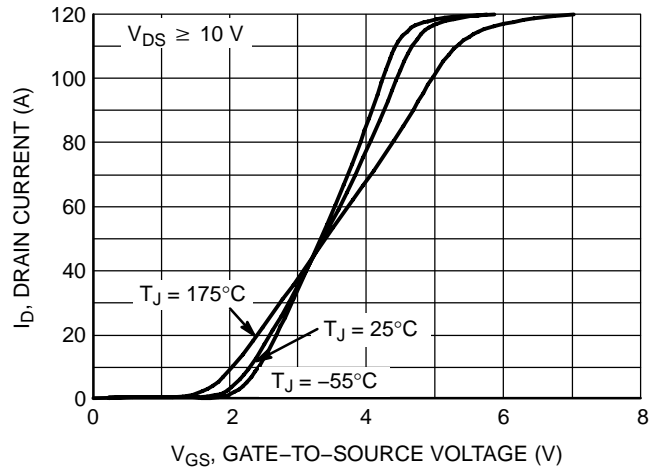


Figure 2. Transfer Characteristics

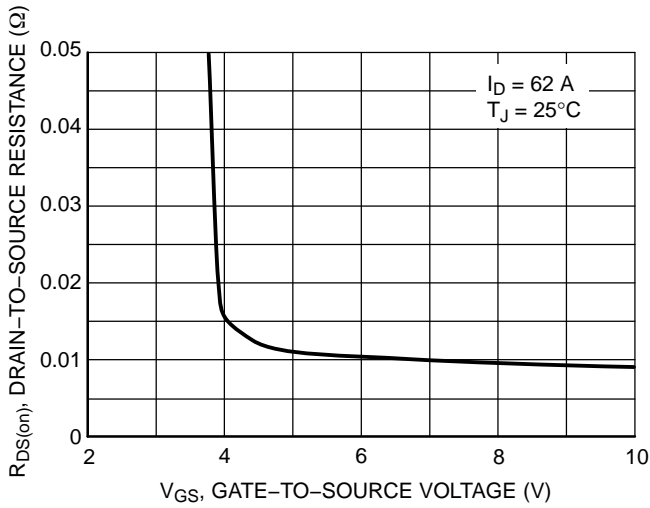


Figure 3. On-Resistance versus Gate-to-Source Voltage

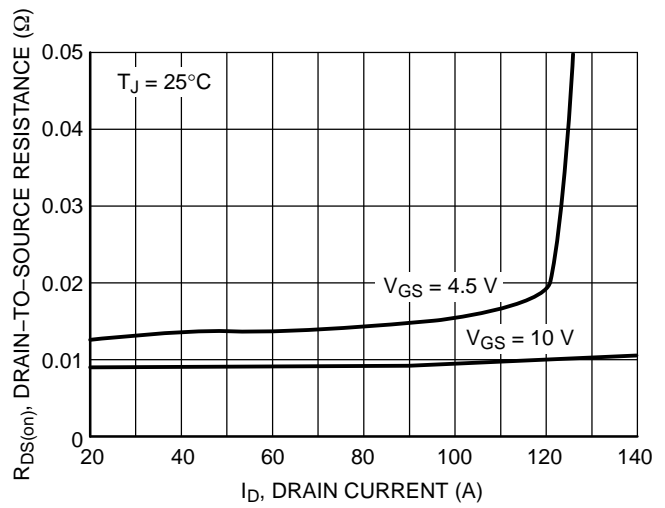


Figure 4. On-Resistance versus Drain Current and Gate Voltage

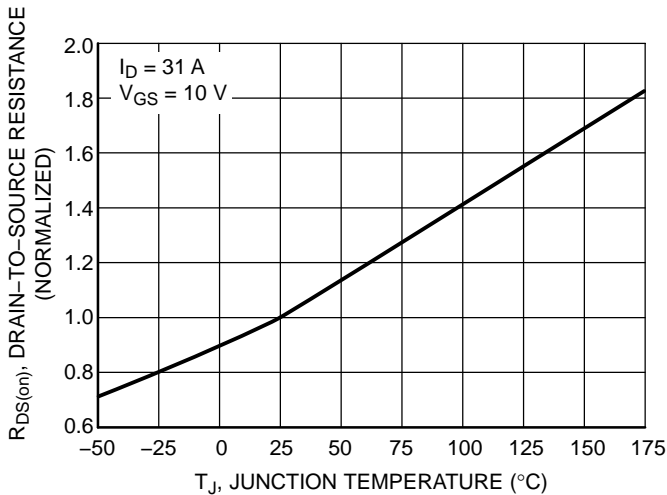


Figure 5. On-Resistance Variation with Temperature

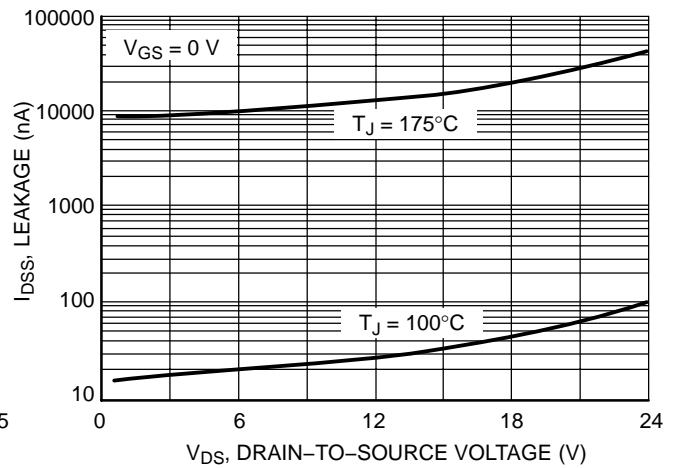


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD60N02R

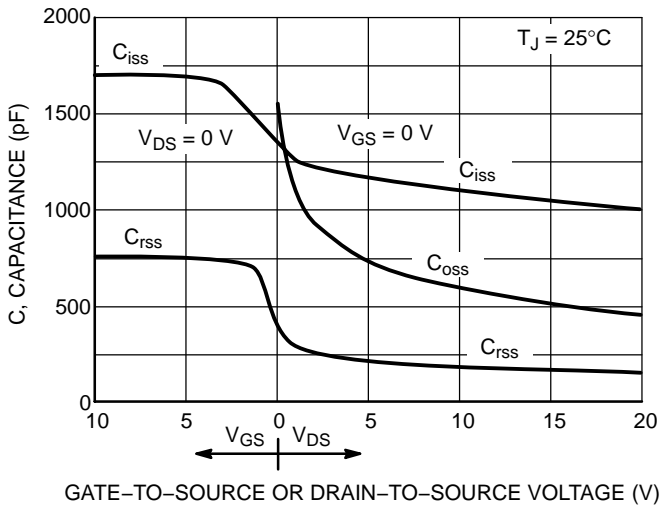


Figure 7. Capacitance Variation

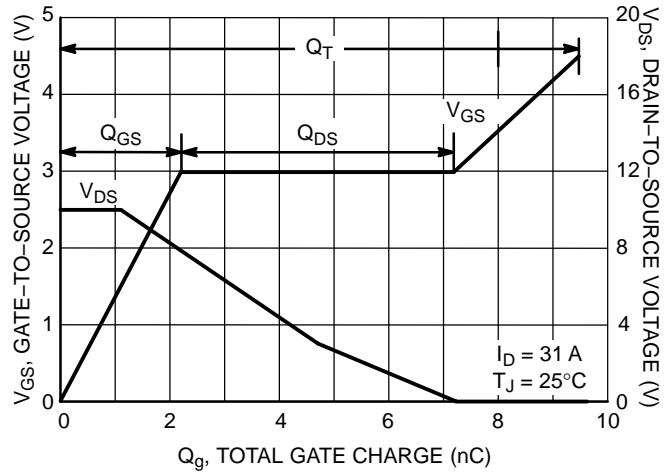


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

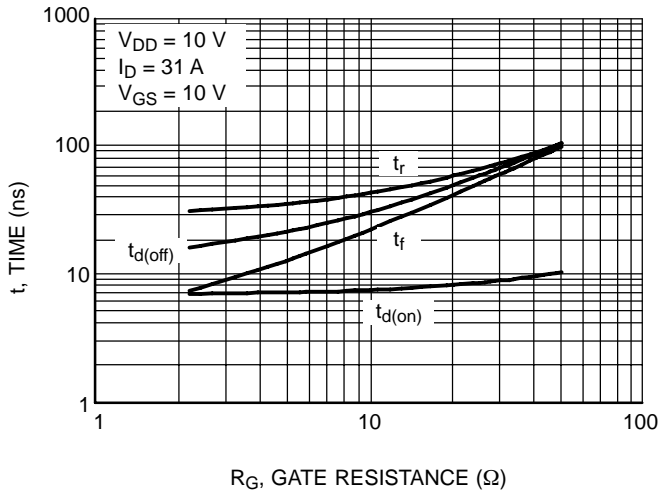


Figure 9. Resistive Switching Time Variation versus Gate Resistance

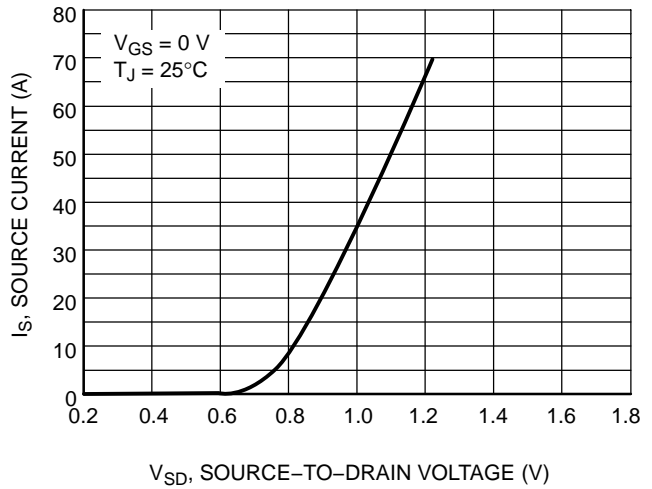


Figure 10. Diode Forward Voltage versus Current

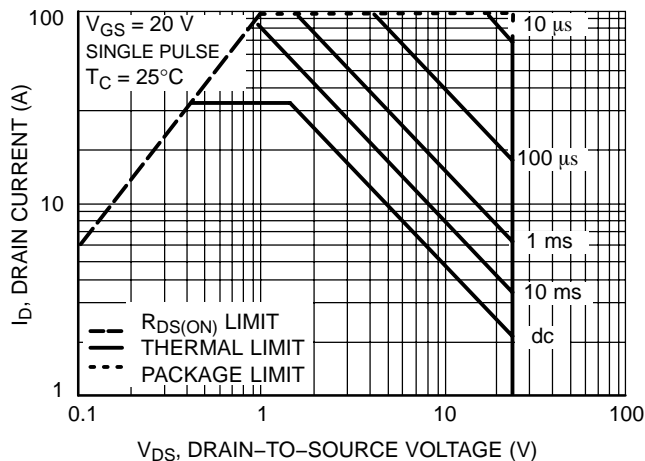


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD60N02R

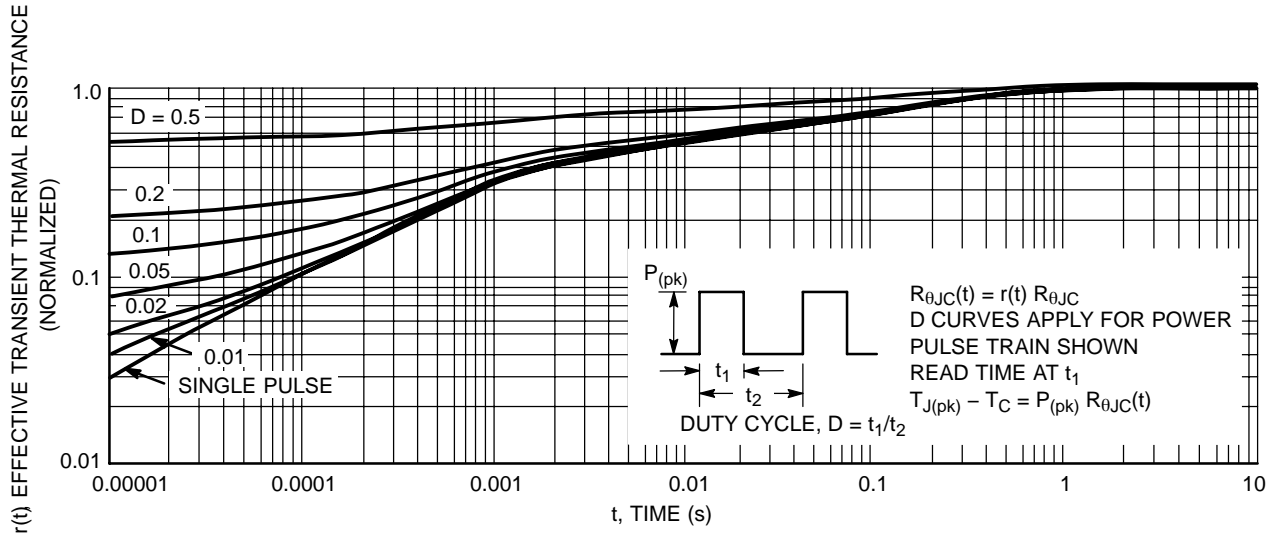


Figure 12. Thermal Response

ORDERING INFORMATION

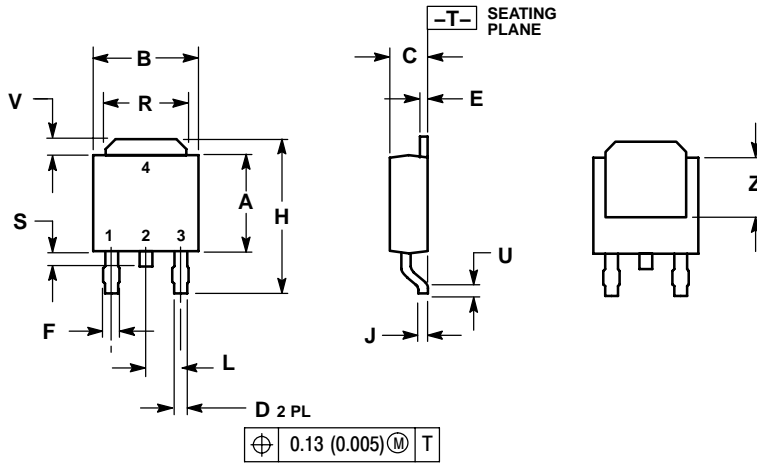
Order Number	Package	Shipping†
NTD60N02R	DPAK-3	75 Units / Rail
NTD60N02RG	DPAK-3 (Pb-Free)	75 Units / Rail
NTD60N02RT4	DPAK-3	2500 / Tape & Reel
NTD60N02RT4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD60N02R-1	DPAK-3 Straight Lead	75 Units / Rail
NTD60N02R-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail
NTD60N02R-35	DPAK-3 Straight Lead (3.5 ± 0.15 mm)	75 Units / Rail
NTD60N02R-35G	DPAK-3 Straight Lead (3.5 ± 0.15 mm) (Pb-Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD60N02R

PACKAGE DIMENSIONS

DPAK
CASE 369AA-01
ISSUE A

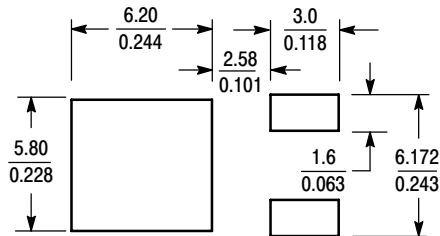


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	----	0.51	----
V	0.035	0.050	0.89	1.27
Z	0.155	----	3.93	----

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



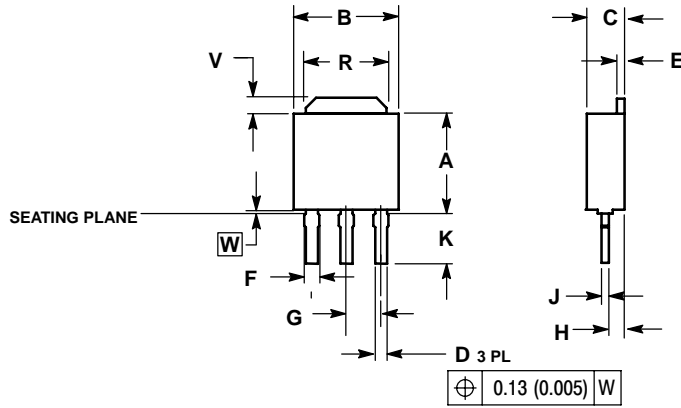
SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD60N02R

PACKAGE DIMENSIONS

3 IPAК, STRAIGHT LEAD CASE 369AC-01 ISSUE O



NOTES:

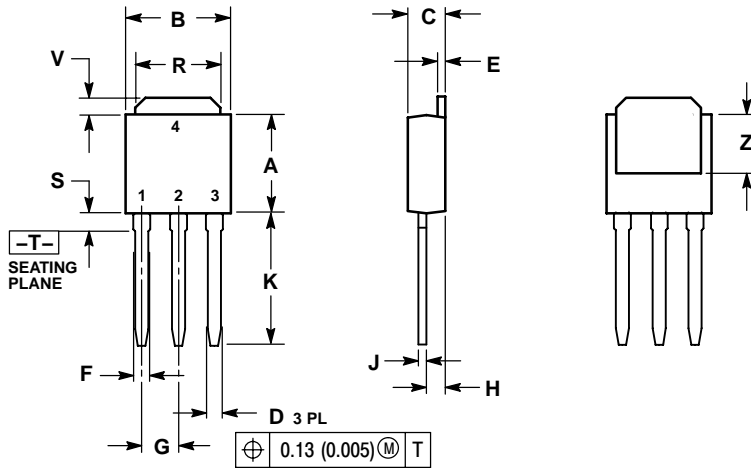
- 1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2.. CONTROLLING DIMENSION: INCH.
- 3.. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
- 4.. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

NTD60N02R

PACKAGE DIMENSIONS

DPAK
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850



ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NTD60N02R/D

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View NTD60N02R-035 on WIN SOURCE](#)
-  [ON Semiconductor Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management