



**THE DATASHEET OF  
NTD70N03R-001**



# NTD70N03R

## Power MOSFET

72 A, 25 V, N-Channel DPAK

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{ISS}$  to Minimize Driver Loss
- Low Gate Charge
- Pb-Free Packages are Available

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	25	$V_{dc}$
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 20$	$V_{dc}$
Thermal Resistance - Junction-to-Case	$R_{\theta JC}$	2.4	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	62.5	W
Drain Current			
- Continuous @ $T_C = 25^\circ\text{C}$ , Chip	$I_D$	72.0	A
- Continuous @ $T_C = 25^\circ\text{C}$ , Limited by Package	$I_D$	62.8	A
- Continuous @ $T_A = 25^\circ\text{C}$ , Limited by Wires	$I_D$	32	A
- Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_{DM}$	140	A
Thermal Resistance - Junction-to-Ambient (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.87	W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	12.0	A
Thermal Resistance - Junction-to-Ambient (Note 2)	$R_{\theta JA}$	110	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.36	W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	10.0	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 30 V_{dc}$ , $V_{GS} = 10 V_{dc}$ , $I_L = 12 A_{pk}$ , $L = 1 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	71.7	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 s	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

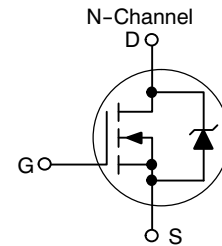
1. When surface mounted to an FR4 board using 0.5 sq. in. pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.



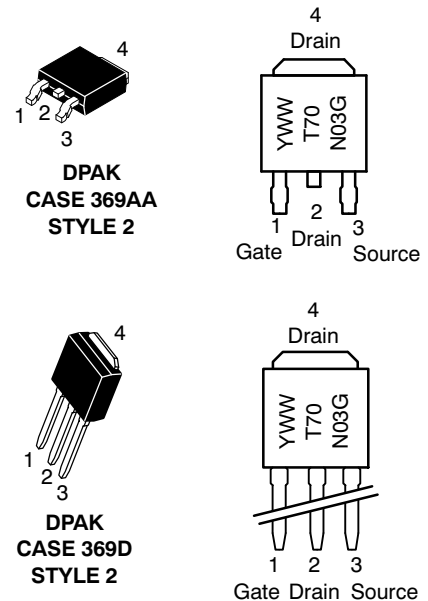
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
25 V	5.6 m $\Omega$	72 A



### MARKING DIAGRAMS



70N03 = Device Code  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD70N03R

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Temperature Coefficient (Positive)	V <sub>(br)DSS</sub>	25 -	28 20.5	- -	V <sub>dc</sub> mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.5 10	μA <sub>dc</sub>
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V <sub>dc</sub> , V <sub>DS</sub> = 0 V <sub>dc</sub> )	I <sub>GSS</sub>	-	-	±100	nA <sub>dc</sub>

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 -	1.5 4.0	2.0 -	V <sub>dc</sub> mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> ) (V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> )	R <sub>DS(on)</sub>	- -	8.1 5.6	13 8.0	mΩ
Forward Transconductance (Note 3) (V <sub>DS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub> )	g <sub>FS</sub>	-	27	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V, f = 1 MHz)	C <sub>ISS</sub>	-	1333	-	pF
Output Capacitance		C <sub>OSS</sub>	-	600	-	
Transfer Capacitance		C <sub>RSS</sub>	-	218	-	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>GS</sub> = 10 V <sub>dc</sub> , V <sub>DD</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 36 A <sub>dc</sub> , R <sub>G</sub> = 3 Ω)	t <sub>d(on)</sub>	-	6.9	-	ns
Rise Time		t <sub>r</sub>	-	1.3	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	18.4	-	
Fall Time		t <sub>f</sub>	-	5.5	-	
Gate Charge	(V <sub>GS</sub> = 5 V <sub>dc</sub> , I <sub>D</sub> = 36 A <sub>dc</sub> , V <sub>DS</sub> = 10 V <sub>dc</sub> ) (Note 3)	Q <sub>T</sub>	-	13.2	-	nC
		Q <sub>GS</sub>	-	3.3	-	
		Q <sub>DS</sub>	-	6.5	-	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (Note 3) (I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	0.86 0.73	1.2 -	V <sub>dc</sub>
Reverse Recovery Time	(I <sub>S</sub> = 36 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , dI <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	27.9	-	ns
		t <sub>a</sub>	-	14.8	-	
		t <sub>b</sub>	-	13.1	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	19	-	nC

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

4. Switching characteristics are independent of operating junction temperatures.

# NTD70N03R

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

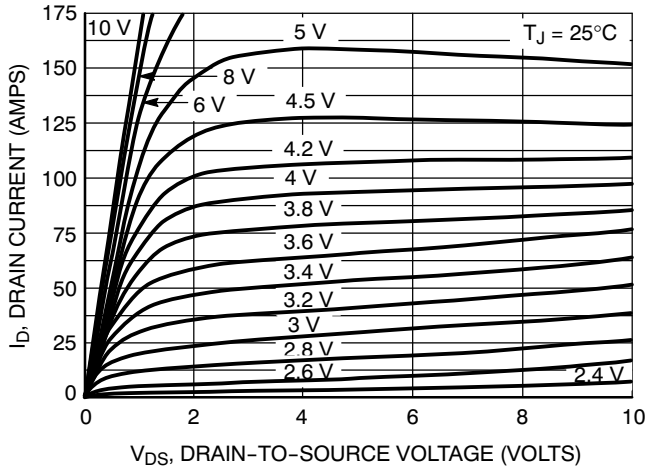


Figure 1. On-Region Characteristics

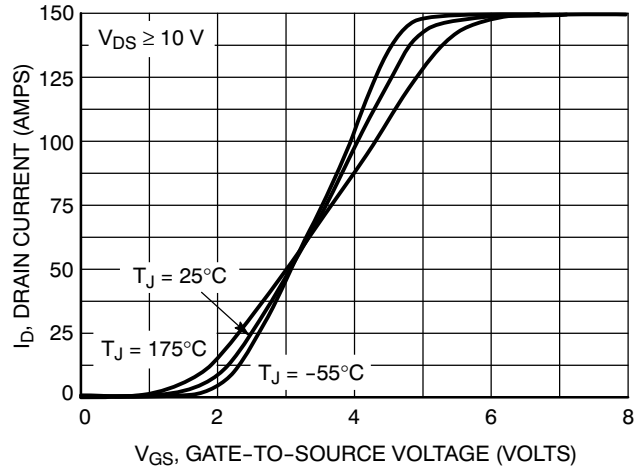


Figure 2. Transfer Characteristics

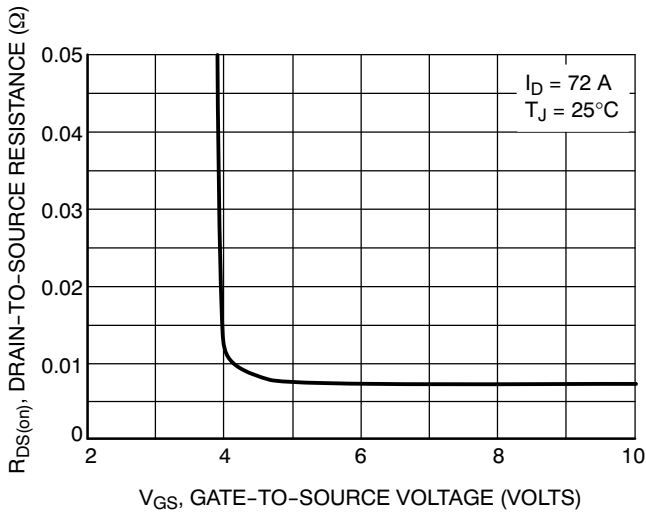


Figure 3. On-Resistance versus Gate-to-Source Voltage

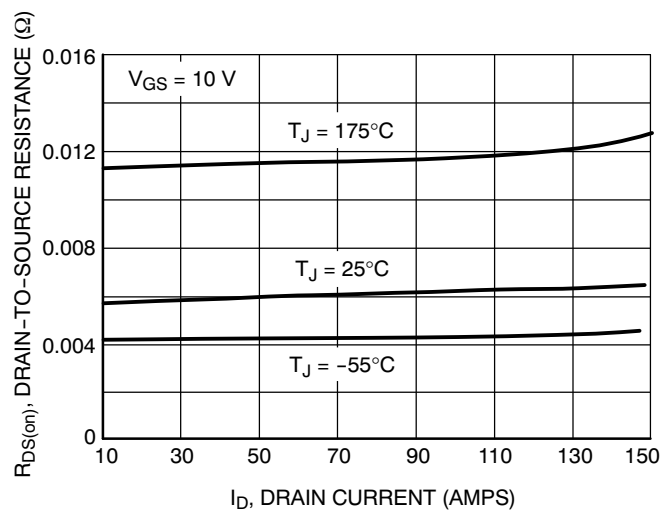


Figure 4. On-Resistance versus Drain Current and Gate Voltage

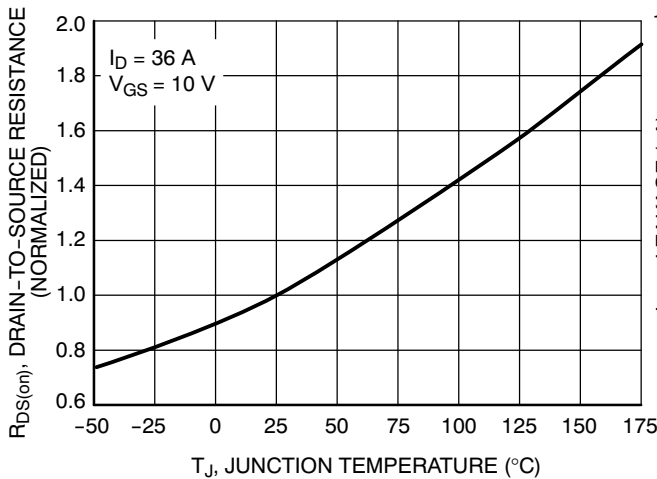


Figure 5. On-Resistance Variation with Temperature

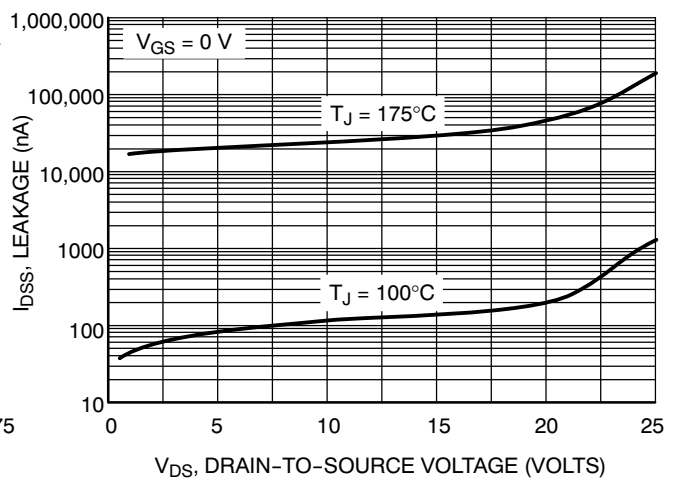
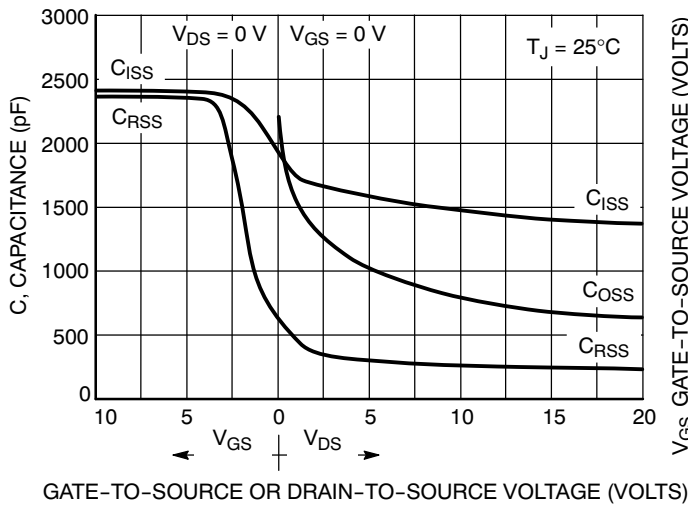
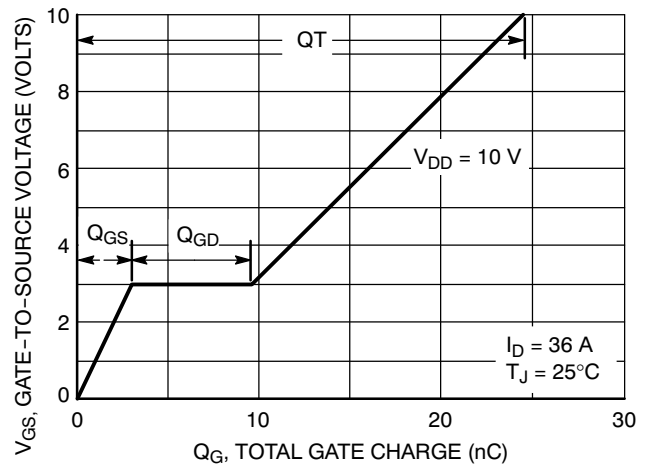


Figure 6. Drain-to-Source Leakage Current versus Voltage

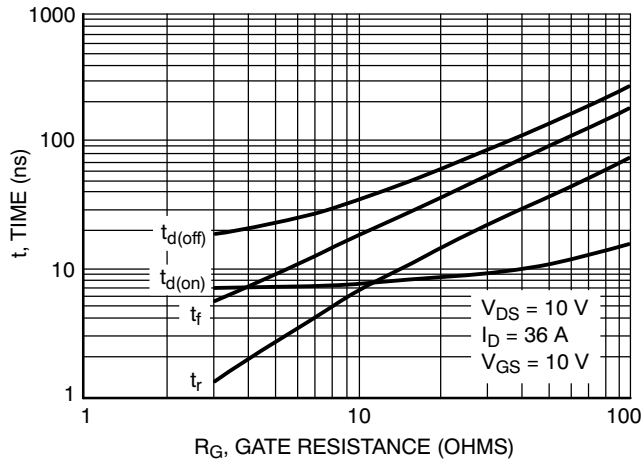
# NTD70N03R



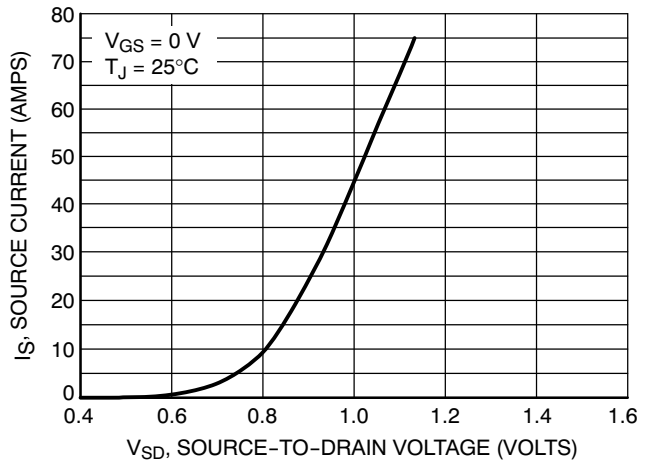
**Figure 7. Capacitance Variation**



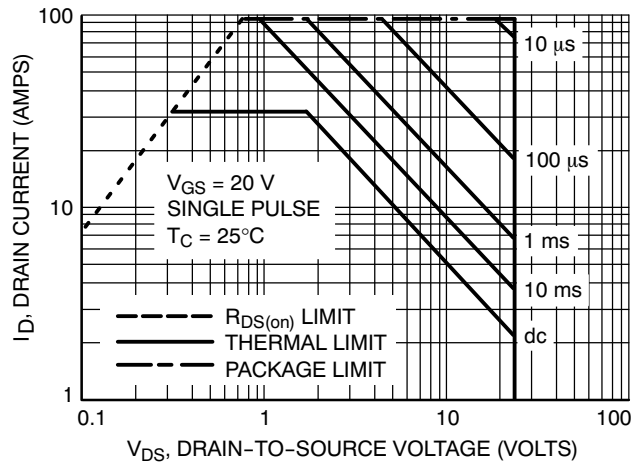
**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



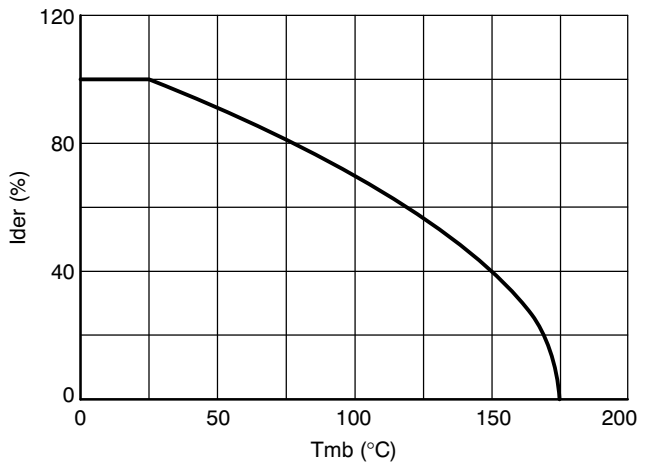
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Normalized Continuous Drain Current as a function of Mounting Base Temperature**

# NTD70N03R

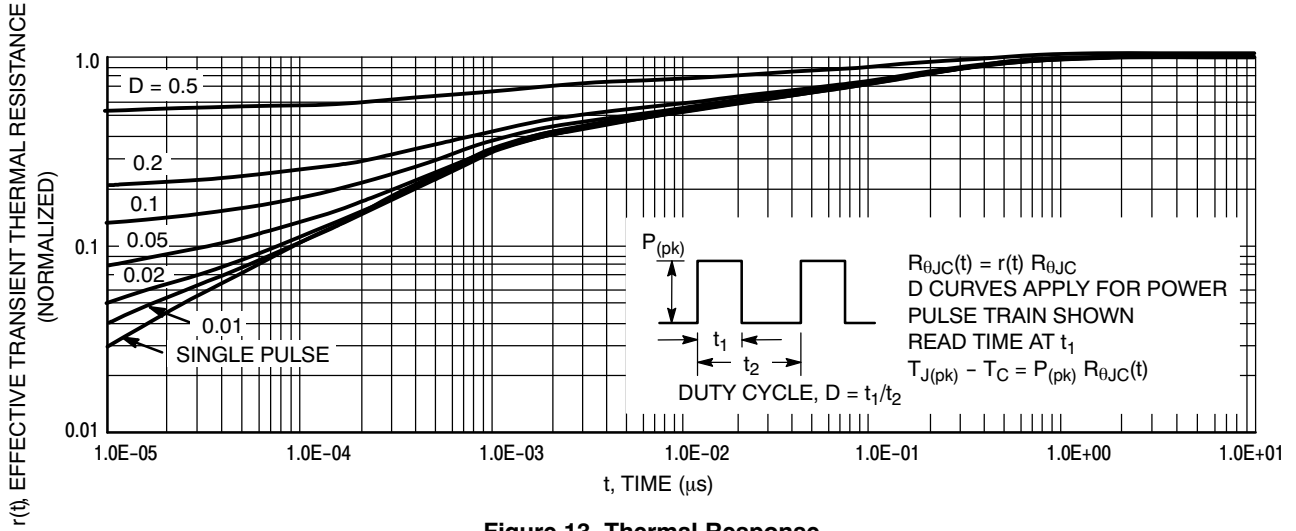


Figure 13. Thermal Response

## ORDERING INFORMATION

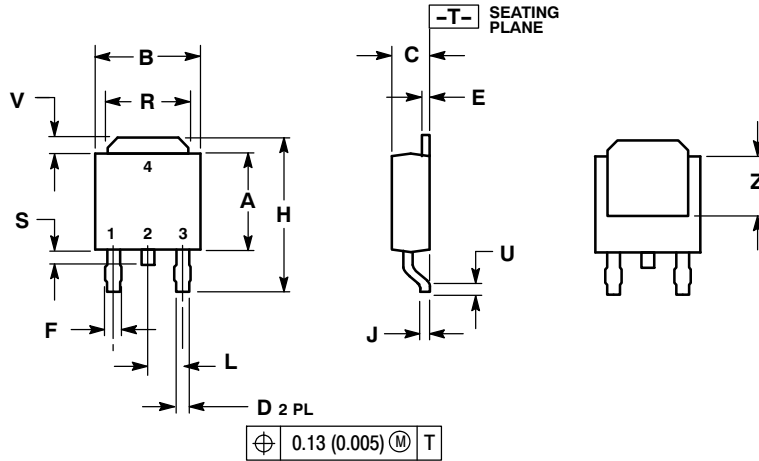
Order Number	Package	Shipping <sup>†</sup>
NTD70N03R	DPAK-3	75 Units / Rail
NTD70N03RG	DPAK-3 (Pb-Free)	75 Units / Rail
NTD70N03RT4	DPAK-3	2500 / Tape & Reel
NTD70N03RT4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD70N03R-1	DPAK-3 Straight Lead	75 Units / Rail
NTD70N03R-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD70N03R

## PACKAGE DIMENSIONS

DPAK  
CASE 369AA-01  
ISSUE A

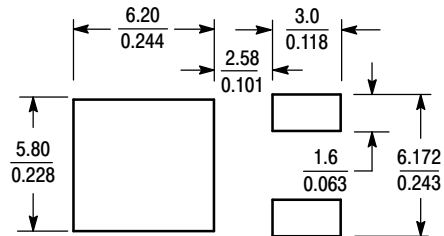


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

## SOLDERING FOOTPRINT\*



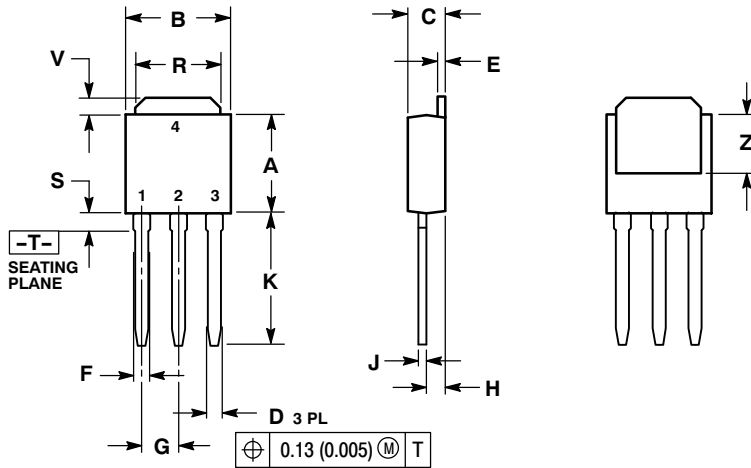
SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTD70N03R

## PACKAGE DIMENSIONS

### DPAK CASE 369D-01 ISSUE B




**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

**STYLE 2:**

- PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View NTD70N03R-001](#) on WIN SOURCE

 [ON Semiconductor](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management