



**THE DATASHEET OF
NTMS4816NR2G**



NTMS4816N

MOSFET – Power, N-Channel, SO-8 30 V, 11 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Disk Drives
- DC-DC Converters
- Printers

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	9.0	A
		$T_A = 70^\circ\text{C}$		7.2	
Power Dissipation $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.37	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	6.8	A
		$T_A = 70^\circ\text{C}$		5.4	
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 25^\circ\text{C}$	P_D	0.78	W
Continuous Drain Current $R_{\theta JA}$, $t \leq 10$ s (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	11	A
		$T_A = 70^\circ\text{C}$		8.8	
Power Dissipation $R_{\theta JA}$, $t \leq 10$ s (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	2.04	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$		I_{DM}	33	A
Operating Junction and Storage Temperature			T_J , T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	2.7	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_L = 12.5$ A _{pk} , $L = 1.0$ mH, $R_G = 25 \Omega$)			E_{AS}	78	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	91.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	61.3	
Junction-to-Foot (Drain)	$R_{\theta JF}$	22.5	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	159.5	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

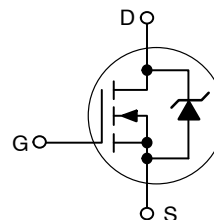


ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	10 m Ω @ 10 V	11 A
	16 m Ω @ 4.5 V	

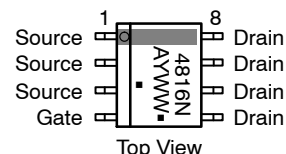
N-Channel



MARKING DIAGRAM/ PIN ASSIGNMENT



1
SO-8
CASE 751
STYLE 12



4816N = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4816NR2G	SO-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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1. Surfaced mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surfaced mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 100^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$		8.2	10	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 7.2\text{ A}$		12.7	16	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 9\text{ A}$		26		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1060		pF
Output Capacitance	C_{oss}			220		
Reverse Transfer Capacitance	C_{rss}			126		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 9\text{ A}$		9.2		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.4		
Gate-to-Source Charge	Q_{GS}			4.4		
Gate-to-Drain Charge	Q_{GD}			3.8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 9\text{ A}$		18.3		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 6.0\ \Omega$		8.0		ns
Rise Time	t_r			3.8		
Turn-Off Delay Time	$t_{d(off)}$			21.6		
Fall Time	t_f			8.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 2.7\text{ A}$	$T_J = 25^\circ\text{C}$	0.75	1.0	V
			$T_J = 125^\circ\text{C}$	0.55		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 2.7\text{ A}$		20		ns
Charge Time	t_a			9.0		
Discharge Time	t_b			11		
Reverse Recovery Charge	Q_{RR}			9.0		nC

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.66		nH
Drain Inductance	L_D	$T_A = 25^\circ\text{C}$		0.20		nH
Gate Inductance	L_G	$T_A = 25^\circ\text{C}$		1.5		nH
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.5	2.3	Ω

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3. Pulse Test: pulse width = 300 μ s, duty cycle \leq 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

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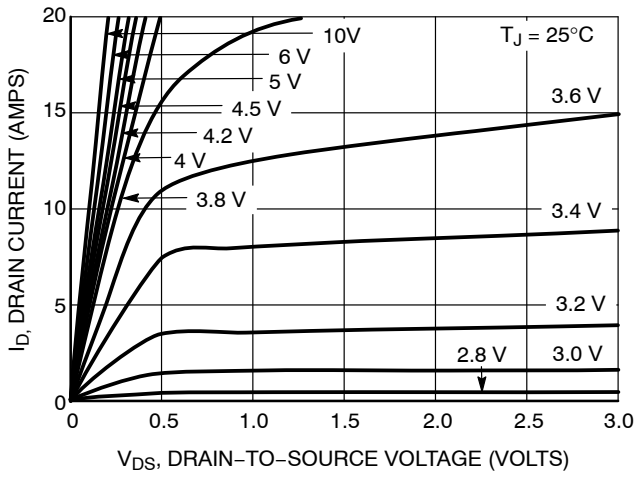


Figure 1. On-Region Characteristics

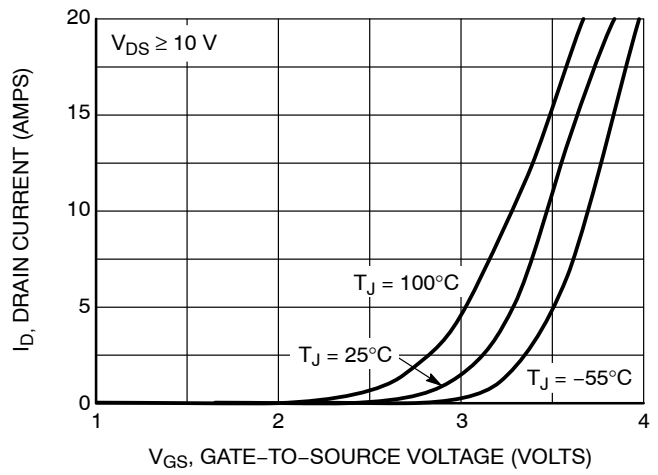


Figure 2. Transfer Characteristics

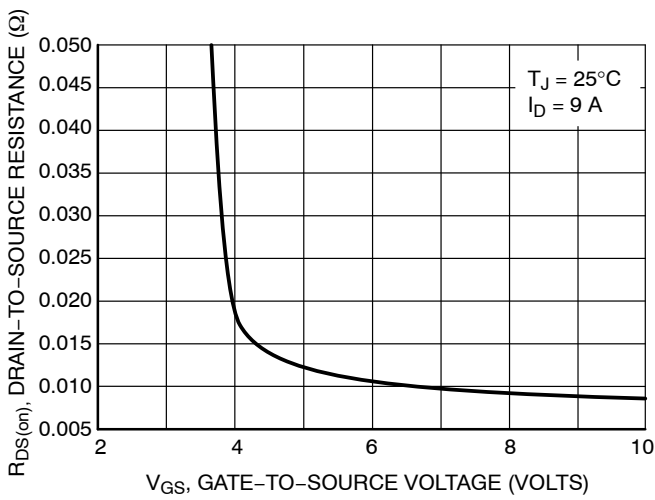


Figure 3. On-Resistance vs. Gate-to-Source Voltage

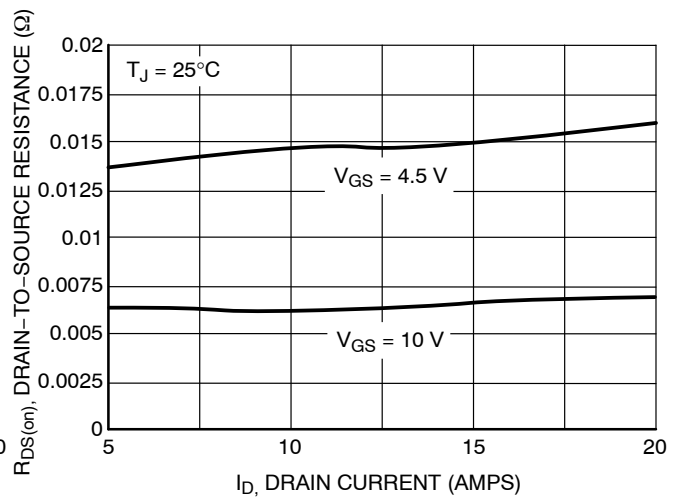


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

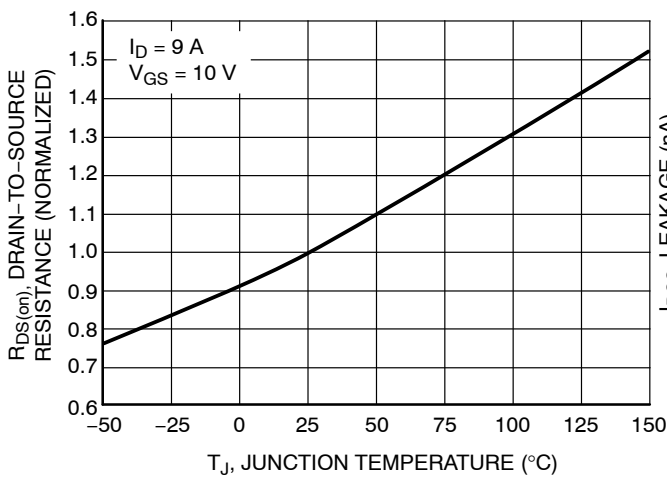


Figure 5. On-Resistance Variation with Temperature

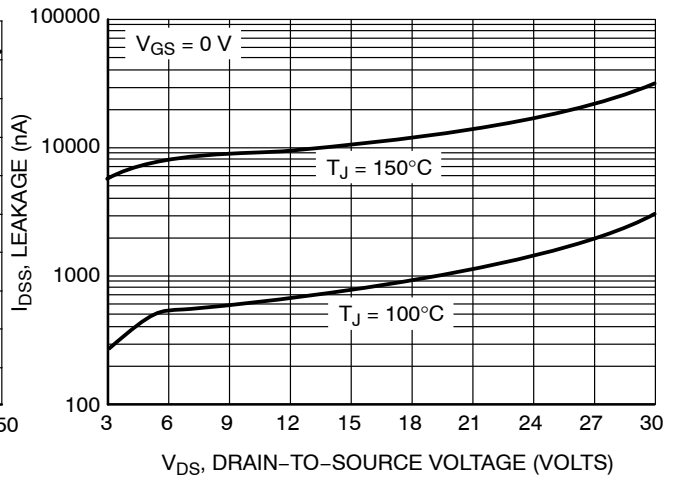


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES

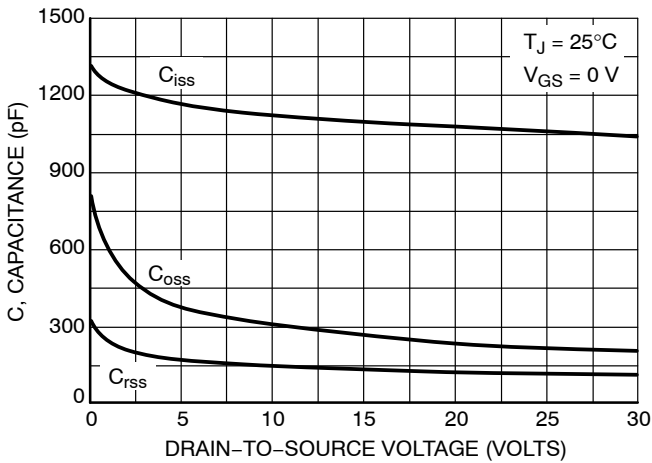


Figure 7. Capacitance Variation

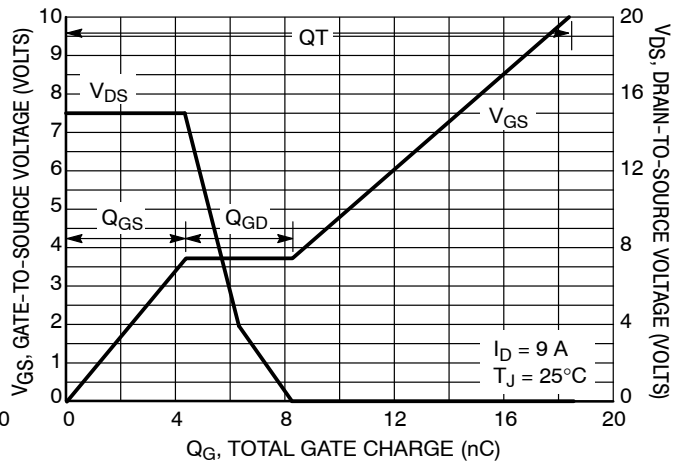


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

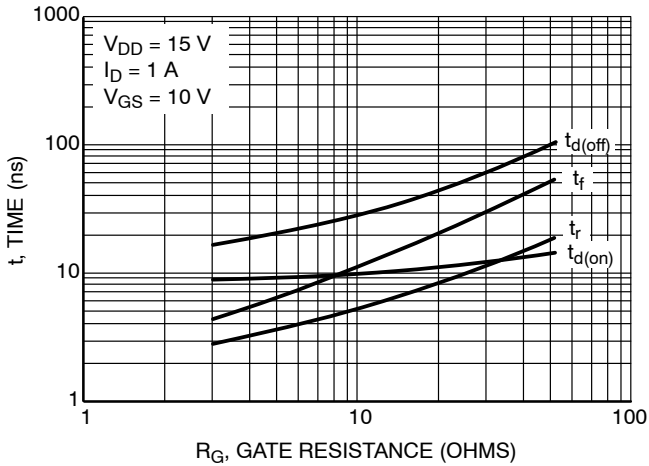


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

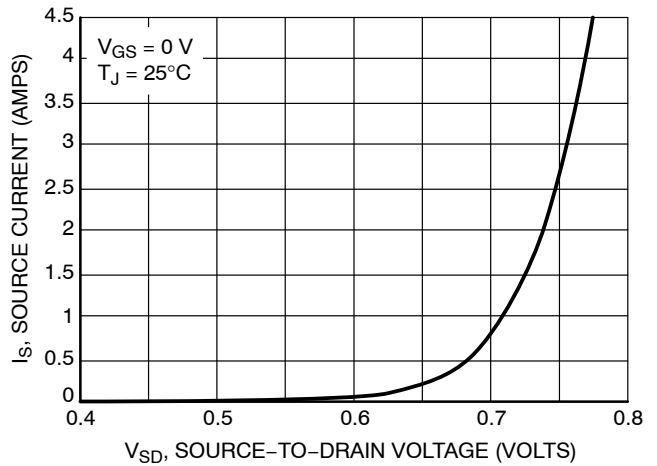


Figure 10. Diode Forward Voltage vs. Current

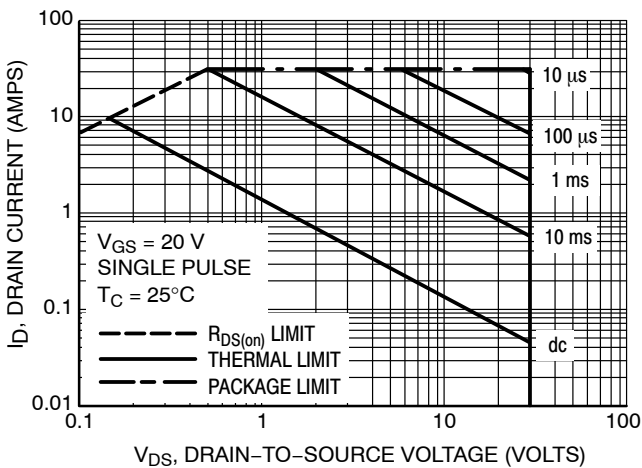


Figure 11. Maximum Rated Forward Biased Safe Operating Area

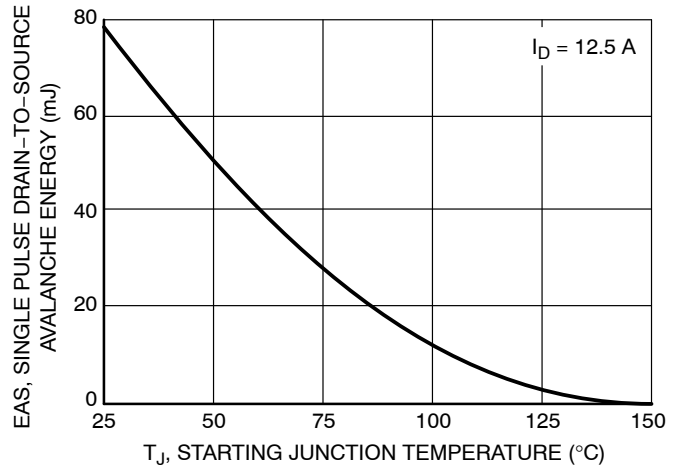
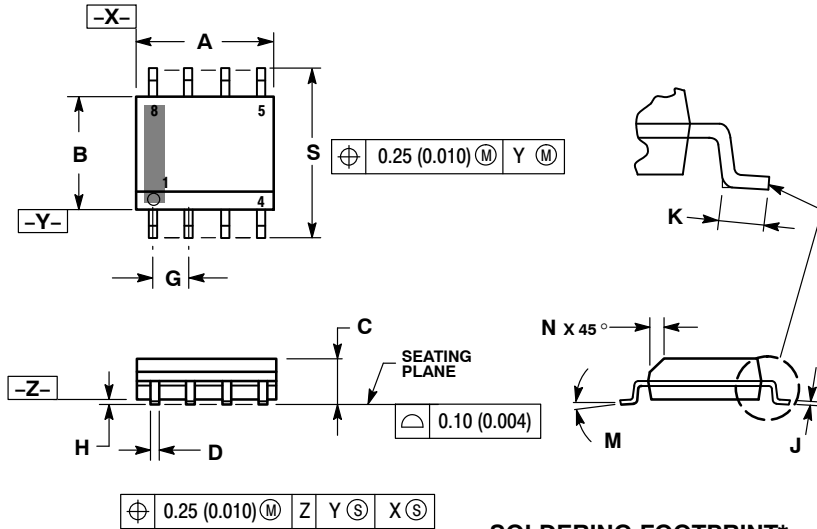


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

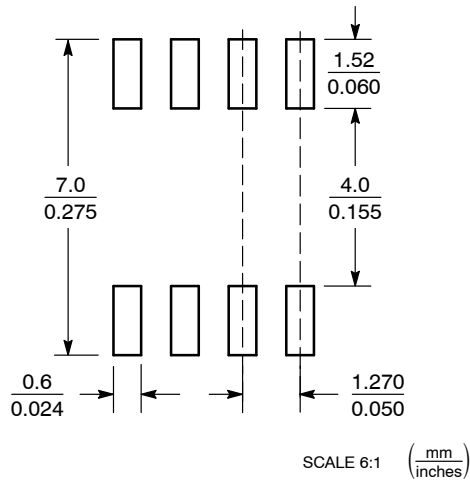


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



STYLE 12:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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