



**THE DATASHEET OF  
NTQD6968NR2**



# NTQD6968N

## Power MOSFET

7.0 A, 20 V, Common Drain,  
Dual N-Channel, TSSOP-8



ON Semiconductor®

<http://onsemi.com>

### Features

- Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- 3 mm Wide TSSOP-8 Surface Mount Package
- High Speed, Soft Recovery Diode
- TSSOP-8 Mounting Information Provided
- Pb-Free Package is Available

### Applications

- Battery Protection Circuits

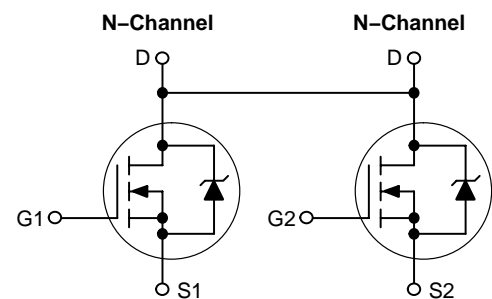
### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	20	Vdc
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 12$	Vdc
Drain Current	$I_D$	7.0	Adc
– Continuous @ $T_A 25^\circ\text{C}$ (Note 1)	$I_D$	5.6	
– Continuous @ $T_A 70^\circ\text{C}$ (Note 1)	$I_{DM}$	20	
– Pulsed (Note 3)			
Total Power Dissipation @ $T_A 25^\circ\text{C}$ (Note 1)	$P_D$	1.81	W
Drain Current	$I_D$	6.2	Adc
– Continuous @ $T_A 25^\circ\text{C}$ (Note 2)	$I_D$	4.9	
– Continuous @ $T_A 70^\circ\text{C}$ (Note 2)	$I_{DM}$	18	
– Pulsed (Note 3)			
Total Power Dissipation @ $T_A 25^\circ\text{C}$ (Note 2)	$P_D$	1.39	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JA}$	69 90	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes for 10 seconds	TL	260	$^\circ\text{C}$

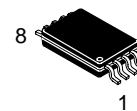
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted onto a 2" square FR-4 Board  
(1 in sq, 2 oz. Cu 0.06" thick single sided),  $t \leq 10$  sec.
2. Mounted onto a 2" square FR-4 Board  
(1 in sq, 2 oz. Cu 0.06" thick single sided), Steady State.
3. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%.

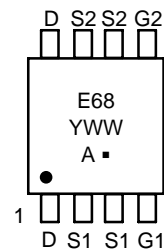
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
20 V	17 m $\Omega$ @ 4.5 V	7.0 A



### MARKING DIAGRAM & PIN ASSIGNMENT



TSSOP-8  
CASE 948S  
PLASTIC



E68 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NTQD6968N	TSSOP-8	100 Units / Rail
NTQD6968NR2	TSSOP-8	4000/Tape & Reel
NTQD6968NR2G	TSSOP-8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTQD6968N

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	20 -	- 16	- -	Vdc mV/°C
Zero Gate Voltage Collector Current (V <sub>DS</sub> = 16 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 25°C) (V <sub>DS</sub> = 16 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±12 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc

## ON CHARACTERISTICS

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	0.6 -	0.75 3.0	1.2 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 7.0 Adc) (V <sub>GS</sub> = 2.5 Vdc, I <sub>D</sub> = 7.0 Adc) (V <sub>GS</sub> = 2.5 Vdc, I <sub>D</sub> = 3.5 Adc)	R <sub>DS(on)</sub>	- - -	0.017 0.022 0.022	0.022 0.030 0.030	Ω
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 7.0 Adc)	g <sub>FS</sub>	-	19.2	-	Mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 16 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	630	-	pF
Output Capacitance		C <sub>oss</sub>	-	260	-	
Transfer Capacitance		C <sub>rss</sub>	-	95	-	

## SWITCHING CHARACTERISTICS (Notes 4 and 5)

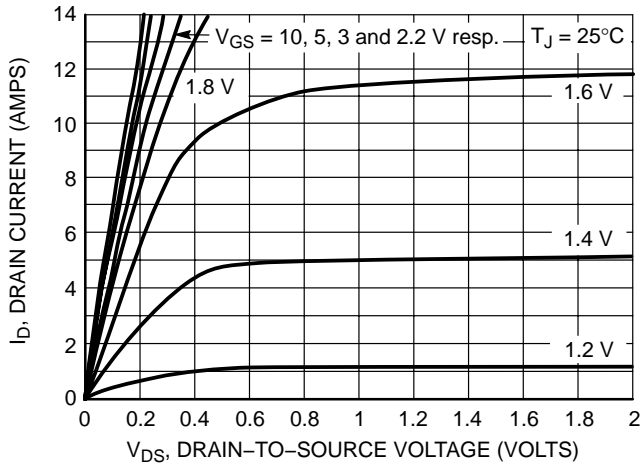
Turn-On Delay Time	(V <sub>DD</sub> = 16 Vdc, I <sub>D</sub> = 7.0 Adc, V <sub>GS</sub> = 4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	8.0	-	ns
Rise Time		t <sub>r</sub>	-	25	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	60	-	
Fall Time		t <sub>f</sub>	-	65	-	
Gate Charge	(V <sub>DS</sub> = 16 Vdc, V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 7.0 Adc)	Q <sub>tot</sub>	-	12.5	17	nC
		Q <sub>gs</sub>	-	1.0	-	
		Q <sub>gd</sub>	-	5.0	-	

## BODY-DRAIN DIODE RATINGS (Note 4)

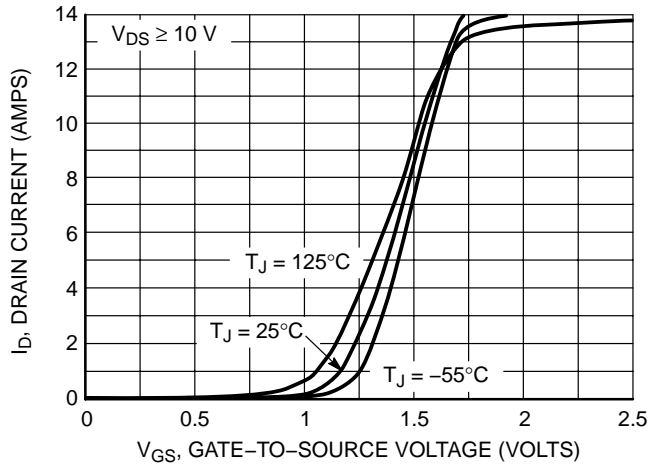
Forward On-Voltage	(I <sub>S</sub> = 7.0 Adc, V <sub>GS</sub> = 0 Vdc)	V <sub>SD</sub>	-	0.82	1.2	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 7.0 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	-	35	-	ns
		t <sub>a</sub>	-	15	-	
		t <sub>b</sub>	-	20	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.02	-	μC

4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
5. Switching characteristics are independent of operating junction temperature.

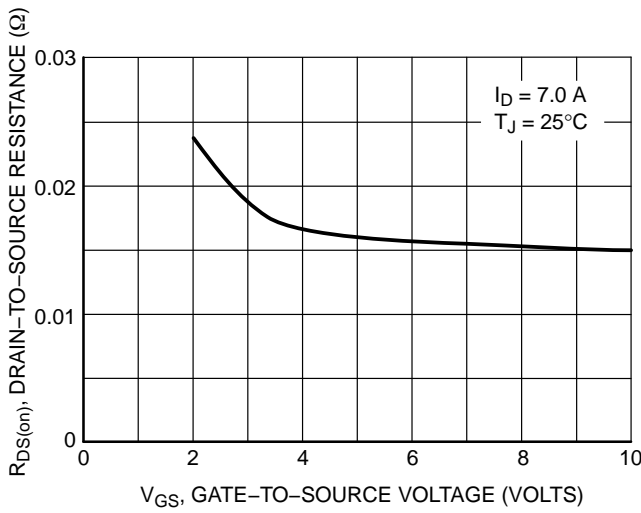
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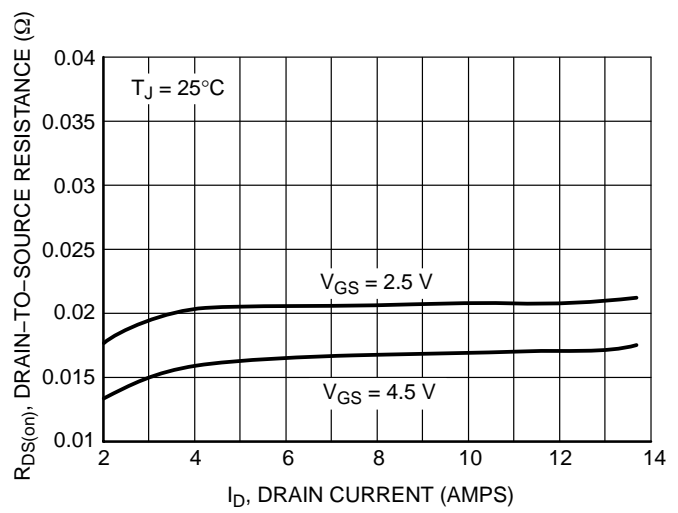
**Figure 1. On-Region Characteristics**



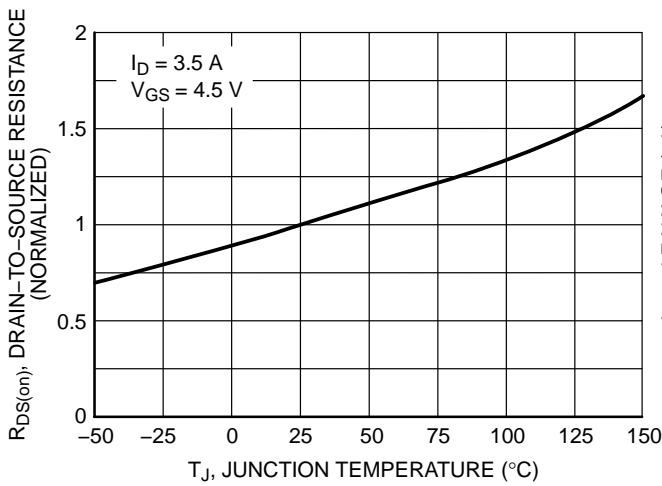
**Figure 2. Transfer Characteristics**



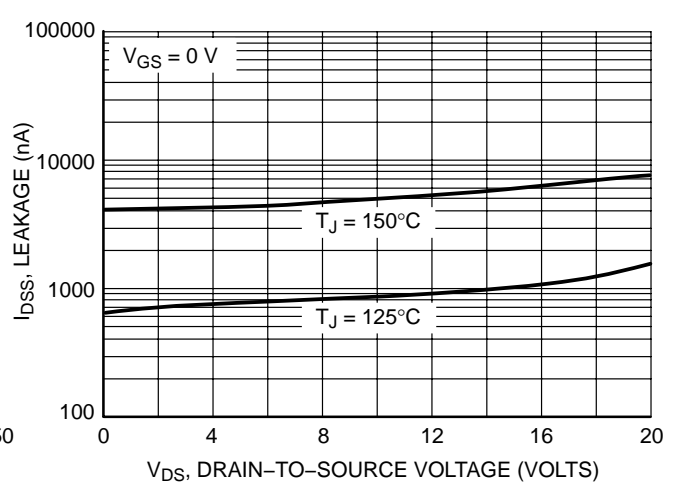
**Figure 3. On-Resistance versus Gate-to-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

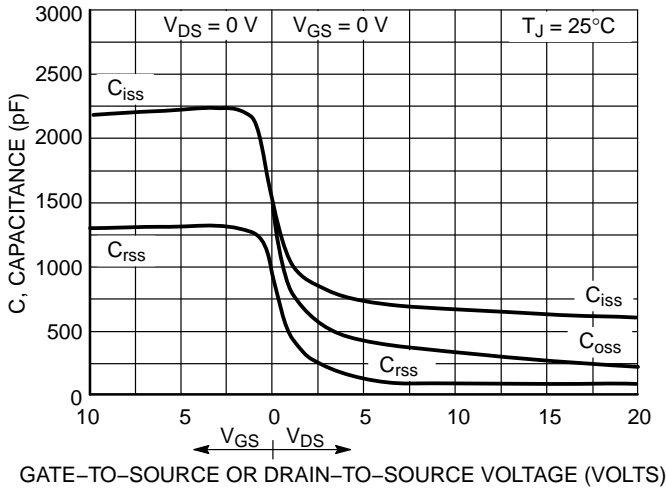


**Figure 5. On-Resistance Variation with Temperature**

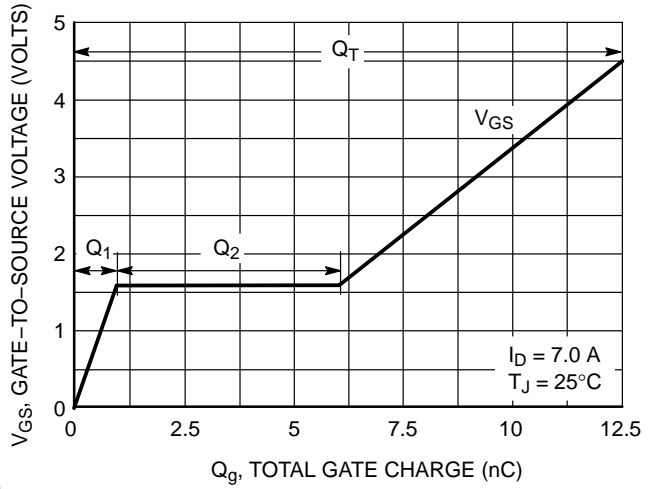


**Figure 6. Drain-to-Source Leakage Current versus Voltage**

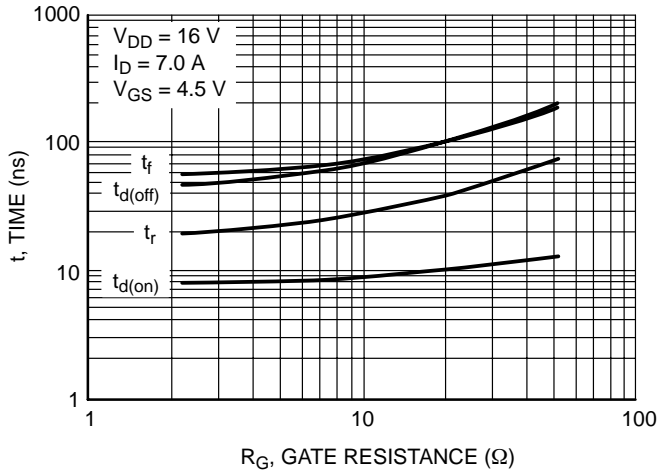
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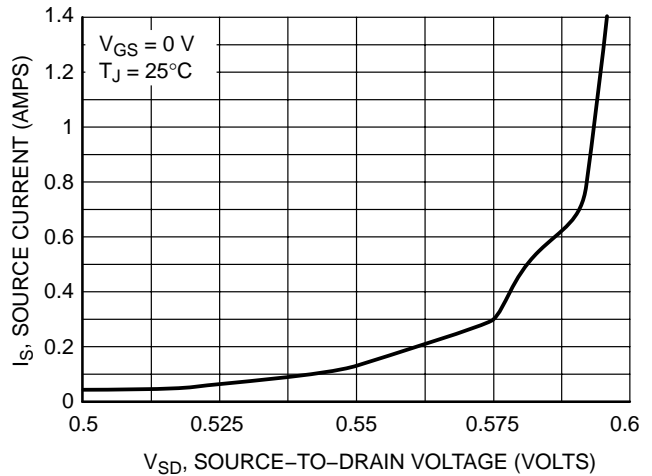
**Figure 7. Capacitance Variation**



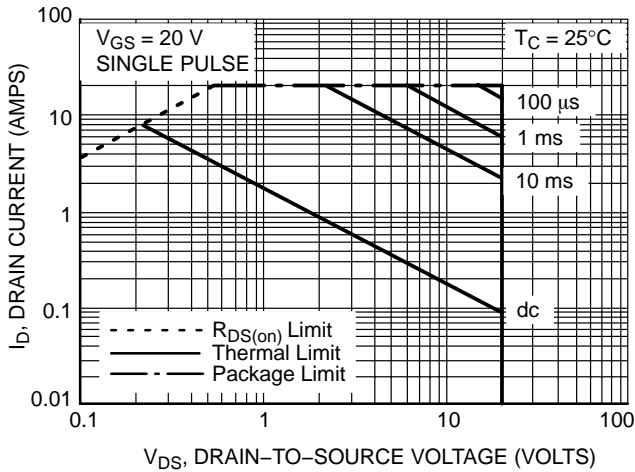
**Figure 8. Gate-to-Source Voltage versus Total Charge**



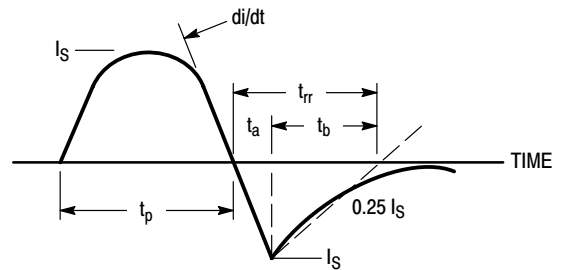
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Diode Reverse Recovery Waveform**

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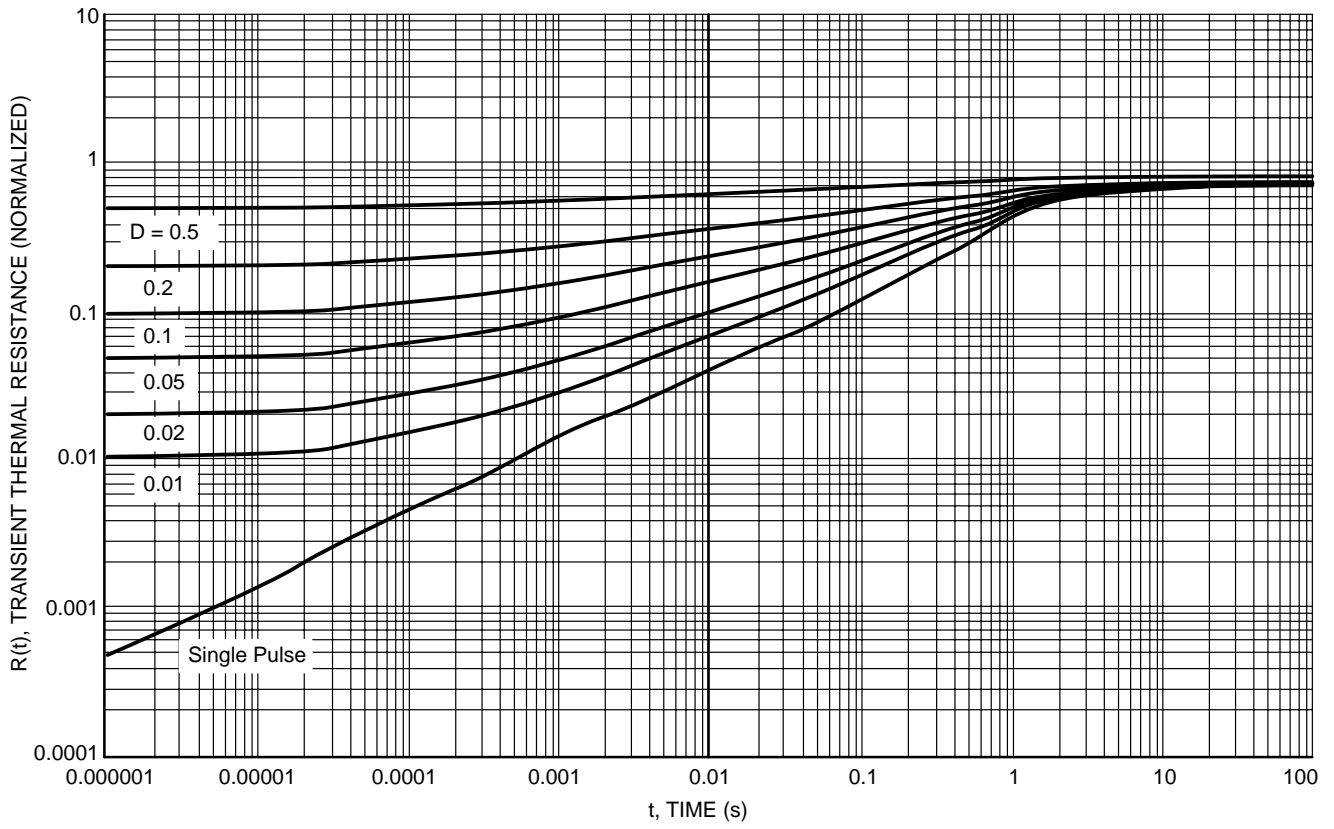
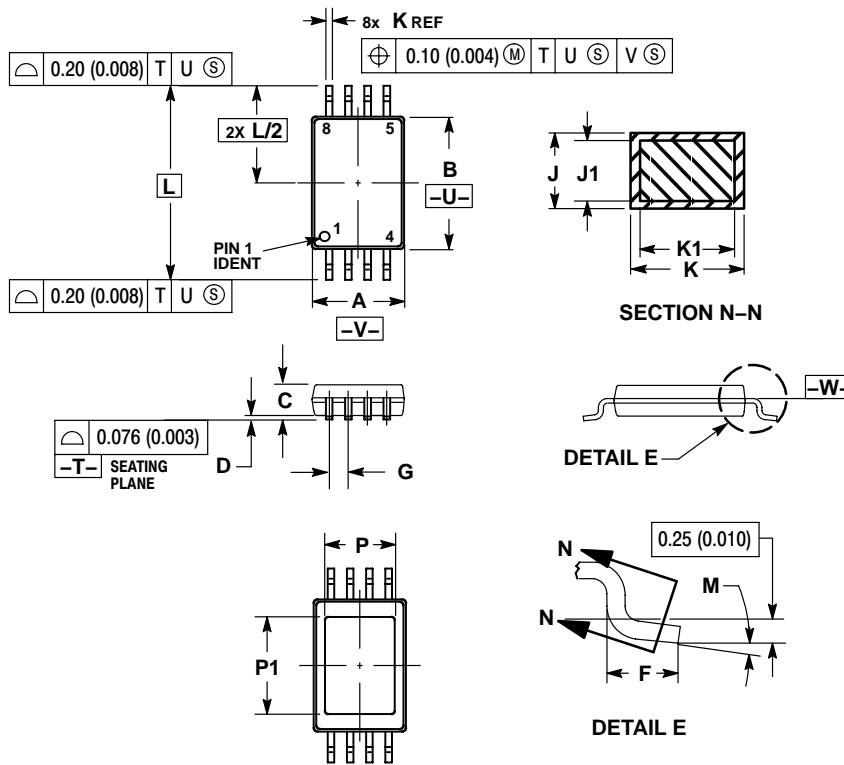


Figure 13. Thermal Response

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## PACKAGE DIMENSIONS

TSSOP-8  
CASE 948S-01  
ISSUE A

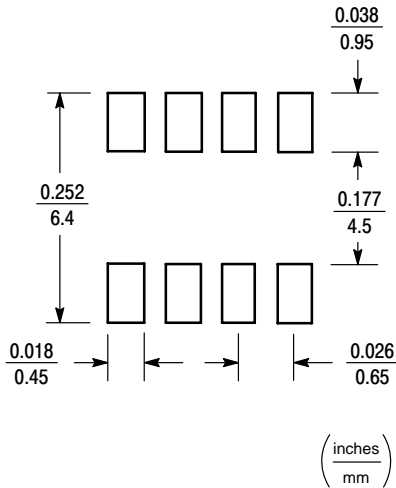


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°
P	---	2.20	---	0.087
P1	---	3.20	---	0.126

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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