THE DATASHEET OF

OP482GPZ

Dual/Quad, Low Power, High Speed JFET Operational Amplifiers

Data Sheet

OP282/OP482

FEATURES

High slew rate: 9 V/µs
Wide bandwidth: 4 MHz
Low supply current: 250 µA/amplifier maximum
Low offset voltage: 3 mV maximum
Low bias current: 100 pA maximum
Fast settling time
Common-mode range includes V+
Unity-gain stable
14-ball wafer level chip scale for quad

APPLICATIONS

Active filters
Fast amplifiers
Integrators
Supply current monitoring

GENERAL DESCRIPTION

The OP282/OP482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. The slew rate is typically 9 V/µs with a supply current of less than 250 µA per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the OP282/OP482 ensures that the bias current is typically a few picoamps and is less than 500 pA over the full temperature range. The offset voltage is less than 3 mV for the dual amplifier and less than 4 mV for the quad amplifier.

With a wide output swing (within 1.5 V of each supply), low power consumption, and high slew rate, the OP282/OP482 are ideal for battery-powered systems or power-restricted applications. An input common-mode range that includes the positive supply makes the OP282/OP482 an excellent choice for high-side signal conditioning.

The OP282/OP482 are specified over the extended industrial temperature range. The OP282 is available in the standard 8-lead, narrow SOIC and MSOP packages. The OP482 is available in the PDIP and narrow SOIC packages, as well as a 14-ball WLCSP.

PIN CONNECTIONS

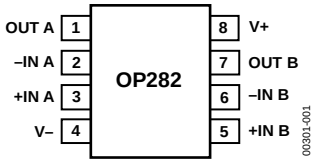

Figure 1. 8-Lead, Narrow-Body SOIC (S-Suffix) [R-8]

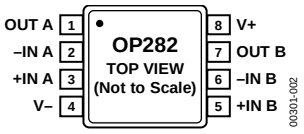

Figure 2. 8-Lead MSOP [RM-8]

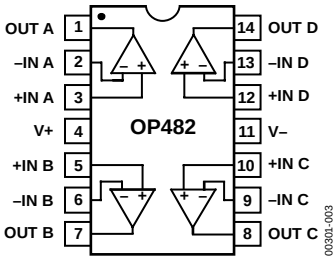

Figure 3. 14-Lead PDIP (P-Suffix) [N-14]

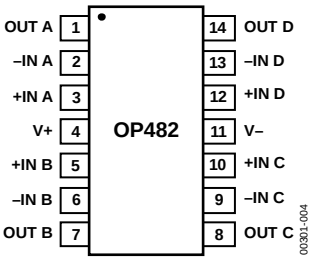

Figure 4. 14-Lead, Narrow-Body SOIC (S-Suffix) [R-14]

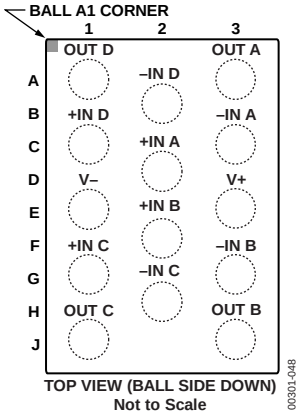

Figure 5. 14-Ball WLCSP [CB-14-2]

Rev. I **Document Feedback**

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REVISION HISTORY

9/13—Rev. H to Rev. I

Changes to Figure 5 ... 1
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 16

9/10—Rev. G to Rev. H

Added WLCSP ... Universal
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7/08—Rev. F to Rev. G

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Added Figure 45 and Figure 46 ... 12
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10/04—Rev. E to Rev. F

Deleted 8-Lead PDIP ... Universal
Added 8-Lead MSOP ... Universal
Changes to Format and Layout ... Universal
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10/02—Rev. D to Rev. E

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Edits to Ordering Guide ... 3
Edits to Outline Dimensions ... 11

9/02—Rev. C to Rev. D

Edits to 14-Lead SOIC (S-Suffix) Pin ... 1
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4/02—Rev. B to Rev. C

Wafer Test Limits Deleted ... 2
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At V_S = ±15.0 V, T_A = 25°C, unless otherwise noted; applies to both A and G grades.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP282		0.2	3	mV
		OP282, −40°C ≤ T_A ≤ +85°C			4.5	mV
		OP482		0.2	4	mV
		OP482, −40°C ≤ T_A ≤ +85°C			6	mV
Input Bias Current	I_B	V_{CM} = 0 V		3	100	pA
		V_{CM} = 0 V[1]			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	50	pA
		V_{CM} = 0 V[1]			250	pA
Input Voltage Range			−11		+15	V
Common-Mode Rejection Ratio	CMRR	−11 V ≤ V_{CM} ≤ +15 V, −40°C ≤ T_A ≤ +85°C	70	90		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = ±13.5 V	20			V/mV
		R_L = 10 kΩ, −40°C ≤ T_A ≤ +85°C	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	13.5	13.9		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ		−13.9	−13.5	V
Short-Circuit Limit	I_{SC}	Source	3	10		mA
		Sink		−12	−8	mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, −40°C ≤ T_A ≤ +85°C		25	316	µV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, −40°C ≤ T_A ≤ 85°C		210	250	µA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Full-Power Bandwidth	BW_P	1% distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$Ø_M$			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

[1] The input bias and offset currents are characterized at T_A = T_J = 85°C. Bias and offset currents are guaranteed but not tested at −40°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[1]	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device in socket for PDIP. θ_{JA} is specified for a device soldered in the circuit board for SOIC_N, MSOP, and WLCSP packages. This was measured using a standard 4-layer board.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP [RM]	142	45	°C/W
8-Lead SOIC_N (S-Suffix) [R]	120	45	°C/W
14-Lead PDIP (P-Suffix) [N]	83	39	°C/W
14-Lead SOIC_N (S-Suffix) [R]	112	35	°C/W
14-Ball WLCSP [CB][1, 2]	70	16	°C/W

[1] Simulated thermal numbers per JESD51-9.
[2] Junction-to-board thermal resistance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

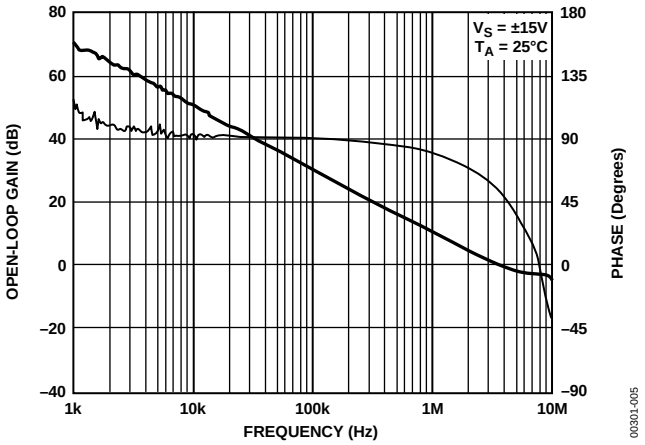


Figure 6. OP282 Open-Loop Gain and Phase vs. Frequency

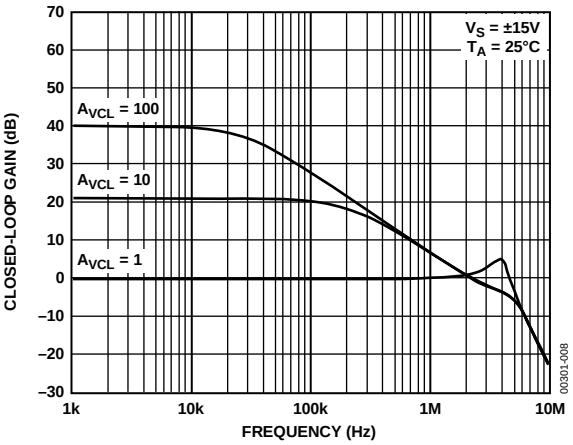


Figure 9. OP282 Closed-Loop Gain vs. Frequency

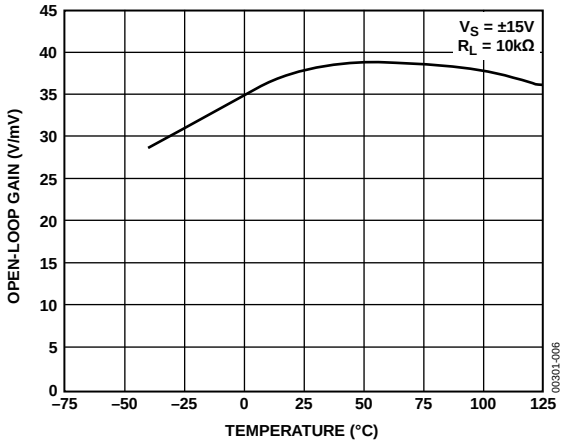


Figure 7. OP282 Open-Loop Gain vs. Temperature

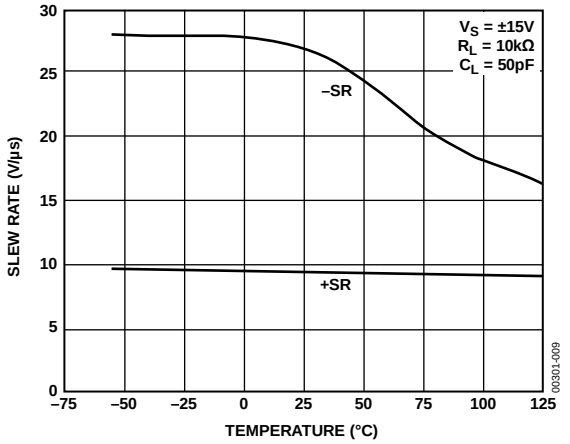


Figure 10. OP282 Slew Rate vs. Temperature

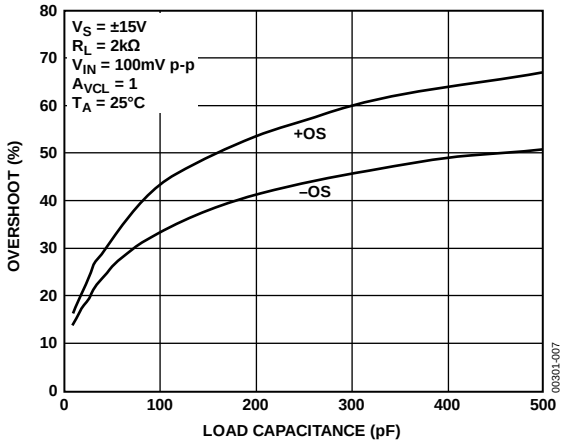


Figure 8. OP282 Small-Signal Overshoot vs. Load Capacitance

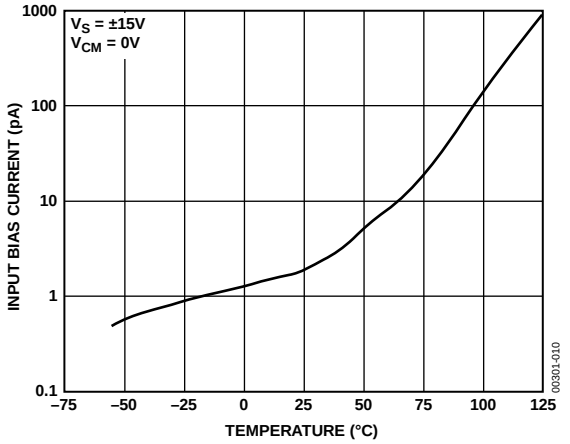


Figure 11. OP282 Input Bias Current vs. Temperature

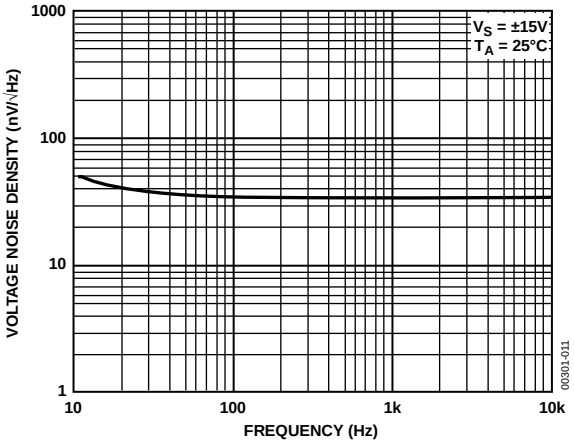


Figure 12. OP282 Voltage Noise Density vs. Frequency

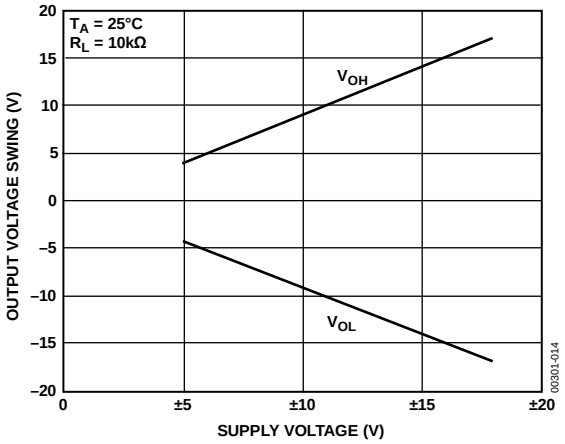


Figure 15. OP282 Output Voltage Swing vs. Supply Voltage

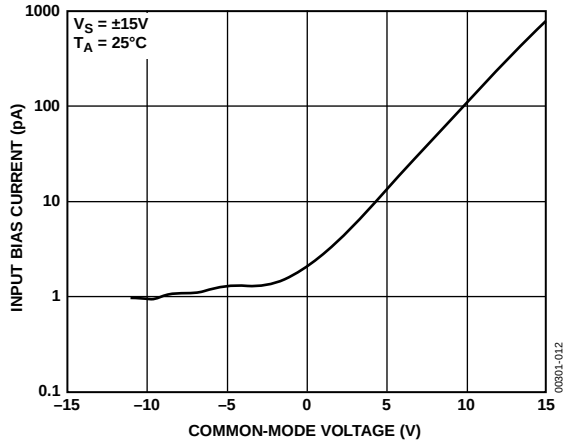


Figure 13. OP282 Input Bias Current vs. Common-Mode Voltage

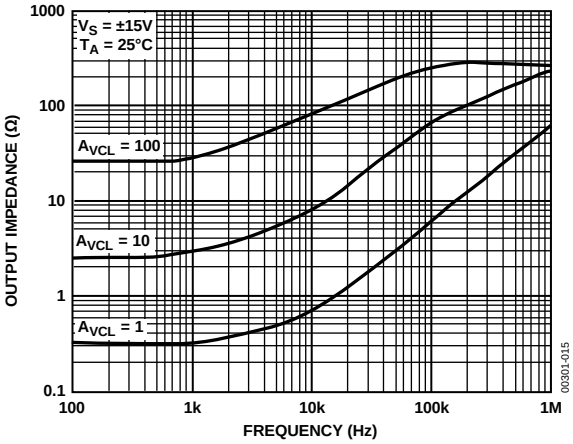


Figure 16. OP282 Closed-Loop Output Impedance vs. Frequency

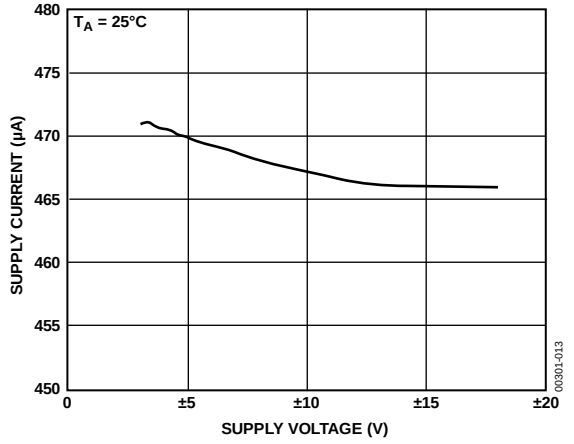


Figure 14. OP282 Supply Current vs. Supply Voltage

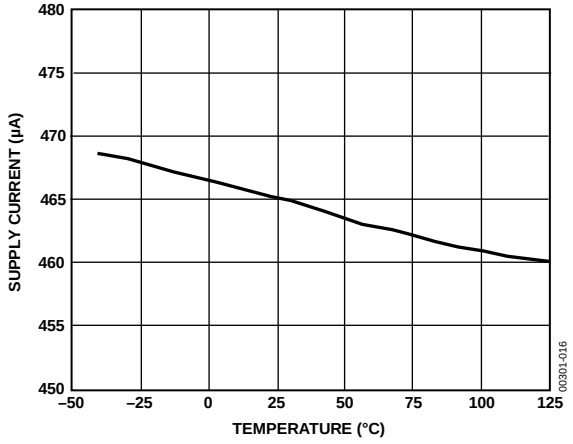


Figure 17. OP282 Supply Current vs. Temperature

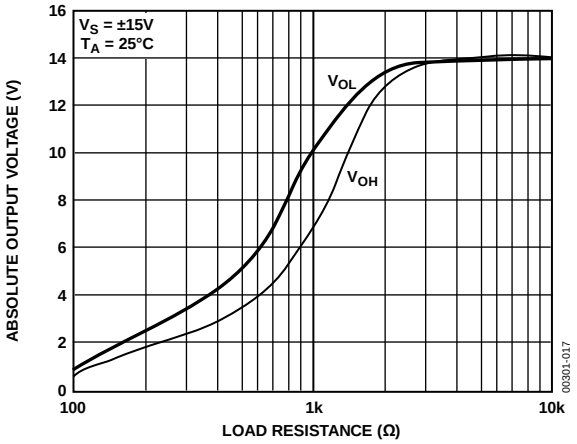


Figure 18. OP282 Absolute Output Voltage vs. Load Resistance

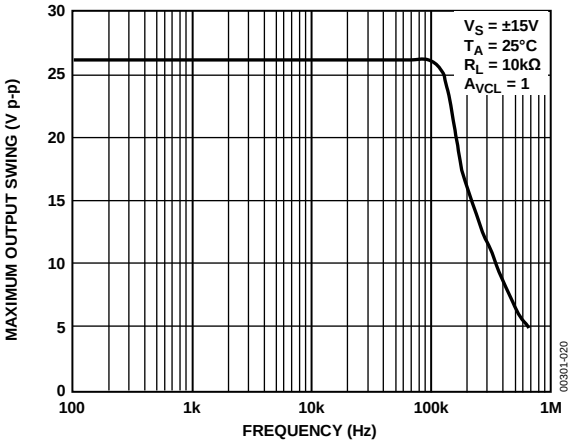


Figure 21. OP282 Maximum Output Swing vs. Frequency

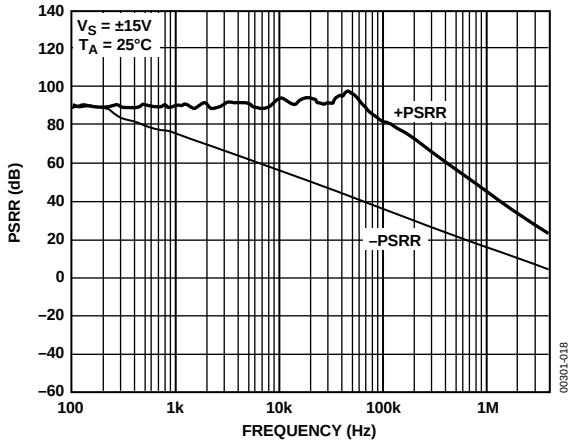


Figure 19. OP282 PSRR vs. Frequency

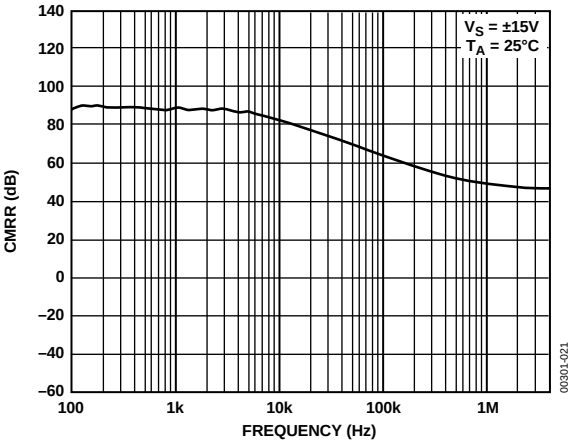


Figure 22. OP282 CMRR vs. Frequency

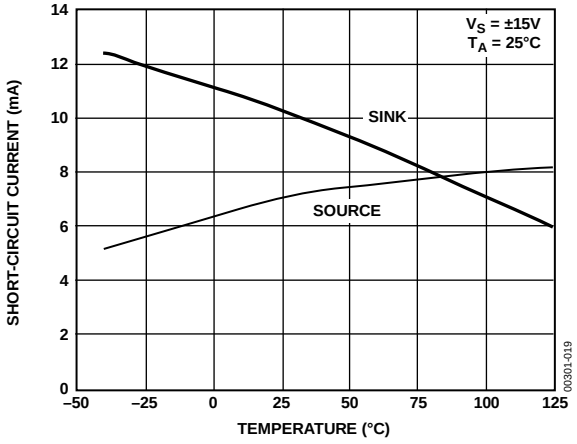


Figure 20. OP282 Short-Circuit Current vs. Temperature

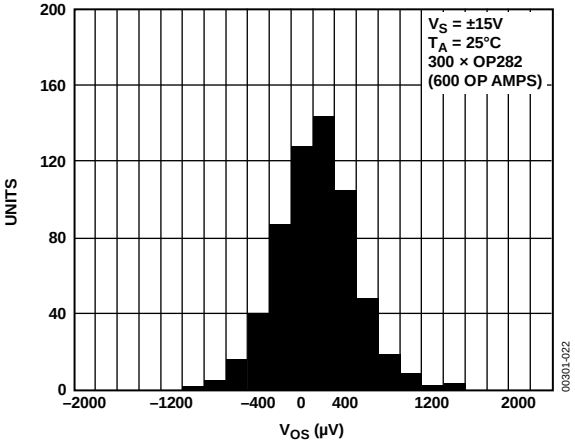


Figure 23. OP282 VOS Distribution, SOIC_N Package

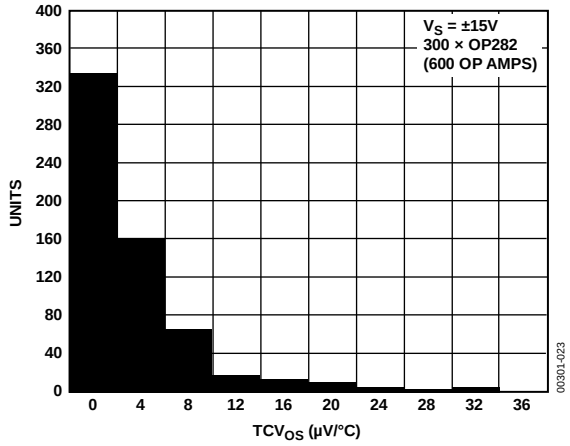


Figure 24. OP282 TCVOS Distribution, SOIC_N Package

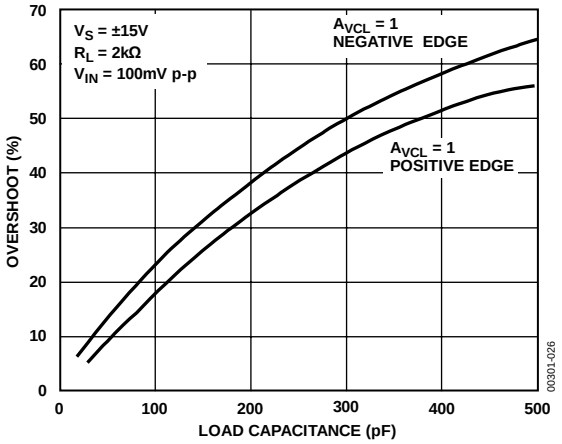


Figure 27. OP482 Small-Signal Overshoot vs. Load Capacitance

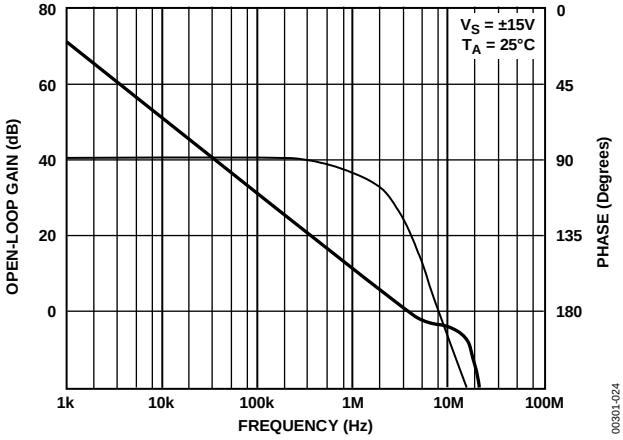


Figure 25. OP482 Open-Loop Gain and Phase vs. Frequency

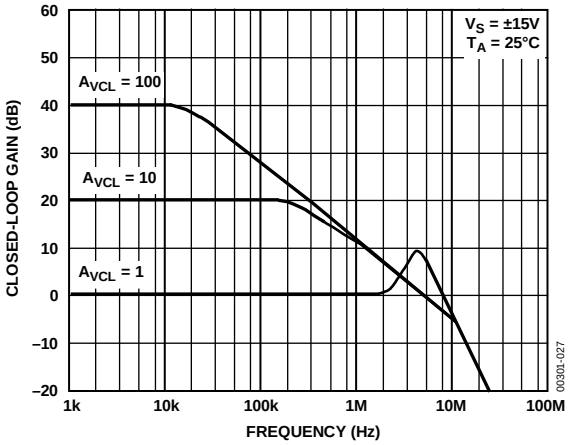


Figure 28. OP482 Closed-Loop Gain vs. Frequency

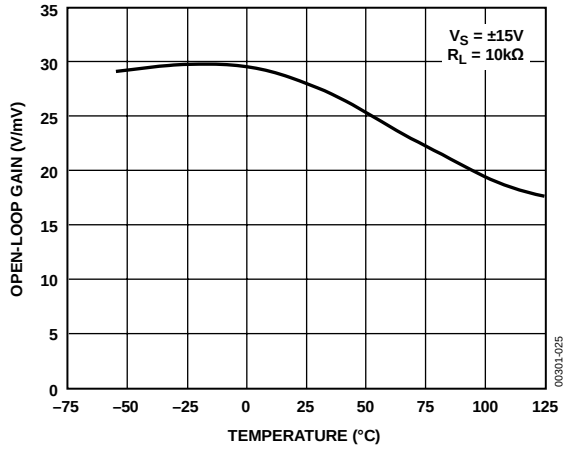


Figure 26. OP482 Open-Loop Gain vs. Temperature

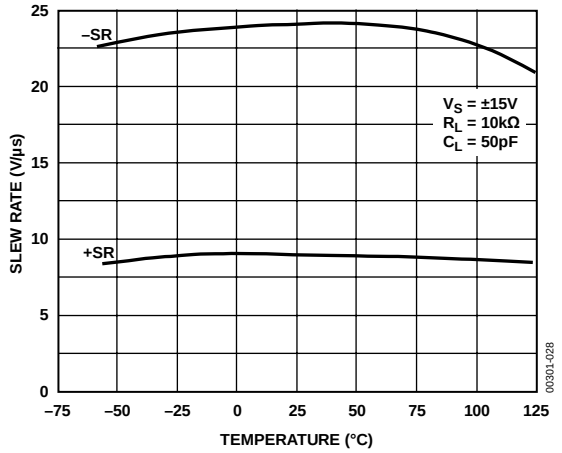


Figure 29. OP482 Slew Rate vs. Temperature

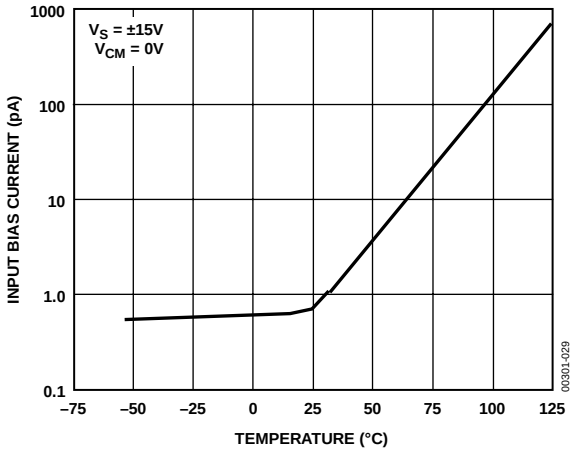


Figure 30. OP482 Input Bias Current vs. Temperature

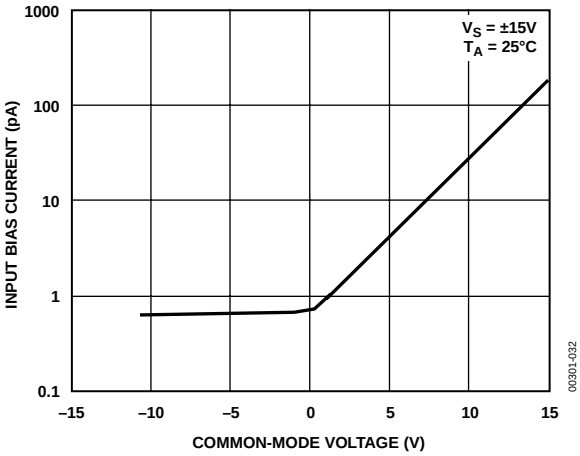


Figure 33. OP482 Input Bias Current vs. Common-Mode Voltage

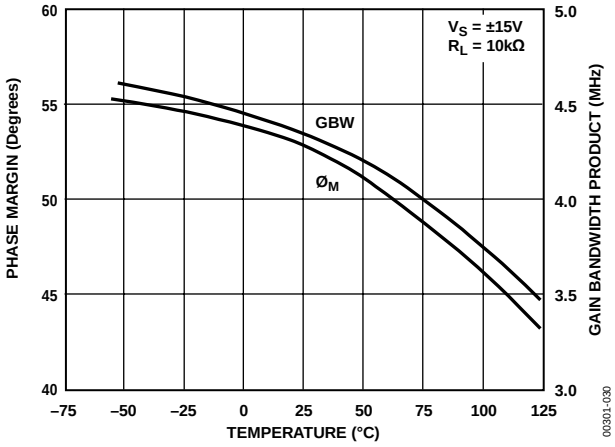


Figure 31. OP482 Phase Margin and Gain Bandwidth Product vs. Temperature

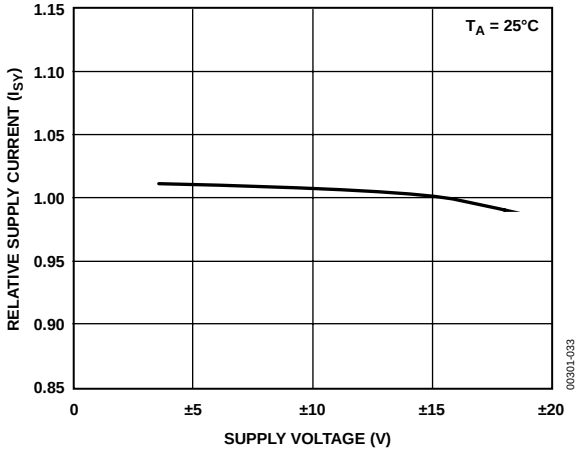


Figure 34. OP482 Relative Supply Current vs. Supply Voltage

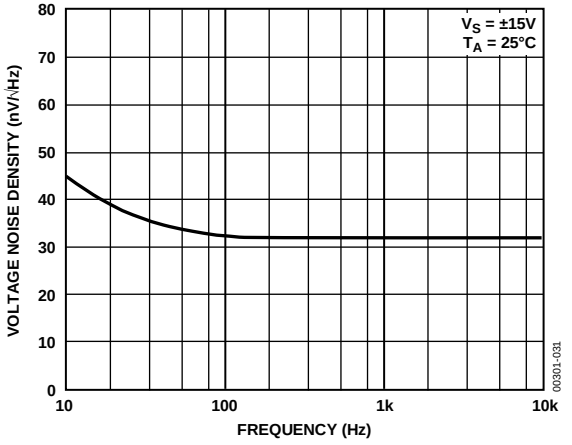


Figure 32. OP482 Voltage Noise Density vs. Frequency

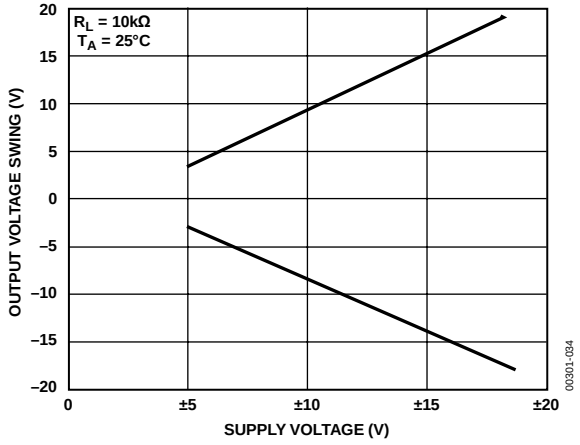


Figure 35. OP482 Output Voltage Swing vs. Supply Voltage

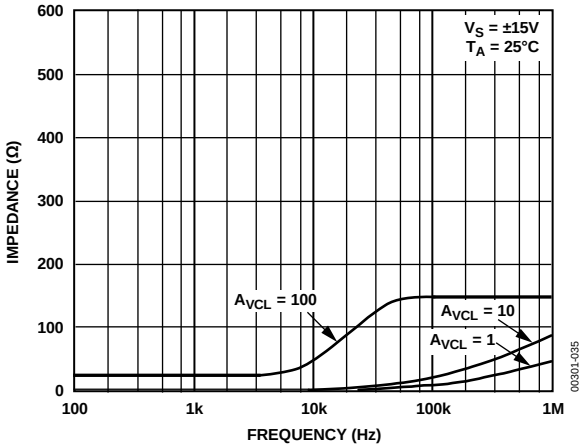


Figure 36. OP482 Closed-Loop Output Impedance vs. Frequency

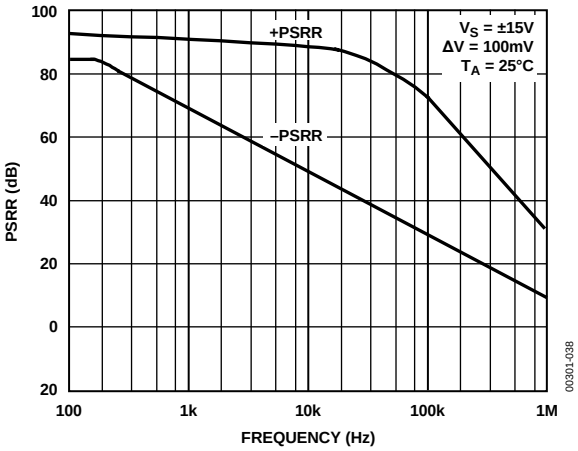


Figure 39. OP482 Power Supply Rejection Ratio (PSRR) vs. Frequency

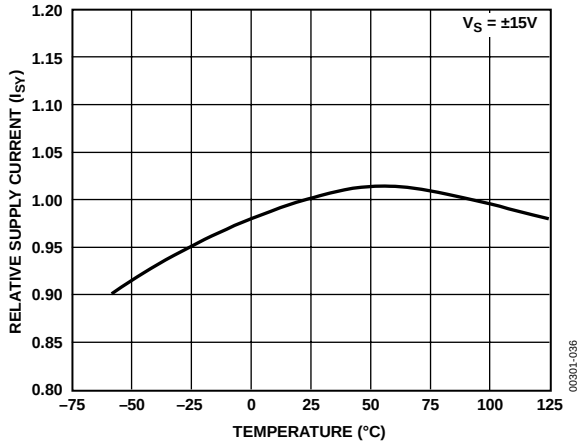


Figure 37. OP482 Relative Supply Current vs. Temperature

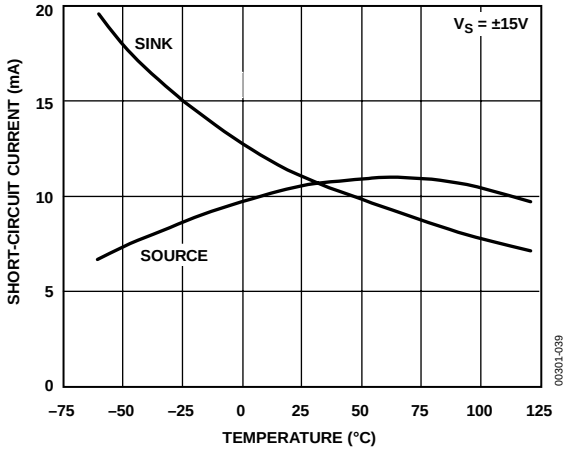


Figure 40. OP482 Short-Circuit Current vs. Temperature

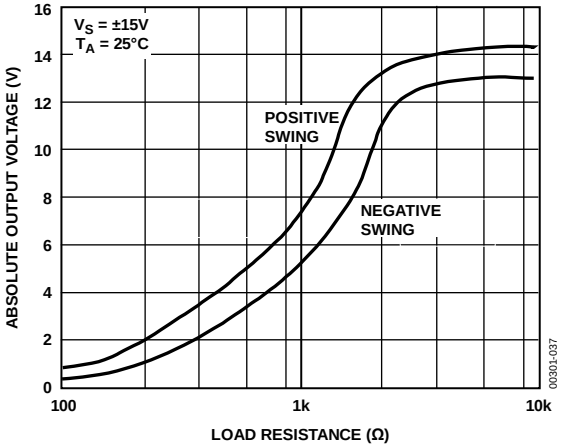


Figure 38. OP482 Maximum Output Voltage vs. Load Resistance

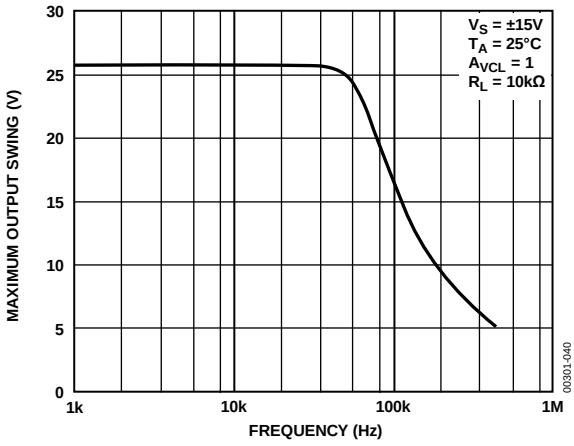


Figure 41. OP482 Maximum Output Swing vs. Frequency

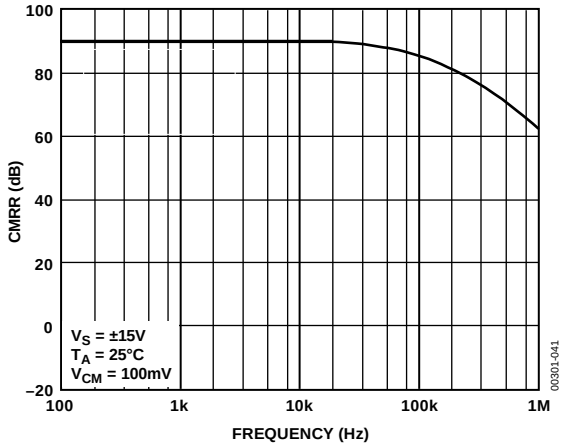


Figure 42. OP482 Common-Mode Rejection Ratio (CMRR) vs. Frequency

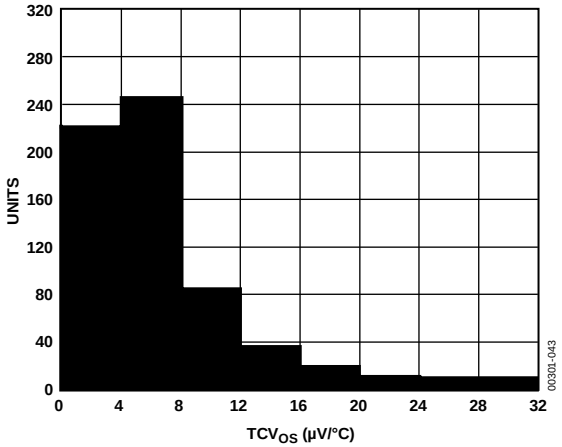


Figure 44. OP482 TCV_{OS} Distribution, PDIP Package

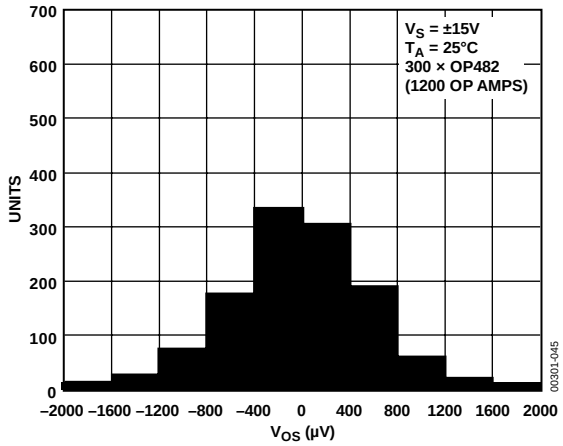


Figure 43. OP482 VOS Distribution, PDIP Package

APPLICATIONS INFORMATION

The OP282 and OP482 are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

HIGH-SIDE SIGNAL CONDITIONING

Many applications require the sensing of signals near the positive rail. OP282 and OP482 were tested and are guaranteed over a common-mode range ($-11\ V \le V_{CM} \le +15\ V$) that includes the positive supply.

One application where such sensing is commonly used is in the sensing of power supply currents. Therefore, the OP282/OP482 can be used in current sensing applications, such as the partial circuit shown in Figure 45. In this circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown here, is amplified and compared to 7.5 V. The output can then be used for current limiting.

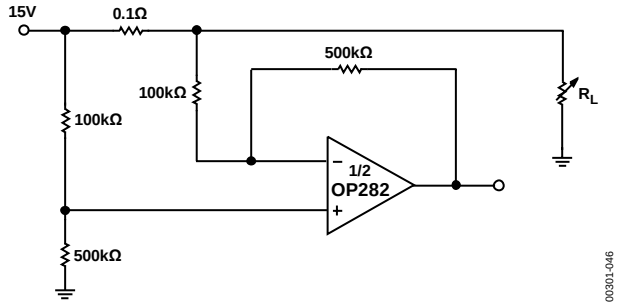


Figure 45. High-Side Signal Conditioning

PHASE INVERSION

Most JFET input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the OP282/OP482, a negative signal in excess of 11 V causes phase inversion. This is caused by saturation of the input stage, leading to the forward-biasing of a gate-drain diode. Phase reversal in the OP282/OP482 can be prevented by using Schottky diodes to clamp the input terminals to each other and to the supplies. In the simple buffer circuit shown in Figure 46, D1 protects the op amp against phase reversal. R1, D2, and D3 limit the input current when the input exceeds the supply rail. The resistor should be selected to limit the amount of input current below the absolute maximum rating.

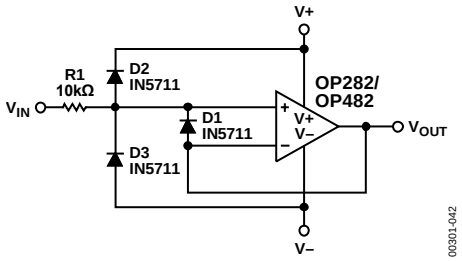


Figure 46. Phase Reversal Solution Circuit

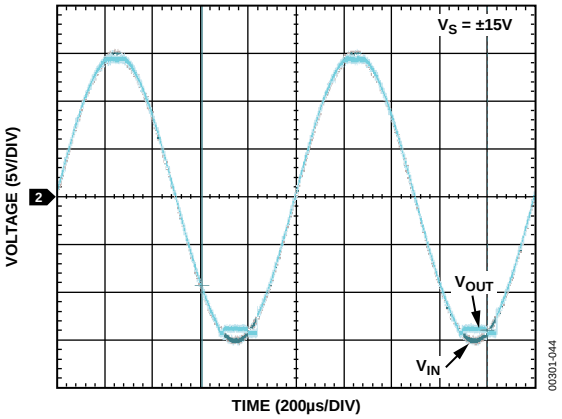


Figure 47. No Phase Reversal

ACTIVE FILTERS

The wide bandwidth and high slew rates of the OP282/OP482 make either one an excellent choice for many filter applications.

There are many active filter configurations, but the four most popular configurations are Butterworth, elliptic, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic, as shown in Table 4.

Table 4. Active Filter Configurations

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good		Maximum flat	
Chebyshev	Good	Moderate	Nonlinear	Equal ripple	
Elliptic	Best	Poor		Equal ripple	Equal ripple
Bessel (Thompson)	Poor	Best	Linear		

PROGRAMMABLE STATE VARIABLE FILTER

The circuit shown in Figure 48 can be used to accurately program the Q, the cutoff frequency (f_C), and the gain of a two-pole state variable filter. OP482 devices have been used in this design because of their high bandwidths, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are used in the voltage mode; therefore, many values are dependent on the accuracy of the DAC only and not on the absolute values of the DAC's resistive ladders. This makes this circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1.

This cutoff frequency can now be expressed as

$$f_C = \frac{1}{2\pi R1C1}\left(\frac{D1}{256}\right)$$

where *D1* is the digital code for the DAC.

The gain of this circuit is set by adjusting D3. The gain equation is

$$Gain = \frac{R4}{R5}\left(\frac{D3}{256}\right)$$

DAC 2 is used to set the Q of the circuit. Adjusting this DAC controls the amount of feedback from the band-pass node to the input summing node. Note that the digital value of the DAC is in the numerator; therefore, zero code is not a valid operating point.

$$Q = \frac{R2}{R3}\left(\frac{256}{D2}\right)$$

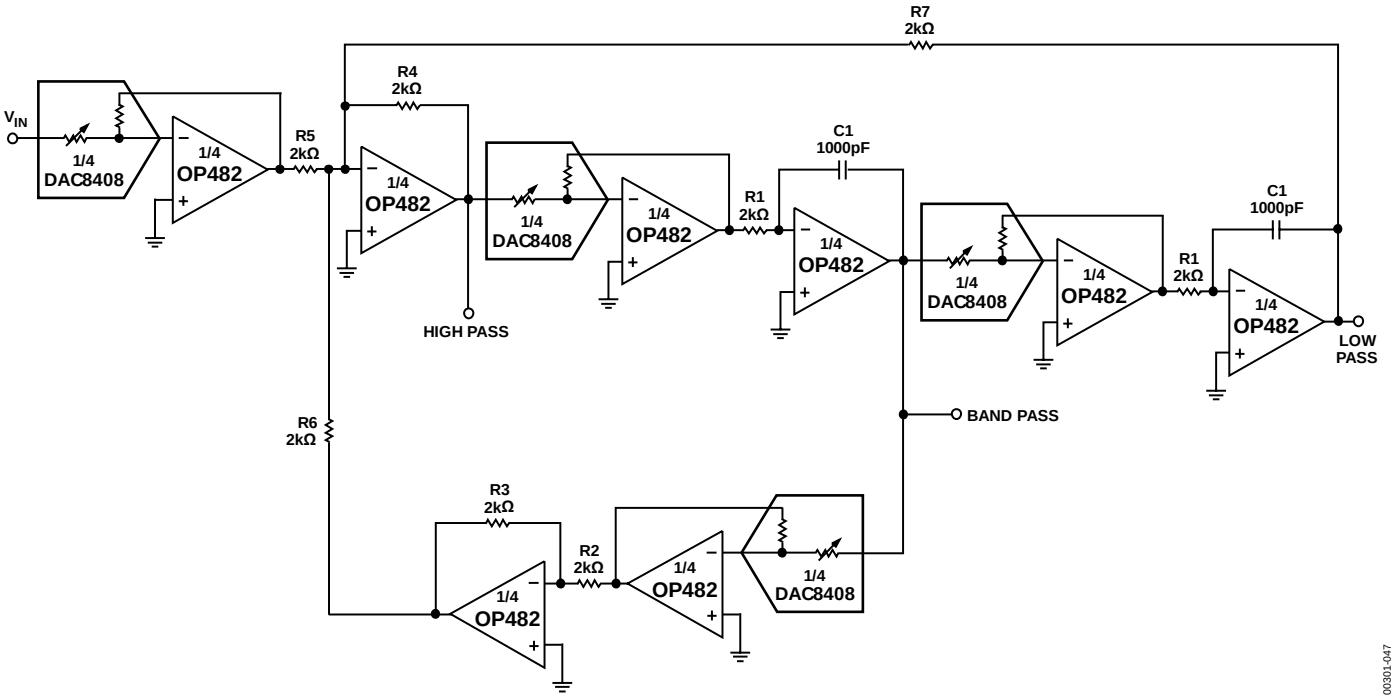
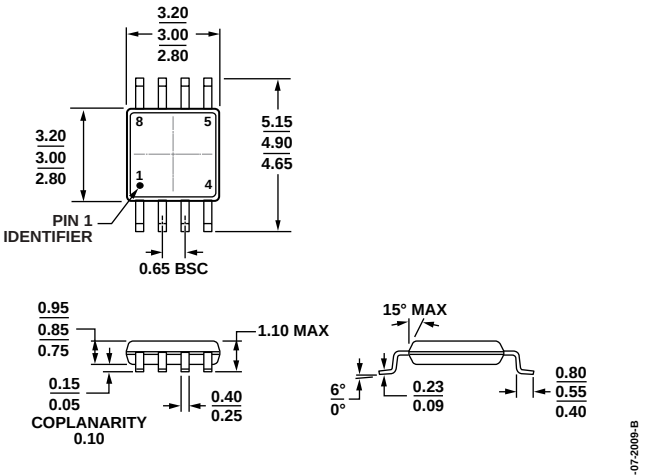


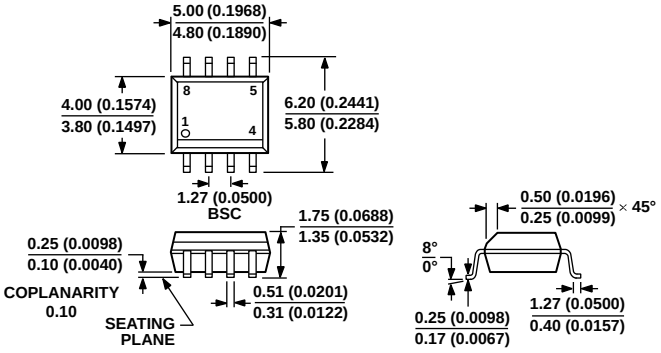
Figure 48. Programmable State Variable Filter

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

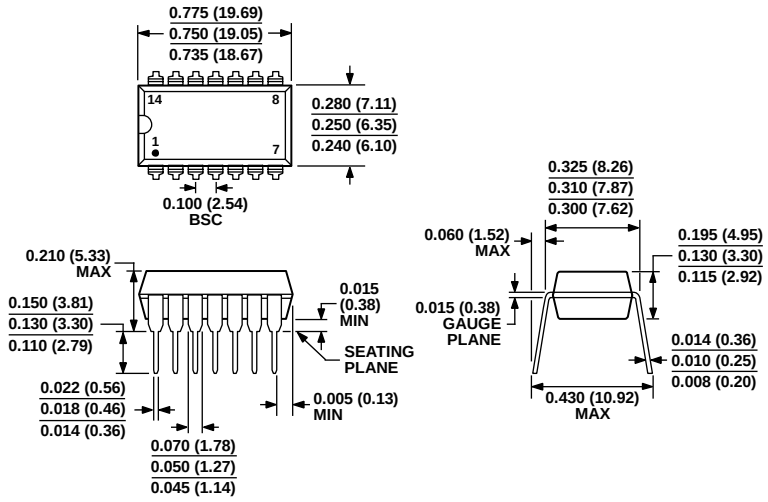
Figure 49. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

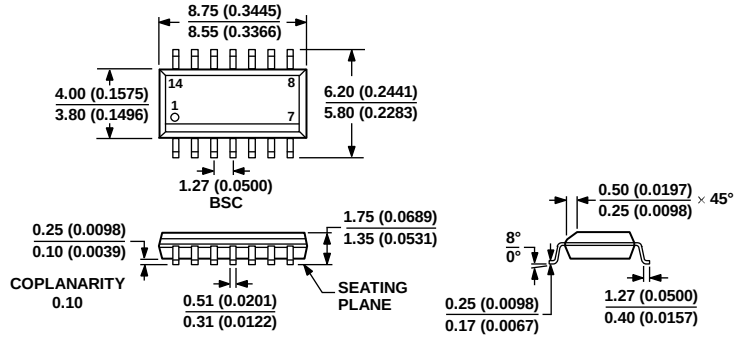
Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
S-Suffix (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 51. 14-Lead Plastic Dual In-Line Package [PDIP]
P-Suffix (N-14)
Dimension shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 52. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
S-Suffix (R-14)
Dimensions shown in millimeters and (inches)

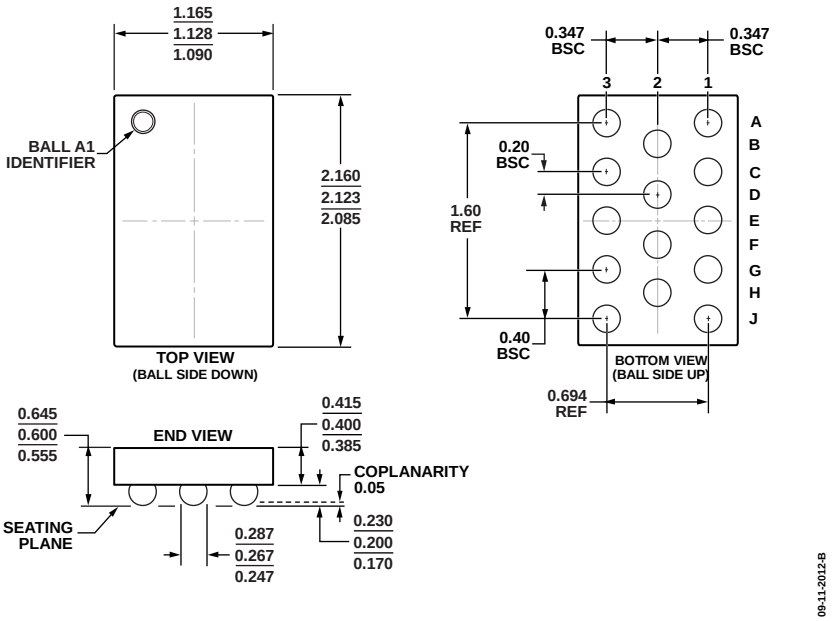


Figure 53. 14-Ball Wafer Level Chip Scale Package [WLCSP]
CB-14-2
Controlling dimensions are millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
OP282ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282ARMZ-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP482ACBZ-RL	−40°C to +85°C	14-Ball WLCSP	CB-14-2	A2J
OP482ACBZ-R7	−40°C to +85°C	14-Ball WLCSP	CB-14-2	A2J
OP482GPZ	−40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)	
OP482GS	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL7	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL7	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	

[1] Z = RoHS Compliant Part.

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D00301-0-9/13(I)

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