THE DATASHEET OF

OP492GS-REEL

Dual/Quad Single-Supply Operational Amplifiers

Data Sheet

OP292/OP492

FEATURES

- Single-supply operation: 4.5 V to 33 V
- Input common-mode includes ground
- Output swings to ground
- High slew rate: 3 V/µs
- High gain bandwidth: 4 MHz
- Low input offset voltage
- High open-loop gain
- No phase inversion

APPLICATIONS

- Disk drives
- Mobile phones
- Servo controls
- Modems and fax machines
- Pagers
- Power supply monitors and controls
- Battery-operated instrumentation

PIN CONFIGURATIONS

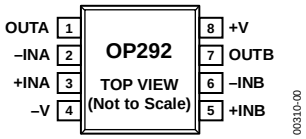

Figure 1. 8-Lead Narrow-Body SOIC (S-Suffix)

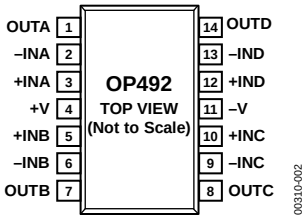

Figure 2. 14-Lead Narrow-Body SOIC (S-Suffix)

GENERAL DESCRIPTION

The OP292/OP492 are low cost, general-purpose dual and quad operational amplifiers designed for single-supply applications and are ideal for 5 V systems.

Fabricated on Analog Devices, Inc., CBCMOS process, the OP292/OP492 series has a PNP input stage that allows the input voltage range to include ground. A BiCMOS output stage enables the output to swing to ground while sinking current.

The OP292/OP492 series is unity-gain stable and features an outstanding combination of speed and performance for single- or dual-supply operation. The OP292/OP492 provide a high slew rate, high bandwidth, with open-loop gain exceeding 40,000 and offset voltage under 0.8 mV (OP292) and 1 mV (OP492). With these combinations of features and low supply current, the OP292/OP492 series is an excellent choice for battery-operated applications.

The OP292/OP492 series performance is specified for single- or dual-supply voltage operation over the extended industrial temperature range (−40°C to +125°C).

Rev. D

Document Feedback

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REVISION HISTORY

8/15—Rev. C to Rev. D

Change to General Description Section ... 1
Changes to Ordering Guide ... 17

5/09—Rev. B to Rev. C

Deleted 8-Lead PDIP and 14-Lead PDIP ... Universal
Changes to Features Section and General Description Section ... 1
Changed V_S = 5 V to V_S = ±15 V ... 4
Changes to Table 3 and Table 4 ... 6
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10/02—Rev. A to Rev. B

Edits to Outline Dimensions ... 18

1/02—Rev. 0 to Rev. A

Deleted Wafer Test Limits ... 4
Deleted Dice Characteristics ... 4
Edits to Ordering Guide ... 20

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 5 V, V_{CM} = 0 V, V_O = 2 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP292	V_{OS}			0.1	0.8	mV
		−40°C ≤ T_A ≤ +85°C		0.3	1.2	mV
		−40°C ≤ T_A ≤ +125°C		0.5	2.5	mV
OP492	V_{OS}			0.1	1	mV
		−40°C ≤ T_A ≤ +85°C		0.3	1.5	mV
		−40°C ≤ T_A ≤ +125°C		0.5	2.5	mV
Input Bias Current	I_B			450	700	nA
		−40°C ≤ T_A ≤ +85°C		0.75	2.5	µA
		−40°C ≤ T_A ≤ +125°C		3.0	5.0	µA
Input Offset Current	I_{OS}			7	50	nA
		−40°C ≤ T_A ≤ +85°C		100	700	nA
		−40°C ≤ T_A ≤ +125°C		0.4	1.2	µA
Input Voltage Range			0		4.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.0 V	75	95		dB
		−40°C ≤ T_A ≤ +85°C	70	93		dB
		−40°C ≤ T_A ≤ +125°C	65	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4 V	25	200		V/mV
		−40°C ≤ T_A ≤ +85°C	10	100		V/mV
		−40°C ≤ T_A ≤ +125°C	5	50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		2	10	µV/°C
Long-Term V_{OS} Drift[1]	$\Delta V_{OS}/\Delta T$			1		µV/Month
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +85°C		6		pA/°C
		−40°C ≤ T_A ≤ +125°C		400		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		1.5		pA/°C
		−40°C ≤ T_A ≤ +125°C		2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing						
High	V_{OUT}	R_L = 100 kΩ to GND				
		−40°C ≤ T_A ≤ +125°C	4.0	4.3		V
		R_L = 2 kΩ to GND	3.8	4.1		V
		−40°C ≤ T_A ≤ +125°C	3.7	3.9		V
Low	V_{OUT}	R_L = 100 kΩ to V+		8	20	mV
		−40°C ≤ T_A ≤ +125°C		12	20	mV
		R_L = 2 kΩ to V+		280	450	mV
		−40°C ≤ T_A ≤ +125°C		300	550	mV
Short-Circuit Current Limit	I_{SC}		5	8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 30 V, V_O = 2 V	75	95		dB
		−40°C ≤ T_A ≤ +125°C	70	90		dB
Supply Current Per Amp	I_{SY}	V_O = 2 V		0.8	1.2	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		3		V/µs
		−40°C ≤ T_A ≤ +125°C	1	2		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	φ_m			75		Degrees
Channel Separation	CS	f_O = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n			0.7		pA/√Hz

[1] Long-term offset voltage drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C with LTPD of 1.3.

V_S =±15 V, V_{CM} = 0 V, V_O = 2 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP292	V_{OS}			1.0	2.0	mV
		−40°C ≤ T_A ≤ +85°C		1.2	2.5	mV
		−40°C ≤ T_A ≤ +125°C		1.5	3	mV
OP492	V_{OS}			1.4	2.5	mV
		−40°C ≤ T_A ≤ +85°C		1.7	2.8	mV
		−40°C ≤ T_A ≤ +125°C		2	3	mV
Input Bias Current	I_B			375	700	nA
		−40°C ≤ T_A ≤ +125°C		0.5	1	µA
Input Offset Current	I_{OS}			7	50	nA
		−40°C ≤ T_A ≤ +85°C		20	100	nA
		−40°C ≤ T_A ≤ +125°C		0.4	1.2	µA
Input Voltage Range[1]			−11		+11	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	78	100		dB
		−40°C ≤ T_A ≤ +125°C	75	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O =±10 V	25	120		V/mV
		−40°C ≤ T_A ≤ +85°C	10	75		V/mV
		−40°C ≤ T_A ≤ +125°C	5	60		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		4	10	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$	−40°C ≤ T_A ≤ +125°C		3		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ to GND	±11	±12.2		V
		−40°C ≤ T_A ≤ +125°C	±10	±11		V
		R_L = 100 kΩ to GND	±13.8	±14.3		V
		−40°C ≤ T_A ≤ +125°C	±13.5	±14.0		mV
Short-Circuit Current Limit	I_{SC}	Short circuit to GND	8	10.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.25 V to ±15 V	75	86		dB
		−40°C ≤ T_A ≤ +125°C	70	83		dB
Supply Current Per Amp	I_{SY}	V_O = 0 V		1	1.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ	2.5	4		V/µs
		−40°C ≤ T_A ≤ +125°C	2	3		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	φ_m			75		Degrees
Channel Separation	CS	f_O = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		25		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n			0.7		pA/√Hz

[1] Input voltage range is guaranteed by CMRR tests.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	33 V
Input Voltage Range[1]	−15 V to +14 V
Differential Input Voltage[1]	V[1]
Output Short-Circuit Duration	Unlimited
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	300°C

[1] For supply voltages less than 36 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in the circuit board for the surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	158	43	°C/W
14-Lead SOIC	120	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

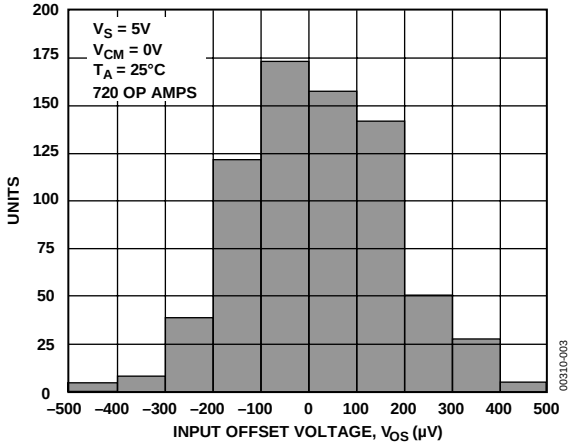


Figure 3. OP292 Input Offset Voltage Distribution @ 5 V

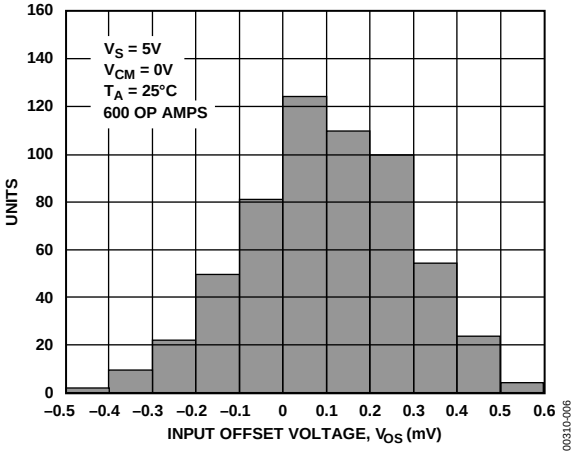


Figure 6. OP492 Input Offset Voltage Distribution @ 5 V

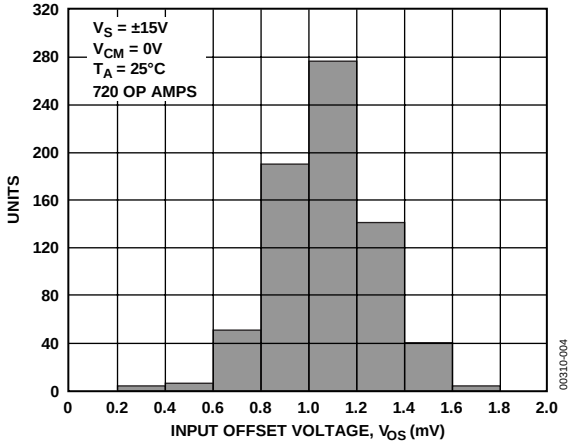


Figure 4. OP292 Input Offset Voltage Distribution @ ±15 V

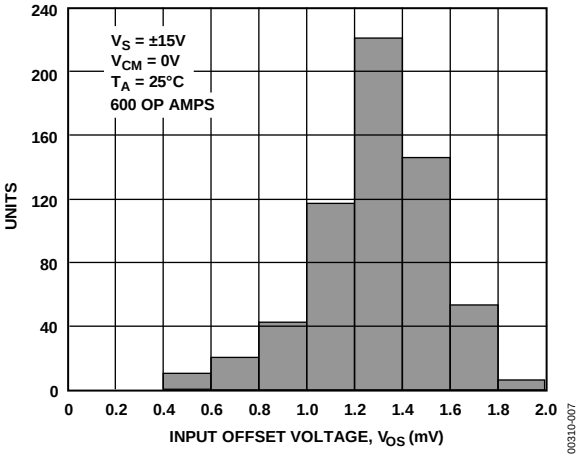


Figure 7. OP492 Input Offset Voltage Distribution @ ±15 V

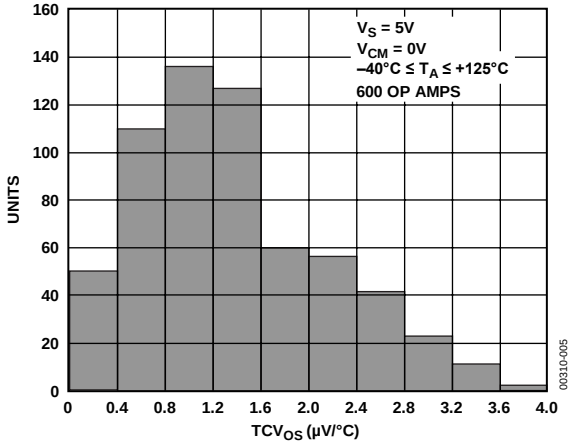


Figure 5. OP292 Temperature Drift (TCV_{OS}) Distribution @ 5 V

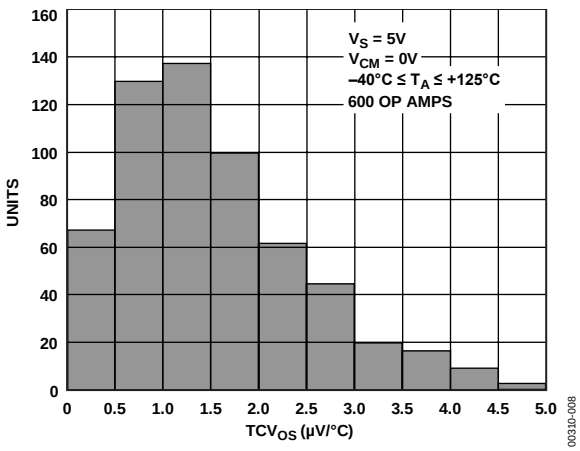


Figure 8. OP492 Temperature Drift (TCV_{OS}) Distribution @ 5 V

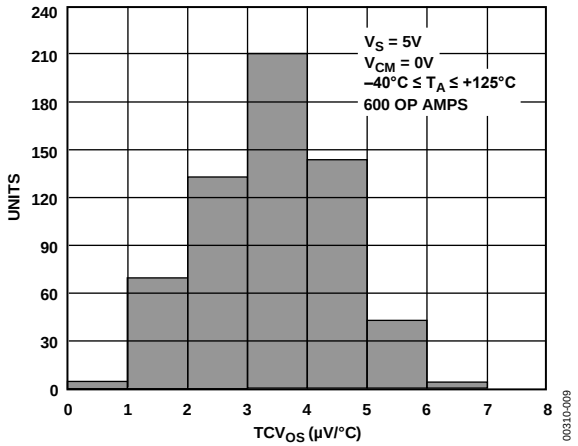


Figure 9. OP292 Temperature Drift (TCV_{OS}) Distribution @ ±15 V

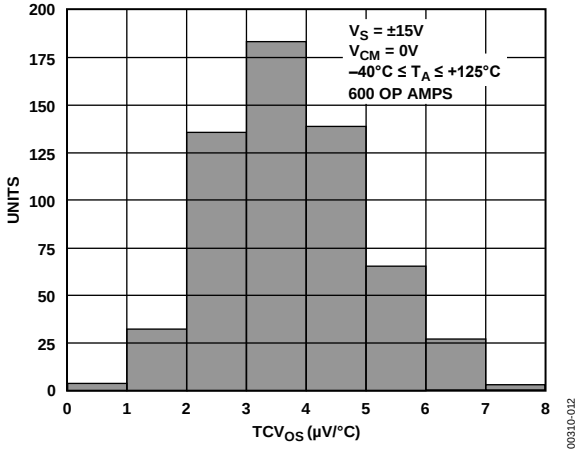


Figure 12. OP492 Temperature Drift (TCV_{OS}) Distribution @ ±15 V

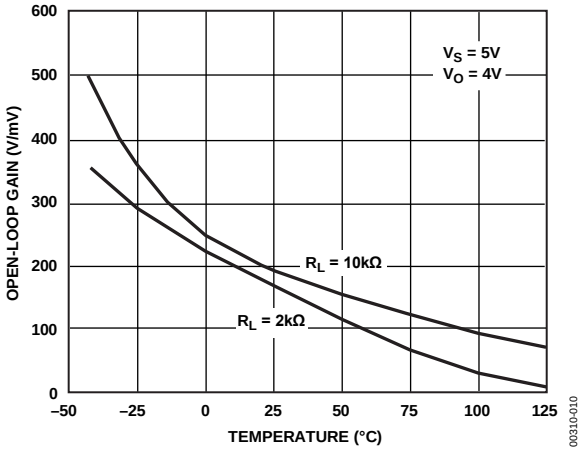


Figure 10. OP292 Open-Loop Gain vs. Temperature @ 5 V

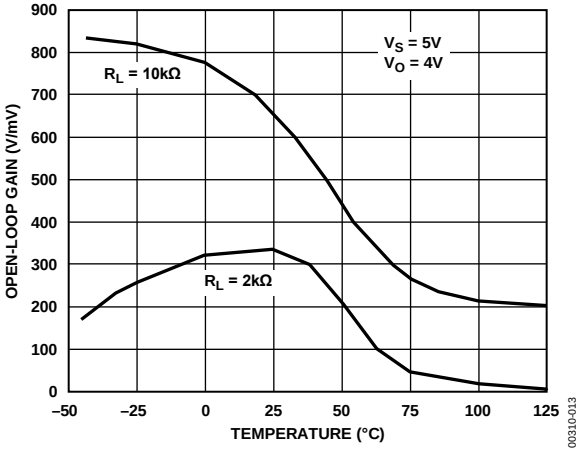


Figure 13. OP492 Open-Loop Gain vs. Temperature @ 5 V

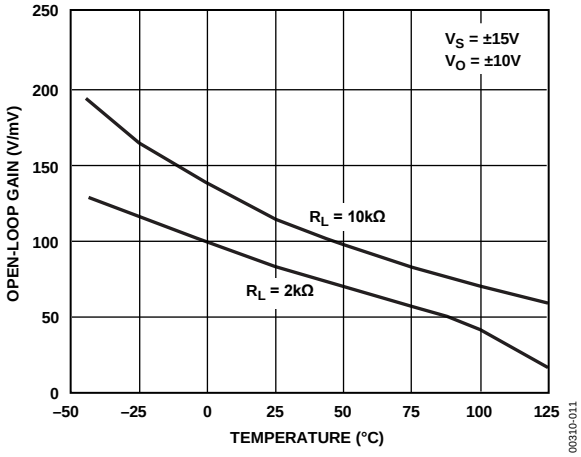


Figure 11. OP292 Open-Loop Gain vs. Temperature @ ±15 V

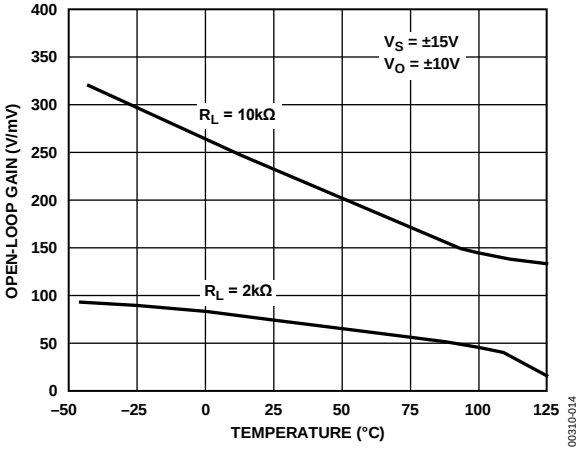


Figure 14. OP492 Open-Loop Gain vs. Temperature @ ±15 V

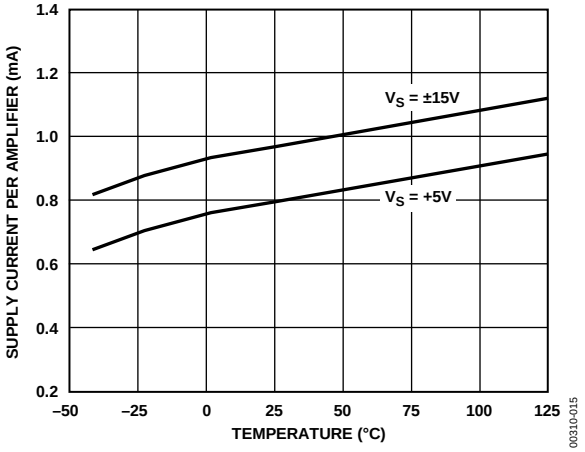


Figure 15. OP292 Supply Current per Amplifier vs. Temperature

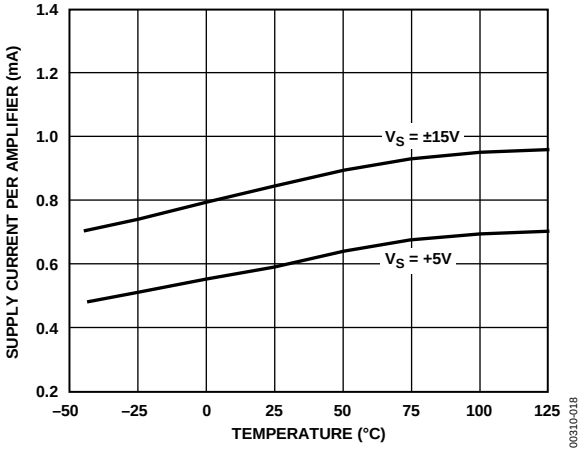


Figure 18. OP492 Supply Current per Amplifier vs. Temperature

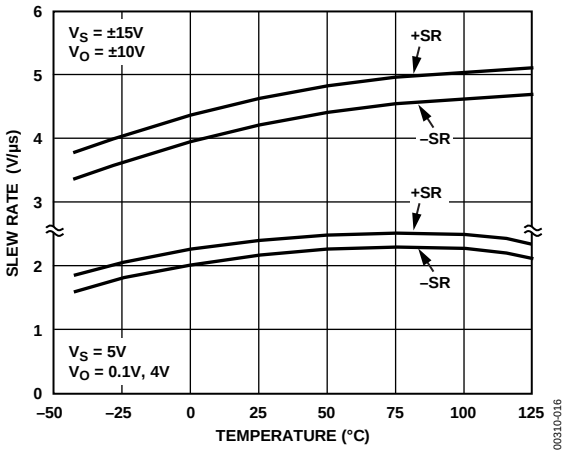


Figure 16. OP292 Slew Rate vs. Temperature

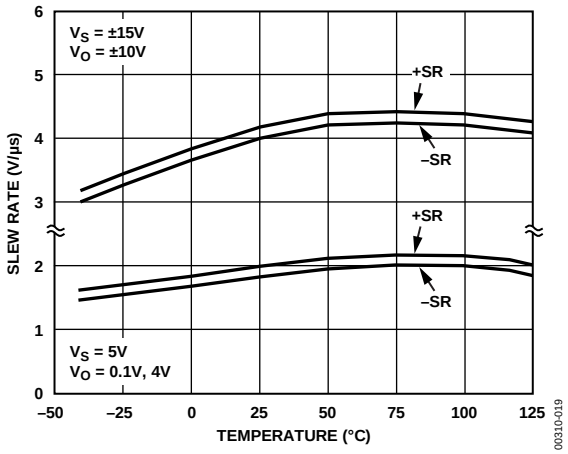


Figure 19. OP492 Slew Rate vs. Temperature

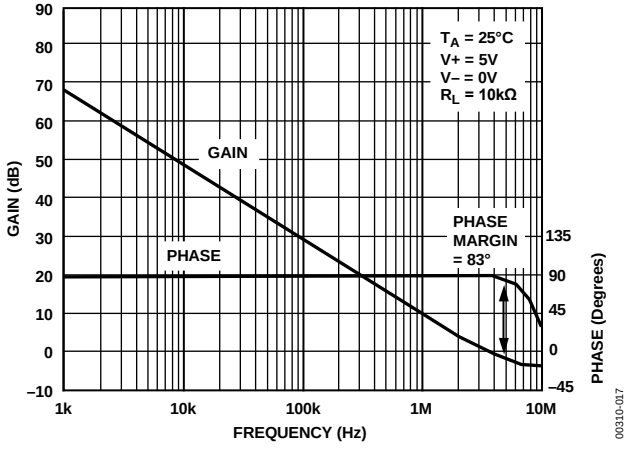


Figure 17. OP292/OP492 Open-Loop Gain and Phase vs. Frequency @ 5 V

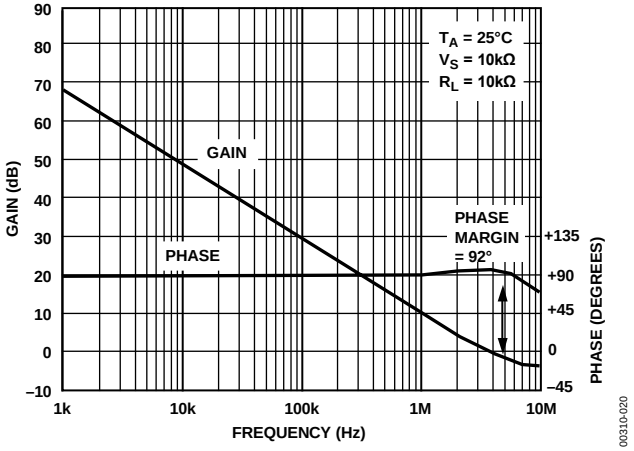


Figure 20. OP292/OP492 Open-Loop Gain and Phase vs. Frequency @ ±15 V

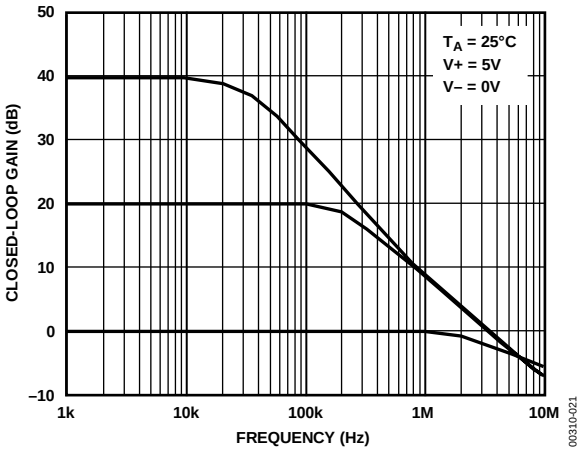


Figure 21. OP292/OP492 Closed-Loop Gain vs. Frequency @ 5 V

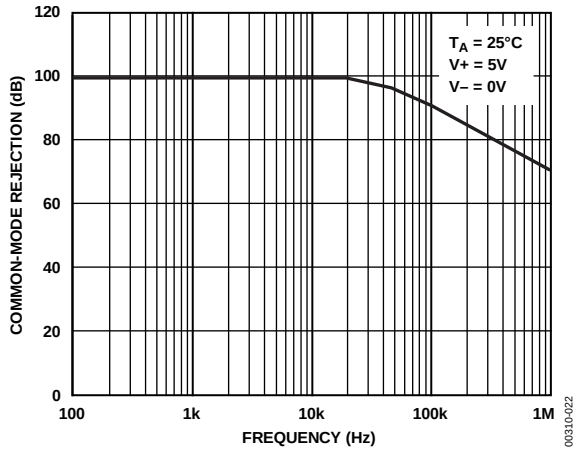


Figure 22. OP292/OP492 CMR vs. Frequency @ 5 V

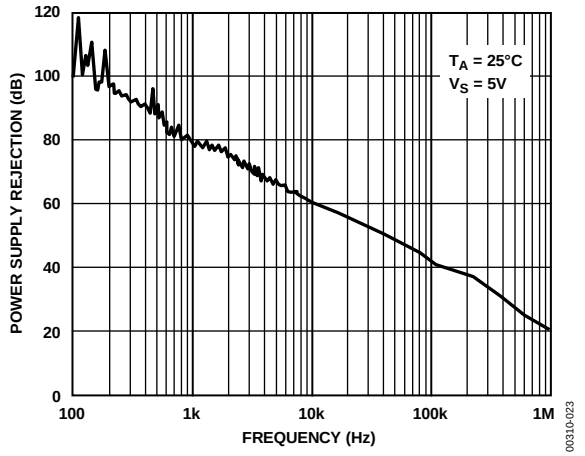


Figure 23. OP292/OP492 PSR vs. Frequency @ 5 V

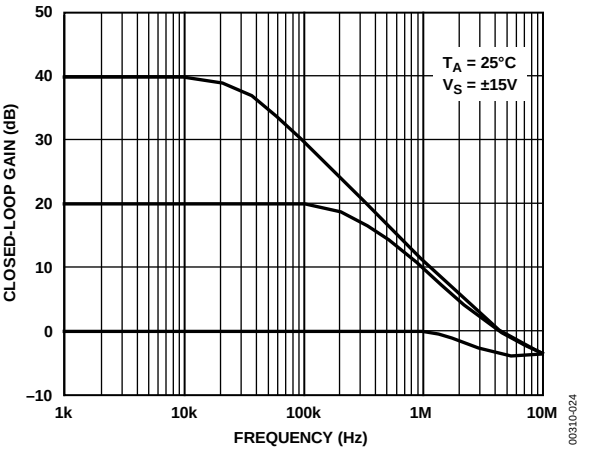


Figure 24. OP292/OP492 Closed-Loop Gain vs. Frequency @ ±15 V

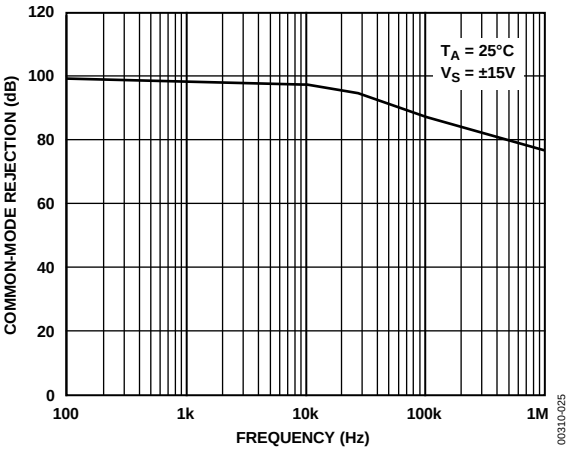


Figure 25. OP292/OP492 CMR vs. Frequency @ ±15 V

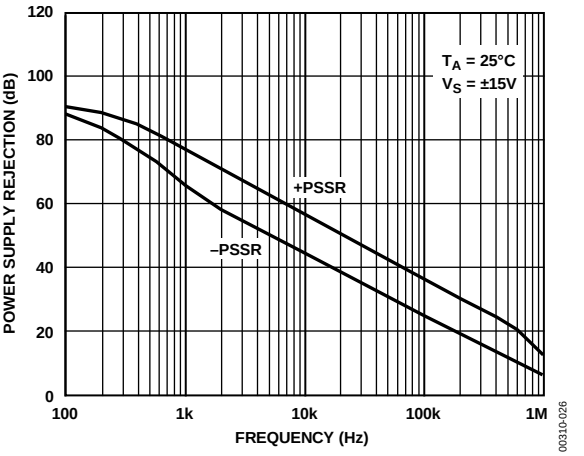


Figure 26. OP292/OP492 PSR vs. Frequency @ ±15 V

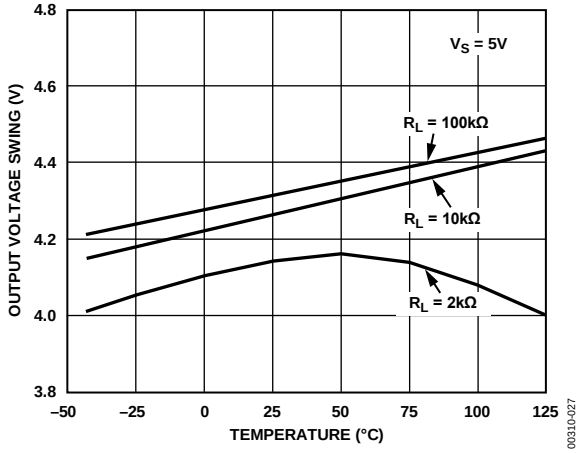


Figure 27. OP292/OP492 V_{OUT} Swing vs. Temperature @ 5 V

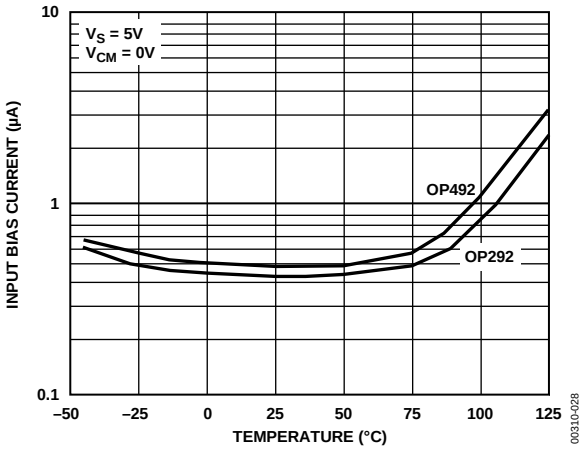


Figure 28. OP292/OP492 Input Bias Current vs. Temperature @ 5 V

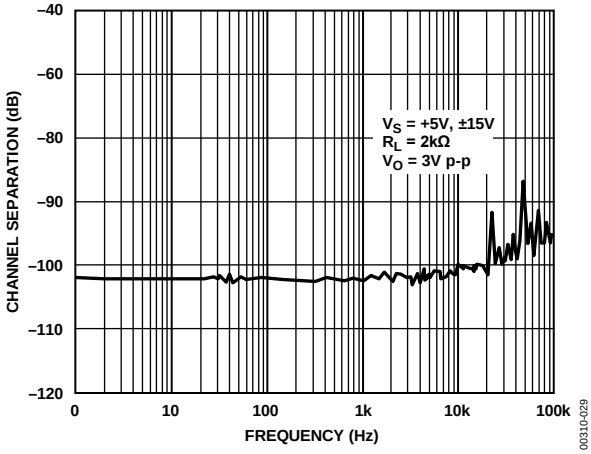


Figure 29. OP292/OP492 Channel Separation

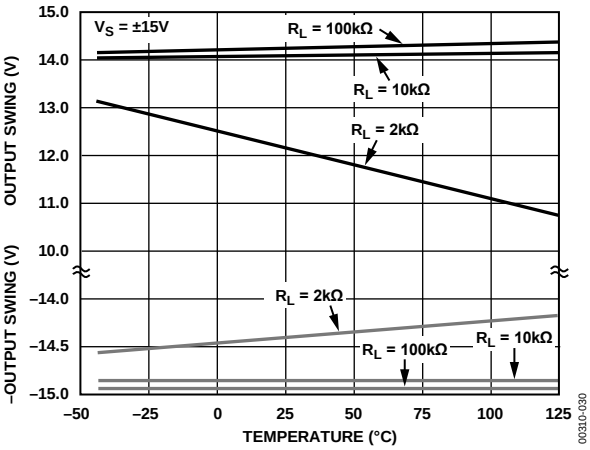


Figure 30. OP292/OP492 V_{OUT} Swing vs. Temperature @ ±15 V

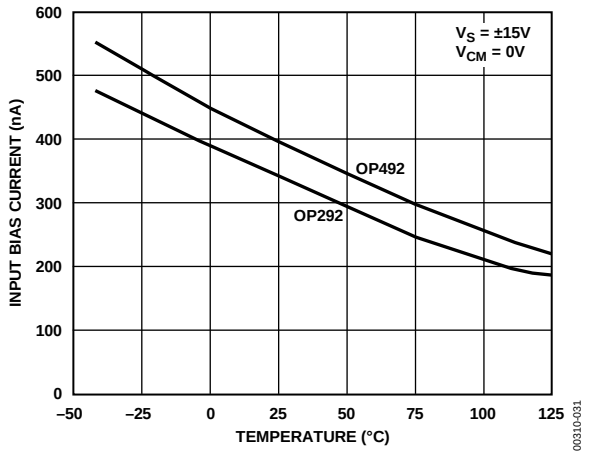


Figure 31. OP292/OP492 Input Bias Current vs. Temperature @ ±15 V

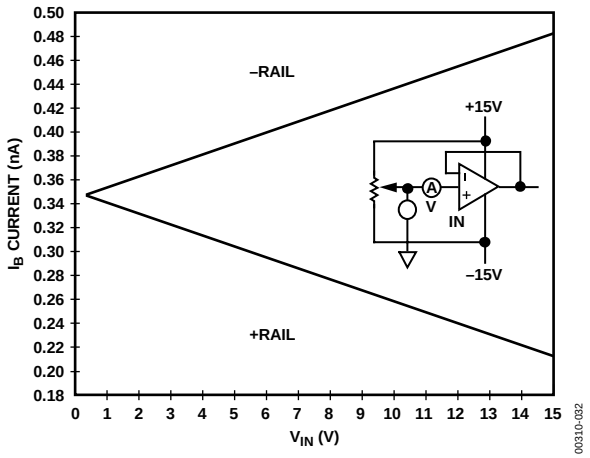


Figure 32. OP292/OP492 I_B Current vs. Common-Mode Voltage

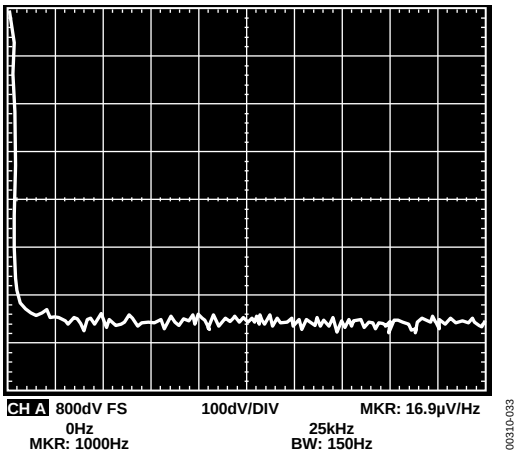


Figure 33. Voltage Noise Density

APPLICATIONS INFORMATION

PHASE REVERSAL

The OP492 has built-in protection against phase reversal when the input voltage goes to either supply rail. In fact, it is safe for the input to exceed either supply rail by up to 0.6 V with no risk of phase reversal. However, the input should not go beyond the positive supply rail by more than 0.9 V; otherwise, the output will reverse phase. If this condition occurs, the problem can be fixed by adding a 5 kΩ current limiting resistor in series with the input pin. With this addition, the input can go to more than 5 V beyond the positive rail without phase reversal.

An input voltage that is as much as 5 V below the negative rail will not result in phase reversal.

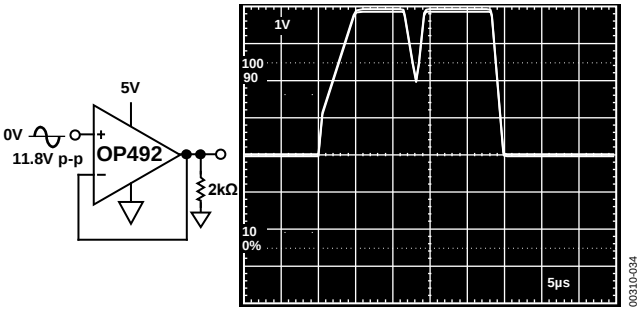


Figure 34. Output Phase Reverse If Input Exceeds the Positive Supply (V+) by More Than 0.9 V

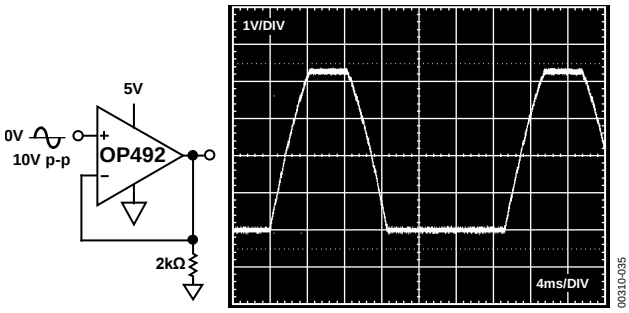


Figure 35. No Negative Rail Phase Reversal, Even with Input Signal at 5 V Below Ground

POWER SUPPLY CONSIDERATIONS

The OP292/OP492 are designed to operate equally well at single +5 V or ±15 V supplies. The lowest supply voltage recommended is 4.5 V.

It is a good design practice to bypass the supply pins with a 0.1 µF ceramic capacitor. It helps improve filtering of high frequency noise.

For dual-supply operation, the negative supply (V−) must be applied at the same time, or before V+. If V+ is applied before V−, or in the case of a loss of the V− supply, while either input is connected to ground or another low impedance source, excessive input current may result. Potentially damaging levels of input current can destroy the amplifier. If this condition can exist, simply add a l kΩ or larger resistor in series with the input to eliminate the problem.

TYPICAL APPLICATIONS

DIRECT ACCESS ARRANGEMENT FOR TELEPHONE LINE INTERFACE

Figure 36 shows a 5 V single-supply transmit/receive telephone line interface for a modem circuit. It allows full duplex transmission of modem signals on a transformer-coupled 600 V line in a differential manner. The transmit section gain can be set for the specific modem device output. Similarly, the receive amplifier gain can be appropriately selected based on the modem device input requirements. The circuit operates on a single 5 V supply. The standard value resistors allow the use of a SIP-packaged resistor array; coupled with a quad op amp in a single package, this offers a compact, low part count solution.

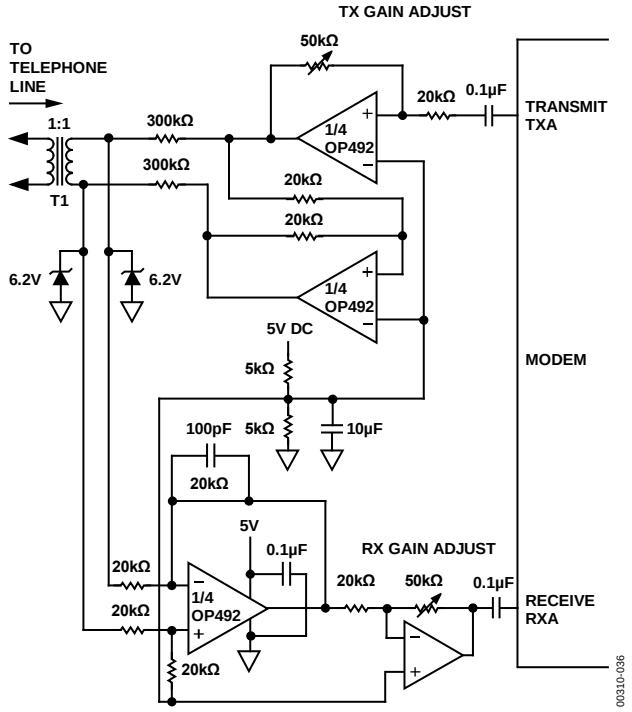


Figure 36. Universal Direct Access Arrangement for Telephone Line Interface

SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER

A low cost, single-supply instrumentation amplifier can be built as shown in Figure 37. The circuit uses two op amps to form a high input impedance differential amplifier. Gain can be set by selecting resistor R_G, which can be calculated using the transfer function equation. Normally, V_{REF} is set to 0 V. Then the output voltage is a function of the gain times the differential input voltage. However, the output can be offset by setting V_{REF} from 0 V to 4 V, as long as the input common-mode voltage of the amplifier is not exceeded.

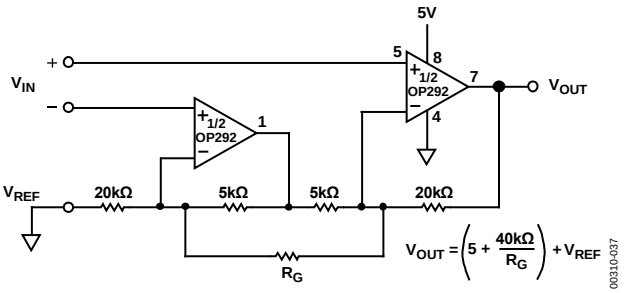


Figure 37. Single-Supply Instrumentation Amplifier

In this configuration, the output can swing to near 0 V; however, be careful because the common-mode voltage range of the input cannot operate to 0 V. This is because of the limitation of the circuit configuration where the first amplifier must be able to swing below ground to attain a 0 V common-mode voltage, which it cannot do. Depending on the gain of the instrumentation amplifier, the input common-mode extends to within about 0.3 V of zero. The worst-case common-mode limit for a given gain can be easily calculated.

DAC OUTPUT AMPLIFIER

The OP292/OP492 are ideal for buffering the output of single-supply digital-to-analog converters (DACs). Figure 38 shows a typical amplifier used to buffer the output of a CMOS DAC that is connected for single-supply operation. To do that, the normally current output 12-bit CMOS DAC (R-2R ladder type) is connected backward to produce a voltage output. This operating configuration necessitates a low voltage reference. In this case, a 1.235 V low power reference is used. The relatively high output impedance (10 kΩ) is buffered by the OP292, and at the same time, gained up to a much more usable level. The potentiometer provides an accurate gain trim for a 4.095 V full-scale, allowing 1 mV increment per LSB of control resolution.

The DAC8043 device comes in an 8-lead PDIP package, providing a cost-effective, compact solution to a 12-bit analog channel.

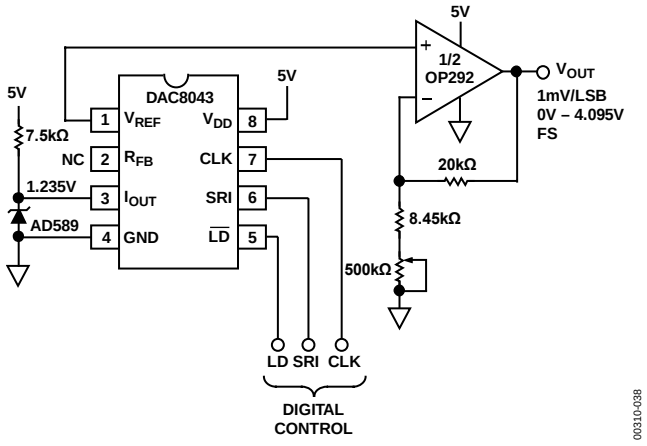
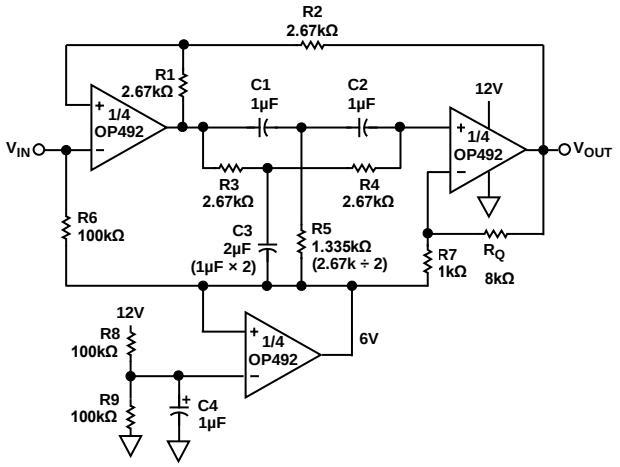


Figure 38. 12-Bit Single-Supply DAC with Serial Bus Control

50 Hz/60 Hz SINGLE-SUPPLY NOTCH FILTER

Figure 39 shows a notch filter that achieves nearly 30 dB of 60 Hz rejection while powered by only a single 12 V supply. The circuit also works well on 5 V systems. The filter uses a twin-T configuration, whose frequency selectivity depends heavily on the relative matching of the capacitors and resistors in the twin-T section. Mylar is a good choice for the capacitors of the twin-T, and the relative matching of the capacitors and resistors determines the pass-band symmetry of the filter. Using 1% resistors and 5% capacitors produces satisfactory results.

The amount of rejection and the Q of the filter is solely determined by one resistor and is shown in the table with Figure 39. The bottom amplifier is used to split the supply to bias the amplifier to midlevel. The circuit can be modified to reject 50 Hz by simply changing the resistors in the twin-T section (R1 through R4) from 2.67 kΩ to 3.16 kΩ and by changing R5 to ½ of 3.16 kΩ. For best results, the common value resistors can be from a resistor array for optimum matching characteristics.



FILTER Q	R_Q (kΩ)	REJECTION (dB)	VOLTAGE GAIN
0.75	1.0	40	1.33
1.00	2.0	35	1.50
1.25	3.0	30	1.60
2.50	8.0	25	1.80
5.00	18	20	1.90
10.00	38	15	1.95

NOTES
1. FOR 50Hz APPLICATION CHANGE R12 TO R4 TO 3.16kΩ AND R5 TO 1.58kΩ (3.16kΩ ÷ 2)

Figure 39. Single-Supply 50 Hz/60 Hz Notch Filter

FOUR-POLE BESSEL LOW-PASS FILTER

The linear phase filter in Figure 40 is designed to roll off at a voice-band cutoff frequency of 3.6 kHz. The four poles are formed by two cascading stages of 2-pole Sallen-Key filters.

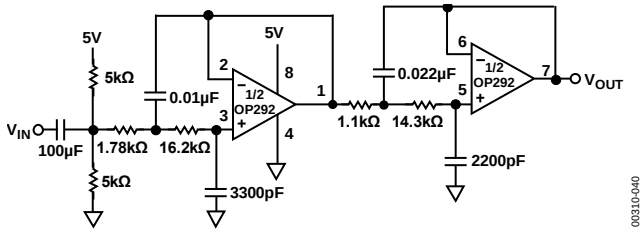


Figure 40. Four-Pole Bessel Low-Pass Filter Using Sallen-Key Topology

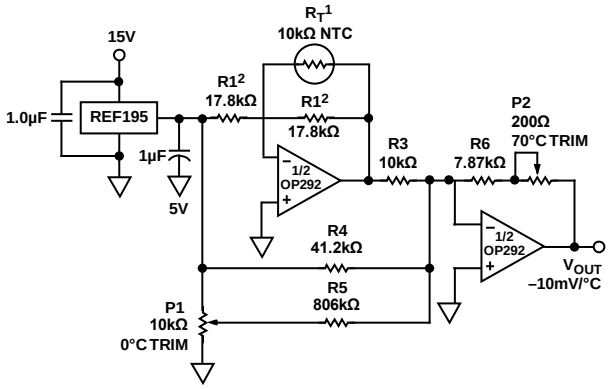
LOW COST, LINEARIZED THERMISTOR AMPLIFIER

An inexpensive thermometer amplifier circuit can be implemented using low cost thermistors. One such implementation is shown in Figure 41. The circuit measures temperature over the range of 0°C to 70°C to an accuracy of ±0.3°C as the linearization circuit works well within a narrow temperature range. However, it can measure higher temperatures but at a slightly reduced accuracy. To achieve the aforementioned accuracy, the nonlinearity of the thermistor must be corrected. This is done by connecting the thermistor in parallel with the 10 kΩ in the feedback loop of the first stage amplifier. A constant operating current of 281 µA is supplied by the resistor R1 with the 5 V reference from the REF195 such that the self-heating error of the thermistor is kept below 0.1°C.

In many cases, the thermistor is placed some distance from the signal conditioning circuit. Under this condition, a 0.1 µF capacitor placed across R2 will help to suppress noise pickup.

This linearization network creates an offset voltage that is corrected by summing a compensating current with Potentiometer P1. The temperature dependent signal is amplified by the second stage, producing a transfer coefficient of −10 mV/°C at the output.

To calibrate, a precision decade box can be used in place of the thermistor. For 0°C trim, the decade box is set to 32.650 kΩ, and P1 is adjusted until the output of the circuit reads 0 V. To trim the circuit at the full-scale temperature of 70°C, the decade box is then set to 1.752 kΩ, and P2 is adjusted until the circuit reads −0.70 V.



[1]R_T = ALPHA THERMISTOR 13A1002-C3.
[2]R1 = 0.1% IMPERIAL ASTRONICS M015.

NOTES
1. ALL RESISTORS ARE 1%, 25ppm/°C EXCEPT R5 = 1%, 100ppm/°C.

Figure 41. Low Cost Linearized Thermistor Amplifier

SINGLE-SUPPLY ULTRASONIC CLAMPING/LIMITING RECEIVER AMPLIFIER

Figure 42 shows an ultrasonic receiver amplifier using the nonlinear impedance of low cost diodes to effectively control the gain for wide dynamic range. This circuit amplifies a 40 kHz ultrasonic signal through a pair of low cost clamping amplifiers before feeding a band-pass filter to extract a clean 40 kHz signal for processing.

The signal is ac-coupled into the false-ground bias node by virtue of the capacitive piezoelectric sensing element. Rather than using an amplifier to generate a supply splitting bias, the false ground voltage is generated by a low cost resistive voltage divider.

Each amplifier stage provides ac gain while passing on the dc self-bias. As long as the output signal at each stage is less than the forward voltage of a diode, each amplifier has unrestricted gain to amplify low level signals. However, as the signal strength increases, the feedback diodes begin to conduct, shunting the feedback current, and thus reducing the gain. Although distorting the waveform, the diodes effectively maintain a relatively constant amplitude even with large signals that otherwise would saturate the amplifier. In addition, this design is considerably more stable than the feedback type AGC.

The overall circuit has a gain range from −2 to −400, where the inversion comes from the band-pass filter stage. Operating with a Q of 5, the filter restores a clean, undistorted signal to the output. The circuit also works well with 5 V supply systems.

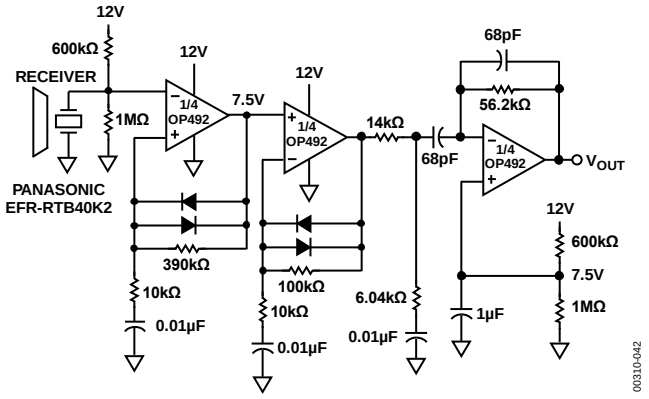


Figure 42. 40 kHz Ultrasonic Clamping/Limiting Receiver Amplifier

PRECISION SINGLE-SUPPLY VOLTAGE COMPARATOR

The OP292/OP492 have excellent overload recovery characteristics, making them suitable for precision comparator applications. Figure 43 shows the saturation recovery characteristics of the OP492. The amplifier exhibits very little propagation delay. The amplifier compares a signal to precisely <0.5 mV offset error.

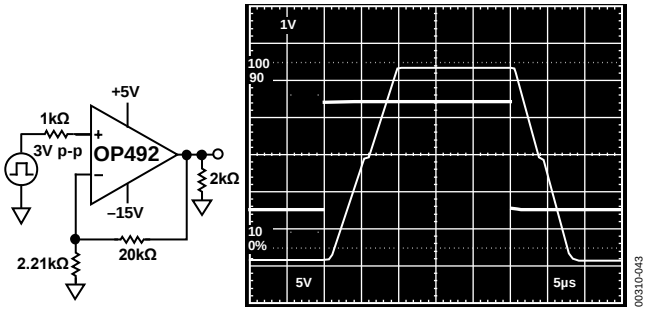


Figure 43. OP492 Has Fast Overload Recovery for Comparator Applications

PROGRAMMABLE PRECISION WINDOW COMPARATOR

The OP292/OP492 can be used for precise level detection, such as in test equipment where a signal is measured within a range (see Figure 44). A pair of 12-bit DACs sets the threshold voltage level. The DACs have serial interface, which minimizes interconnection requirements. The DAC8512 has a control resolution of 1 mV/bit. Therefore, for 5 V supply operation, the maximum DAC output is 4.095 V. However, the OP292 accepts a maximum input of 4.0 V.

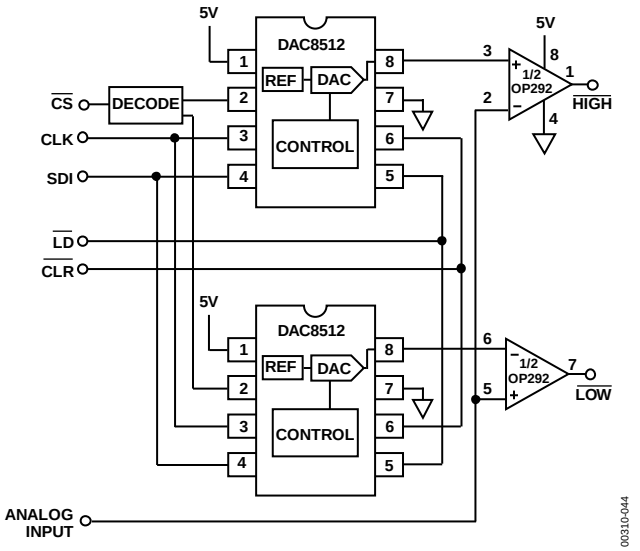
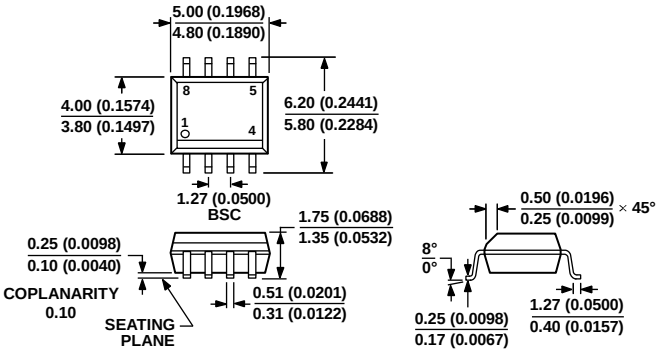


Figure 44. Programmable Window Comparator with 12-Bit Threshold Level Control

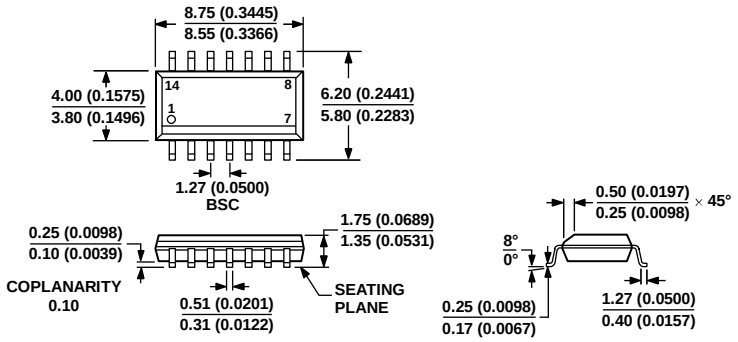
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 45. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 46. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP292GS	−40°C to +125°C	8-Lead Narrow Body SOIC_N	R-8
OP292GS-REEL	−40°C to +125°C	8-Lead Narrow Body SOIC_N	R-8
OP292GSZ	−40°C to +125°C	8-Lead Narrow Body SOIC_N	R-8
OP292GSZ-REEL	−40°C to +125°C	8-Lead Narrow Body SOIC_N	R-8
OP492GSZ	−40°C to +125°C	14-Lead Narrow Body SOIC_N	R-14
OP492GSZ-REEL	−40°C to +125°C	14-Lead Narrow Body SOIC_N	R-14

[1] Z = RoHS Compliant Part.

NOTES

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- Shortage Management
- Alternative Solution
- Excess Inventory Management