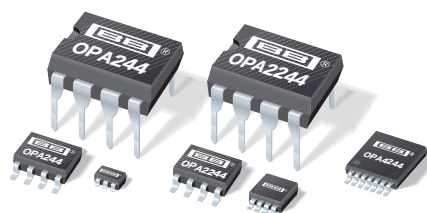




THE DATASHEET OF OPA244UA/2K5



OPA244
OPA2244
OPA4244

MicroPower, Single-Supply **OPERATIONAL AMPLIFIERS** *MicroAmplifier™ Series*

FEATURES

- **MicroSIZE PACKAGES**
 OPA244 (Single): SOT-23-5
 OPA2244 (Dual): MSOP-8
 OPA4244 (Quad): TSSOP-14
- **MicroPOWER:** $I_Q = 50\mu\text{A}/\text{channel}$
- **SINGLE SUPPLY OPERATION**
- **WIDE BANDWIDTH:** 430kHz
- **WIDE SUPPLY RANGE:**
 Single Supply: 2.2V to 36V
 Dual Supply: $\pm 1.1\text{V}$ to $\pm 18\text{V}$

APPLICATIONS

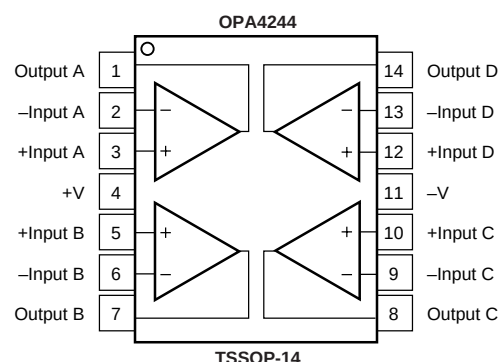
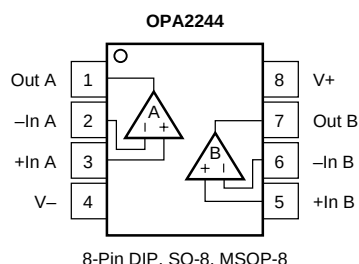
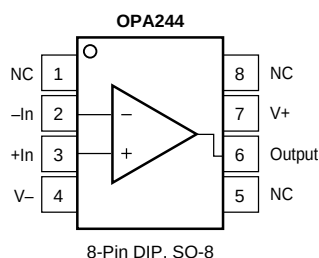
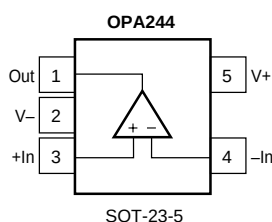
- **BATTERY POWERED SYSTEMS**
- **PORTABLE EQUIPMENT**
- **PCMCIA CARDS**
- **BATTERY PACKS AND POWER SUPPLIES**
- **CONSUMER PRODUCTS**

DESCRIPTION

The OPA244 (single), OPA2244 (dual), and OPA4244 (quad) op amps are designed for very low quiescent current ($50\mu\text{A}/\text{channel}$), yet achieve excellent bandwidth. Ideal for battery powered and portable instrumentation, all versions are offered in micro packages for space-limited applications. The dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The OPA244 series is easy to use and free from phase inversion and overload problems found in some other op amps. These amplifiers are stable in unity gain and excellent performance is maintained as they swing to their specified limits. They can be operated from single (+2.2V to +36V) or dual supplies ($\pm 1.1\text{V}$ to $\pm 18\text{V}$). The input common-mode voltage range includes ground—ideal for many single supply applications. All versions have similar performance. However, there are some differences, such as common-mode rejection. All versions are interchangeable in most applications.

All versions are offered in miniature, surface-mount packages. OPA244 (single version) comes in the tiny 5-lead SOT-23-5 surface mount, SO-8 surface mount, and 8-pin DIP. OPA2244 (dual version) is available in the MSOP-8 surface mount, SO-8 surface-mount, and 8-pin DIP. The OPA4244 (quad) comes in the TSSOP-14 surface mount. They are fully specified from -40°C to $+85^\circ\text{C}$ and operate from -55°C to $+125^\circ\text{C}$. A SPICE Macromodel is available for design analysis.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
 Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS: $V_S = +2.6V$ to $+36V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

At $T_A = +25^\circ\text{C}$, $R_L = 20\text{k}\Omega$ connected to ground, unless otherwise noted.

PARAMETER		CONDITION	OPA244NA, PA, UA			UNITS
			MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE Input Offset Voltage $T_A = -40^{\circ}\text{C}$ to 85°C vs Temperature vs Power Supply $T_A = -40^{\circ}\text{C}$ to 85°C		$V_S = \pm 7.5\text{V}, V_{CM} = 0$ $T_A = -40^{\circ}\text{C}$ to 85°C $V_S = +2.6\text{V}$ to $+36\text{V}$ $V_S = +2.6\text{V}$ to $+36\text{V}$		± 0.7 ± 4 5	± 1.5 ± 2 50 50	mV mV $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V/V}$ $\mu\text{V/V}$
INPUT BIAS CURRENT Input Bias Current Input Offset Current		I_B I_{OS} $V_{CM} = V_S/2$ $V_{CM} = V_S/2$		-10 ± 1	-25 ± 10	nA nA
NOISE Input Voltage Noise, $f = 0.1\text{kHz}$ to 10kHz Input Voltage Noise Density, $f = 1\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$		 e_n i_n		0.4 22 40		$\mu\text{Vp-p}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection $T_A = -40^{\circ}\text{C}$ to 85°C		V_{CM} CMRR $V_S = \pm 18\text{V}, V_{CM} = -18\text{V}$ to $+17.1\text{V}$ $V_S = \pm 18\text{V}, V_{CM} = -18\text{V}$ to $+17.1\text{V}$	0 84 84	 98	$(V^+) - 0.9$	V dB dB
INPUT IMPEDANCE Differential Common-Mode				$10^6 \parallel 2$ $10^9 \parallel 2$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-Loop Voltage Gain $T_A = -40^{\circ}\text{C}$ to 85°C		A_{OL} $V_O = 0.5\text{V}$ to $(V^+) - 0.9$ $V_O = 0.5\text{V}$ to $(V^+) - 0.9$	86 86	106		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.01% Overload Recovery Time		GBW SR $G = 1$ 10V Step $V_{IN} \bullet \text{Gain} = V_S$		430 $-0.1/+0.16$ 150 8		kHz V/ μs μs μs
OUTPUT Voltage Output, Positive $T_A = -40^{\circ}\text{C}$ to 85°C Voltage Output, Negative $T_A = -40^{\circ}\text{C}$ to 85°C Voltage Output, Positive $T_A = -40^{\circ}\text{C}$ to 85°C Voltage Output, Negative $T_A = -40^{\circ}\text{C}$ to 85°C Short-Circuit Current Capacitive Load Drive		V_O $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$ $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$ $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$ $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$ $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground $A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground I_{SC} C_{LOAD}	$(V^+) - 0.9$ $(V^+) - 0.9$ 0.5 0.5 0.5 $(V^+) - 0.75$ $(V^+) - 0.75$ 0.1 0.1 $-25/+12$	$(V^+) - 0.75$ $(V^+) - 0.75$ 0.2 0.2 $(V^+) - 0.75$ $(V^+) - 0.75$ 0.1 0.1		V V V V V V V V mA
See Typical Curve						
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Quiescent Current $T_A = -40^{\circ}\text{C}$ to 85°C		V_S I_Q $T_A = -40^{\circ}\text{C}$ to 85°C	$T_A = -40^{\circ}\text{C}$ to 85°C $I_O = 0$ $I_O = 0$	+2.6 +2.2 50	+36 60 70	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT-23-5 Surface-Mount SO-8 Surface-Mount 8-Pin DIP		 θ_{JA}	 			

NOTE: (1) $V_S = +15V$.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS: $V_S = +2.6V$ to $+36V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

At $T_A = +25^{\circ}C$, $R_L = 20k\Omega$ connected to ground, unless otherwise noted.

PARAMETER	CONDITION	OPA2244EA, PA, UA			UNITS
		MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE Input Offset Voltage $T_A = -40^{\circ}C$ to $85^{\circ}C$ vs Temperature vs Power Supply $T_A = -40^{\circ}C$ to $85^{\circ}C$ Channel Separation	V_{OS} $V_S = \pm 7.5V$, $V_{CM} = 0$ dV_{OS}/dT $PSRR$ $T_A = -40^{\circ}C$ to $85^{\circ}C$ $V_S = +2.6V$ to $+36V$ $V_S = +2.6V$ to $+36V$		± 0.7 ± 4 5 140	± 1.5 ± 2 50 50	mV mV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$ dB
INPUT BIAS CURRENT Input Bias Current Input Offset Current	I_B I_{OS} $V_{CM} = V_S/2$ $V_{CM} = V_S/2$		-10 ± 1	-25 ± 10	nA nA
NOISE Input Voltage Noise, $f = 0.1kHz$ to $10kHz$ Input Voltage Noise Density, $f = 1kHz$ Current Noise Density, $f = 1kHz$	e_n i_n		0.4 22 40		$\mu Vp-p$ $nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection $T_A = -40^{\circ}C$ to $85^{\circ}C$	V_{CM} CMRR $V_S = \pm 18V$, $V_{CM} = -18V$ to $+17.1V$ $V_S = \pm 18V$, $V_{CM} = -18V$ to $+17.1V$	0 72 72	98	$(V+) - 0.9$	V dB dB
INPUT IMPEDANCE Differential Common-Mode			$10^6 \parallel 2$ $10^9 \parallel 2$		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain $T_A = -40^{\circ}C$ to $85^{\circ}C$	A_{OL} $V_O = 0.5V$ to $(V+) - 0.9$ $V_O = 0.5V$ to $(V+) - 0.9$	86 86	106		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.01% Overload Recovery Time	GBW SR $G = 1$ 10V Step $V_{IN} \cdot \text{Gain} = V_S$		430 $-0.1/+0.16$ 150 8		kHz V/ μs μs μs
OUTPUT Voltage Output, Positive $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Negative $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Positive $T_A = -40^{\circ}C$ to $85^{\circ}C$ Voltage Output, Negative $T_A = -40^{\circ}C$ to $85^{\circ}C$ Short-Circuit Current Capacitive Load Drive	V_O I_{SC} C_{LOAD} $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to $V_S/2$ $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to Ground $A_{OL} \geq 80dB$, $R_L = 20k\Omega$ to Ground	$(V+) - 0.9$ $(V+) - 0.9$ 0.5 0.5	$(V+) - 0.75$ $(V+) - 0.75$ 0.2 0.2 $(V+) - 0.75$ $(V+) - 0.75$ 0.1 0.1 $-25/+12$ See Typical Curve		V V V V V V V V mA
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Quiescent Current (per amplifier) $T_A = -40^{\circ}C$ to $85^{\circ}C$	V_S I_Q $T_A = -40^{\circ}C$ to $85^{\circ}C$ $I_O = 0$ $I_O = 0$	+2.6	+2.2 40	+36 50 63	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance MSOP-8 Surface-Mount SO-8 Surface-Mount 8-Pin DIP	θ_{JA}	-40 -55 -65		85 125 150	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$

NOTE: (1) $V_S = +15V$.

SPECIFICATIONS: $V_S = +2.6V$ to $+36V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

At $T_A = +25^\circ\text{C}$, $R_I = 20\text{k}\Omega$ connected to ground, unless otherwise noted.

			OPA4244EA			
PARAMETER		CONDITION	MIN	TYP ⁽¹⁾	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage $T_A = -40^{\circ}\text{C}$ to 85°C	V_{OS}	$V_S = \pm 7.5\text{V}, V_{CM} = 0$		± 0.7	± 1.5	mV
vs Temperature	dV_{OS}/dT	$T_A = -40^{\circ}\text{C}$ to 85°C		± 4	± 2	mV/ $^{\circ}\text{C}$
vs Power Supply	PSRR	$V_S = +2.6\text{V}$ to $+36\text{V}$		5	50	$\mu\text{V/V}$
$T_A = -40^{\circ}\text{C}$ to 85°C		$V_S = +2.6\text{V}$ to $+36\text{V}$			50	$\mu\text{V/V}$
Channel Separation				140		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B	$V_{CM} = V_S/2$		-10	-25	nA
Input Offset Current	I_{OS}	$V_{CM} = V_S/2$		± 1	± 10	nA
NOISE						
Input Voltage Noise, f = 0.1kHz to 10kHz				0.4		$\mu\text{V/p-p}$
Input Voltage Noise Density, f = 1kHz	e_n			22		nV/ $\sqrt{\text{Hz}}$
Current Noise Density, f = 1kHz	i_n			40		fA/ $\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	$V_S = \pm 18\text{V}, V_{CM} = -18\text{V}$ to $+17.1\text{V}$	0		(V+) – 0.9	V
Common-Mode Rejection	CMRR	$V_S = \pm 18\text{V}, V_{CM} = -18\text{V}$ to $+17.1\text{V}$	82	104		dB
$T_A = -40^{\circ}\text{C}$ to 85°C			82			dB
INPUT IMPEDANCE						
Differential				$10^6 \parallel 2$		$\Omega \parallel \text{pF}$
Common-Mode				$10^9 \parallel 2$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	$V_O = 0.5\text{V}$ to (V+) – 0.9	86	106		dB
$T_A = -40^{\circ}\text{C}$ to 85°C		$V_O = 0.5\text{V}$ to (V+) – 0.9	86			dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			430		kHz
Slew Rate	SR	G = 1		-0.1/+0.16		V/ μs
Settling Time 0.01%		10V Step		150		μs
Overload Recovery Time		$V_{IN} \bullet \text{Gain} = V_S$		8		μs
OUTPUT						
Voltage Output, Positive	V_O	$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$	(V+) – 0.9	(V+) – 0.75		V
$T_A = -40^{\circ}\text{C}$ to 85°C		$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$	(V+) – 0.9	(V+) – 0.75		V
Voltage Output, Negative		$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$	0.5	0.2		V
$T_A = -40^{\circ}\text{C}$ to 85°C		$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to $V_S/2$	0.5	0.2		V
Voltage Output, Positive		$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground		(V+) – 0.75		V
$T_A = -40^{\circ}\text{C}$ to 85°C		$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground		(V+) – 0.75		V
Voltage Output, Negative		$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground		0.1		V
$T_A = -40^{\circ}\text{C}$ to 85°C		$A_{OL} \geq 80\text{dB}, R_L = 20\text{k}\Omega$ to Ground		0.1		V
Short-Circuit Current	I_{SC}			-25/+12		mA
Capacitive Load Drive	C_{LOAD}		See Typical Curve			
POWER SUPPLY						
Specified Voltage Range	V_S	$T_A = -40^{\circ}\text{C}$ to 85°C	+2.6		+36	V
Minimum Operating Voltage				+2.2		V
Quiescent Current (per amplifier)	I_Q	$I_O = 0$		40	60	μA
$T_A = -40^{\circ}\text{C}$ to 85°C		$I_O = 0$			70	μA
TEMPERATURE RANGE						
Specified Range			-40		85	$^{\circ}\text{C}$
Operating Range			-55		125	$^{\circ}\text{C}$
Storage Range			-65		150	$^{\circ}\text{C}$
Thermal Resistance	θ_{JA}					
TSSOP-14 Surface Mount				100		$^{\circ}\text{C/W}$

NOTE: (1) $V_S = +15V$.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	36V
Input Voltage Range ⁽²⁾	(V-) – 0.3V to (V+) + 0.3V
Input Current ⁽²⁾	10mA
Output Short-Circuit ⁽³⁾	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Capability	2000V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Inputs are diode-clamped to the supply rails and should be current-limited to 10mA or less if input voltages can exceed rails by more than 0.3V. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

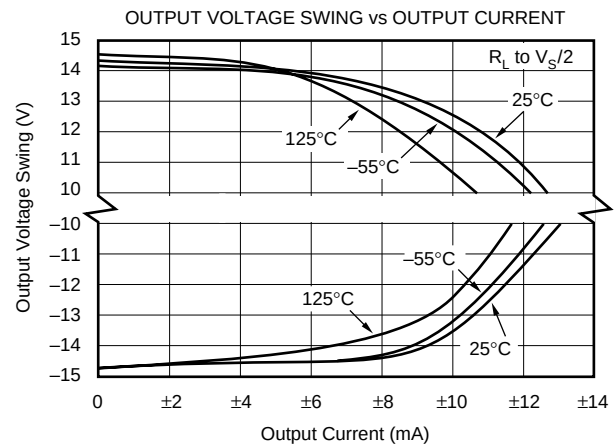
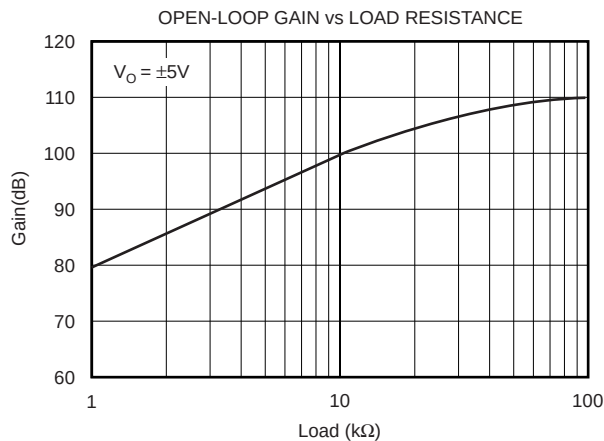
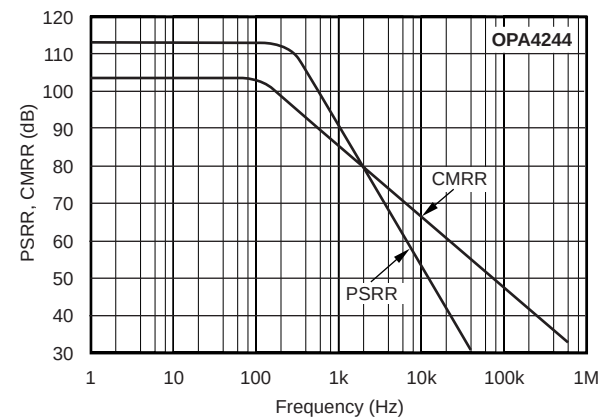
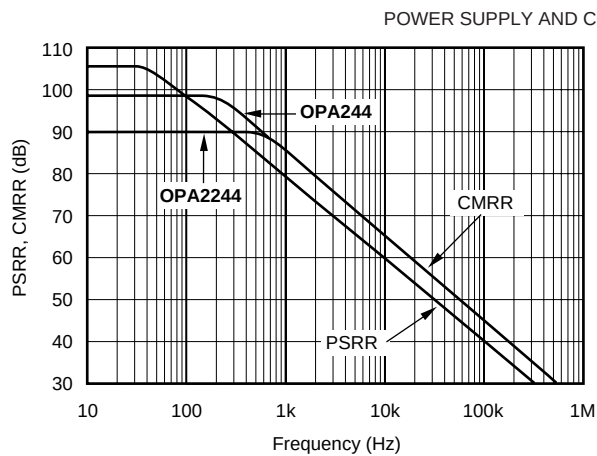
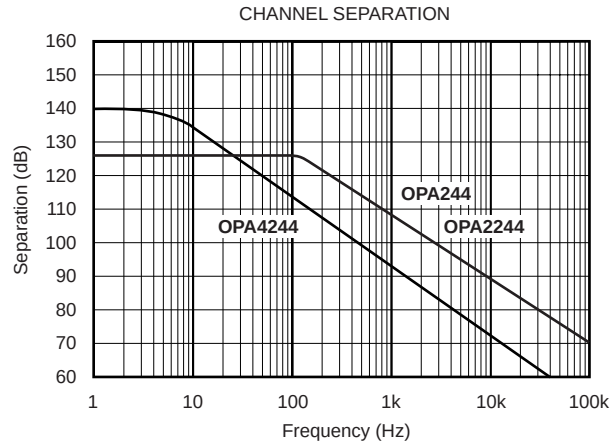
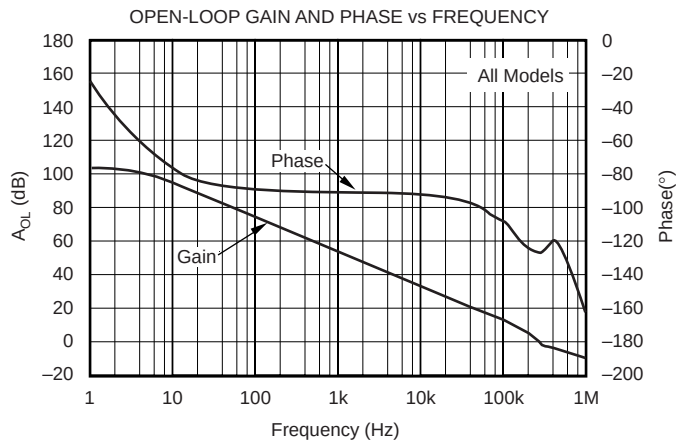
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
Single						
OPA244NA	SOT-23-5 Surface-Mount	331	–40°C to +85°C	A44	OPA244NA/250	Tape and Reel
"	"	"	"	"	OPA244NA/3K	Tape and Reel
OPA244PA	8-Pin DIP	006	–40°C to +85°C	OPA244PA	OPA244PA	Rails
OPA244UA	SO-8 Surface-Mount	182	–40°C to +85°C	OPA244UA	OPA244UA	Rails
"	"	"	"	"	OPA244UA/2K5	Tape and Reel
Dual						
OPA2244EA	MSOP-8 Surface-Mount	337	–40°C to +85°C	A44	OPA2244EA/250	Tape and Reel
"	"	"	"	"	OPA2244EA/2K5	Tape and Reel
OPA2244PA	8-Pin DIP	006	–40°C to +85°C	OPA2244PA	OPA2244PA	Rails
OPA2244UA	SO-8 Surface-Mount	182	–40°C to +85°C	OPA2244UA	OPA2244UA	Rails
"	"	"	"	"	OPA2244UA/2K5	Tape and Reel
Quad						
OPA4244EA	TSSOP-14 Surface-Mount	357	–40°C to +85°C	OPA4244EA	OPA4244EA/250	Tape and Reel
"	"	"	"	"	OPA4244EA/2K5	Tape and Reel

NOTE: (1) Products followed by a slash (/) are only available in Tape and Reel in the quantities indicated (e.g., /250 indicates 250 devices per reel). Ordering 3000 pieces of "OPA244NA/3K" will get a single 3000 piece Tape and Reel.

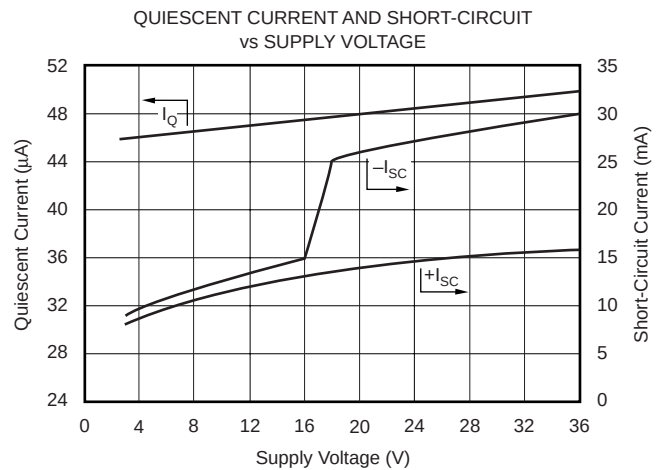
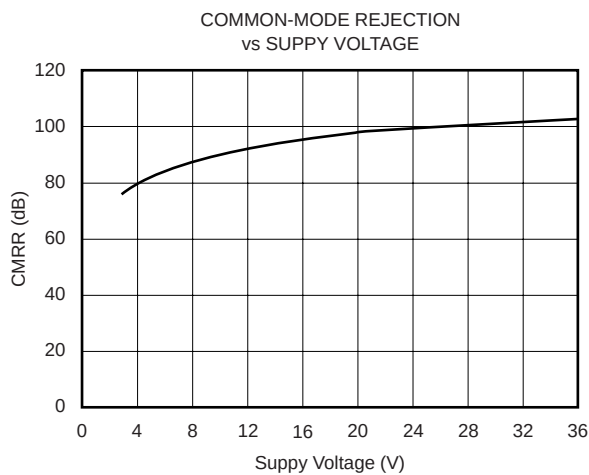
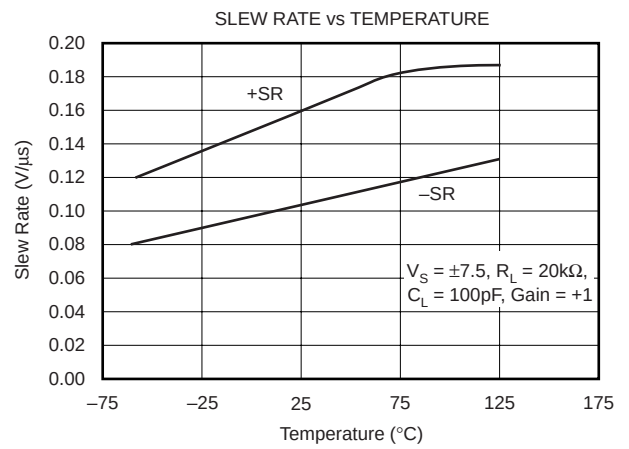
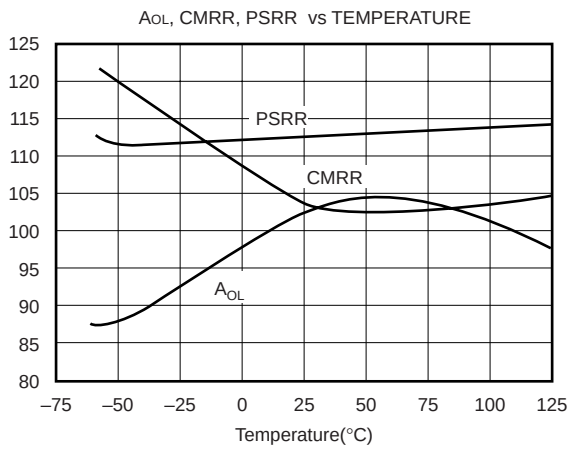
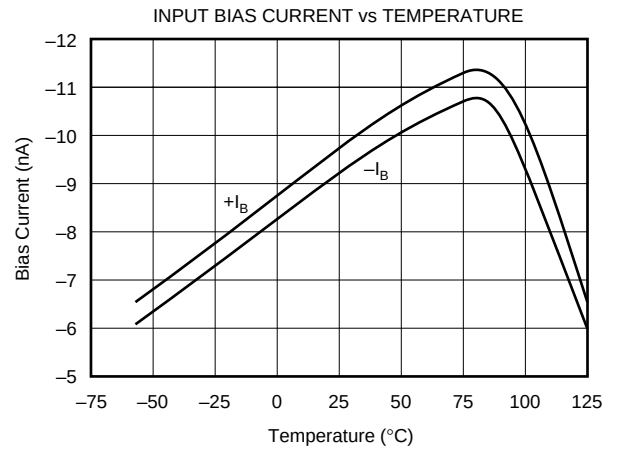
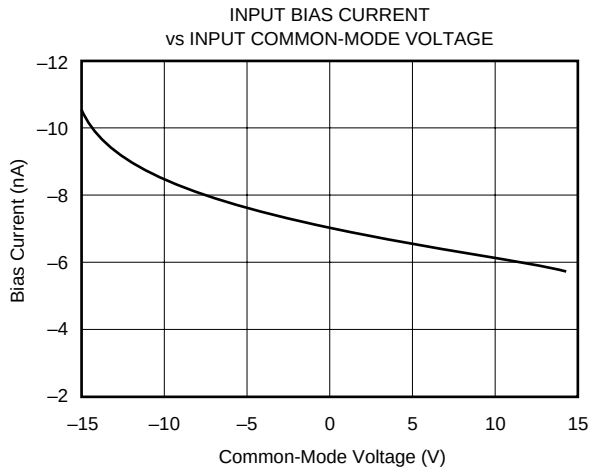
TYPICAL PERFORMANCE CURVES

At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (Cont.)

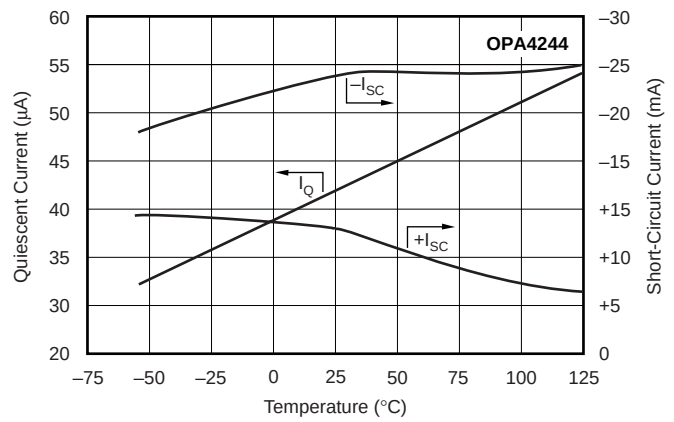
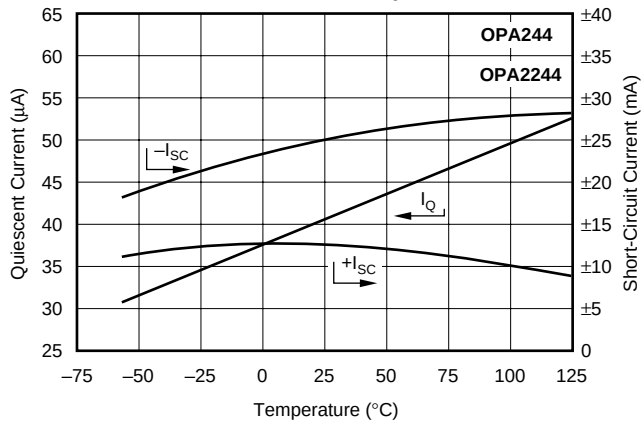
At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.



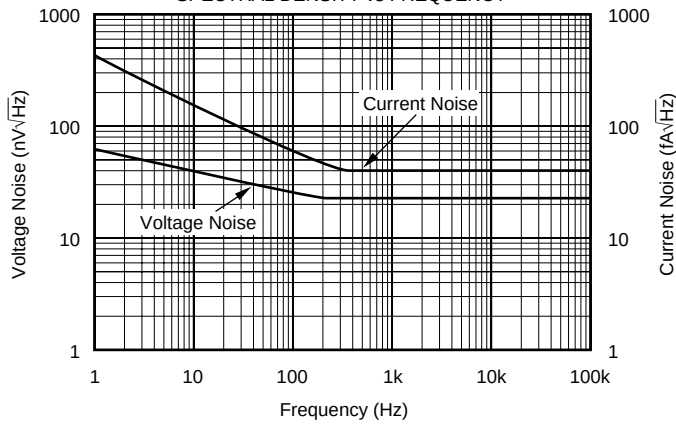
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.

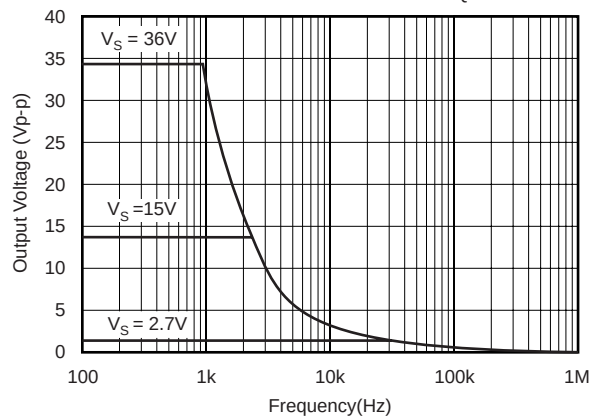
QUIESCENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



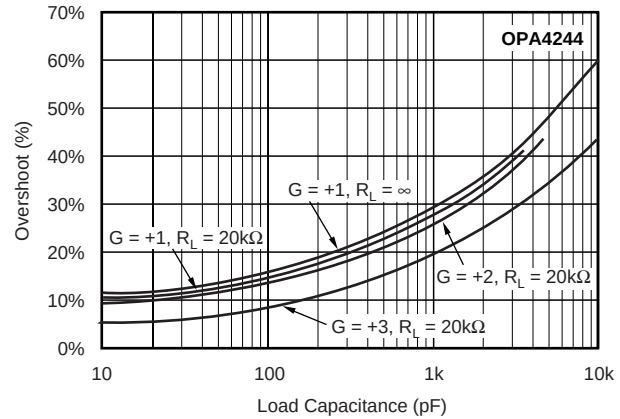
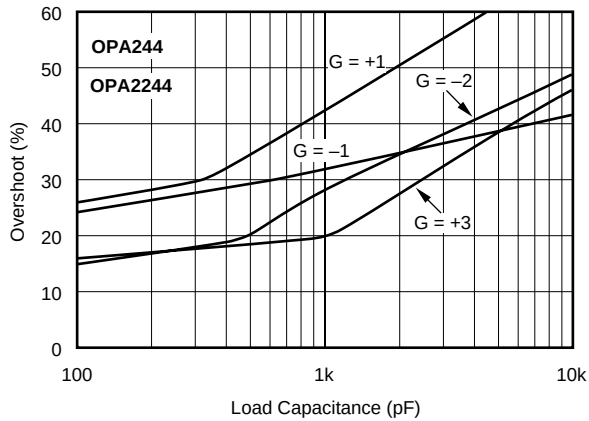
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



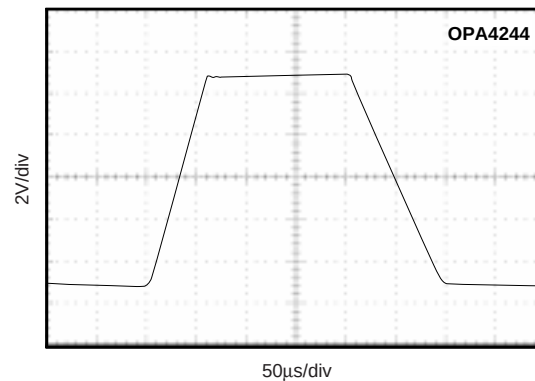
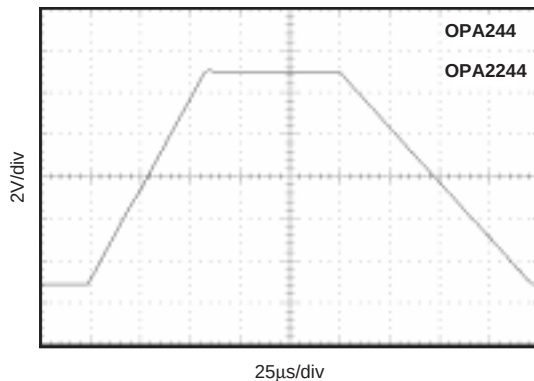
SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE



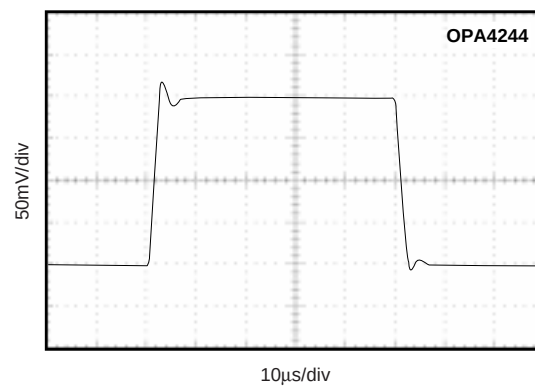
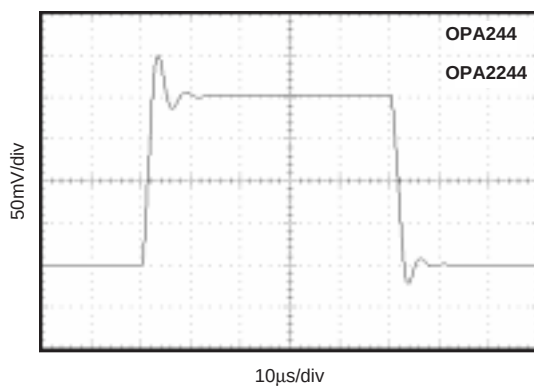
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = 25^\circ\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.

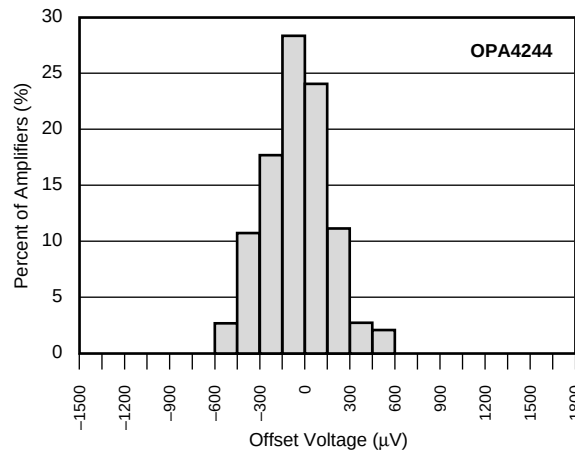
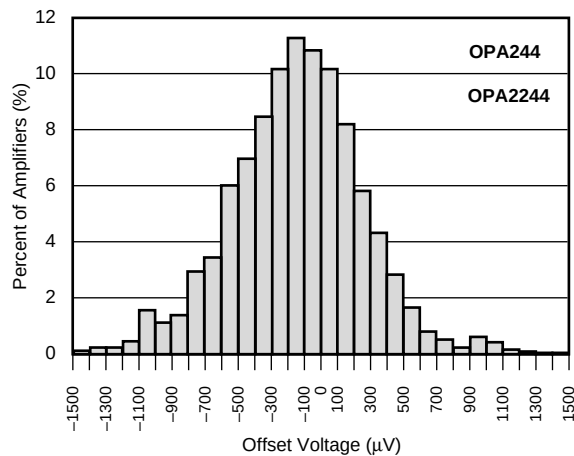
LARGE-SIGNAL STEP RESPONSE, $G = 1$, $C_L = 100\text{pF}$



SMALL-SIGNAL STEP RESPONSE, $G = 1$, $C_L = 100\text{pF}$

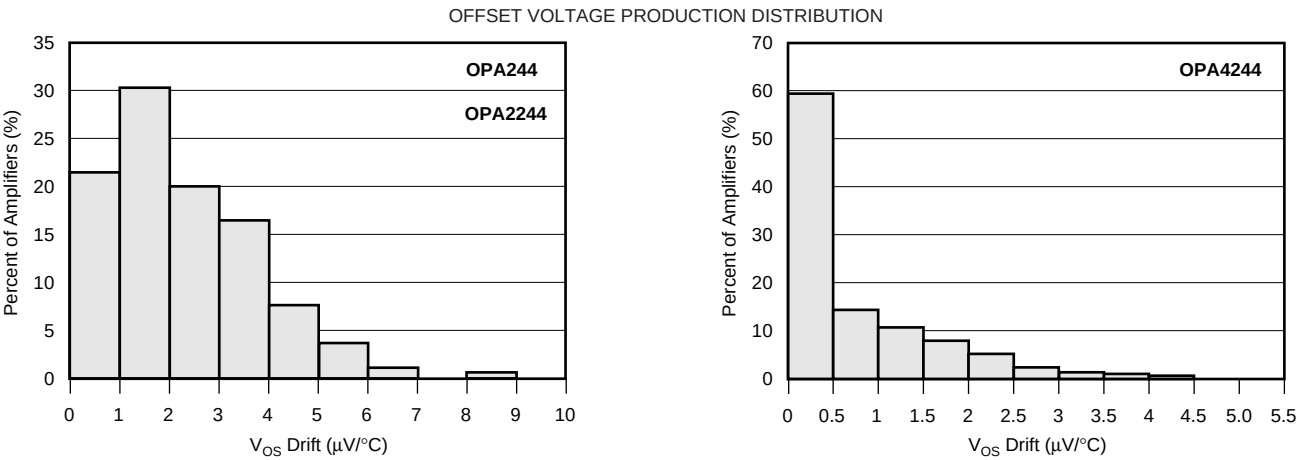


OFFSET VOLTAGE PRODUCTION DISTRIBUTION



TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = 25^{\circ}\text{C}$, $V_S = +15\text{V}$, and $R_L = 20\text{k}\Omega$ connected to Ground, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA244 is unity-gain stable and suitable for a wide range of general purpose applications. Power supply pins should be bypassed with 0.01μF ceramic capacitors.

OPERATING VOLTAGE

The OPA244 can operate from single supply (+2.2V to +36V) or dual supplies (±1.1 to ±18V) with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA244 is specified for real world applications; a single set of specifications applies throughout the +2.6V to +36V (±1.3 to ±18V) supply range.

This allows a designer to have the same assured performance at any supply voltage within this range. In addition, many key parameters are guaranteed over the specified temperature range, -40°C to +85°C. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

Useful information on solder pad design for printed circuit boards can be found in Burr-Brown's Application Bulletin AB-132B, "Solder Pad Recommendations for Surface-Mount Devices," easily found at Burr-Brown's web site (<http://www.burr-brown.com>).

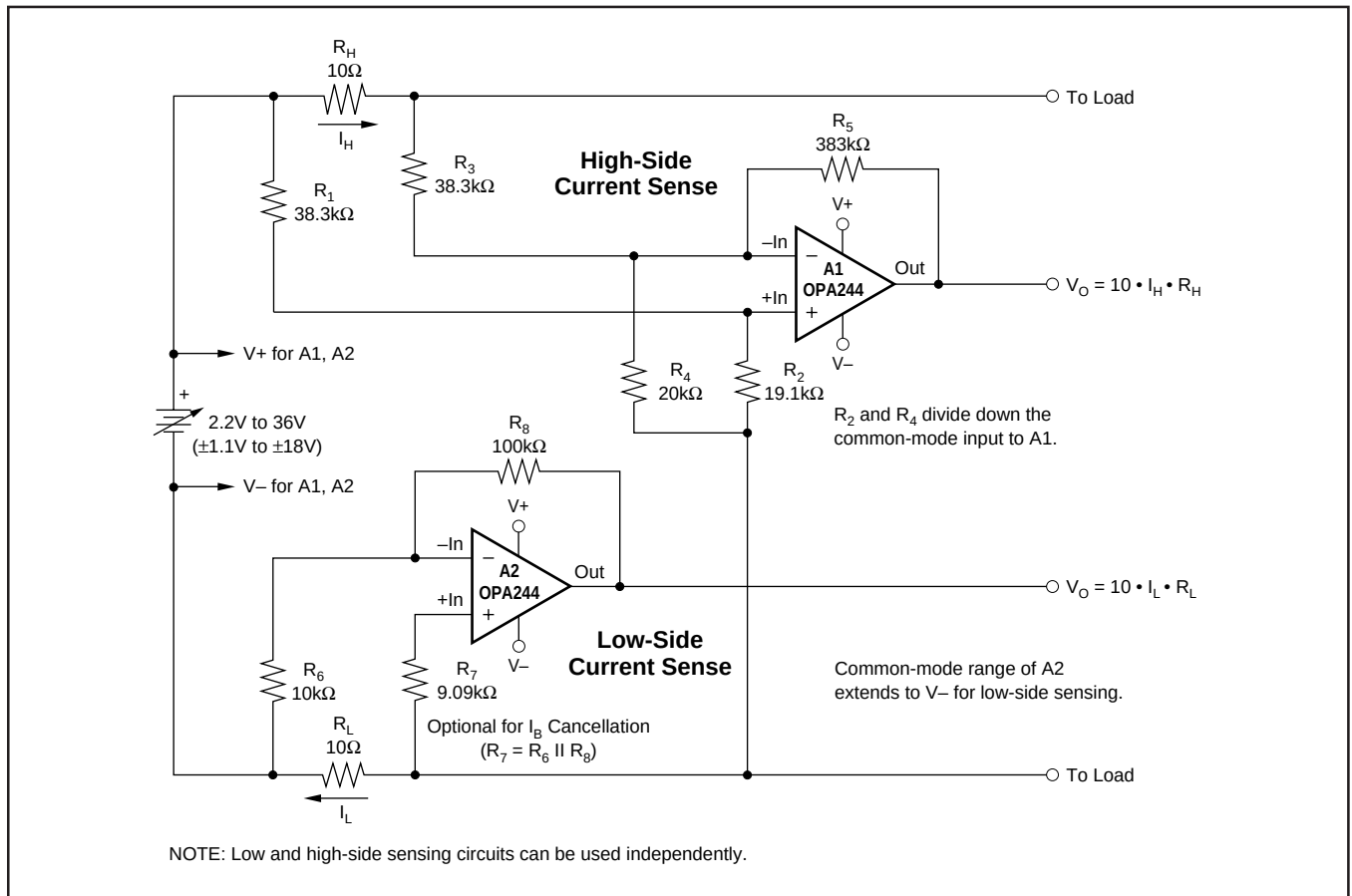


FIGURE 1. Low and High-Side Battery Current Sensing.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2244EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA2244EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA2244EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA2244EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA2244PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2244PA	Samples
OPA2244UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2244UA	Samples
OPA2244UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2244UA	Samples
OPA2244UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2244UA	Samples
OPA244NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA244NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA244NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA244NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA244UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 244UA	Samples
OPA244UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 244UA	Samples
OPA4244EA/250	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 4244EA	Samples
OPA4244EA/250E4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 4244EA	Samples
OPA4244EA/2K5	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 4244EA	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

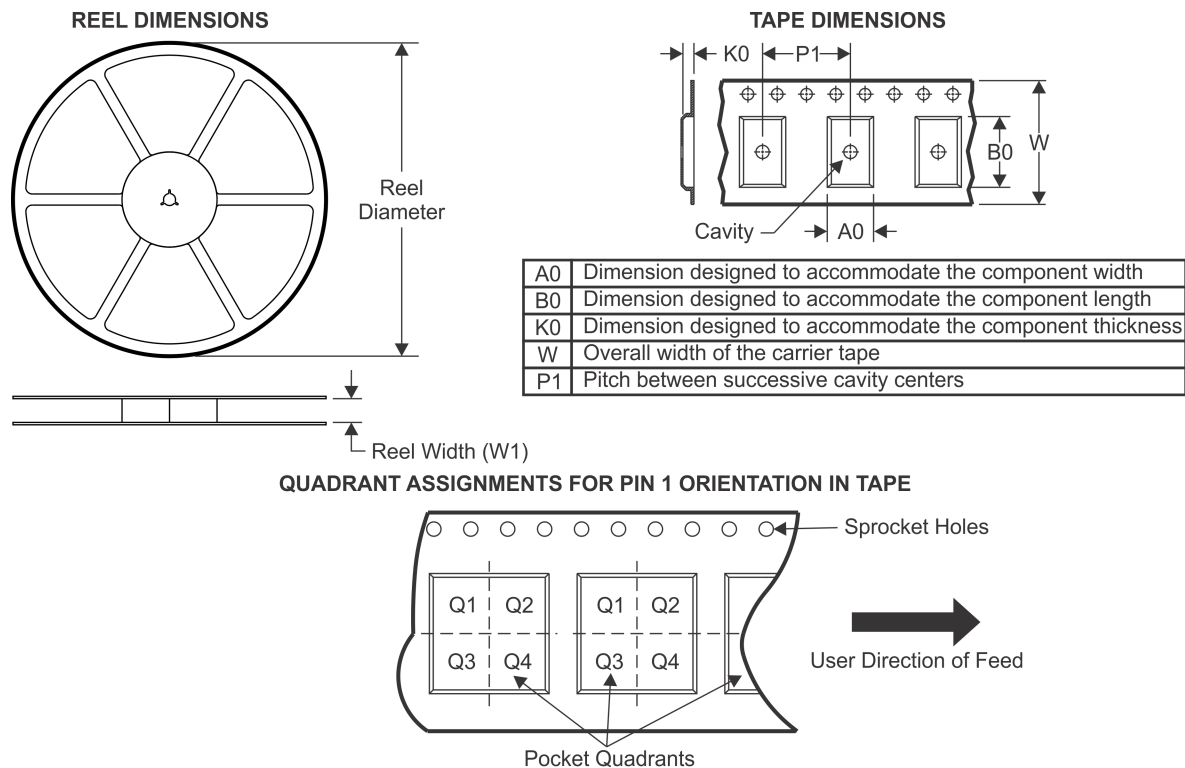
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

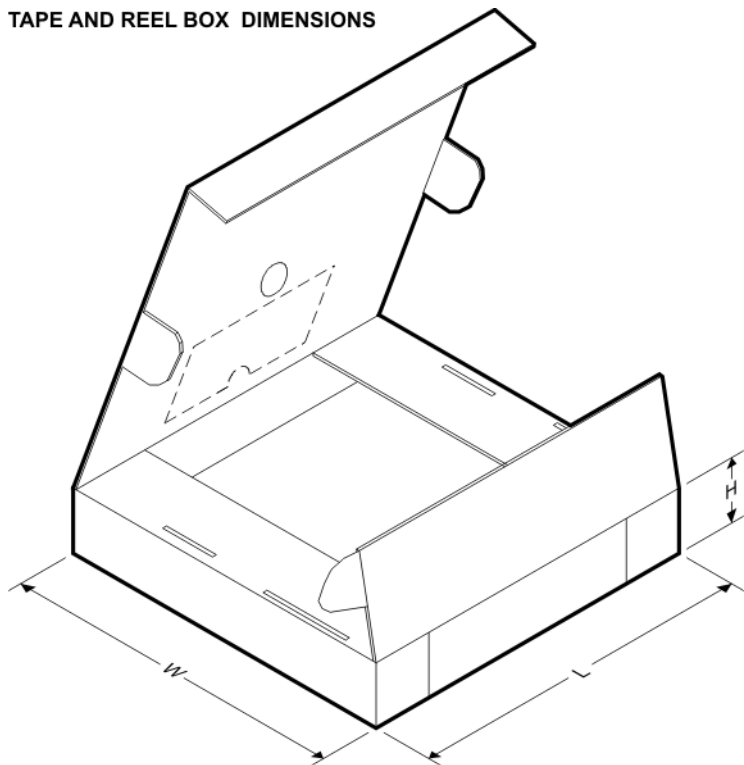
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2244EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2244EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2244UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA244NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA244NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA244UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4244EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4244EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

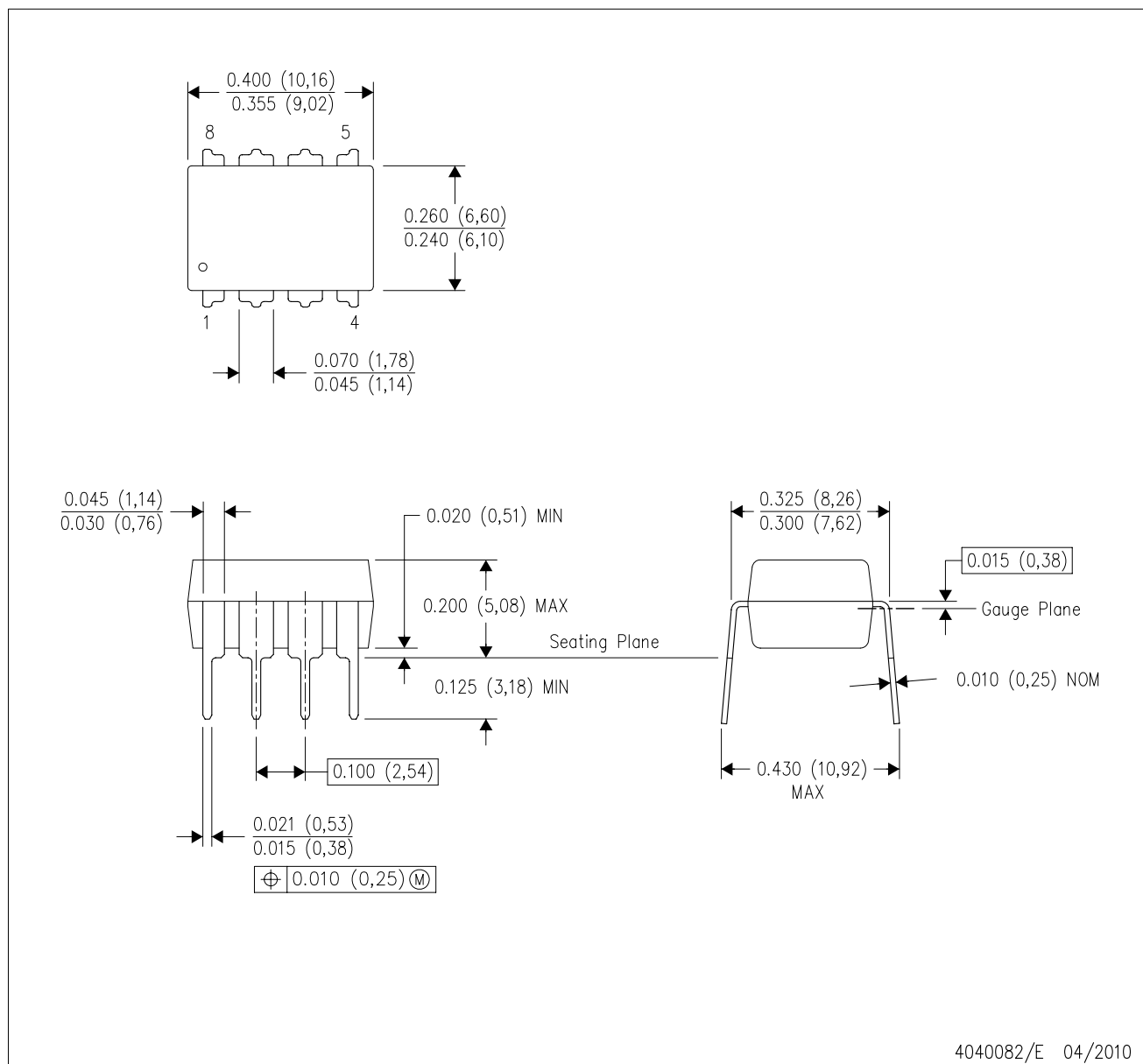


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2244EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2244EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2244UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA244NA/250	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA244NA/3K	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA244UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4244EA/250	TSSOP	PW	14	250	210.0	185.0	35.0
OPA4244EA/2K5	TSSOP	PW	14	2500	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

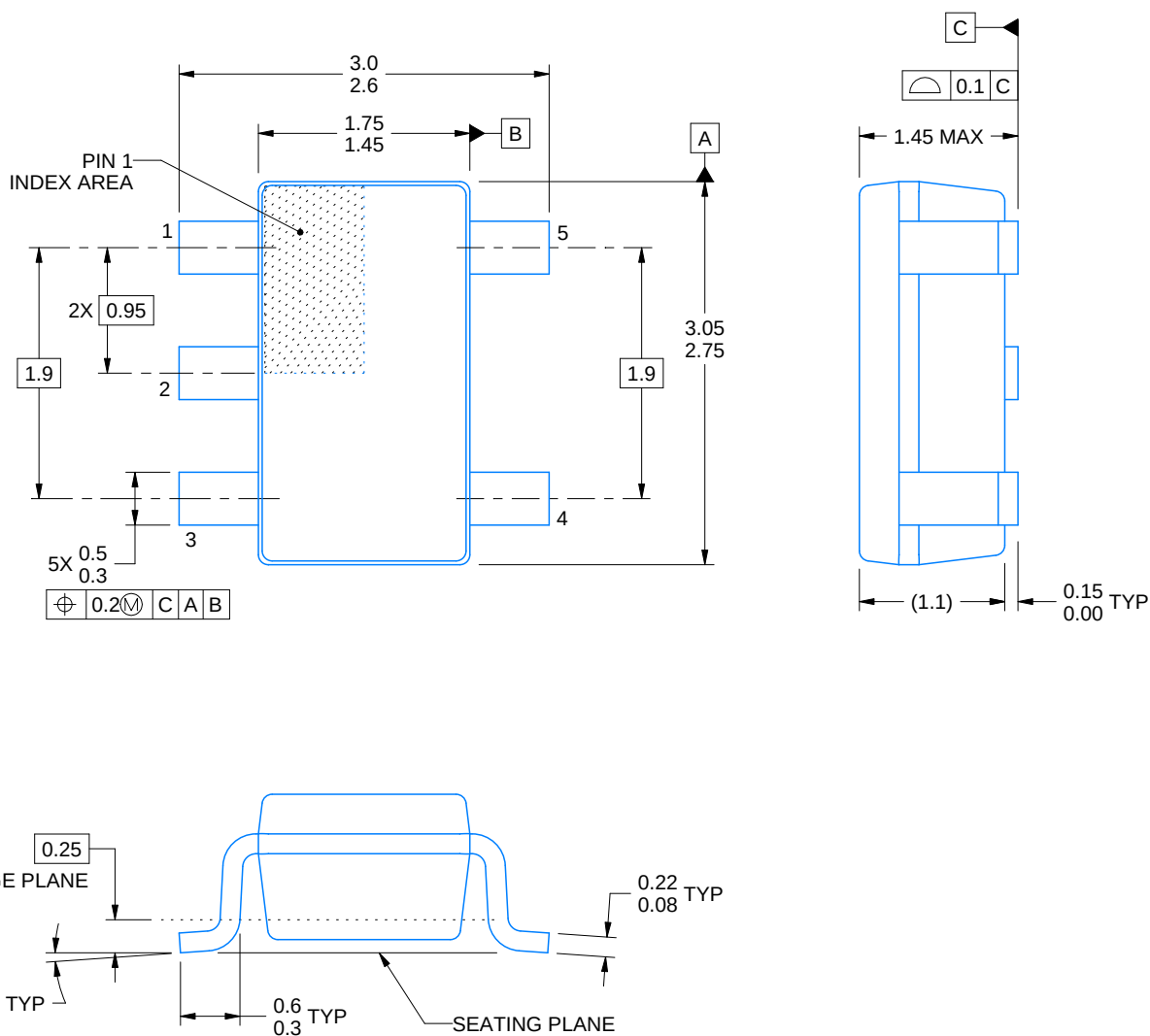


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

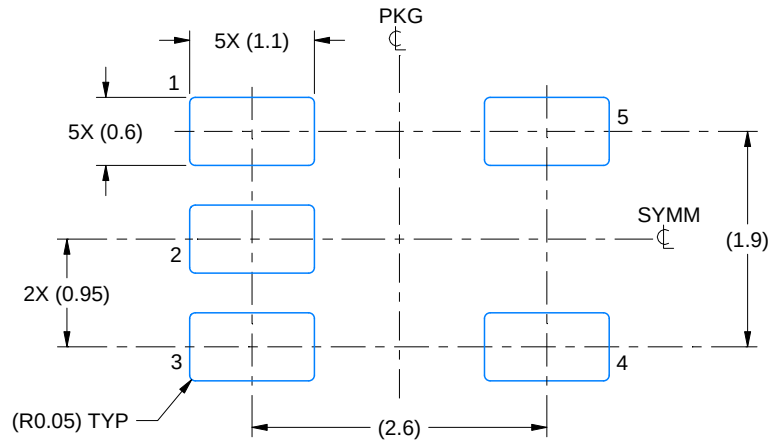
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

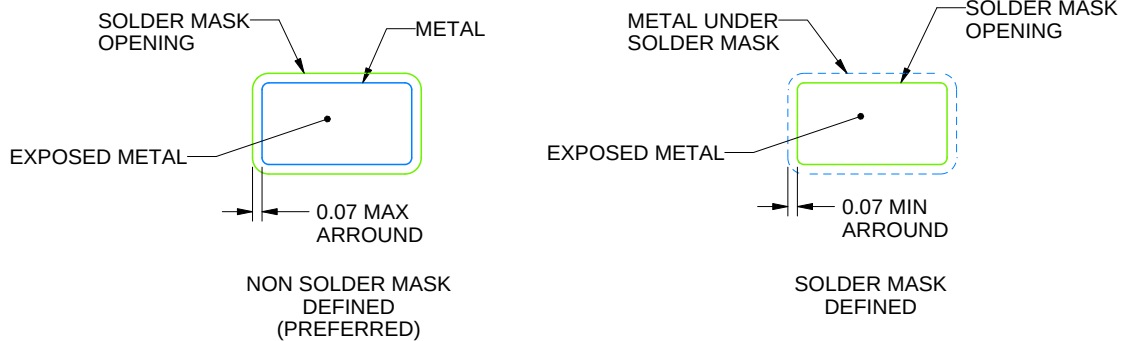
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

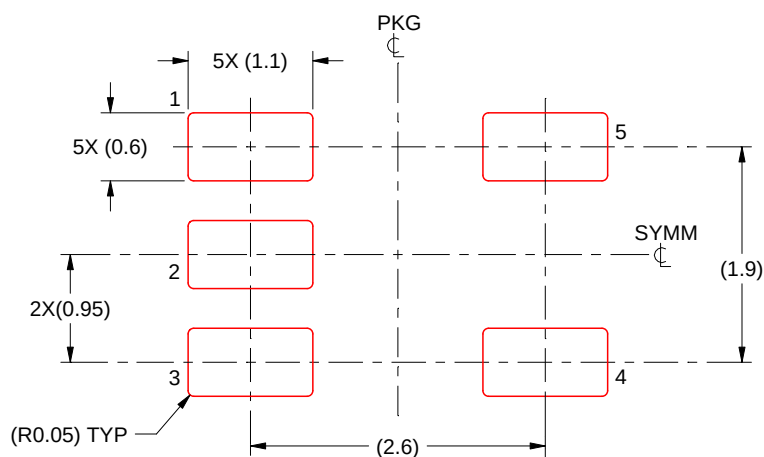
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

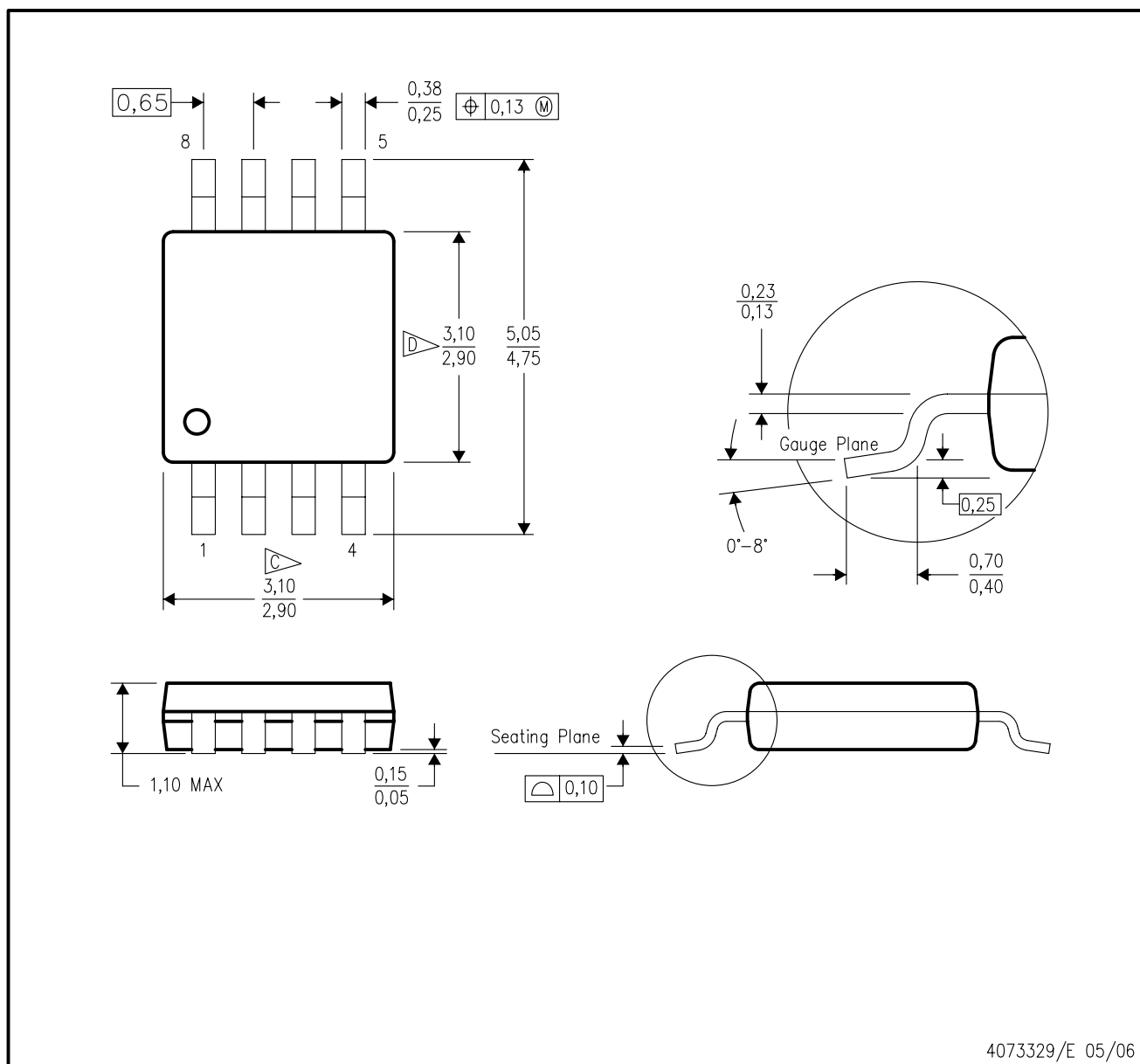
4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



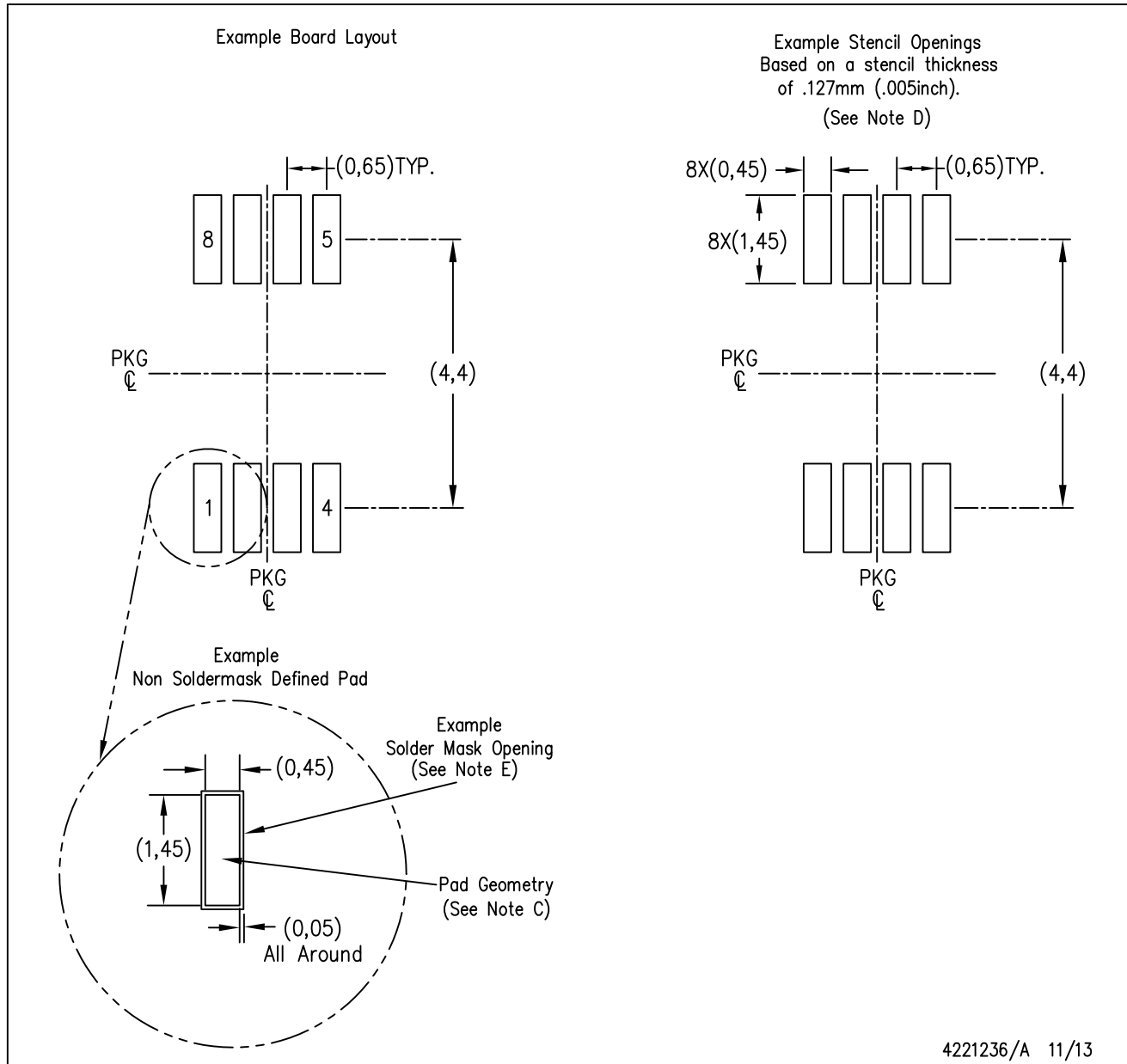
4073329/E 05/06

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

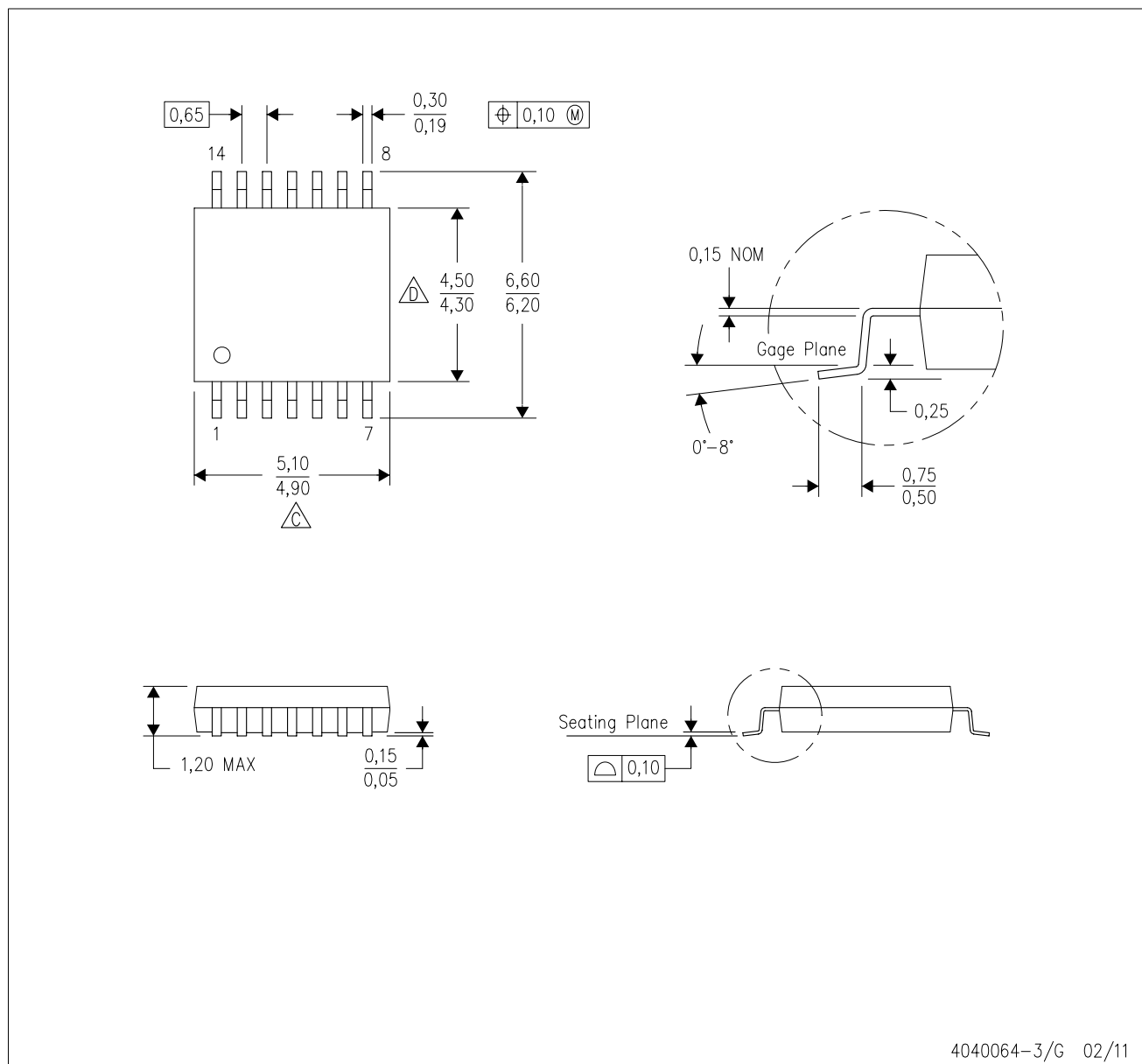
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

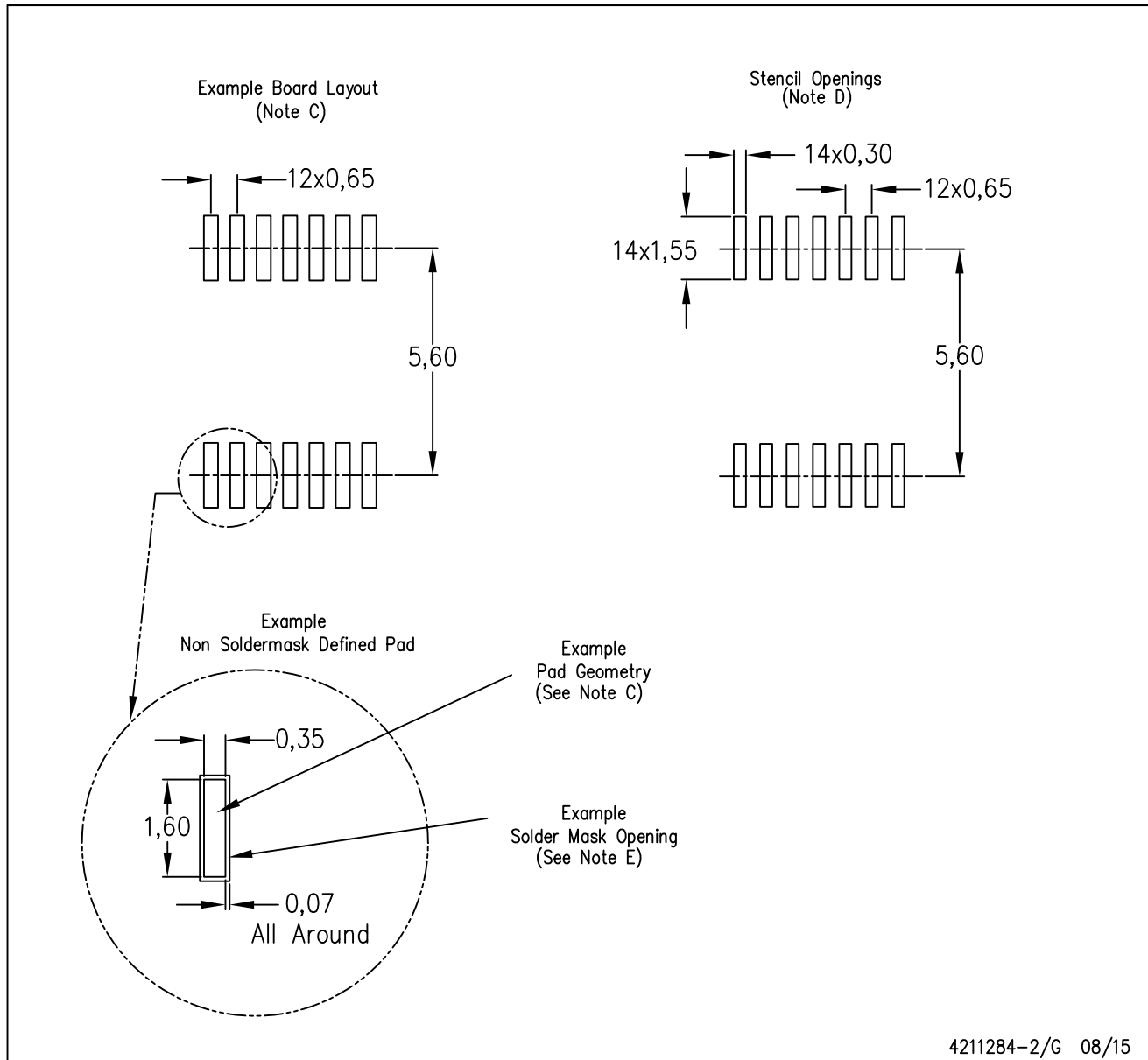
PLASTIC SMALL OUTLINE



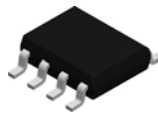
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

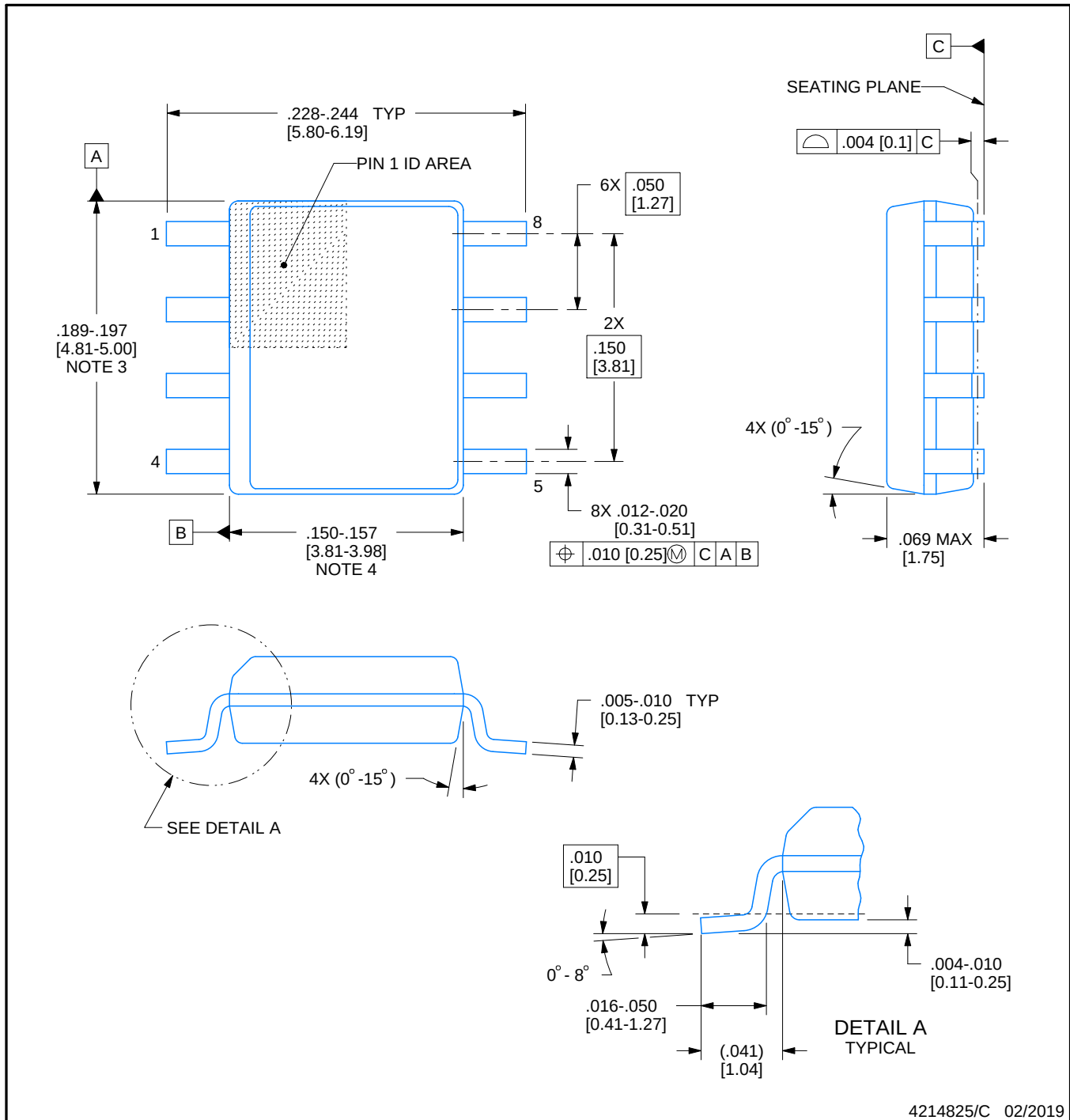


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

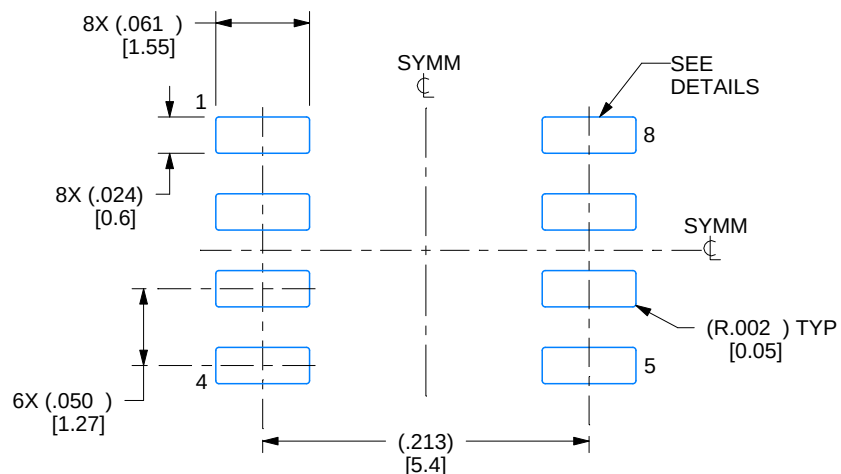
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

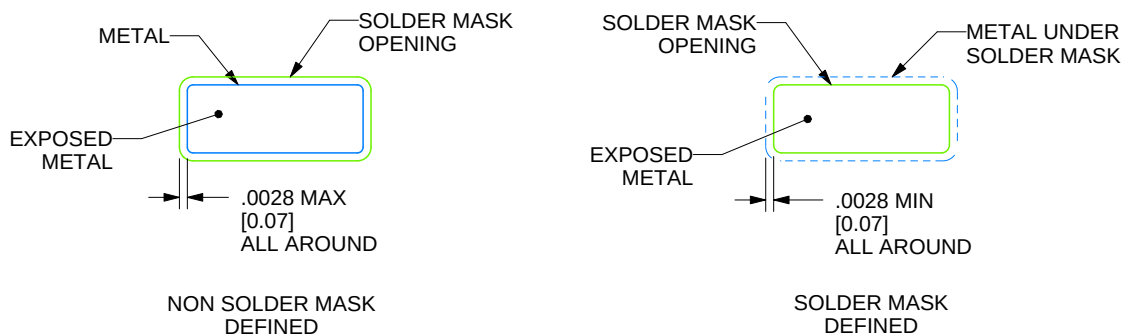
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

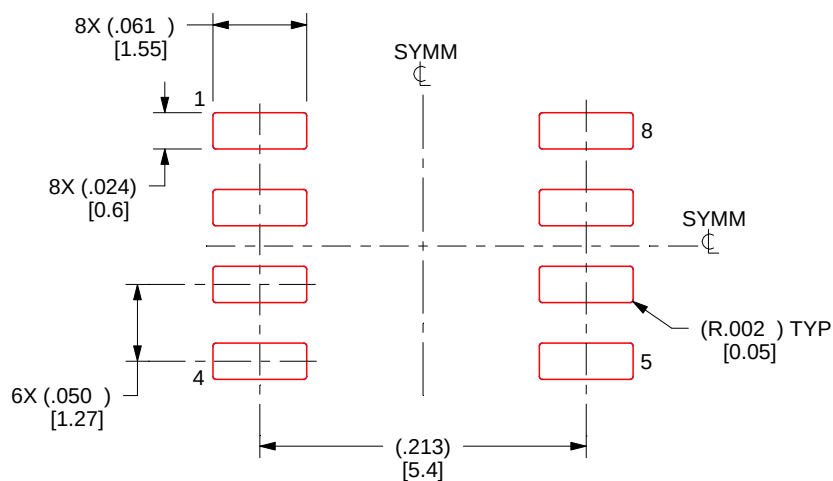
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 View [OPA244UA/2K5](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management