THE DATASHEET OF

OPA2674IDRG4

www.win-source.net 0086-755-83957316

SBOS270C − AUGUST 2003 − REVISED AUGUST 2008

Dual Wideband, High Output Current Operational Amplifier with Current Limit

FEATURES

- WIDEBAND +12V OPERATION: 220MHz (G = +4)
- UNITY-GAIN STABLE: 250MHz (G = +1)
- HIGH OUTPUT CURRENT: 500mA
- OUTPUT VOLTAGE SWING: $10V_{PP}$
- HIGH SLEW RATE: 2000V/µs
- LOW SUPPLY CURRENT: 18mA
- FLEXIBLE POWER CONTROL: SO-14 Only
- OUTPUT CURRENT LIMIT (±800mA)

APPLICATIONS

- POWER LINE MODEM
- xDSL LINE DRIVERS
- CABLE MODEM DRIVERS
- MATCHED I/Q CHANNEL AMPLIFIERS
- BROADBAND VIDEO LINE DRIVERS
- ARB LINE DRIVERS
- HIGH CAP LOAD DRIVER

OPA2674 RELATED PRODUCTS

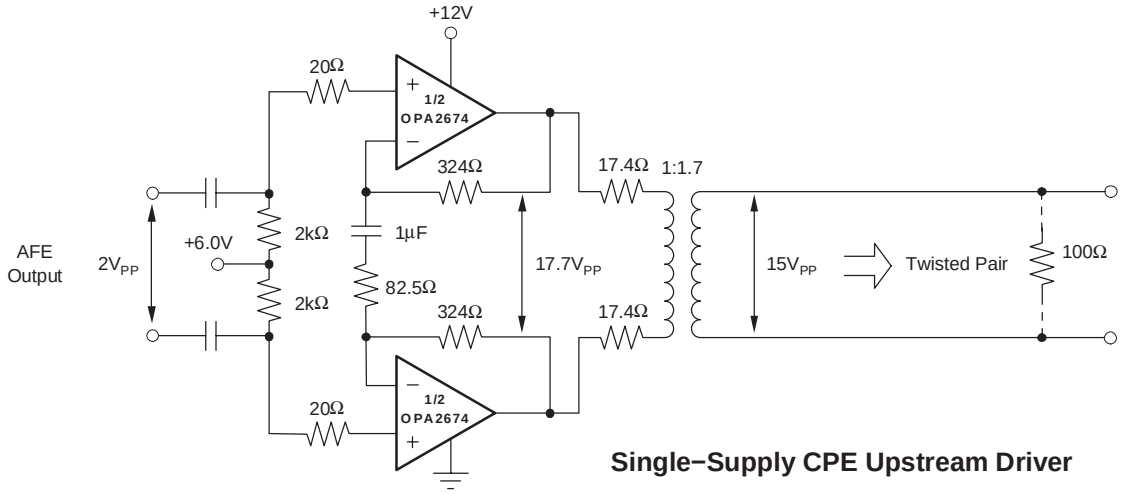
SINGLES	DUALS	TRIPLES	NOTES
OPA691	OPA2691	OPA3691	Single +12V Capable
—	THS6042	—	±15V Capable
—	OPA2677	—	Single +12V Capable

DESCRIPTION

The OPA2674 provides the high output current and low distortion required in emerging xDSL and Power Line Modem driver applications. Operating on a single +12V supply, the OPA2674 consumes a low 9mA/ch quiescent current to deliver a very high 500mA output current. This output current supports even the most demanding ADSL CPE requirements with > 380mA minimum output current (+25°C minimum value) with low harmonic distortion. Differential driver applications deliver < −85dBc distortion at the peak upstream power levels of full rate ADSL. The high 200MHz bandwidth also supports the most demanding VDSL line driver requirements.

Power control features are included in the SO-14 package version to allow system power to be minimized. Two logic control lines allow four quiescent power settings. These include full power, power cutback for short loops, idle state for no signal transmission but line match maintenance, and shutdown for power off with a high impedance output.

Specified on ±6V supplies (to support +12V operation), the OPA2674 will also support a single +5V or dual ±5V supply. Video applications will benefit from a very high output current to drive up to 10 parallel video loads (15Ω) with < 0.1%/0.1°dG/dP nonlinearity.



Single−Supply CPE Upstream Driver

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2674	SO-8	D	−40°C to +85°C	OPA2674ID	OPA2674ID	Rails, 100
″	″	″	″	″	OPA2674IDR	Tape and Reel, 2500
OPA2674	SO-14	D	−40°C to +85°C	OPA2674I-14D	OPA2674I-14D	Rails, 58
″	″	″	″	″	OPA2674I-14DR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	$\pm V_S$
Storage Temperature Range: D, -14D	−65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating	
Human Body Model (HBM)(2)	2000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	100V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

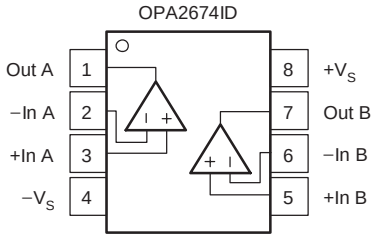
(2) Pins 2 and 6 on SO-8 package, and pins 1 and 7 on SO-14 package > 500V HBM.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

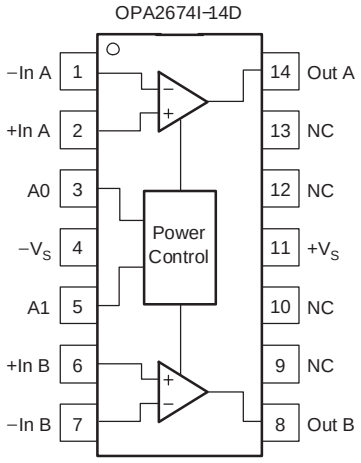
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS

TOP VIEW **SO−8**



TOP VIEW **SO−14**



NC = No Connection

ELECTRICAL CHARACTERISTICS: V_S = ±6V

Boldface limits are tested at **+25°C.**

At T_A = +25°C, A_1 = A_0 = 1 (full power: for SO-14 only), G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 1 for AC performance only.

PARAMETER	TEST CONDITIONS	OPA2674ID, OPA2674I-14D						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
AC Performance (see Figure 1)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 511Ω	250				MHz	typ	C
	G = +2, R_F = 475Ω	225	170	165	160	MHz	min	B
	G = +4, R_F = 402Ω	220	170	165	160	MHz	min	B
	G = +8, R_F = 250Ω	260	200	195	190	MHz	min	B
Peaking at a Gain of +1	G = +1, R_F = 511Ω	0.2				dB	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +4, V_O = 0.5V_{PP}	100	40	35	30	MHz	min	B
Large-Signal Bandwidth	G = +4, V_O = 5V_{PP}	220	160	155	150	MHz	typ	C
Slew Rate	G = +4, 5V step	2000	1500	1450	1400	V/µs	min	B
Rise Time and Fall Time	G = +4, V_O = 2V step	1.6				ns	typ	C
Harmonic Distortion	G = +4, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	−72	−68	−67	−66	dBc	max	B
	R_L ≥ 500Ω	−82	−80	−79	−78	dBc	max	B
3rd-Harmonic	R_L = 100Ω	−81	−79	−78	−77	dBc	max	B
	R_L ≥ 500Ω	−93	−91	−90	−89	dBc	max	B
Input Voltage Noise	f > 1MHz	2	2.6	2.9	3.1	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	16	20	21	22	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	24	29	30	31	pA/√Hz	max	B
NTSC Differential Gain	NTSC, G = +2, R_L = 150Ω	0.03				%	typ	C
	NTSC, G = +2, R_L = 37.5Ω	0.05				%	typ	C
NTCS Differential Phase	NTSC, G = +2, R_L = 150Ω	0.01				deg	typ	C
	NTSC, G = +2, R_L = 37.5Ω	0.04				deg	typ	C
Channel-to-Channel Crosstalk	f = 5MHz, Input-Referred	−92				dB	typ	C
DC Performance(4)								
Open-Loop Transimpedance Gain	V_O = 0V, R_L = 100Ω	135	**80**	76	75	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1	±**4.5**	±5	±5.3	mV	max	A
Offset Voltage Drift	V_{CM} = 0V	±4	±10	±10	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	±10	±**30**	±32	±35	µA	max	A
Noninverting Input Bias Current Drift	V_{CM} = 0V	±5	±50	±50	±75	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±10	±**35**	±40	±45	µA	max	A
Inverting Input Bias Current Drift	V_{CM} = 0V	±10	±100	±100	±150	nA/°C	max	B
Input(4)								
Common-Mode Input Range (CMIR)(5)		±4.5	±**4.1**	±4.0	±4.0	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V, Input-Referred	55	**51**	50	50	dB	min	A
Noninverting Input Impedance		250 ||2				kΩ ||pF	typ	C
Minimum Inverting Input Resistance	Open-Loop	22	12			Ω	min	B
Maximum Inverting Input Resistance	Open-Loop	22	35			Ω	max	B
Output(4)								
Output Voltage Swing	No Load	±5.1	±**4.9**	±4.8	±4.7	V	min	A
	R_L = 100Ω	±5.0	±**4.8**	±4.7	±4.5	V	min	A
	R_L = 25Ω	±4.8				V	typ	C
Current Output	V_O = 0	±500	±**380**	±350	±320	mA	min	A
Short-Circuit Current	V_O = 0	±800				mA	typ	C
Closed-Loop Output Impedance	G = +4, f ≤ 100kHz	0.01				Ω	typ	C
Output(4) (SO-14 Only)								
Current Output at Full Power	A1 = 1, A0 = 1, V_O = 0	±500	±**380**	±350	±320	mA	min	A
Current Output at Power Cutback	A1 = 1, A0 = 0, V_O = 0	±450	±**350**	±320	±300	mA	min	A
Current Output at Idle Power	A1 = 0, A0 = 1, V_O = 0	±100	±**60**	±55	±50	mA	min	A

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±6V (continued)

Boldface limits are tested at **+25°C.**

At T_A = +25°C, A_1 = A_0 = 1 (full power: for SO-14 only), G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figure 1 for AC performance only.

PARAMETER	TEST CONDITIONS	OPA2674ID, OPA2674I-14D						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
Power Supply								
Specified Operating Voltage		±6				V	typ	C
Maximum Operating Voltage			**±6.3**	**±6.3**	**±6.3**	V	max	A
Maximum Quiescent Current	V_S = ±6V, Both Channels	18	**18.6**	18.8	19.2	mA	max	A
Minimum Quiescent Current	V_S = ±6V, Both Channels	18	**17.4**	16.5	16.0	mA	min	A
Power-Supply Rejection Ratio (PSRR)	f = 100kHz, Input-Referred	56	**51**	49	48	dB	min	A
Power Supply (SO-14 Only)								
Maximum Logic 0	A1, A0, +V_S = +6V	2.5	**2.0**	1.8	1.5	V	max	A
Minimum Logic 1	A1, A0, +V_S = +6V	3.3	**3.6**	4.0	4.2	V	min	A
Logic Input Current	A1 = 0V, A0 = 0V, Each Line	60	**90**	100	105	µA	max	A
Supply Current at Full Power	A1 = 1, A0 = 1, Both Channels	18.0	**18.6**	18.8	19.2	mA	max	A
Supply Current at Power Cutback	A1 = 1, A0 = 0, Both Channels	13.3	**14.2**	14.4	14.8	mA	max	A
Supply Current at Idle Power	A1 = 0, A0 = 1, Both Channels	4.0	**4.8**	5.1	5.3	mA	max	A
Supply Current at Shutdown	A1 = 0, A0 = 0, Both Channels	1.0	**1.3**	1.4	1.5	mA	max	A
Output Impedance in Idle Power	G = +4, f < 1MHz	0.1				Ω	typ	C
Output Impedance in Shutdown		100 ||4				kΩ ||pF	typ	C
Supply Current Step Time	10% to 90% Change	200				ns	typ	C
Output Switching Glitch	Inputs at GND	±20				mV	typ	C
Shutdown Isolation	G = +4, 1MHz, A1 = 0, A0 = 0	85				dB	typ	C
Thermal Characteristics								
Specification: ID, I-14D		−40 to +85				°C		
Thermal Resistance, θ_{JA}								
ID SO-8	Junction-to-Ambient	125				°C/W	typ	C
I-14D SO-14		100				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At T_A = +25°C, A_1 = 1, A_0 = 1 (Full Power: for SO-14 only), G = +4, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted. See Figure 3 for AC performance only.

PARAMETER	TEST CONDITIONS	OPA2674ID, OPA2674I-14D						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
AC Performance (see Figure 3)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 536Ω	220				MHz	typ	C
	G = +2, R_F = 511Ω	175	140	130	120	MHz	min	B
	G = +4, R_F = 453Ω	168	130	126	120	MHz	min	B
	G = +8, R_F = 332Ω	175	140	130	125	MHz	min	B
Peaking at a Gain of +1	G = +1, R_F = 511Ω	0.6				dB	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +4, V_O = 0.5V_{PP}	34	24	22	20	MHz	min	B
Large-Signal Bandwidth	G = +4, V_O = 5V_{PP}	190	140	135	130	MHz	typ	C
Slew Rate	G = +4, 2V Step	900	650	625	600	V/µs	min	B
Rise Time and Fall Time	G = +4, V_O = 2V Step	2				ns	typ	C
Harmonic Distortion	G = +4, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	−65	−63	−62	−61	dBc	max	B
	R_L ≥ 500Ω	−72	−70	−69	−68	dBc	max	B
3rd-Harmonic	R_L = 100Ω	−72	−70	−69	−68	dBc	max	B
	R_L ≥ 500Ω	−74	−71	−70	−69	dBc	max	B
Input Voltage Noise	f > 1MHz	2	2.6	2.9	3.1	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	16	20	21	22	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	24	29	30	31	pA/√Hz	max	B
Channel-to-Channel Crosstalk	f = 5MHz, Input-Referred	−92				dB	typ	C
DC Performance(4)								
Open-Loop Transimpedance Gain	V_O = 0V, R_L = 100Ω	110	**72**	70	68	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±0.8	±**3.5**	±4.0	±4.3	mV	max	A
Offset Voltage Drift	V_{CM} = 0V	±4	±10	±10	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	±10	±**30**	±32	±35	µA	max	A
Noninverting Input Bias Current Drift	V_{CM} = 0V	±5	±50	±50	±75	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±10	±**35**	±40	±45	µA	max	A
Inverting Input Bias Current Drift	V_{CM} = 0V	±10	±100	±100	±150	nA/°C	max	B
Input								
Most Positive Input Voltage(5)		3.7	**3.3**	3.2	3.1	V	min	A
Most Negative Input Voltage(5)		1.3	**1.7**	1.8	1.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 2.5V, Input-Referred	53	**49**	48	47	dB	min	A
Noninverting Input Impedance		250 ‖2				kΩ ‖pF	typ	C
Minimum Inverting Input Resistance	Open-Loop	25	15			Ω	min	B
Maximum Inverting Input Resistance	Open-Loop	25	40			Ω	max	B
Output								
Most Positive Output Voltage	No Load	4.1	**3.9**	3.8	3.6	V	min	A
	R_L = 100Ω	3.9	**3.8**	3.7	3.5	V	min	A
Most Negative Output Voltage	No Load	0.8	**1.0**	1.1	1.3	V	max	A
	R_L = 100Ω	1.0	**1.1**	1.2	1.5	V	max	A
Current Output	V_O = 0	±260	±**200**	±180	±160	mA	min	A
Closed-Loop Output Impedance	G = +4, f ≤ 100kHz	0.02				Ω	typ	C
Output (SO-14 Only)								
Current Output at Full Power	A1 = 1, A0 = 1, V_O = 0	±260	±**200**	±180	±160	mA	min	A
Current Output at Power Cutback	A1 = 1, A0 = 0, V_O = 0	±200	±**160**	±140	±120	mA	min	A
Current Output at Idle Power	A1 = 0, A0 = 1, V_O = 0	±80	±**50**	±45	±40	mA	min	A

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR at min/max input ranges.

ELECTRICAL CHARACTERISTICS: V_S = +5V(continued)

Boldface limits are tested at **+25°C.**

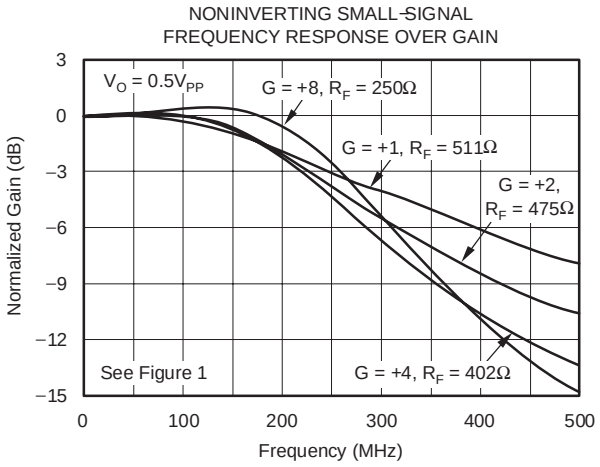
At T_A = +25°C, A_1 = 1, A_0 = 1 (Full Power: for SO-14 only), G = +4, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted. See Figure 3 for AC performance only.

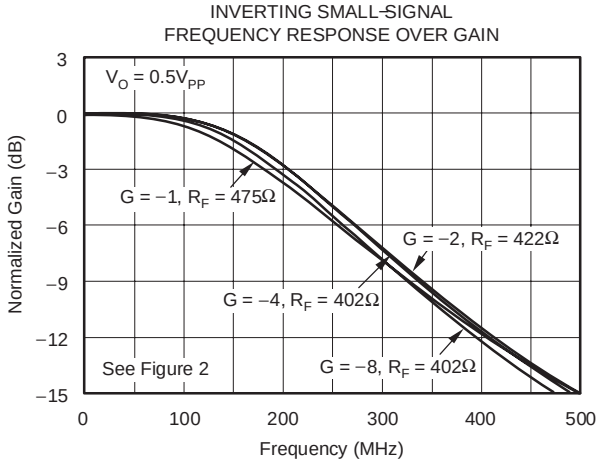
PARAMETER	TEST CONDITIONS	OPA2674ID, OPA2674I-14D						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
Power Supply (Single−Supply Mode)								
Specified Operating Voltage		+5				V	typ	C
Maximum Operating Voltage			**12.6**	12.6	12.6	V	max	A
Maximum Quiescent Current	V_S = +5V, Both Channels	13.6	**14.8**	15.2	15.6	mA	max	A
Minimum Quiescent Current	V_S = +5V, Both Channels	13.6	**12**	11.7	11.4	mA	min	A
Power-Supply Rejection Ratio (PSRR)	f = 100kHz, Input-Referred	52				dB	typ	C
Power Control (SO-14 Only)								
Maximum Logic 0	A1, A0, +V_S = +5V	1.5	**1.0**	0.9	0.8	V	max	A
Minimum Logic 1	A1, A0, +V_S = +5V	2.4	**2.7**	3.1	3.3	V	min	A
Logic Input Current	A1 = 0V, A0 = 0V, Each Line	50	**80**	90	95	µA	max	A
Supply Current at Full Power	A1 = 1, A0 = 1, Both Channels	13.8	**14.8**	15.2	15.6	mA	max	A
Supply Current at Power Cutback	A1 = 1, A0 = 0, Both Channels	10.2	**10.8**	11.1	11.4	mA	max	A
Supply Current at Idle Power	A1 = 1, A0 = 1, Both Channels	3.0	**3.2**	3.5	3.8	mA	max	A
Supply Current at Shutdown	A1 = 0, A0 = 0, Both Channels	0.6	**0.9**	1.0	1.1	mA	max	A
Output Impedance in Idle Power	G = +4, f = 1MHz					Ω	typ	C
Output Impedance in Shutdown		100 ‖4				kΩ ‖pF	typ	C
Supply Current Step Time	10% to 90% Change	200				ns	typ	C
Output Switching Glitch	Inputs at GND	±20				mV	typ	C
Shutdown Isolation	G = +4, 1MHz, A1 = 0, A0 = 0	85				dB	typ	C
Thermal Characteristics								
Specification: ID, I-14D		−40 to +85				°C		
Thermal Resistance, θ_{JA}								
ID SO-8	Junction-to-Ambient	125				°C/W	typ	C
I-14D SO-14		100				°C/W	typ	C

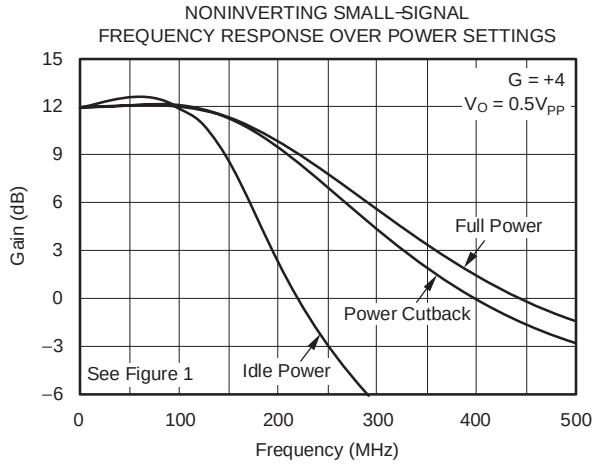
(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current considered positive out of node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR at min/max input ranges.

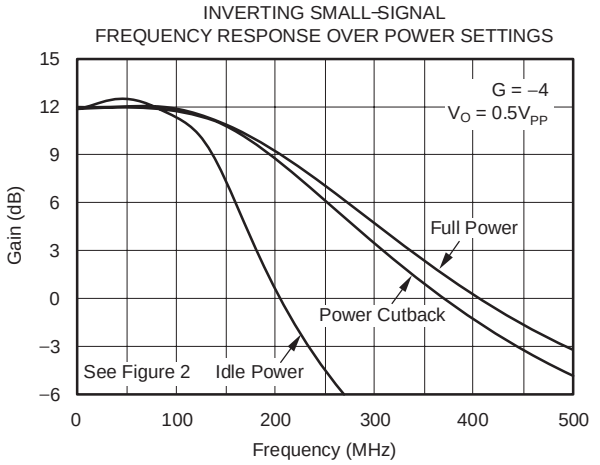
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$

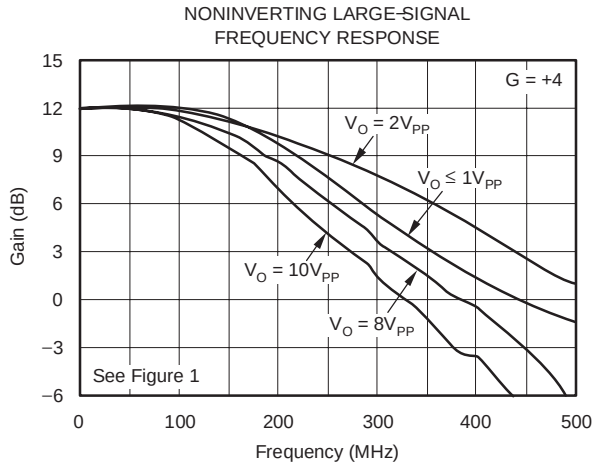
At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

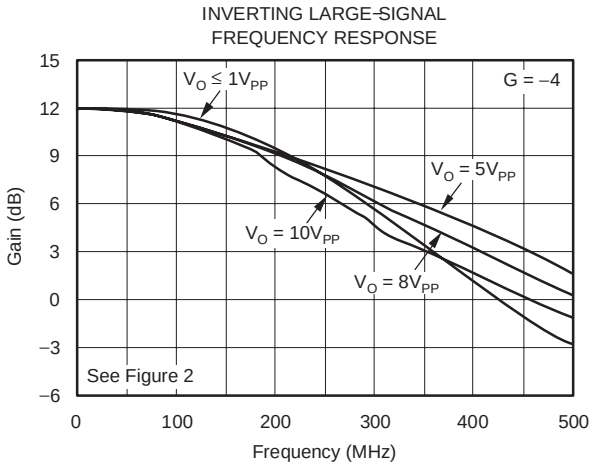








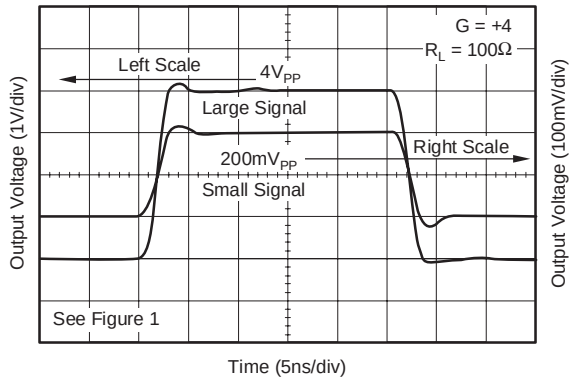




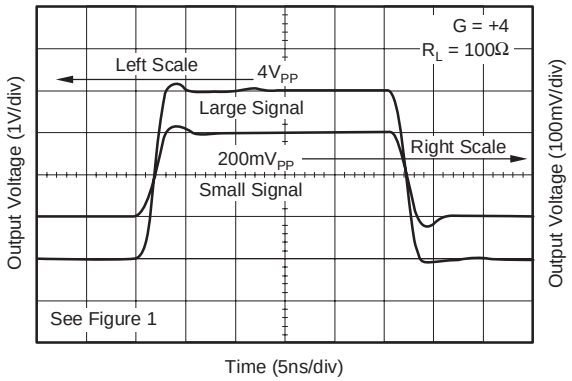
TYPICAL CHARACTERISTICS: V_S = ±6V (continued)

At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

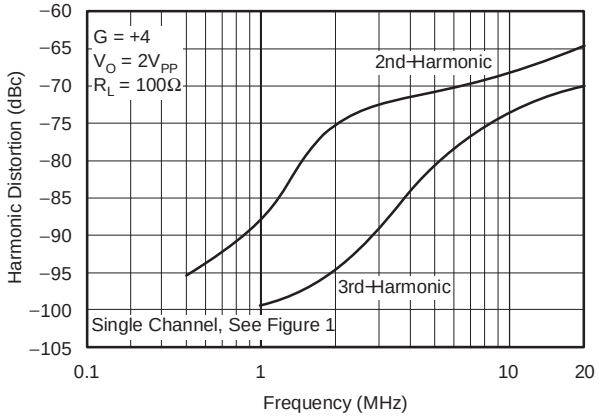
NONINVERTING PULSE RESPONSE



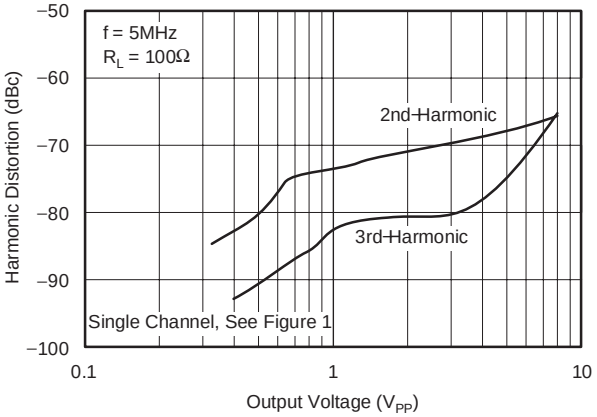
NONINVERTING PULSE RESPONSE



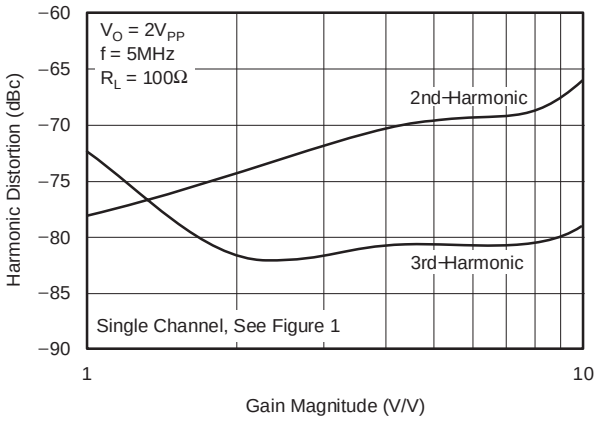
HARMONIC DISTORTION vs FREQUENCY



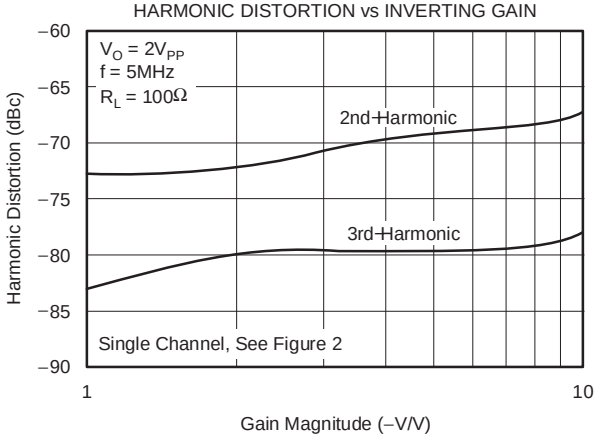
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN

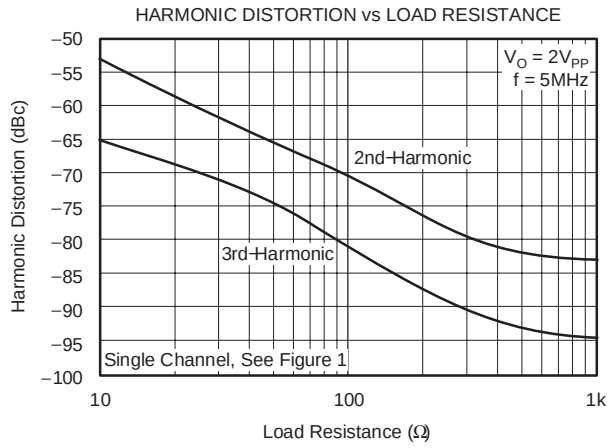


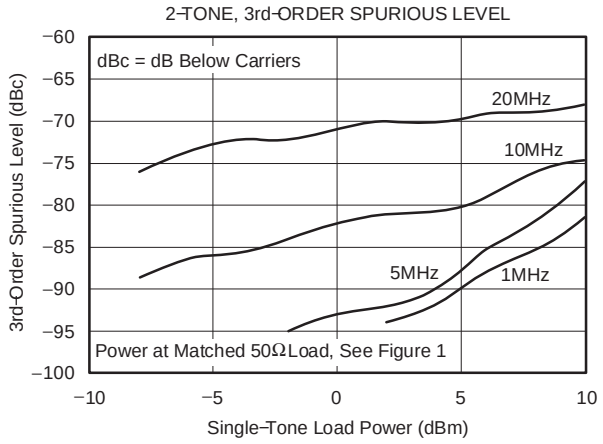
HARMONIC DISTORTION vs INVERTING GAIN

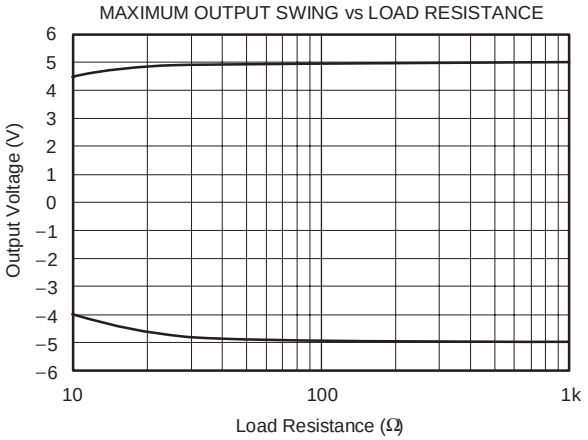


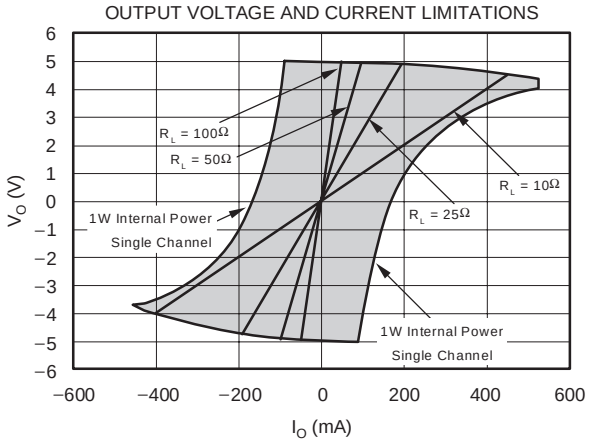
TYPICAL CHARACTERISTICS: V_S = ±6V (continued)

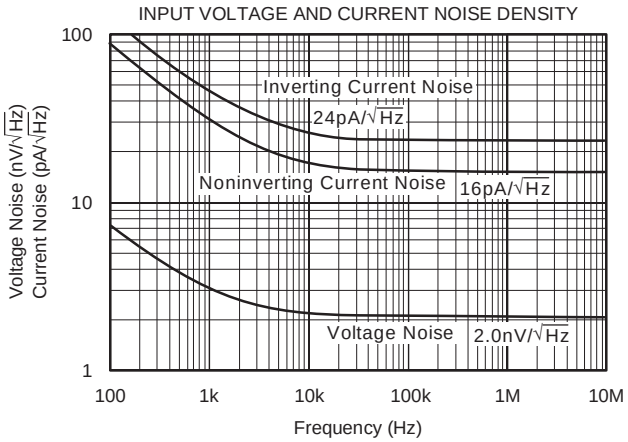
At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

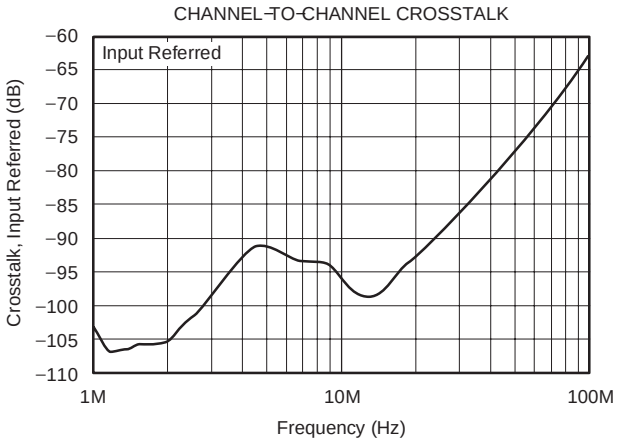






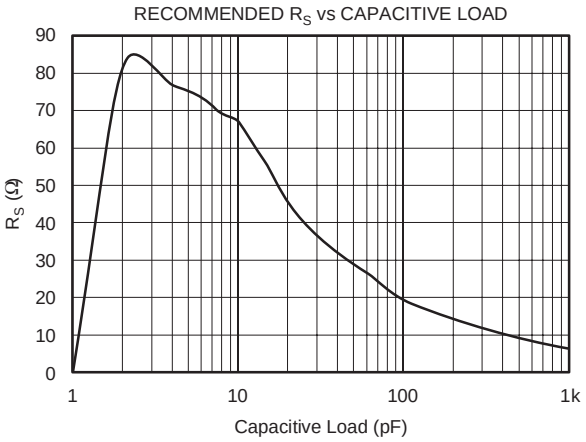


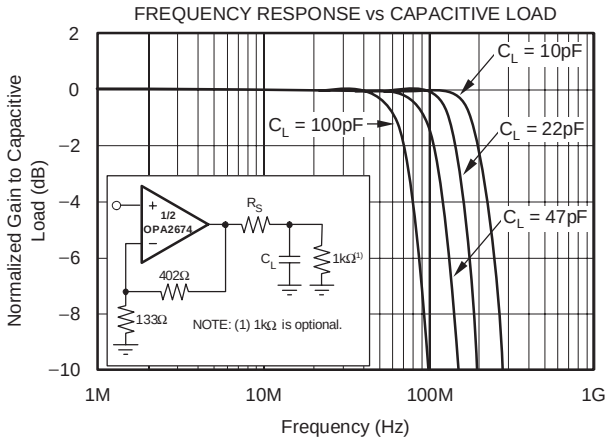


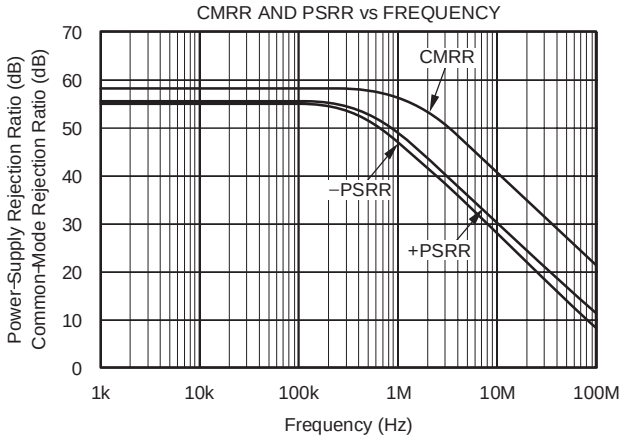


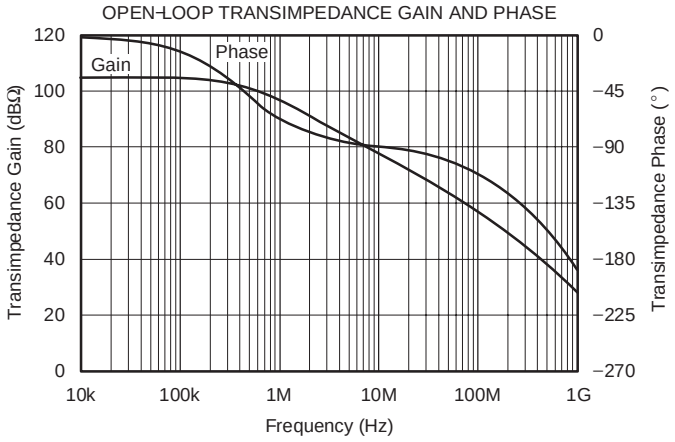
TYPICAL CHARACTERISTICS: V_S = ±6V (continued)

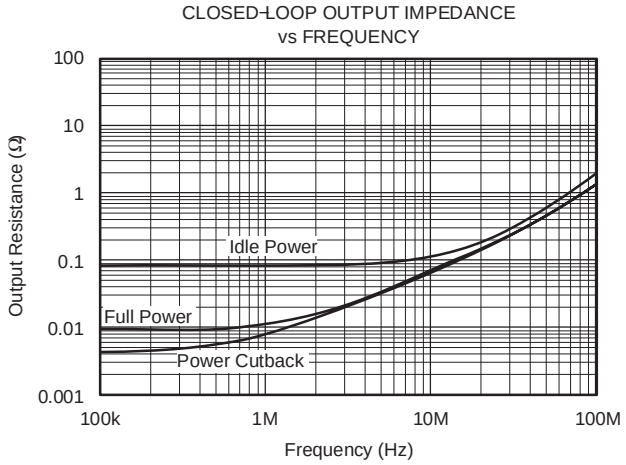
At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

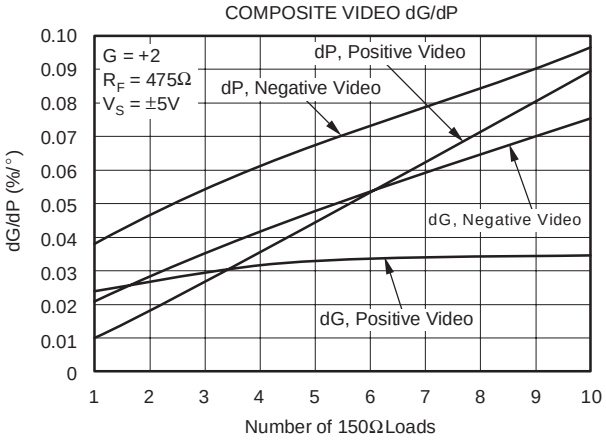






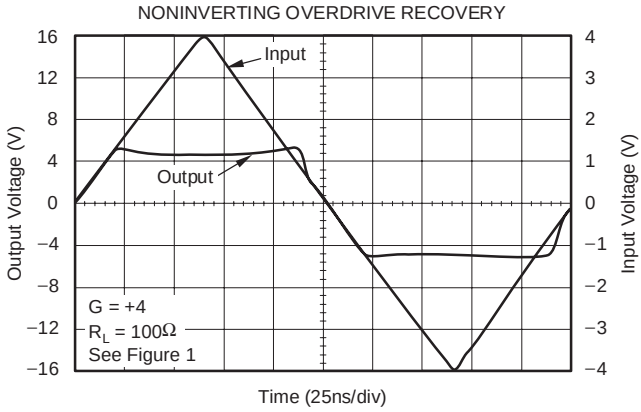


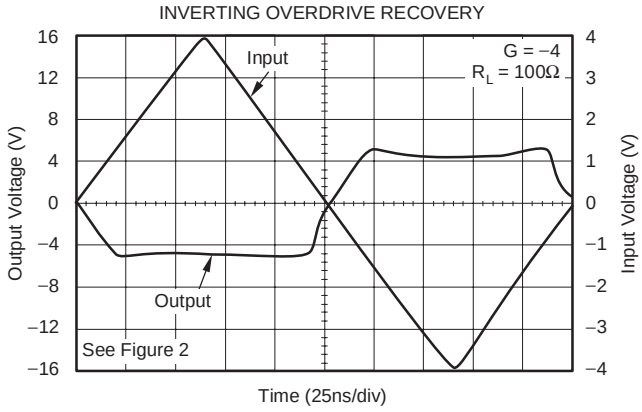


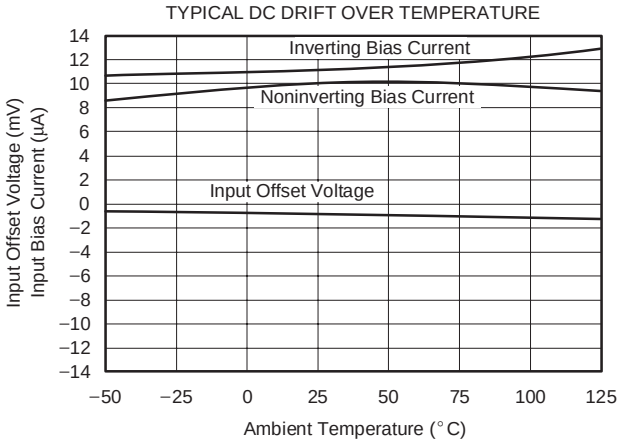


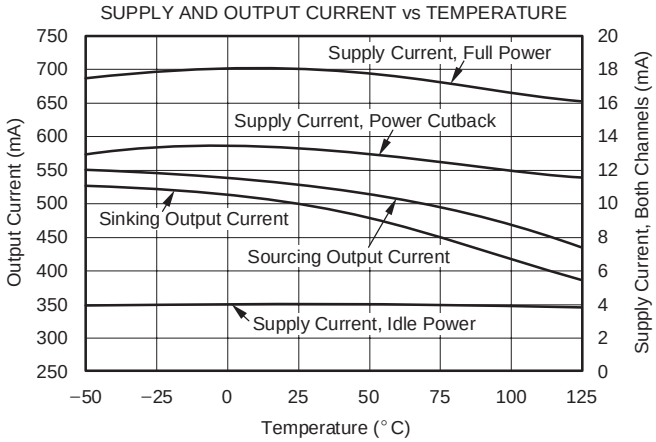
TYPICAL CHARACTERISTICS: V_S = ±6V (continued)

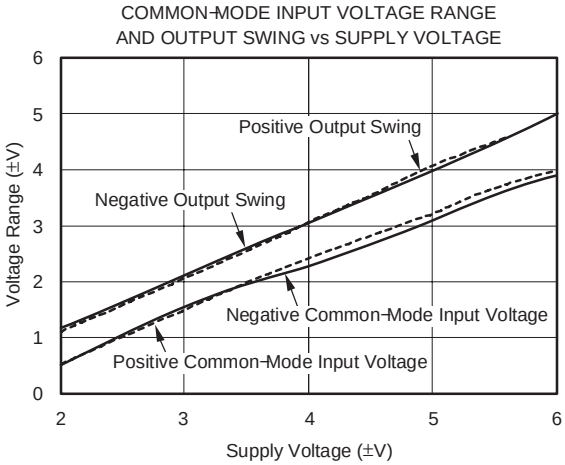
At T_A = +25°C, G = +4, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.





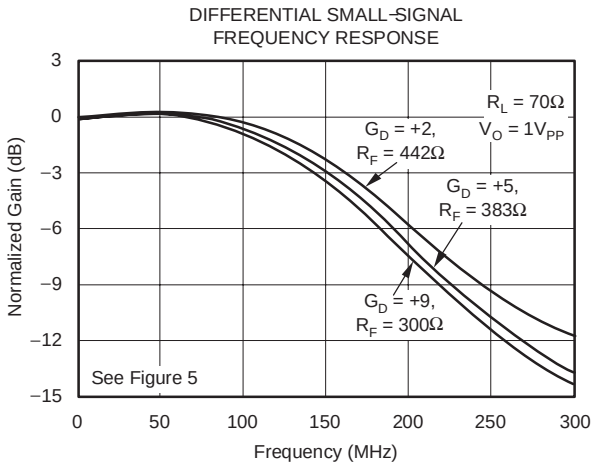


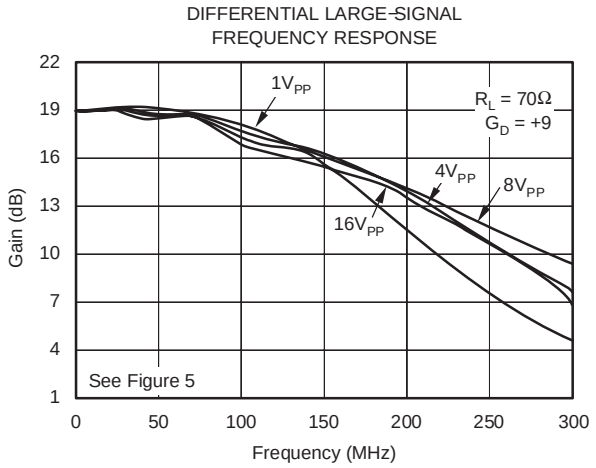


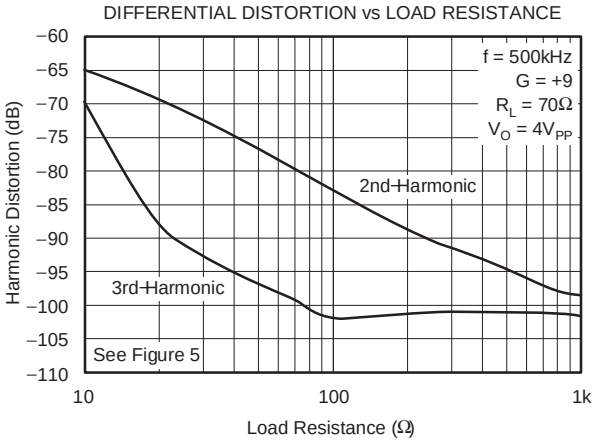


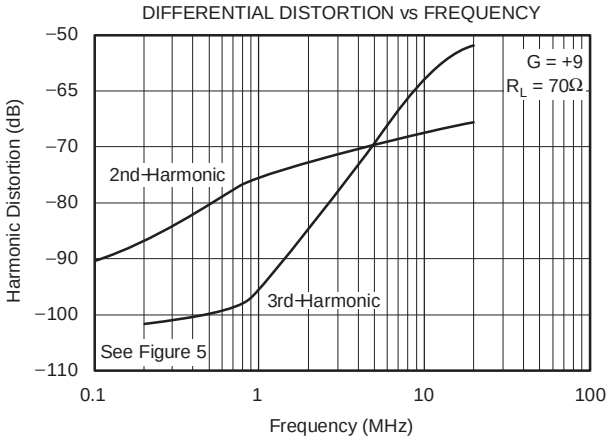
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$

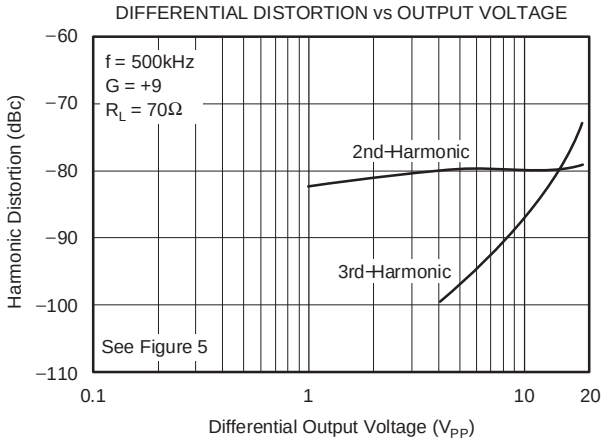
At T_A = +25°C, Differential Gain = +9, R_F = 300Ω, and R_L = 70Ω, unless otherwise noted. See Figure 5 for AC performance only.

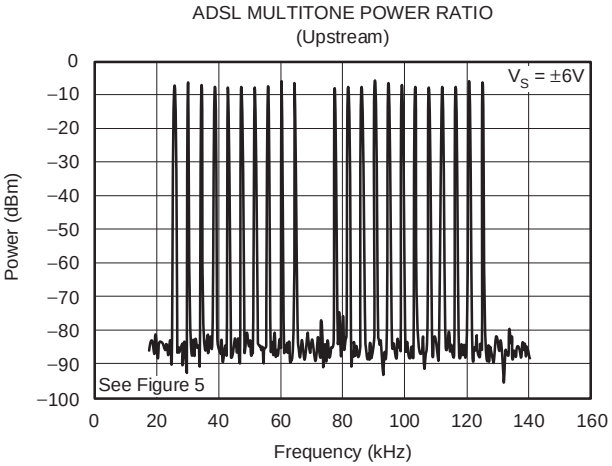








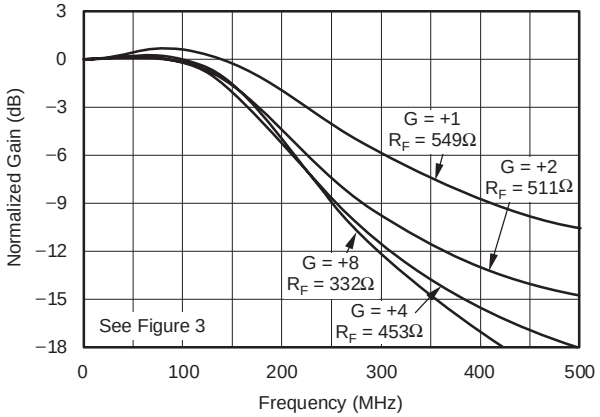




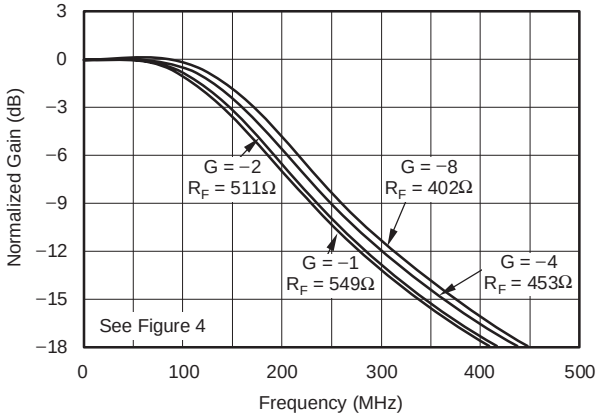
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +4, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted.

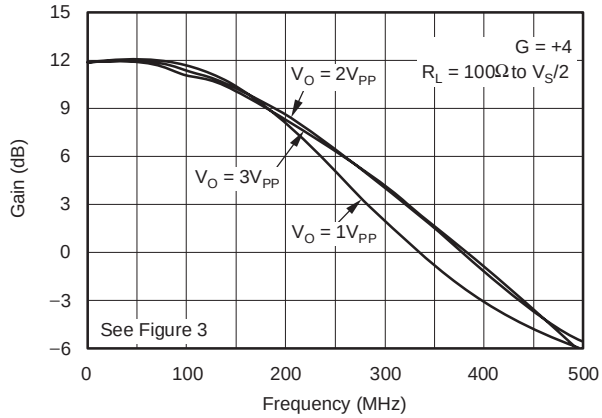
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



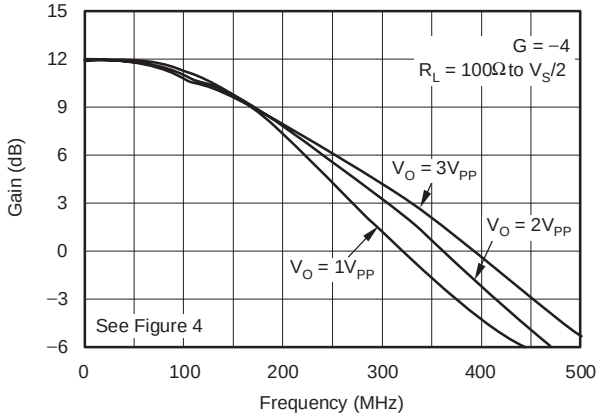
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



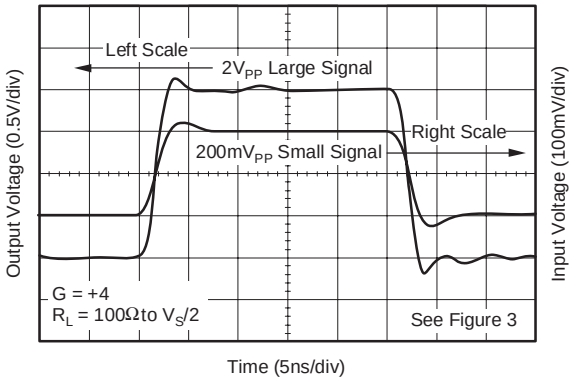
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



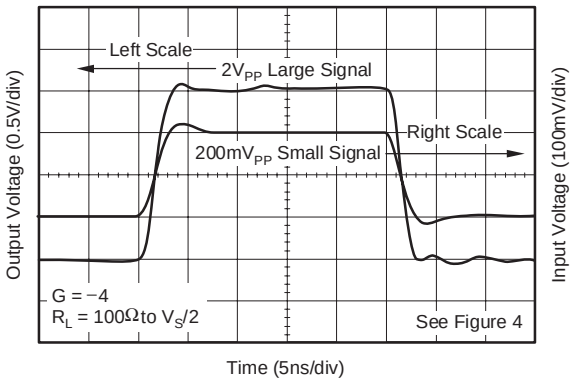
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE

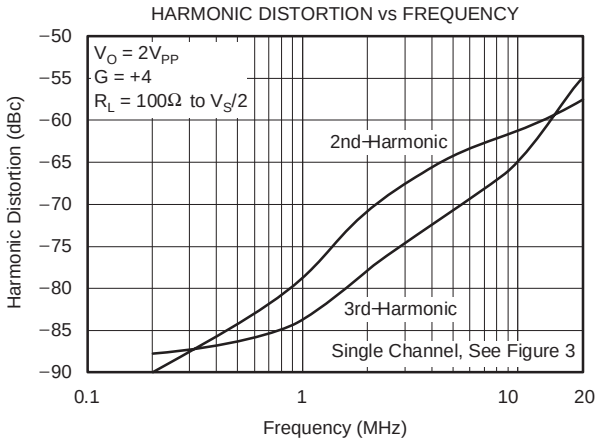


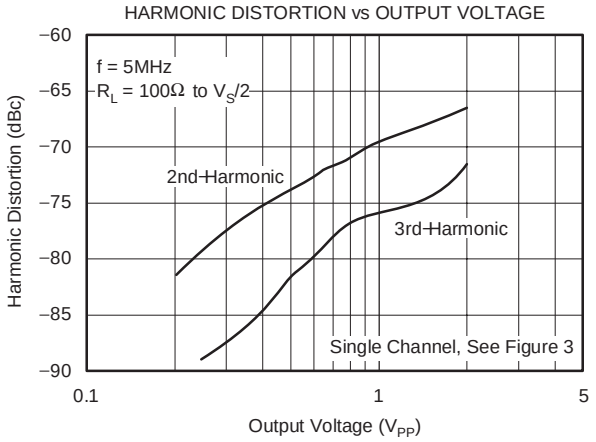
INVERTING PULSE RESPONSE

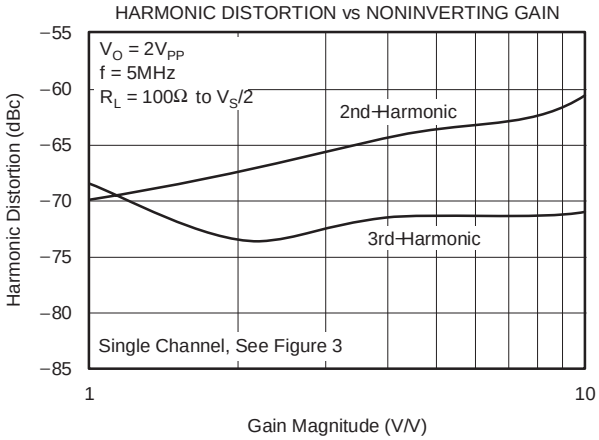


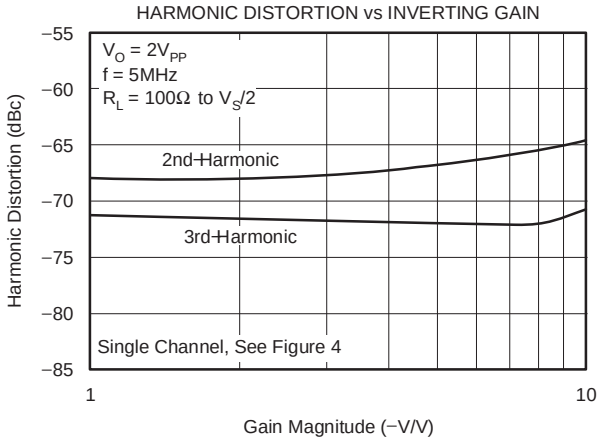
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

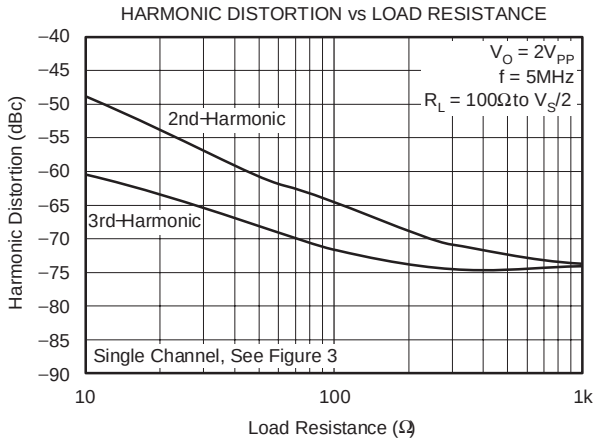
At T_A = +25°C, G = +4, R_F = 453Ω, and R_L = 100Ω, unless otherwise noted.

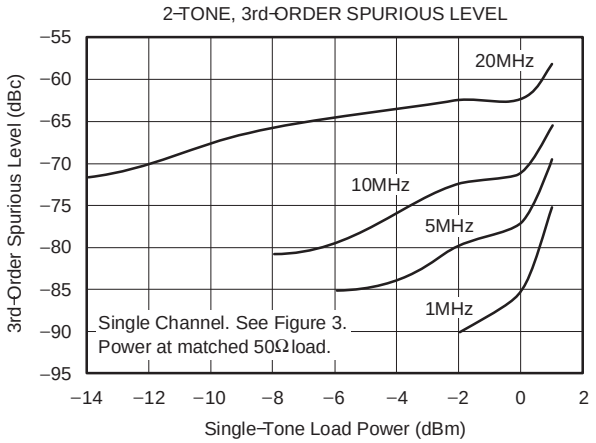








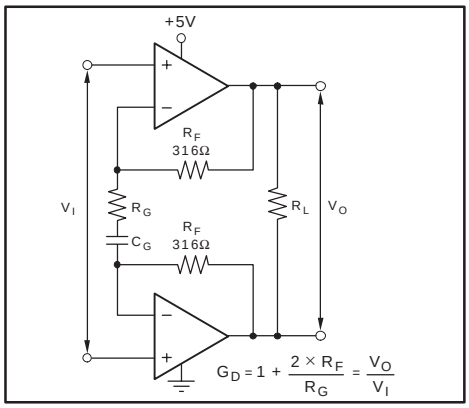




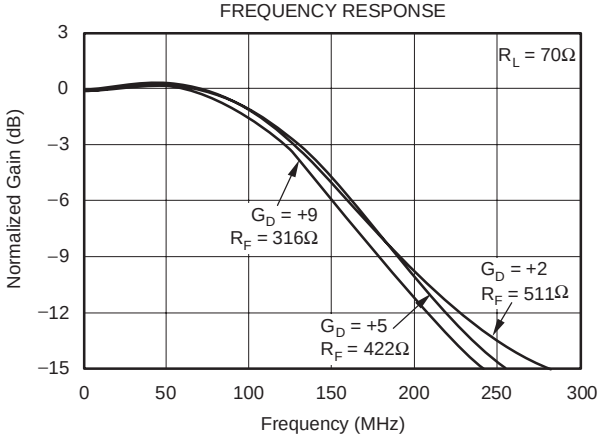
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, Differential Gain = +9, R_F = 316Ω, and R_L = 70Ω, unless otherwise noted.

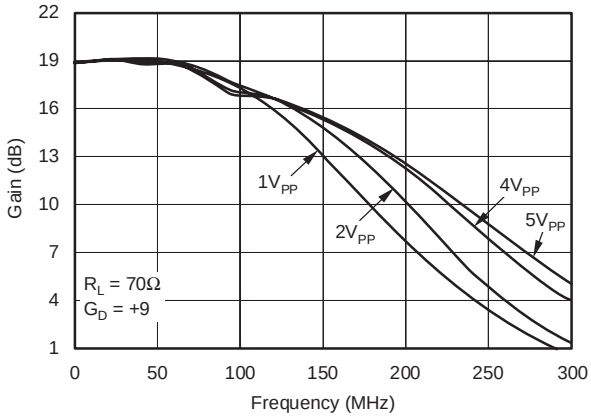
DIFFERENTIAL PERFORMANCE TEST CIRCUIT



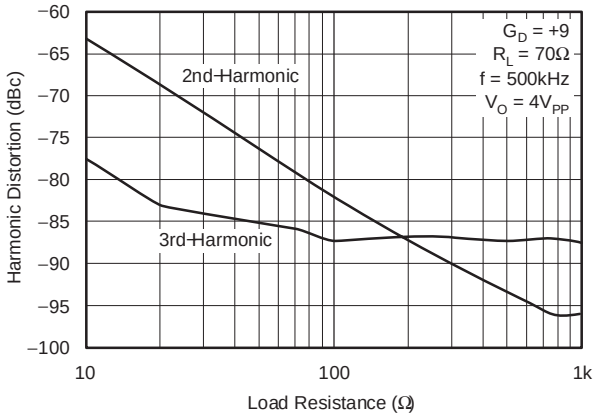
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



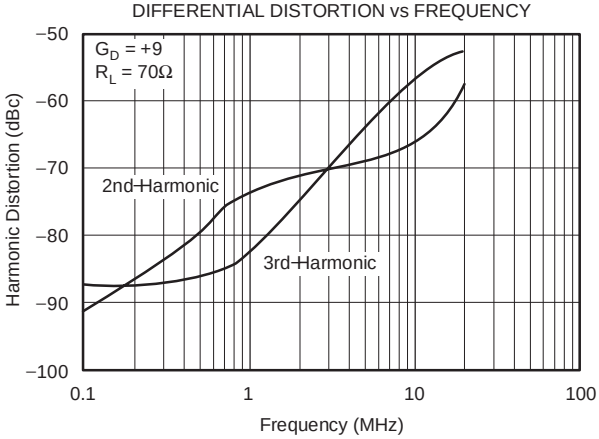
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



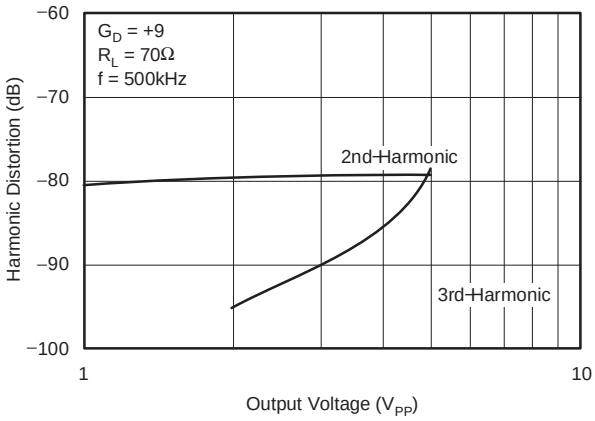
HARMONIC DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs OUTPUT VOLTAGE



APPLICATION INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA2674 gives the exceptional AC performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 9mA/ch quiescent current, the OPA2674 swings to within 1V of either supply rail and delivers in excess of 380mA at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA2674 delivers greater than 150MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion as the output current goes through zero. The OPA2674 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain. Figure 1 shows the DC-coupled, gain of +4, dual power-supply circuit configuration used as the basis of the ±6V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the electrical characteristics are taken directly at the input and output pins whereas load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load is 100Ω || 535Ω = 84Ω.

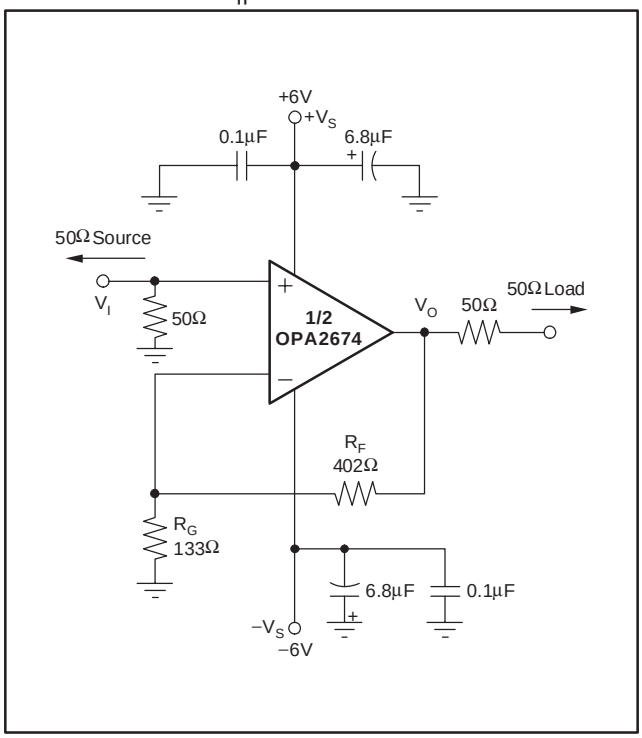


Figure 1. DC-Coupled, G = +4, Bipolar Supply, Specification and Test Circuit

Figure 2 shows the DC-coupled, bipolar supply circuit inverting gain configuration used as the basis for the ±6V Electrical and Typical Characteristics. Key design considerations of the inverting configuration are developed in the Inverting Amplifier Operation discussion.

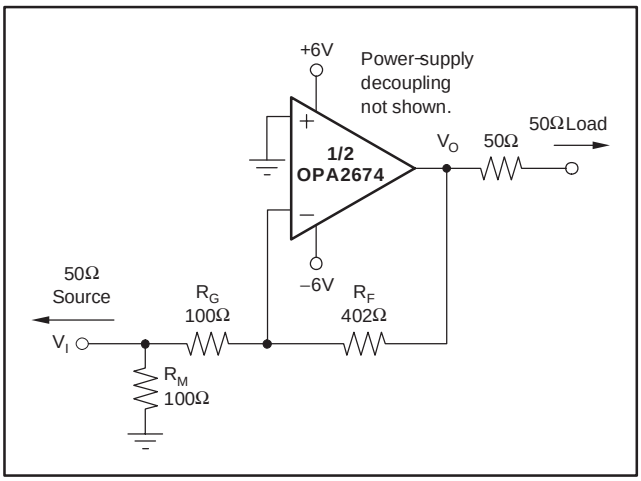


Figure 2. DC-Coupled, G = −4, Bipolar Supply, Specification and Test Circuit

Figure 3 shows the AC-coupled, gain of +4, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a rail-to-rail design, the OPA2674 requires minimal input and output voltage headroom compared to other wideband current-feedback op amps. It will deliver a $3V_{PP}$ output swing on a single +5V supply with greater than 100MHz bandwidth. The key requirement of broadband single- supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.3V of either supply pin, giving a $2.4V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1—which puts the input DC bias voltage (2.5V) on the output as well. The feedback resistor value is adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5V, gain of +4, operation. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 200mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA2674 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, harmonic distortion plots in the Typical Characteristics charts.

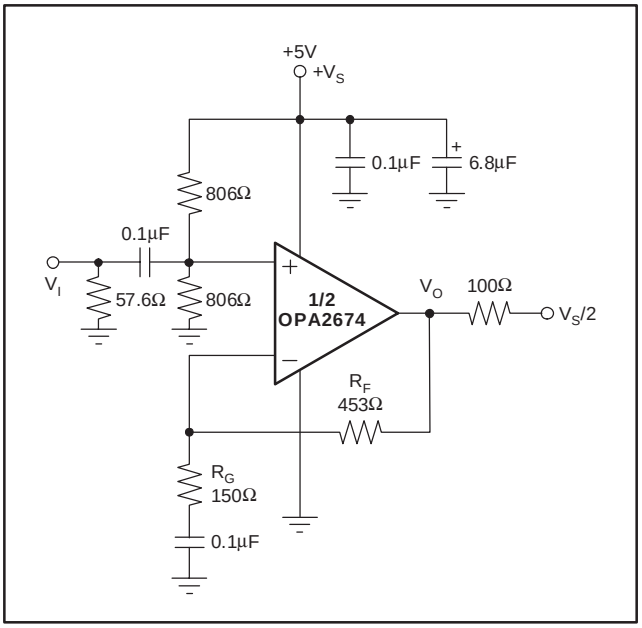


Figure 3. AC-Coupled, G = +4, Single-Supply, Specification and Test Circuit

The last configuration used as the basis of the +5V Electrical and Typical Characteristics is shown in Figure 4. Design considerations for this inverting, bipolar supply configuration are covered either in single-supply configuration (as shown in Figure 3) or in the Inverting Amplifier Operation discussion.

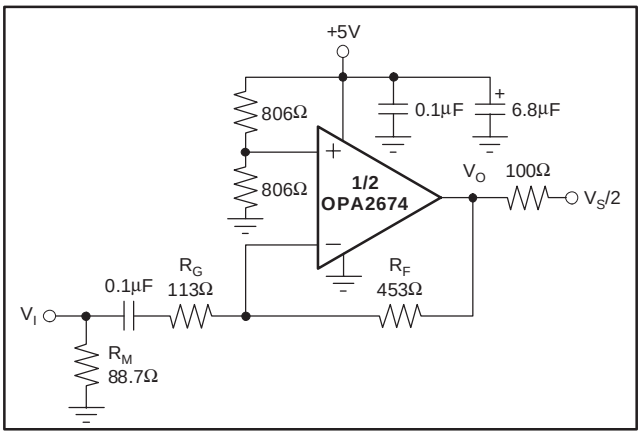


Figure 4. AC-Coupled, G = −4, Single-Supply, Specification and Test Circuit

SINGLE-SUPPLY ADSL UPSTREAM DRIVER

Figure 5 shows a single-supply ADSL upstream driver. The dual OPA2674 is configured as a differential gain stage to provide signal drive to the primary of the transformer (here, a step-up transformer with a turns ratio of 1:1.7). The main advantage of this configuration is the reduction of even-order harmonic distortion products. Another important advantage for ADSL is that each amplifier needs only half of the total output swing required to drive the load.

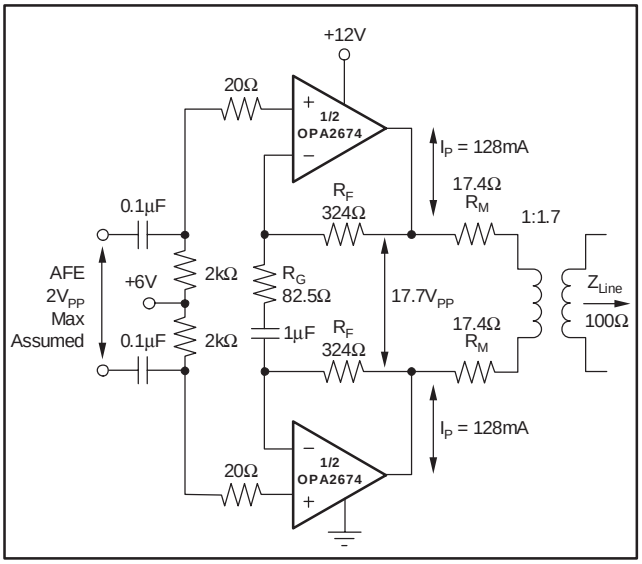


Figure 5. Single-Supply ADSL Upstream Driver

The analog front-end (AFE) signal is AC-coupled to the driver and the noninverting input of each amplifier is biased to the mid-supply voltage (in this case, +6V). Furthermore, by providing the proper biasing to the amplifier, this scheme also provides high-pass filtering with a corner frequency set here at 5kHz. As the upstream signal bandwidth starts at 26kHz, this high-pass filter does not generate any problems and has the advantage of filtering out unwanted lower frequencies.

The input signal is amplified with a gain set by the following equation:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (1)$$

With R_F = 324Ω and R_G = 82.5Ω, the gain for this differential amplifier is 8.85. This gain boosts the AFE signal, assumed to be a maximum of $2V_{PP}$, to a maximum of $17.7V_{PP}$.

Refer to the *Setting Resistor Values to Optimize Bandwidth* section for a discussion on which feedback resistor value to choose.

The two back-termination resistors (17.4Ω each) added at each input of the transformer make the impedance of the modem match the impedance of the phone line, and also provide a means of detecting the received signal for the receiver. The value of these resistors (R_M) is a function of the line impedance and the transformer turns ratio (n), given by the following equation:

$$R_M = \frac{Z_{LINE}}{2n^2} \quad (2)$$

OPA2674 HDSL2 UPSTREAM DRIVER

Figure 6 shows an HDSL2 implementation of a single-supply driver.

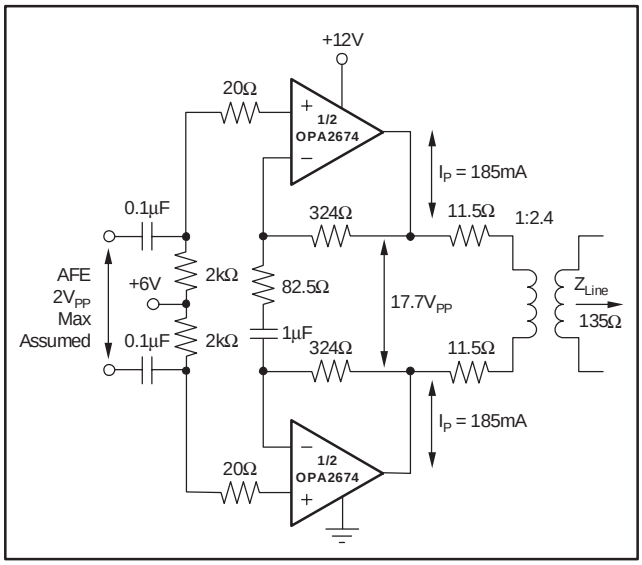


Figure 6. HDSL2 Upstream Driver

The two designs differ by the values of the matching impedance, the load impedance, and the ratio turns of the transformers. All of these differences are reflected in the higher peak current and thus, the higher maximum power dissipation in the output of the driver.

LINE DRIVER HEADROOM MODEL

The first step in a driver design is to compute the peak-to-peak output voltage from the target specifications. This is done using the following equations:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1mW) \times R_L} \quad (3)$$

With P_L power and V_{RMS} voltage at the load, and R_L load impedance, this gives:

$$V_{RMS} = \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (4)$$

$$V_P = \text{CrestFactor} \times V_{RMS} = CF \times V_{RMS} \quad (5)$$

with V_P peak voltage at the load and CF Crest Factor;

$$V_{LPP} = 2 \times CF \times V_{RMS} \quad (6)$$

with V_{LPP}: peak-to-peak voltage at the load.

Consolidating Equations 3 through 6 allows the required peak-to-peak voltage at the load function of the crest factor, the load impedance, and the power in the load to be expressed. Thus:

$$V_{LPP} = 2 \times CF \times \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (7)$$

This V_{LPP} is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step for the driver is to compute the individual amplifier output voltage and currents as a function of V_{PP} on the line and transformer turns ratio. As the turns ratio changes, the minimum allowed supply voltage also changes. The peak current in the amplifier is given by:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4R_M} \quad (8)$$

With V_{LPP} defined in Equation 7 and R_M defined in Equation 2. The peak current is computed in Figure 7 by noting that the total load is $4R_M$ and that the peak current is half of the peak-to-peak calculated using V_{LPP}.

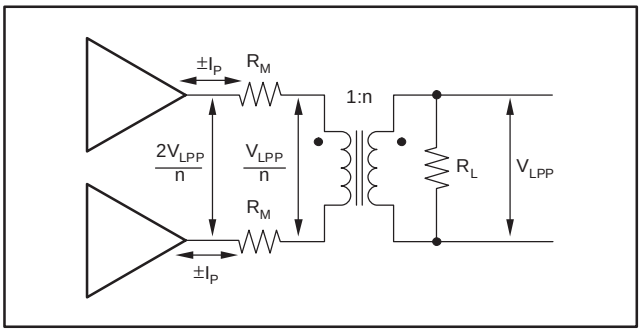


Figure 7. Driver Peak Output Model

With the required output voltage and current versus turns ratio set, an output stage headroom model will allow the required supply voltage versus turns ratio to be developed.

The headroom model (see Figure 8) can be described with the following set of equations:

First, as available output voltage for each amplifier:

$$V_{OPP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (9)$$

Or, second, as required single-supply voltage:

$$V_{CC} = V_{OPP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (10)$$

The minimum supply voltage for a power and load requirement is given by Equation 10.

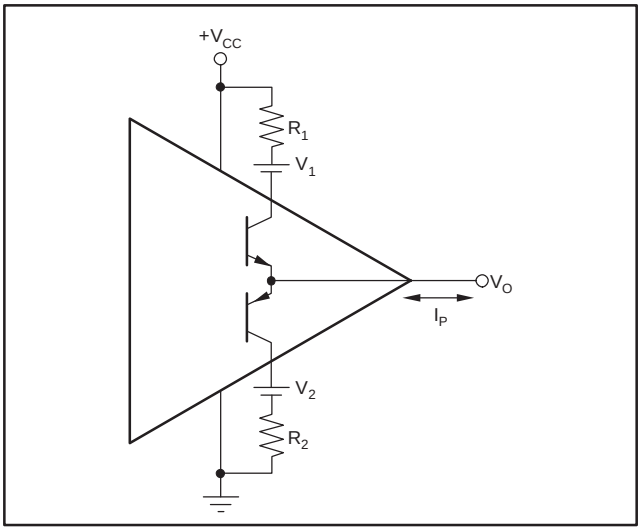


Figure 8. Line Driver Headroom Model

Table 1 gives V_1, V_2, R_1, and R_2 for both +12V and +5V operation of the OPA2674.

Table 1. Line Driver Headroom Model Values

	V_1	R_1	V_2	R_2
+5V	0.9V	5Ω	0.8V	5Ω
+12V	0.9V	2Ω	0.9V	2Ω

TOTAL DRIVER POWER FOR xDSL APPLICATIONS

The total internal power dissipation for the OPA2674 in an xDSL line driver application will be the sum of the quiescent power and the output stage power. The OPA2674 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage will be greater than the solution given in Equation 10). The total output stage power may be computed with reference to Figure 9.

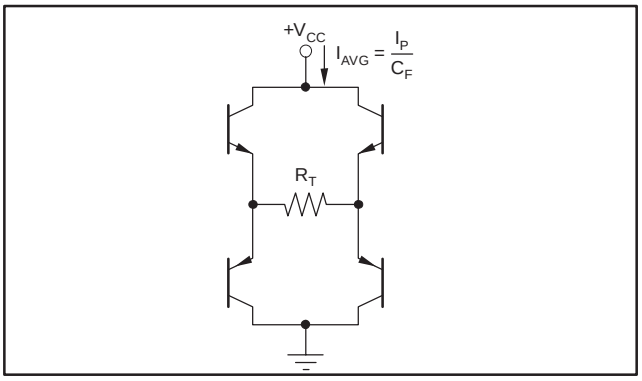


Figure 9. Output Stage Power Model

The two output stages used to drive the load of Figure 7 can be seen as an H-Bridge in Figure 9. The average current drawn from the supply into this H-Bridge and load will be the peak current in the load given by Equation 8 divided by the crest factor (CF) for the xDSL modulation. This total power from the supply is then reduced by the power in R_T to leave the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 2 plus the power lost in the matching elements (R_M). In the examples here, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by Equation 11.

$$P_{OUT} = \frac{I_P}{C_F} \times V_{CC} - 2P_L \tag{11}$$

The total amplifier power is then:

$$P_{TOT} = I_q \times V_{CC} + \frac{I_P}{C_F} \times V_{CC} - 2P_L \tag{12}$$

For the ADSL CPE upstream driver design of Figure 5, the peak current is 128mA for a signal that requires a crest factor of 5.33 with a target line power of 13dBm into 100Ω (20mW). With a typical quiescent current of 18mA and a nominal supply voltage of +12V, the total internal power dissipation for the solution of Figure 5 will be:

$$P_{TOT} = 18mA(12V) + \frac{128mA}{5.33}(12V) - 2(20mW) = 464mW \tag{13}$$

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2674 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 2.

Table 2. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2674ID	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2674I-14D	SO-14	DEM-OPA-SO-2D	SBOU002

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2674 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2674 is available through the

TI web site (www.ti.com). This model does a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions, but does not do as well in predicting the harmonic distortion or dG/dP characteristics. This model does not attempt to distinguish between the package types in small-signal AC performance, nor does it attempt to simulate channel-to- channel coupling.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp such as the OPA2674 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values, which are shown in the Typical Characteristics; the small-signal bandwidth decreases only slightly with increasing gain. These characteristic curves also show that the feedback resistor is changed for each gain setting. The resistor values on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements, whereas the ratios set the signal gain. Figure 10 shows the small-signal frequency response analysis circuit for the OPA2674.

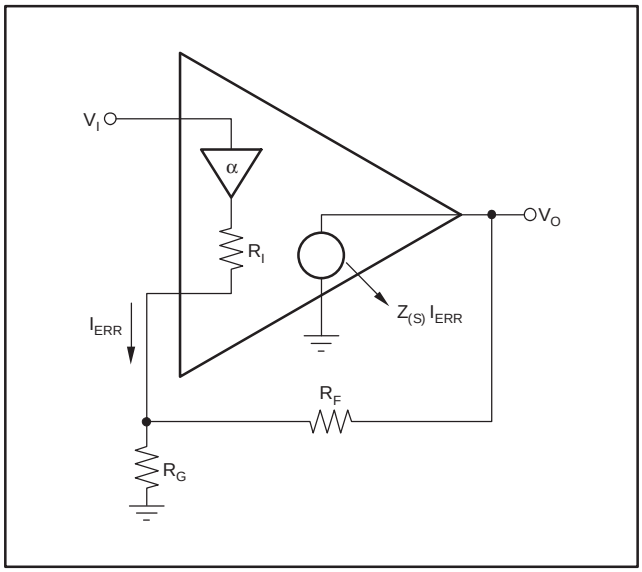


Figure 10. Current-Feedback Transfer Function Analysis Circuit

The key elements of this current-feedback op amp model are:

α = buffer gain from the noninverting input to the inverting input

R_I = buffer output impedance

I_{ERR} = feedback error current signal

Z(s) = frequency dependent open-loop transimpedance gain from I_{ERR} to V_O

$$NG = NoiseGain = 1 + \frac{R_F}{R_G}$$

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. This gain, however, sets the CMRR for a single op amp differential amplifier configuration. For a buffer gain of $\alpha < 1.0$, the CMRR = $-20 \bullet \log(1 - \alpha)$dB.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2674 inverting output impedance is typically 22Ω.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response, which is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 10 gives Equation 14:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1 + \frac{R_F}{R_G}\right)}{1 + \frac{R_F + R_I\left(1 + \frac{R_F}{R_G}\right)}{Z(s)}} = \frac{\alpha \times NG}{1 + \frac{R_F + R_I \times NG}{Z(s)}} \quad (14)$$

This is written in a loop-gain analysis format, where the errors arising from a non-infinite open-loop gain are shown in the denominator. If Z(s) were infinite over all frequencies, the denominator of Equation 14 reduces to 1 and the ideal desired signal gain shown in the numerator is achieved. The fraction in the denominator of Equation 14 determines the frequency response. Equation 15 shows this as the loop-gain equation:

$$\frac{Z(s)}{R_F + R_I \times NG} = LoopGain \quad (15)$$

If 20 log(R_F + NG × R_I) is drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 15, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier closed-loop frequency response given by Equation 14 starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 15 may be controlled somewhat separately from the desired signal gain (or NG). The OPA2674 is internally compensated to give a maximally flat frequency response for R_F = 402Ω at NG = 4 on ±6V supplies. Evaluating the denomi-

nator of Equation 15 (which is the feedback transimpedance) gives an optimal target of 490Ω. As the signal gain changes, the contribution of the $NG \times R_I$ term in the feedback transimpedance changes, but the total can be held constant by adjusting R_F. Equation 16 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 490 - NG \times R_I \qquad (16)$$

As the desired signal gain increases, this equation eventually suggests a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values load both the buffer stage at the input and the output stage if R_F gets too low—actually decreasing the bandwidth. Figure 11 shows the recommended R_F versus NG for both ±6V and a single +5V operation. The values for R_F versus gain shown here are approximately equal to the values used to generate the Typical Characteristics. They differ in that the optimized values used in the Typical Characteristics are also correcting for board parasitic not considered in the simplified analysis leading to Equation 16. The values shown in Figure 11 give a good starting point for designs where bandwidth optimization is desired.

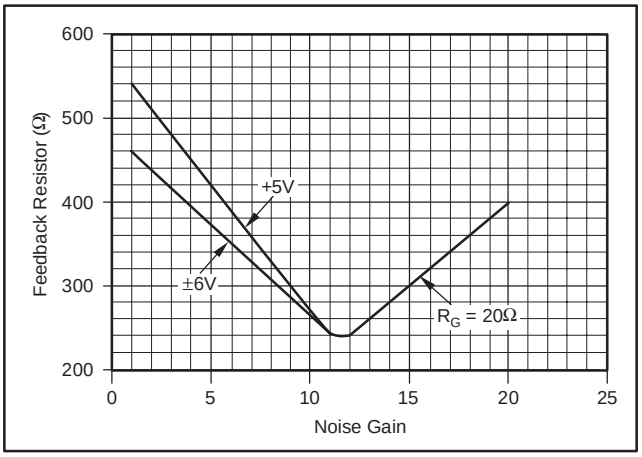


Figure 11. Feedback Resistor vs Noise Gain

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction increases the feedback impedance (the denominator of Equation 15), decreasing the bandwidth. The internal buffer output impedance for the OPA2674 is slightly influenced by the source impedance coming from of the noninverting input terminal. High-source resistors also have the effect of increasing R_I, decreasing the bandwidth. For those single-supply applications that develop a midpoint bias at the noninverting input through high valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, noninverting input noise current shunting, and to minimize the high-frequency value for R_I in Figure 10.

INVERTING AMPLIFIER OPERATION

As the OPA2674 is a general-purpose, wideband current-feedback op amp, most of the familiar op amp application circuits are available to the designer. Those dual op amp applications that require considerable flexibility in the feedback element (for example, integrators, transimpedance, and some filters) should consider a unity-gain stable, voltage-feedback amplifier such as the OPA2822, because the feedback resistor is the compensation element for a current-feedback op amp. Wideband inverting operation (and especially summing) is particularly suited to the OPA2674. Figure 12 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

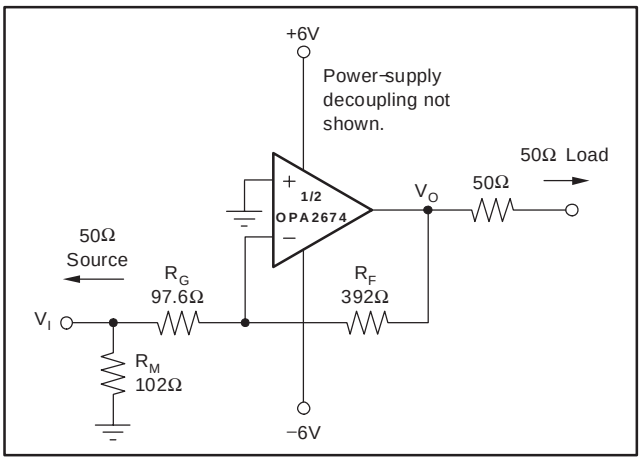


Figure 12. Inverting Gain of −4 with Impedance Matching

In the inverting configuration, two key design considerations must be noted. First, the gain resistor (R_G) becomes part of the signal source input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace, or other transmission line conductor), it is normally necessary to add an additional matching resistor to ground. R_G, by itself, normally is not set to the required input impedance since its value, along with the desired gain, will determine an R_F, which may be nonoptimal from a frequency response standpoint. The total input impedance for the source becomes the parallel combination of R_G and R_M.

The second major consideration is that the signal source impedance becomes part of the noise gain equation and has a slight effect on the bandwidth through Equation 15. The values shown in Figure 12 have accounted for this by slightly decreasing R_F (from the optimum values) to reoptimize the bandwidth for the noise gain of Figure 12 (NG = 3.98). In the example of Figure 12, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 102Ω =

33.5Ω. This impedance is added in series with R_G for calculating the noise gain—which gives NG = 3.98. This value, and the inverting input impedance of 22Ω, are inserted into Equation 16 to get the R_F that appears in Figure 12. Note that the noninverting input in this bipolar supply inverting application is connected directly to ground.

It is often suggested that an additional resistor be connected to ground on the noninverting input to achieve bias current error cancellation at the output. The input bias currents for a current-feedback op amp are not generally matched in either magnitude or polarity. Connecting a resistor to ground on the noninverting input of the OPA2674 in the circuit of Figure 12 actually provides additional gain for that input bias and noise currents, but does not decrease the output DC error because the input bias currents are not matched.

OUTPUT CURRENT AND VOLTAGE

The OPA2674 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; the tested (+25°C) swing limit is within 1.1V of either rail. Into a 6Ω load (the minimum tested load), it delivers more than ±380mA.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current (or V−I product) that is more relevant to circuit operation. Refer to the Output Voltage and Current Limitations plot in the Typical Characteristics (see page 9). The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2674 output drive capabilities, noting that the graph is bounded by a safe operating area of 1W maximum internal power dissipation (in this case, for one channel only). Superimposing resistor load lines onto the plot shows that the OPA2674 can drive ±4V into 10Ω or ±4.5V into 25Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±5.0V output swing capability, as stated in the Electrical Characteristics tables. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristics tables. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an analog-to-digital (A/D) converter—including additional external capacitance that may be recommended to improve the A/D converter linearity. A high-speed, high open-loop gain amplifier like the OPA2674 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The Typical Characteristics show the Recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2674. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2674 output pin (see the *Board Layout Guidelines* section).

DISTORTION PERFORMANCE

The OPA2674 provides good distortion performance into a 100Ω load on ±6V supplies. It also provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1), this is the sum of $R_F + R_G$; in the inverting configuration, it is R_F. Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing directly increases harmonic distortion. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2x rate, whereas the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the

2nd-harmonic decreases less than the expected 6dB, whereas the difference between it and the 3rd-harmonic decreases by less than the expected 12dB. This factor also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low-output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (that is, $2V_{PP}$ for each tone at the load, which requires $8V_{PP}$ for the overall 2-tone envelope at the output pin), the Typical Characteristics show 67dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2674 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (24pA/√Hz) is lower than earlier solutions whereas the input voltage noise (2.0nV/√Hz) is lower than most unity-gain stable, wideband voltage-feedback op amps. This low input voltage noise is achieved at the price of higher noninverting input current noise (16pA/√Hz). As long as the AC source impedance from the noninverting node is less than 100Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 13 shows the op amp noise analysis model with all noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 17 shows the general form for the output noise voltage using the terms given in Figure 13.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN} \times R_S\right)^2 + 4kTR_S + \left(I_{BI} \times R_F\right)^2 + 4kTR_F NG\right)} \quad (17)$$

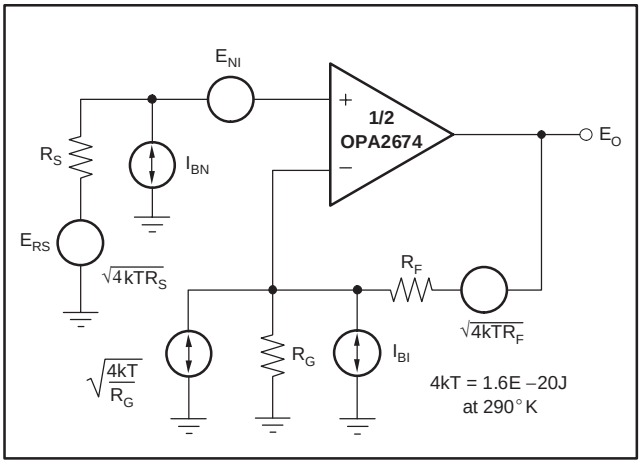


Figure 13. Op Amp Noise Analysis Model

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 18.

$$E_N = \sqrt{\left(E_{NI}^2 + \left(I_{BN} \times R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI} \times R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}\right)} \quad (18)$$

Evaluating these two equations for the OPA2674 circuit and component values of Figure 1 gives a total output spot noise voltage of 14.3nV/√Hz and a total equivalent input spot noise voltage of 3.6nV/√Hz. This total input-referred spot noise voltage is higher than the 2.0nV/√Hz specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input-referred voltage noise given by Equation 18 approaches just the 2.0nV/√Hz of the op amp. For example, going to a gain of +10 using R_F = 298Ω gives a total input-referred noise of 2.3nV/√Hz.

DIFFERENTIAL NOISE PERFORMANCE

As the OPA2674 is used as a differential driver in xDSL applications, it is important to analyze the noise in such a configuration. See Figure 14 for the op amp noise model for the differential configuration.

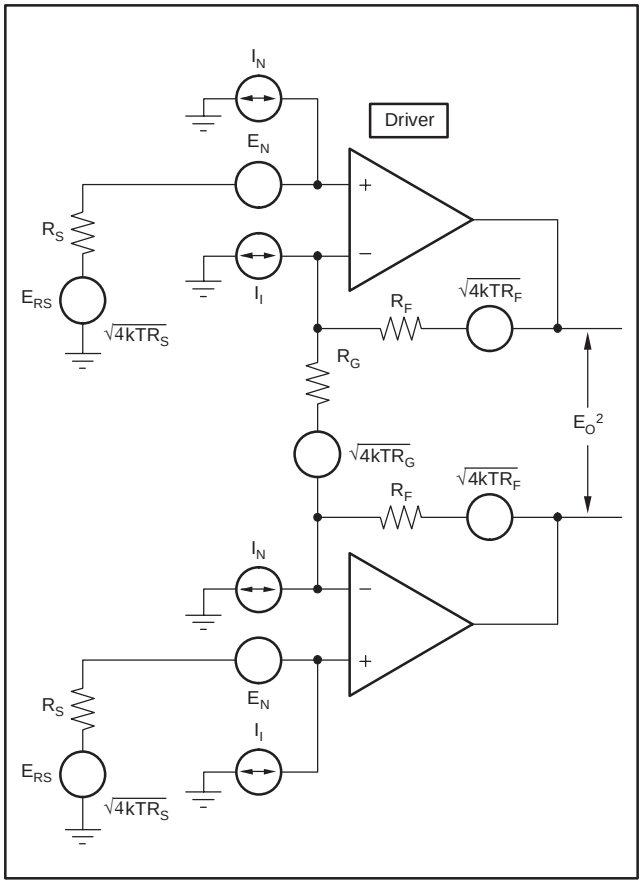


Figure 14. Differential Op Amp Noise Analysis Model

As a reminder, the differential gain is expressed as:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \tag{19}$$

The output noise voltage can be expressed as shown below:

$$e_O^2 = \sqrt{2 \times G_D^2 \times \left(e_N^2 + \left(i_N \times R_S\right)^2 + 4kTR_S\right) + 2\left(i_I R_F\right)^2 + 2\left(4kTR_F G_D\right)} \tag{20}$$

Dividing this expression by the differential noise gain $G_D = (1 + 2R_F/R_G)$ gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 21.

$$e_N = \sqrt{2 \times \left(e_N^2 + \left(i_N \times R_S\right)^2 + 4kTR_S\right) + 2\left(i_I \frac{R_F}{G_D}\right)^2 + 2\left(\frac{4kTR_F}{G_D}\right)} \tag{21}$$

Evaluating this equation for the OPA2674 circuit and component values of Figure 5 gives a total output spot noise voltage of 31.0nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 3.5nV/$\sqrt{Hz}$.

In order to minimize the noise contributed by I_N, it is recommended to keep the noninverting source impedance as low as possible.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the OPA2674 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. While bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$V_{OS} = \pm (NG \times V_{IO(MAX)}) \pm (I_{BN} \times R_S/2 \times NG) \pm (I_{BI} \times R_F)$$

where NG = noninverting signal gain

$$= \pm (4 \times 4.5mV) \pm (30\mu A \times 25\Omega \times 4) \pm (402\Omega \times 35\mu A)$$

$$= \pm 18mV \pm 3mV \pm 14mV$$

$$V_{OS} = \pm 35.0mV \text{ (max at 25°C)}$$

POWER CONTROL OPERATION (SO-14 ONLY)

The OPA2674I-14D provides a power control feature that may be used to reduce system power. The four modes of operation for this power control feature are full-power, power cutback, idle state, and power shutdown. These four operating modes are set through two logic lines A0 and A1. Table 3 shows the different modes of operation.

Table 3. Power Control Mode of Operation

MODE OF OPERATION	A1	A0
Full-Power	1	1
Power Cutback	1	0
Idle State	0	1
Shutdown	0	0

The full-power mode is used for normal operating condition. The power cutback mode brings the quiescent power to 13.5mA. The idle state mode keeps a low output impedance but reduces output power and bandwidth. The shutdown mode has a high output impedance as well as the lowest quiescent power (1.0mA).

If the A0 and A1 pins are left unconnected, the OPA2674I-14D operates normally (full-power).

To change the power mode, the control pins (either A0 or A1) must be asserted low. This logic control is referenced to the positive supply, as shown in the simplified circuit of Figure 15.

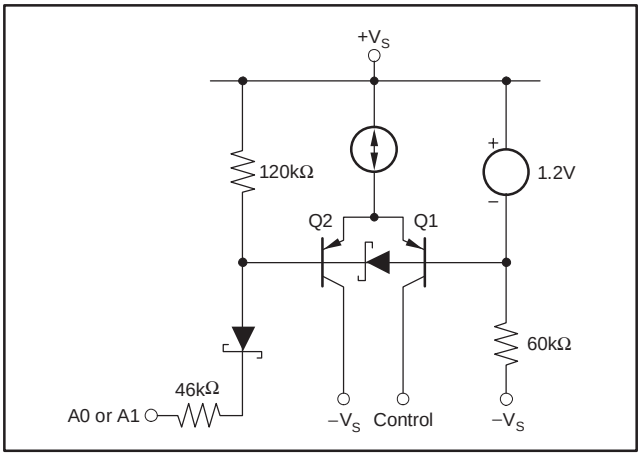


Figure 15. Supply Power Control Circuit

The shutdown feature for the OPA2674 is a positive-supply referenced, current-controlled interface. Open-collector (or drain) interfaces are most effective, as long as the controlling logic can sustain the resulting voltage (in open mode) that appears at the A0 or A1 pins. The A0/A1 pin voltage is one diode below the positive supply voltage applied to the OPA2674 if the logic interface is open. For voltage output logic interfaces, the on/off voltage levels described in the Electrical Characteristics apply only for either the +6V used for the ±6V specifications or the +5V for the single-supply specifications. An open-drain interface is recommended to operate the A1 and A0 pins using a higher positive supply and/or logic families with inadequate high-level voltage swings.

THERMAL ANALYSIS

Due to the high output power capability of the OPA2674, heat-sinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature sets the maximum allowed internal power dissipation, described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load. Using the example power calculation for the ADSL CPE line driver concluded in Equation 13, and a worst-case analysis at +70°C ambient, the maximum internal junction temperature for the SO-8 package will be:

$T_{J\,MAX} = T_{AMBIENT} + P_{MAX} \times 125°C/W$

$T_{J\,MAX} = 70°C + ((12V \times 18.8mA) + 12V \times 128mA/(5.33) - 40mW) \times 125°C/W = 129°C$

This maximum junction temperature is well below the maximum of 150°C but may exceed system design targets. Lower junction temperature would be possible using the SO-14 package and the power cutback feature. Repeating this calculation for that solution gives:

$T_{J\,MAX} = 70°C + ((12V \times 14.2mA) + 12V \times 128mA/(5.33) - 40mW) \times 100°C/W = 112°C$

For extremely high internal power applications, where improved thermal performance is required, consider the PSO-8 package of the OPA2677—a similar part with no output stage current limit and a thermal impedance of less than 50°C/W.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2674 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25″) from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 4 and 8 for an SO-8 package) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at a lower frequency, should also be used on the main supply pins. These can be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2674. Resistors should be of a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the pack-

age on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing it gives a more peaked frequency response. The 402Ω feedback resistor used in the Typical Characteristics at a gain of +4 on ±6V supplies is a good starting point for design. Note that a 511Ω feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load (see page 10). Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA2674 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard. In fact, a higher impedance environment improves distortion; see the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2674 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2674 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of R_S vs Capacitive Load. However, this does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2674 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2674 onto the board.

INPUT AND ESD PROTECTION

The OPA2674 is built using a high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices and are reflected in the absolute maximum ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 16.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2674), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, because high values degrade both noise performance and frequency response.

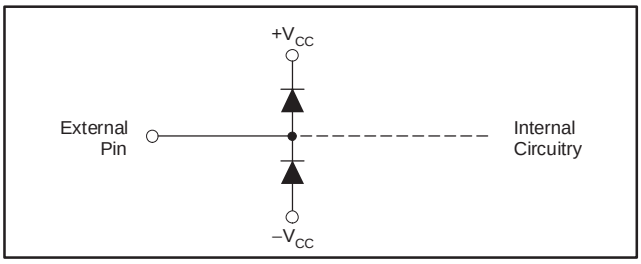


Figure 16. ESD Steering Diodes

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/08	C	2	Absolute Maximum Ratings	Changed Storage Temperature minimum value from −40°C to −65°C.
3/08	B	4, 6	Electrical Characteristics	Added Both Channels; Power Supply and Power Supply (SO−14 only) sections under Conditons.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2674I-14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA2674	Samples
OPA2674I-14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA2674	Samples
OPA2674I-14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA2674	Samples
OPA2674I-14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA2674	Samples
OPA2674ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2674	Samples
OPA2674IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2674	Samples
OPA2674IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2674	Samples
OPA2674IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2674	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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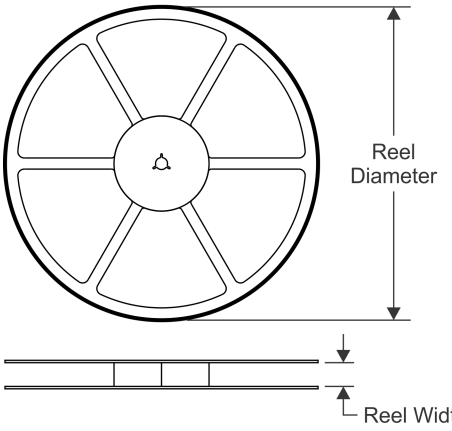
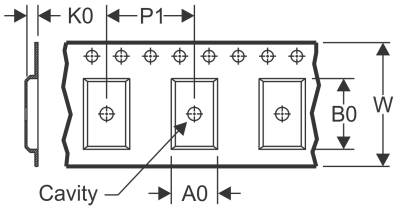
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

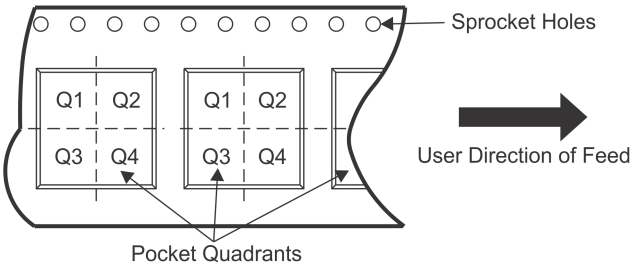


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

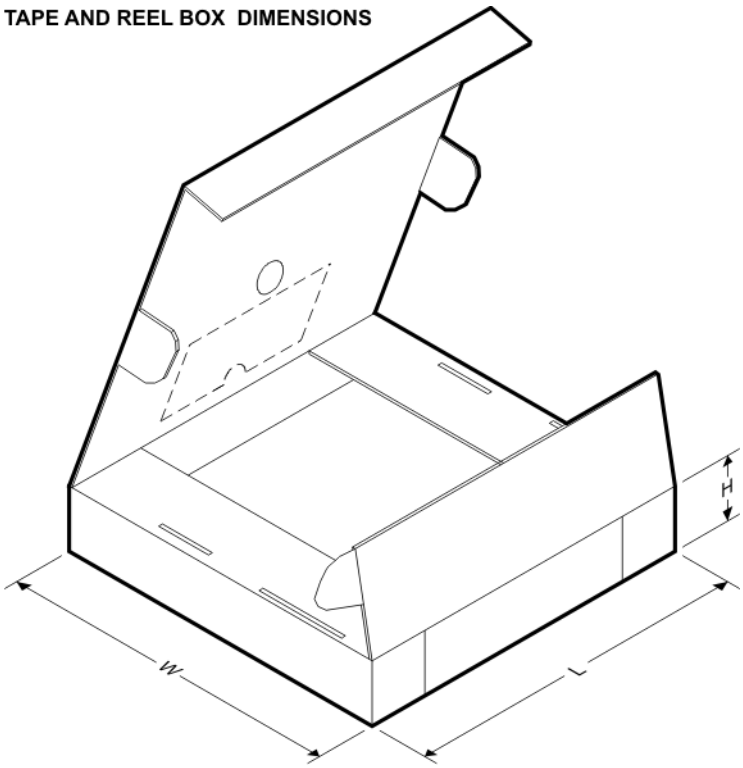
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2674I-14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA2674IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

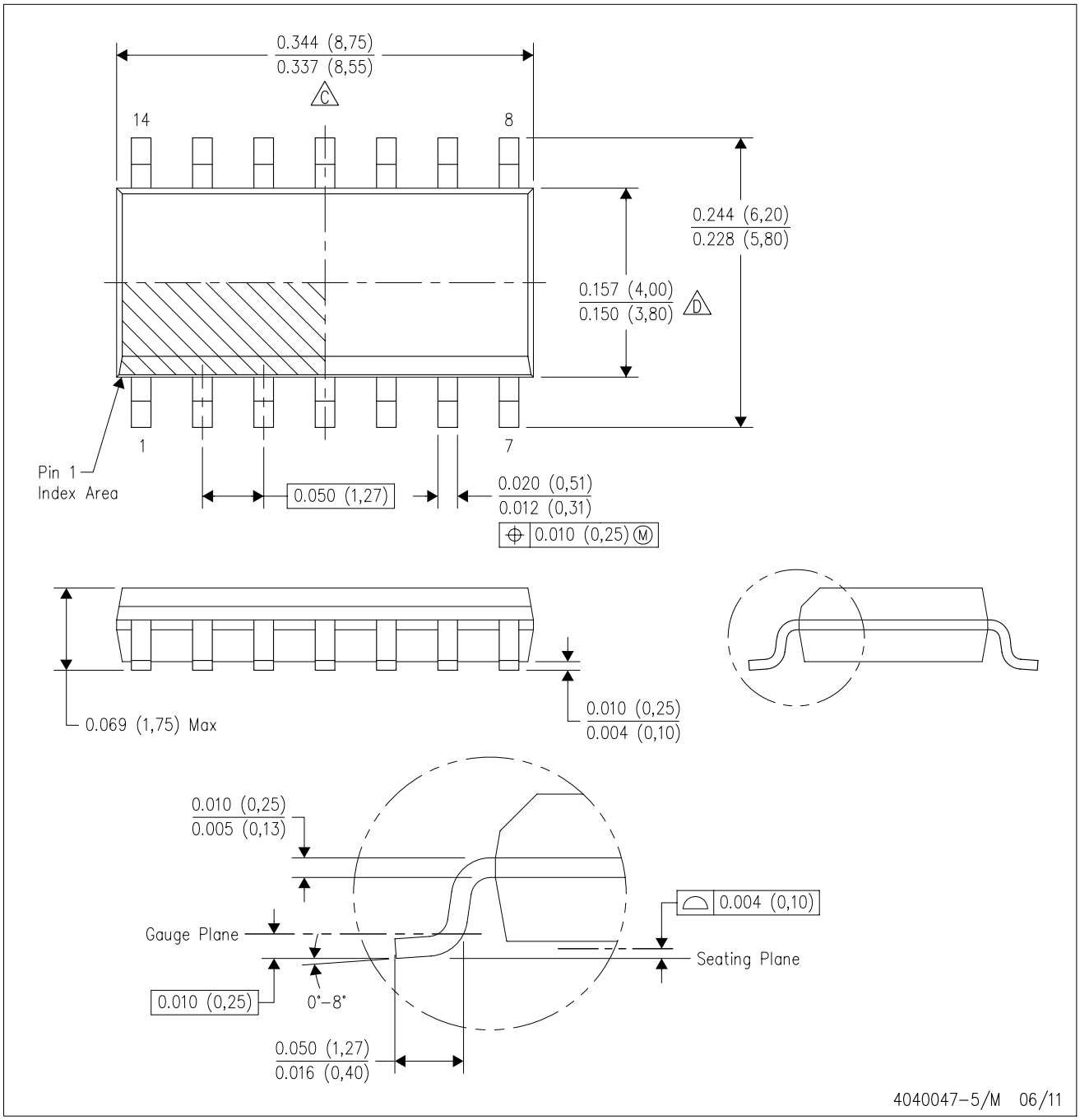
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

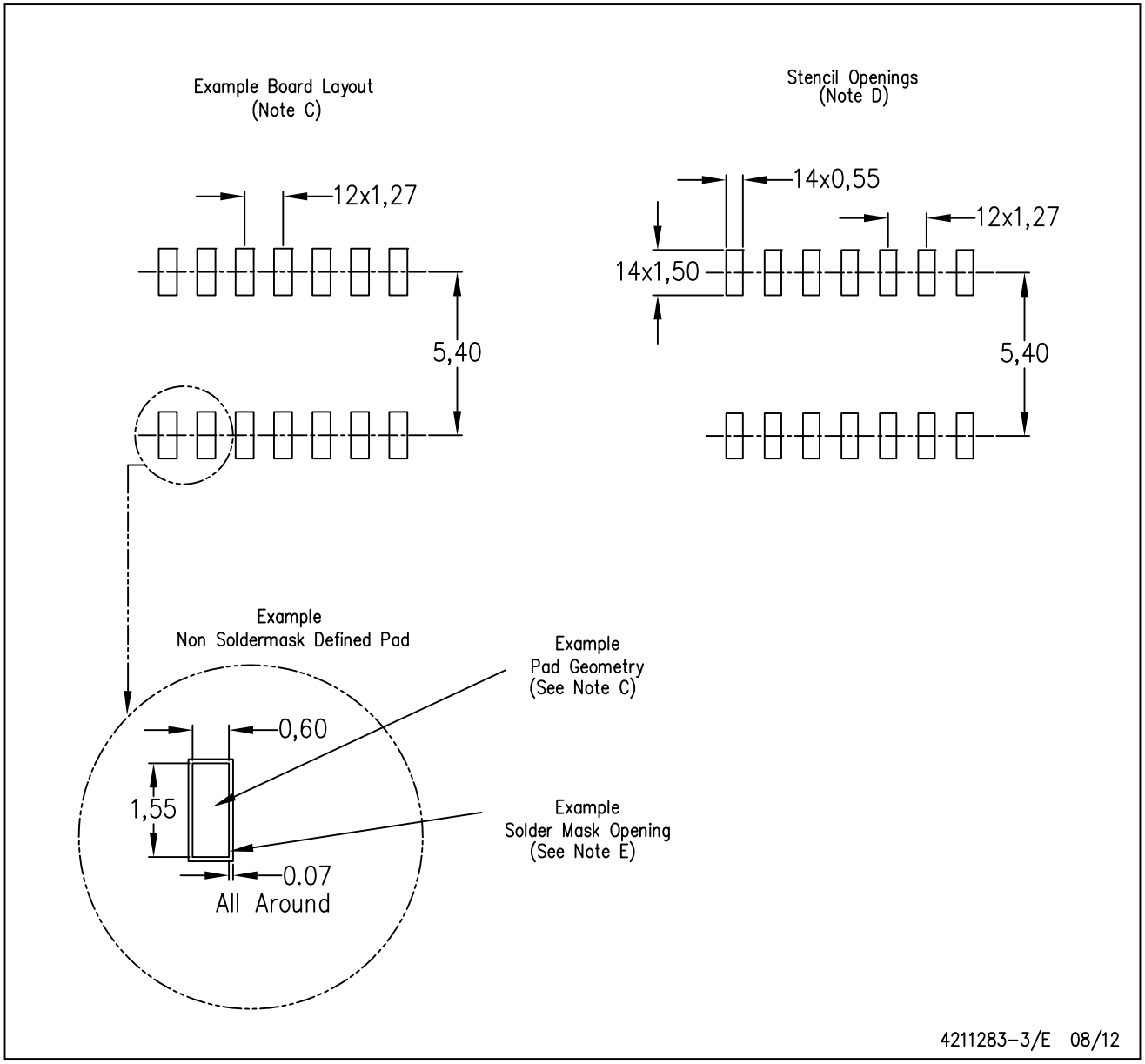
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2674I-14DR	SOIC	D	14	2500	367.0	367.0	38.0
OPA2674IDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

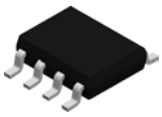


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

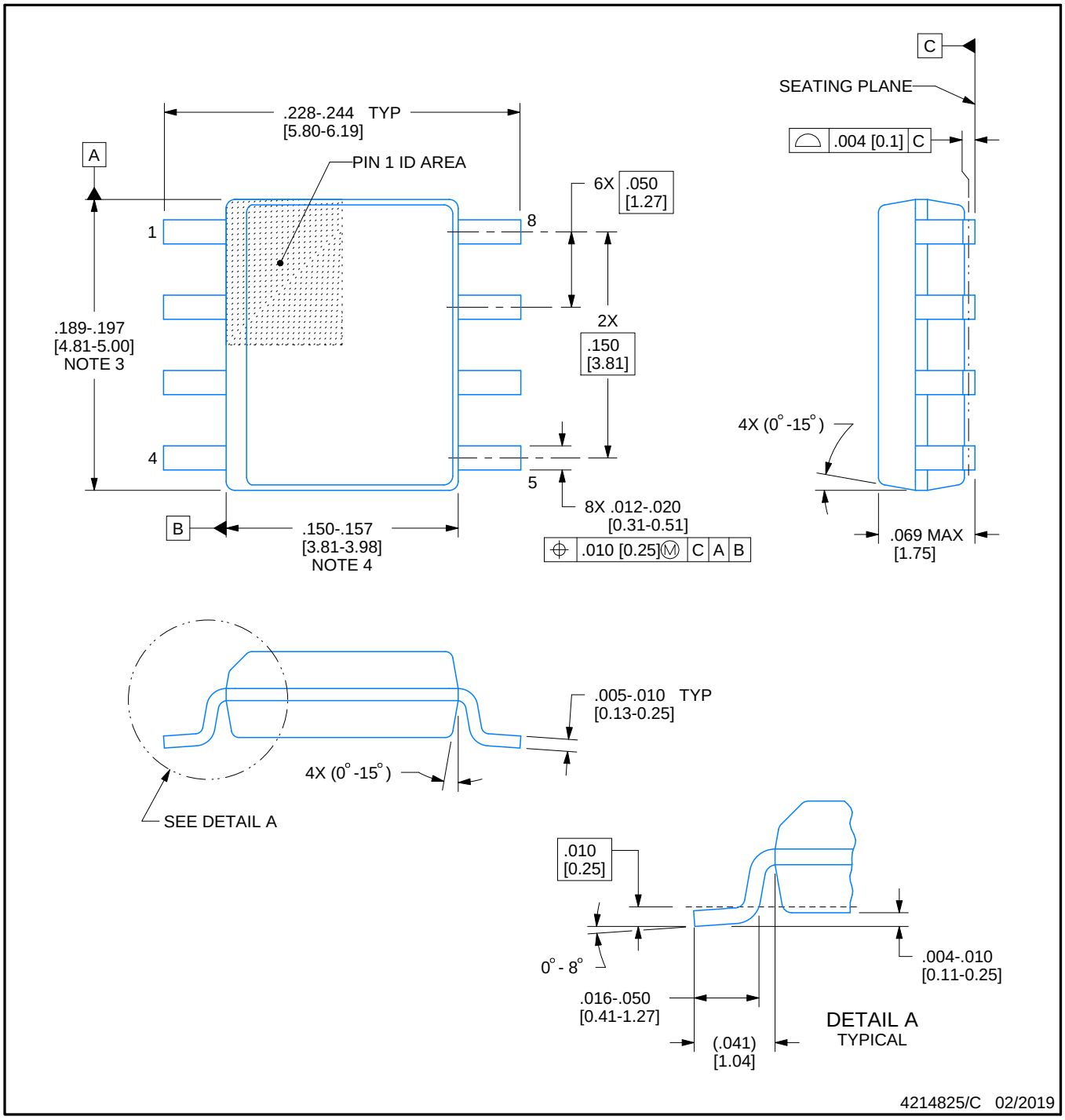


PACKAGE OUTLINE

D0008A

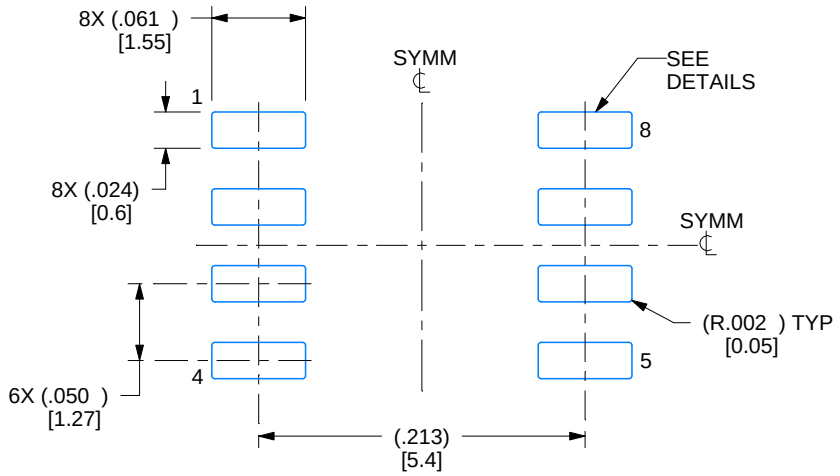
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

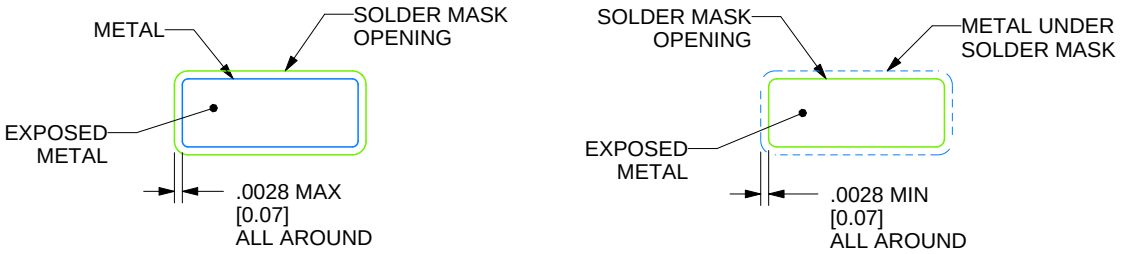


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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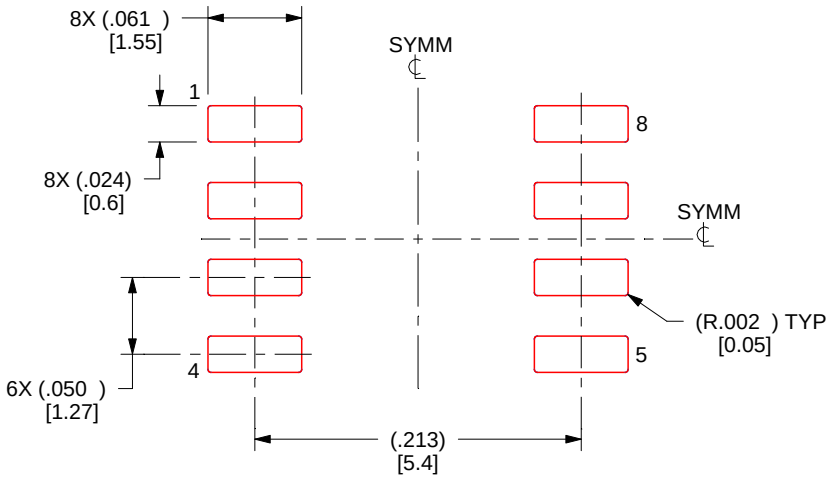
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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