THE DATASHEET OF

OPA2830IDGKRG4

www.win-source.net 0086-755-83957316

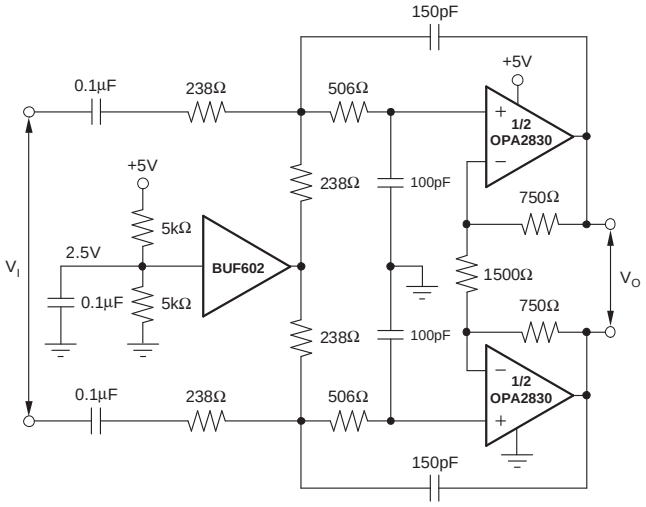
Dual, Low-Power, Single-Supply, Wideband OPERATIONAL AMPLIFIER

FEATURES

- **HIGH BANDWIDTH: 230MHz (G = +1), 100MHz (G = +2)**
- **LOW SUPPLY CURRENT: 7.8mA (V_S = +5V)**
- **FLEXIBLE SUPPLY RANGE: ±1.5V to ±5.5V Dual Supply +3V to +11V Single Supply**
- **INPUT RANGE INCLUDES GROUND ON SINGLE SUPPLY**
- **4.82V_{PP} OUTPUT SWING ON +5V SUPPLY**
- **HIGH SLEW RATE: 500V/µs**
- **LOW INPUT VOLTAGE NOISE: 9.2nV/√Hz**
- **AVAILABLE IN AN MSOP-8 PACKAGE**

APPLICATIONS

- **SINGLE-SUPPLY ADC INPUT BUFFERS**
- **SINGLE-SUPPLY VIDEO LINE DRIVERS**
- **CCD IMAGING CHANNELS**
- **LOW-POWER ULTRASOUND**
- **PLL INTEGRATORS**
- **PORTABLE CONSUMER ELECTRONICS**
- **LOW-POWER ACTIVE FILTERS**



Single-Supply, Differential, 2nd-Order, 5MHz, Low-Pass Sallen-Key Filter

DESCRIPTION

The OPA2830 is a dual, low-power, single-supply, wideband, voltage-feedback amplifier designed to operate on a single +3V or +5V supply. Operation on ±5V or +10V supplies is also supported. The input range extends below ground and to within 1.8V of the positive supply. Using complementary common-emitter outputs provides an output swing to within 25mV of ground and +V_S while driving 150Ω. High output drive current (75mA) and low differential gain and phase errors also make it ideal for single-supply consumer video products.

Low distortion operation is ensured by the high gain bandwidth product (100MHz) and slew rate (500V/µs), making the OPA2830 an ideal input buffer stage to 3V and 5V CMOS Analog-to-Digital Converters (ADCs). Unlike earlier low-power, single-supply amplifiers, distortion performance improves as the signal swing is decreased. A low 9.2nV/√Hz input voltage noise supports wide dynamic range operation.

The OPA2830 is available in an industry-standard SO-8 package. The OPA2830 is also available in a small MSOP-8 package. For fixed-gain and line driver applications, consider the OPA2832.

RELATED PRODUCTS

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-Rail	OPA830	—	—	OPA4830
Rail-to-Rail Fixed-Gain	OPA832	OPA2832	OPA3832	—
General-Purpose (1800V/s slew rate)	OPA690	OPA2690	OPA3690	—
Low-Noise, High DC Precision	OPA820	OPA2822	—	OPA4820

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2830	SO-8 Surface-Mount	D	–40°C to +85°C	OPA2830	OPA2830ID	Rails, 100
					OPA2830IDR	Tape and Reel, 2500
OPA2830	MSOP-8	DGK	–40°C to +85°C	A59	OPA2830IDGKT	Tape and Reel, 250
					OPA2830IDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

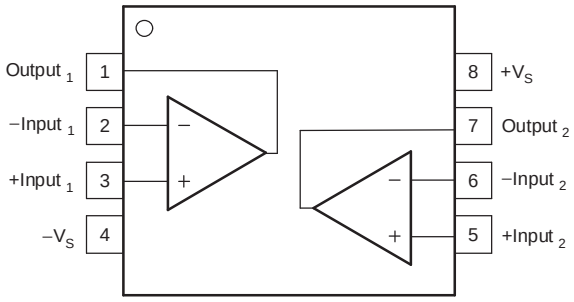
ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$11V_{DC}$
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±2.5V
Input Voltage Range	–0.5V to $+V_S$ + 0.3V
Storage Temperature Range: D, DGK	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

PIN CONFIGURATIONS

Top View **SO, MSOP**



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ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25C**.

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 70).

PARAMETER	CONDITIONS	OPA2830ID, IDGK				UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)			
AC PERFORMANCE (see Figure 70)								
Small-Signal Bandwidth	G = +1, V_O ≤ 0.2V_{PP}	290				MHz	typ	C
	G = +2, V_O ≤ 0.2V_{PP}	105	66	64	61	MHz	min	B
	G = +5, V_O ≤ 0.2V_{PP}	22	16	14	13	MHz	min	B
	G = +10, V_O ≤ 0.2V_{PP}	10	8	7	6	MHz	min	B
Gain Bandwidth Product	G ≥ +10	100	80	77	75	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.2V_{PP}	4				dB	typ	C
Slew Rate	G = +2, 2V Step	560	275	265	255	V/µs	min	B
Rise Time	0.5V Step	3.4	5.9	5.95	6.0	ns	max	B
Fall Time	0.5V Step	3.6	6.0	6.05	6.1	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	43	64	66	67	ns	max	B
Harmonic Distortion	V_O = 2V_{PP}, f = 5MHz							
2nd-Harmonic	R_L = 150Ω	–62	–55	–53	–52	dBc	min	B
	R_L ≥ 500Ω	–66	–58	–57	–56	dBc	min	B
3rd-Harmonic	R_L = 150Ω	–59	–50	–49	–48	dBc	min	B
	R_L ≥ 500Ω	–77	–65	–62	–55	dBc	min	B
Input Voltage Noise	f > 1MHz	9.5	10.6	11.1	11.6	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.7	4.8	5.3	5.8	pA/√Hz	max	B
NTSC Differential Gain		0.07				%	typ	C
NTSC Differential Phase		0.17				°	typ	C
DC PERFORMANCE(4)	R_L = 150Ω							
Open-Loop Voltage Gain		74	**66**	65	64	dB	min	A
Input Offset Voltage		±1.5	**±7.5**	±8.7	±9.3	mV	max	A
Average Offset Voltage Drift		—		±27	±27	µV/°C	max	B
Input Bias Current	V_{CM} = 2.0V	+5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift				±44	±46	nA/°C	max	B
Input Offset Current	V_{CM} = 2.0V	±0.2	**±1.1**	±1.3	±1.5	µA	max	A
Input Offset Current Drift		—		±5	±6	nA/°C	max	B
INPUT								
Negative Input Voltage		–5.5	**–5.4**	–5.3	–5.2	V	max	A
Positive Input Voltage		3.2	**3.1**	3.0	2.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**76**	74	71	dB	min	A
Input Impedance								
Differential Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	G = +2, R_L = 1kΩ to GND	±4.88	**±4.86**	±4.85	±4.84	V	min	A
	G = +2, R_L = 150Ω to GND	±4.64	**±4.60**	±4.58	±4.56	V	min	A
Current Output, Sinking and Sourcing		±82	**±63**	±58	±53	mA	min	A
Short-Circuit Current	Output Shorted to Ground	150				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.06				Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +18°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of pin.

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ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25C**.

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 70).

PARAMETER	CONDITIONS	OPA2830ID, IDGK				UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)			
POWER SUPPLY								
Minimum Operating Voltage		±1.4				V	typ	C
Maximum Operating Voltage			**±5.5**	±5.5	±5.5	V	max	A
Maximum Quiescent Current	V_S = ±5V, Both Channels	8.5	**9.5**	10.7	11.9	mA	max	A
Minimum Quiescent Current	V_S = ±5V, Both Channels	8.5	**8.0**	7.2	6.6	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDGK		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
DGK MSOP-8		150				°C/W	typ	C

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ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to V_S/2, unless otherwise noted (see Figure 72).

PARAMETER	CONDITIONS	OPA2830ID, IDGK				UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)			
AC PERFORMANCE (see Figure 72)								
Small-Signal Bandwidth	G = +1, V_O ≤ 0.2V_{PP}	230				MHz	typ	C
	G = +2, V_O ≤ 0.2V_{PP}	100	70	68	66	MHz	min	B
	G = +5, V_O ≤ 0.2V_{PP}	21	15	14	13	MHz	min	B
	G = +10, V_O ≤ 0.2V_{PP}	10	7	6	5	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	100	75	65	59	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.2V_{PP}	4				dB	typ	C
Slew Rate	G = +2, 2V Step	500	270	260	250	V/µs	min	B
Rise Time	0.5V Step	3.4	5.8	5.9	6.0	ns	max	B
Fall Time	0.5V Step	3.4	5.8	5.9	6.0	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	44	65	67	68	ns	max	B
Harmonic Distortion	V_O = 2V_{PP}, f = 5MHz							
2nd-Harmonic	R_L = 150Ω	–58	–52	–51	–50	dBc	min	B
	R_L ≥ 500Ω	–62	–56	–55	–54	dBc	min	B
3rd-Harmonic	R_L = 150Ω	–58	–50	–49	–48	dBc	min	B
	R_L ≥ 500Ω	–84	–65	–62	–60	dBc	min	B
Input Voltage Noise	f > 1MHz	9.2	10.3	10.8	11.3	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.5	4.6	5.1	5.6	pA/√Hz	max	B
NTSC Differential Gain		0.075				%	typ	C
NTSC Differential Phase		0.087				°	typ	C
DC PERFORMANCE(4)	R_L = 150Ω							
Open-Loop Voltage Gain		72	**66**	65	64	dB	min	A
Input Offset Voltage		±0.5	**±5.5**	±6.5	±7.0	mV	max	A
Average Offset Voltage Drift		—		±22	±22	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	+5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift				±44	±46	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±0.2	**±0.9**	±1.1	±1.3	µA	max	A
Input Offset Current Drift		—		±5	±6	nA/°C	max	B
INPUT								
Least Positive Input Voltage		–0.5	**–0.4**	–0.3	–0.2	V	max	A
Most Positive Input Voltage		3.2	**3.1**	3.0	2.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**76**	74	71	dB	min	A
Input Impedance, Differential Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C
OUTPUT								
Least Positive Output Voltage	G = +5, R_L = 1kΩ to 2.5V	0.09	**0.11**	0.12	0.13	V	max	A
	G = +5, R_L = 150Ω to 2.5V	0.21	**0.24**	0.25	0.26	V	max	A
Most Positive Output Voltage	G = +5, R_L = 1kΩ to 2.5V	4.91	**4.89**	4.88	4.87	V	min	A
	G = +5, R_L = 150Ω to 2.5V	4.78	**4.75**	4.73	4.72	V	min	A
Current Output, Sinking and Sourcing		±75	**±58**	±53	±50	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	140				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.06				Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +6°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of pin.

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ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to V_S/2, unless otherwise noted (see Figure 72).

PARAMETER	CONDITIONS	OPA2830ID, IDGK				UNITS	MIN/ MAX	TEST LEVEL[3]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to +70°C[2]	–40°C to +85°C[2]			
POWER SUPPLY								
Minimum Operating Voltage		+2.8				V	min	B
Maximum Operating Voltage			**+11**	+11	+11	V	max	A
Maximum Quiescent Current	V_S = +5V, Both Channels	7.8	**8.3**	9.7	11.1	mA	max	A
Minimum Quiescent Current	V_S = +5V, Both Channels	7.8	**7.4**	6.8	6.2	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDGK		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
DGK MSOP-8		150				°C/W	typ	C

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ELECTRICAL CHARACTERISTICS: V_S = +3V

Boldface limits are tested at **+25C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 71).

PARAMETER	CONDITIONS	OPA2830ID, IDGK			UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE				
		+25°C	+25°C(1)	0°C to +70°C(2)			
AC PERFORMANCE (see Figure 71)							
Small-Signal Bandwidth	G = +2, V_O ≤ 0.2V_{PP}	90	70	66	MHz	min	B
	G = +5, V_O ≤ 0.2V_{PP}	20	15	14	MHz	min	B
	G = +10, V_O ≤ 0.2V_{PP}	9	7.5	6.5	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	90	75	65	MHz	min	B
Slew Rate	1V Step	220	135	105	V/µs	min	B
Rise Time	0.5V Step	3.4	5.6	5.7	ns	max	B
Fall Time	0.5V Step	3.4	5.6	5.7	ns	max	B
Settling Time to 0.1%	1V Step	46	73	88	ns	max	B
Harmonic Distortion	V_O = 1V_{PP}, f = 5MHz						
2nd-Harmonic	R_L = 150Ω	–60	–56	–54	dBc	min	B
	R_L ≥ 500Ω	–64	–59	–57	dBc	min	B
3rd-Harmonic	R_L = 150Ω	–68	–59	–58	dBc	min	B
	R_L ≥ 500Ω	–72	–65	–64	dBc	min	B
Input Voltage Noise	f > 1MHz	9.2	10.3	10.8	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.5	4.6	5.1	pA/√Hz	max	B
DC PERFORMANCE(4)							
Open-Loop Voltage Gain		72	**66**	65	dB	min	A
Input Offset Voltage		±1.5	**±7.5**	±8.7	mV	max	A
Average Offset Voltage Drift		—		±27	µV/°C	max	B
Input Bias Current	V_{CM} = 1.0V	+5	**+10**	+12	µA	max	A
Input Bias Current Drift				±44	nA/°C	max	B
Input Offset Current	V_{CM} = 1.0V	±0.2	**±1.1**	±1.3	µA	max	A
Input Offset Current Drift		—		±5	nA/°C	max	B
INPUT							
Least Positive Input Voltage		–0.45	**–0.4**	–0.27	V	max	A
Most Positive Input Voltage		1.2	**1.1**	1.0	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**74**	72	dB	min	A
Input Impedance							
Differential Mode		10 || 2.1			kΩ || pF	typ	C
Common-Mode		400 || 1.2			kΩ || pF	typ	C
OUTPUT							
Least Positive Output Voltage	G = +5, R_L = 1kΩ to 1.5V	0.08	**0.11**	0.125	V	max	A
	G = +5, R_L = 150Ω to 1.5V	0.17	**0.39**	0.40	V	max	A
Most Positive Output Voltage	G = +5, R_L = 1kΩ to 1.5V	2.91	**2.88**	2.85	V	min	A
	G = +5, R_L = 150Ω to 1.5V	2.82	**2.74**	2.70	V	min	A
Current Output, Sinking and Sourcing		±30	**±20**	±18	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	45			mA	typ	C
Closed-Loop Output Impedance	See Figure 71, f < 100kHz	0.06			Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +20°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

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ELECTRICAL CHARACTERISTICS: V_S = +3V (continued)

Boldface limits are tested at **+25C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 71).

PARAMETER	CONDITIONS	OPA2830ID, IDGK			UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE				
		+25°C	+25°C(1)	0°C to +70°C(2)			
POWER SUPPLY							
Minimum Operating Voltage		+2.8			V	min	B
Maximum Operating Voltage			**+11**	+11	V	max	A
Maximum Quiescent Current	V_S = +3V, Both Channels	7.4	**8.1**	8.7	mA	max	A
Minimum Quiescent Current	V_S = +3V, Both Channels	7.4	**6.6**	6.2	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	64	**60**	58	dB	min	A
THERMAL CHARACTERISTICS							
Specification: ID, IDGK		–40 to +85			°C	typ	C
Thermal Resistance, θ_{JA}							
D SO-8		125			°C/W	typ	C
DGK MSOP-8		150			°C/W	typ	C

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TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 72).

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

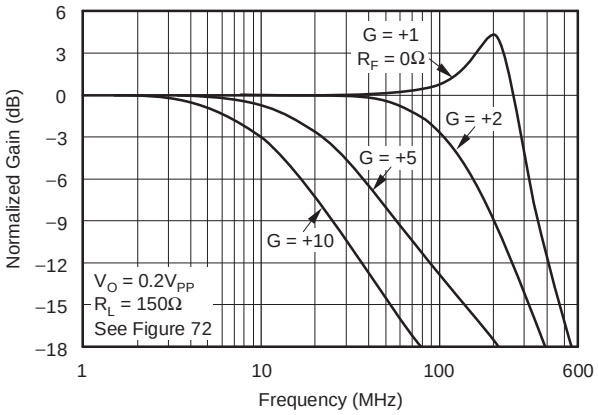

Figure 1.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

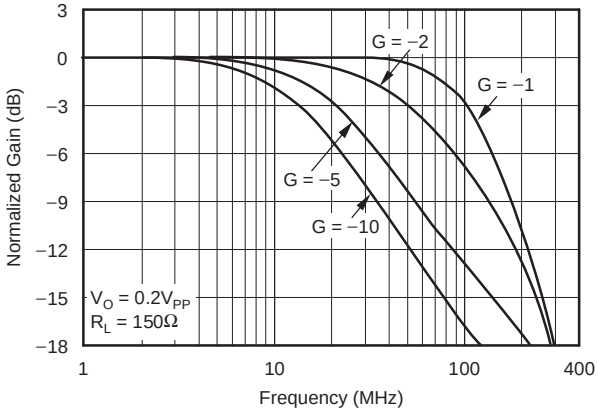

Figure 2.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

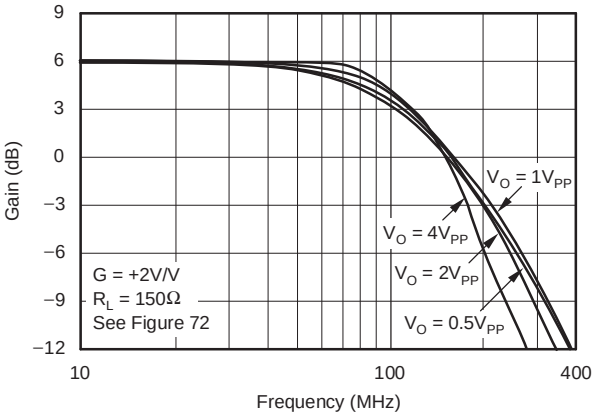

Figure 3.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

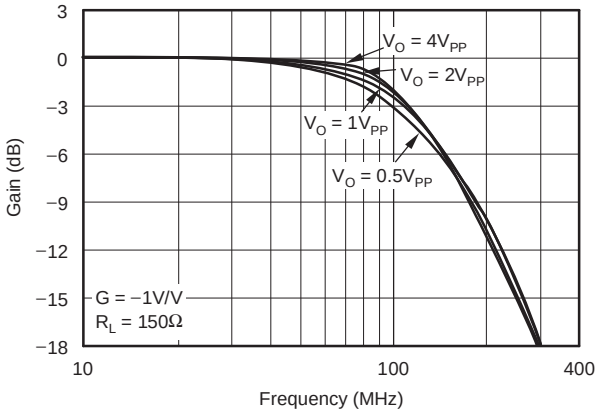

Figure 4.

NONINVERTING PULSE RESPONSE

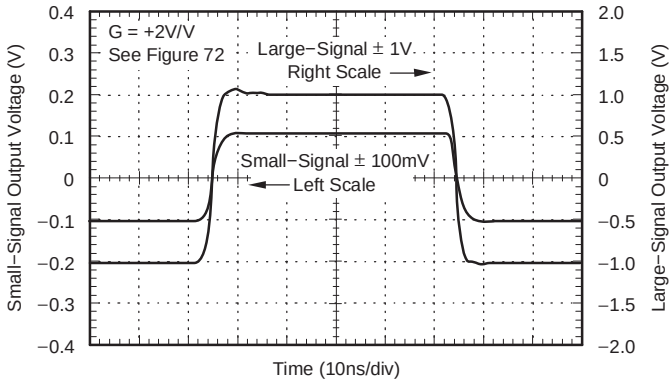

Figure 5.

INVERTING PULSE RESPONSE

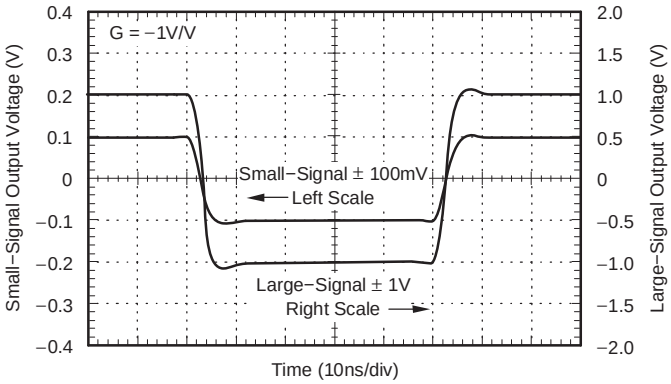

Figure 6.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 72).

HARMONIC DISTORTION vs LOAD RESISTANCE

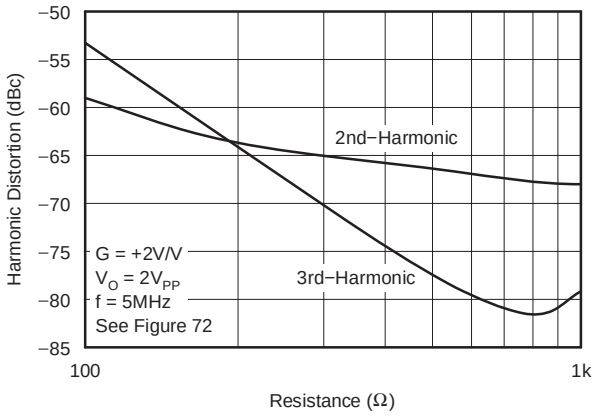

Figure 7.

5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

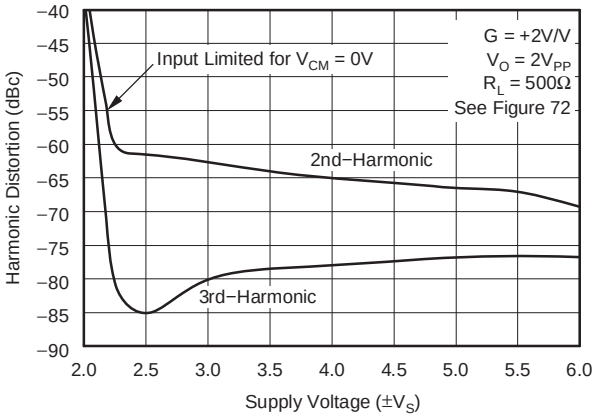

Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

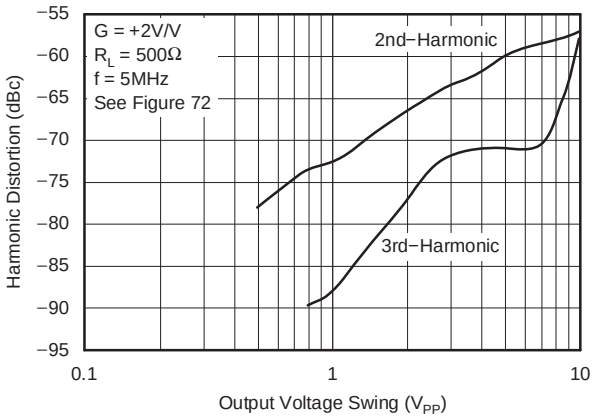

Figure 9.

HARMONIC DISTORTION vs FREQUENCY

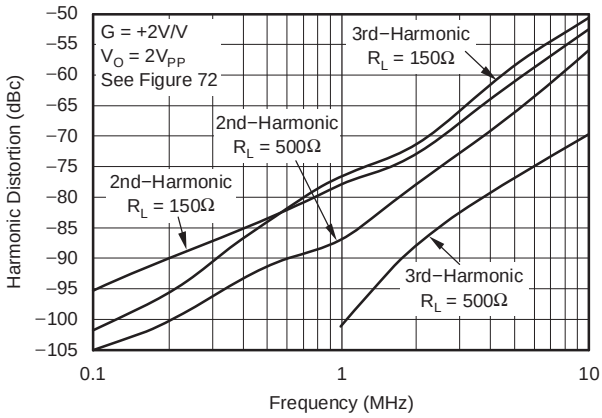

Figure 10.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

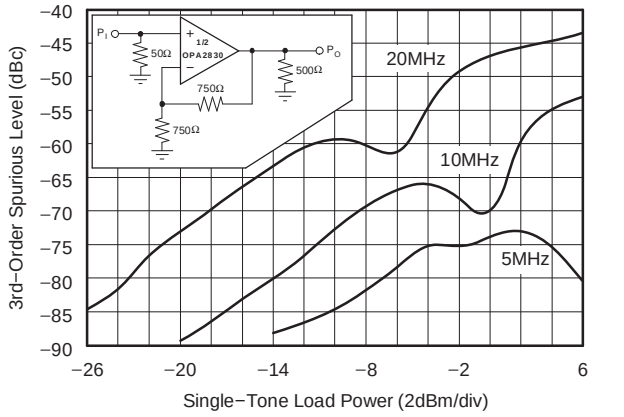

Figure 11.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

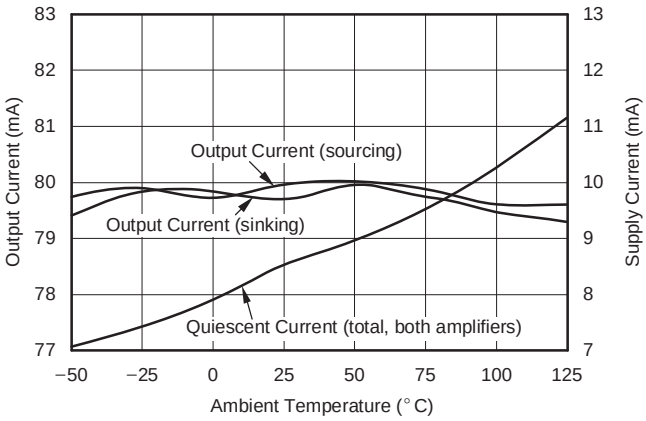

Figure 12.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 72).

FREQUENCY RESPONSE vs CAPACITIVE LOAD

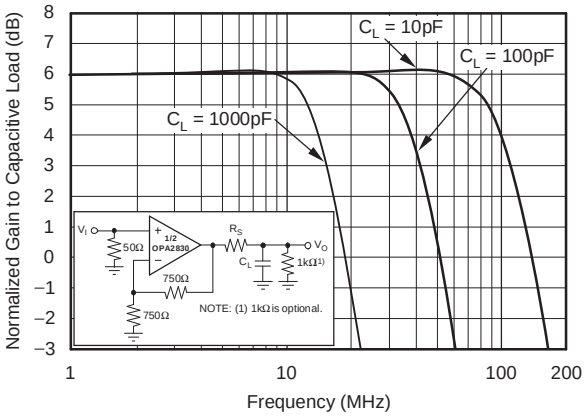

Figure 13.

RECOMMENDED R_S vs CAPACITIVE LOAD

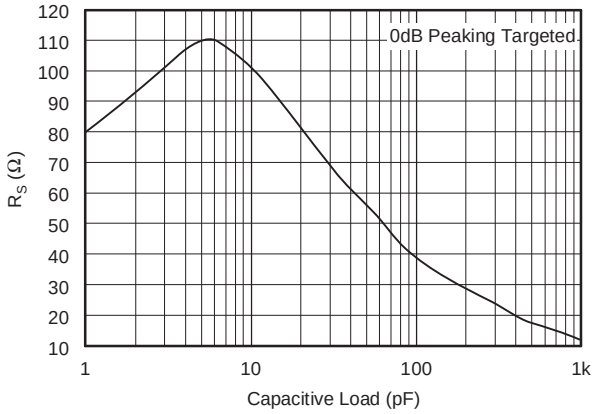

Figure 14.

OUTPUT SWING vs LOAD RESISTANCE

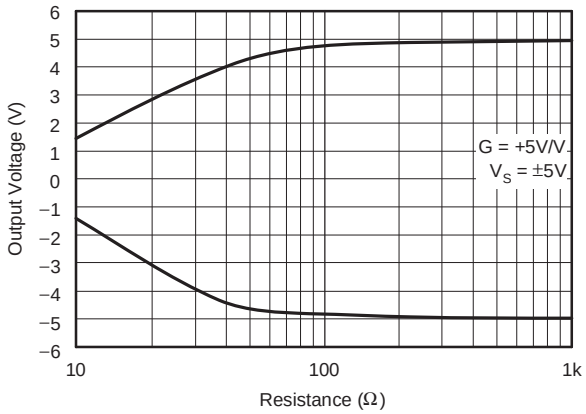

Figure 15.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

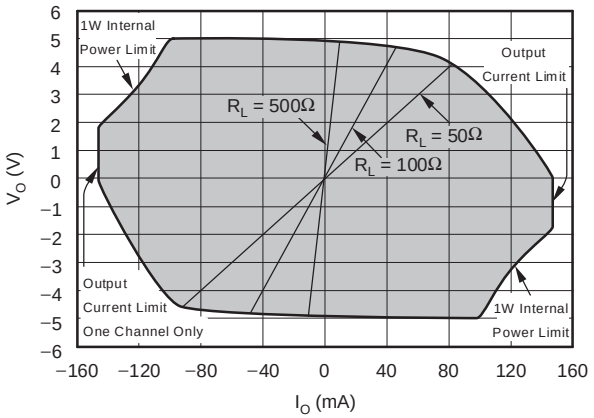

Figure 16.

TYPICAL CHARACTERISTICS: V_S = ±5V, Differential Configuration

At T_A = +25°C, R_F = 604Ω (as shown in Figure 17), and R_L = 500Ω, unless otherwise noted.

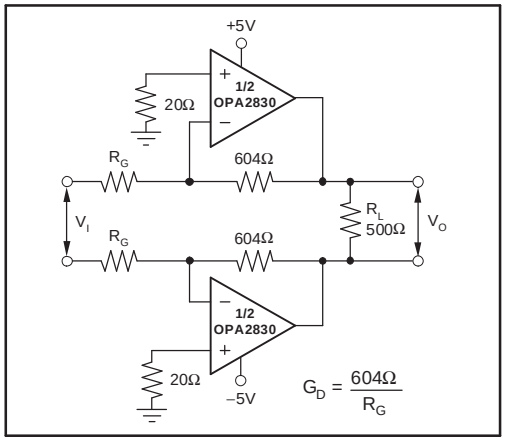

Figure 17.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

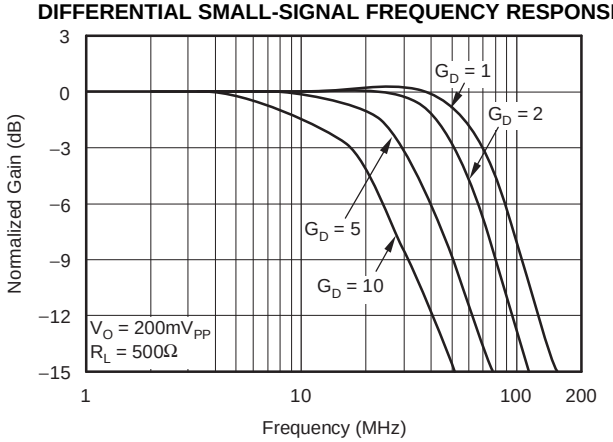

Figure 18.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

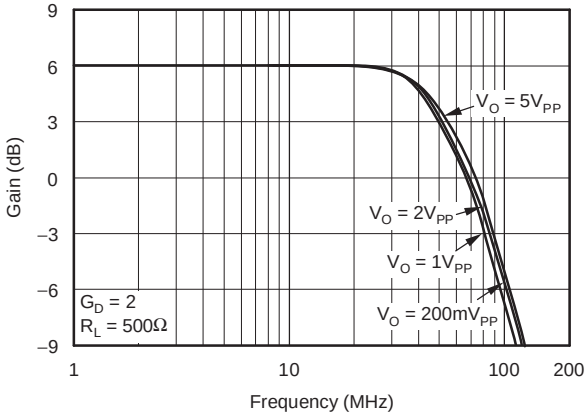

Figure 19.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

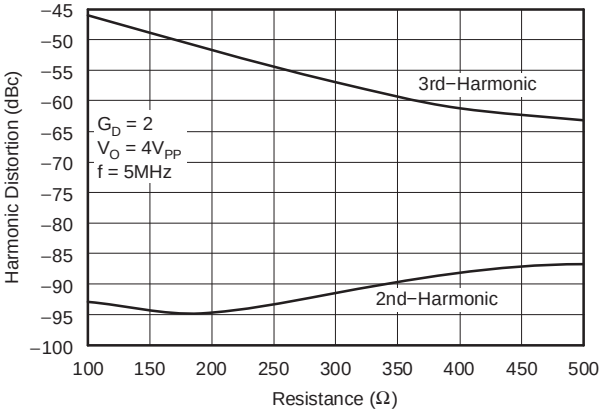

Figure 20.

DIFFERENTIAL DISTORTION vs FREQUENCY

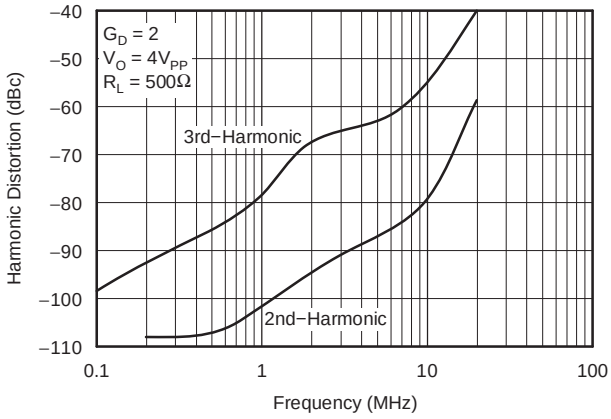

Figure 21.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

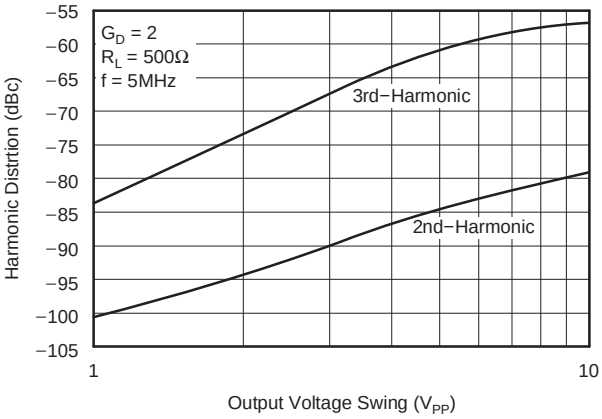

Figure 22.

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TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 70).

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

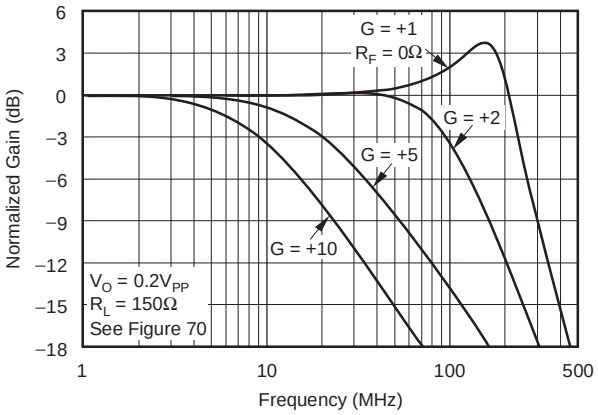

Figure 23.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

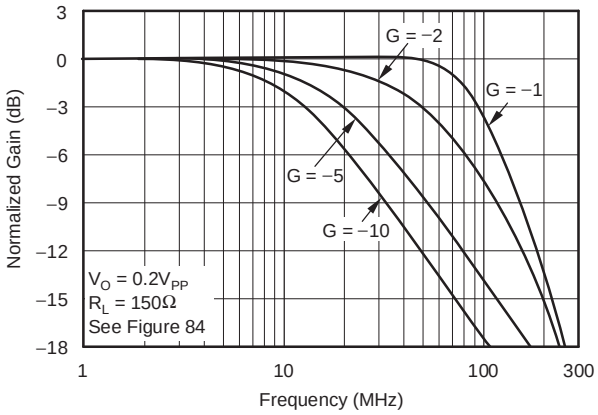

Figure 24.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

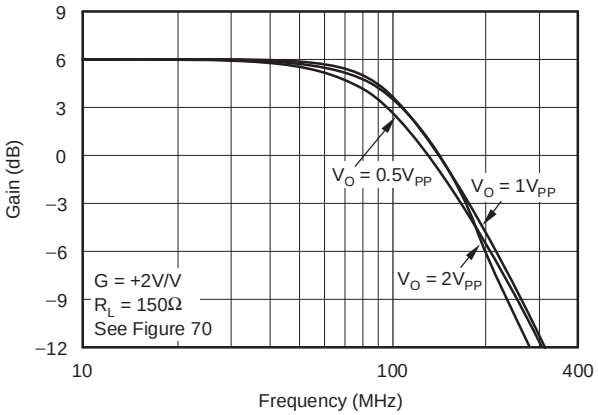

Figure 25.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

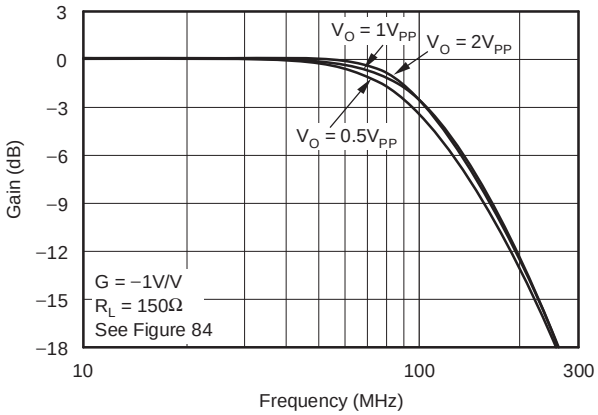

Figure 26.

NONINVERTING PULSE RESPONSE

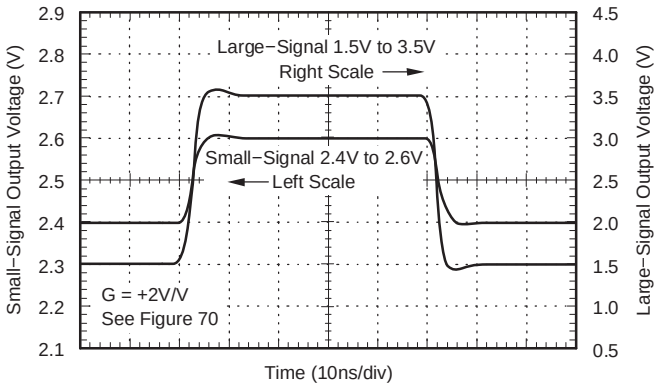

Figure 27.

INVERTING PULSE RESPONSE

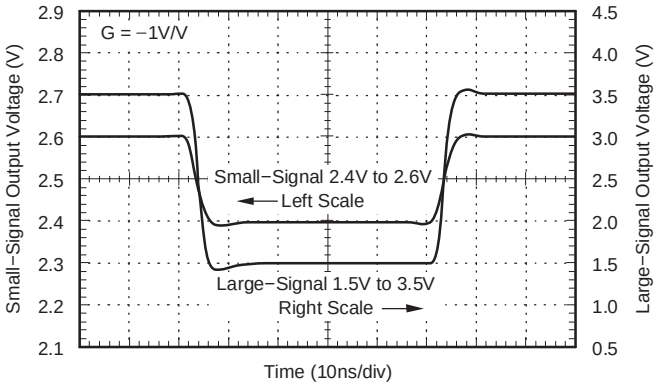

Figure 28.

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TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 70).

HARMONIC DISTORTION vs LOAD RESISTANCE

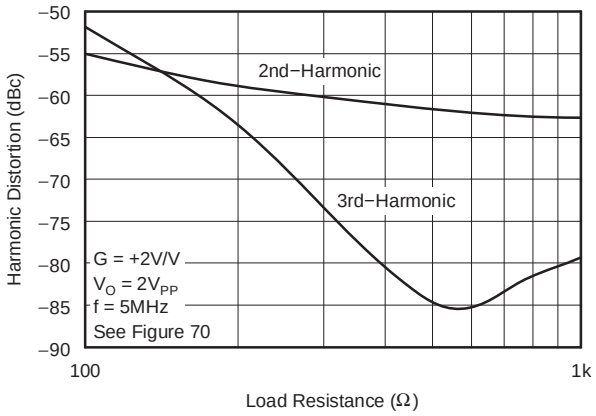

Figure 29.

HARMONIC DISTORTION vs FREQUENCY

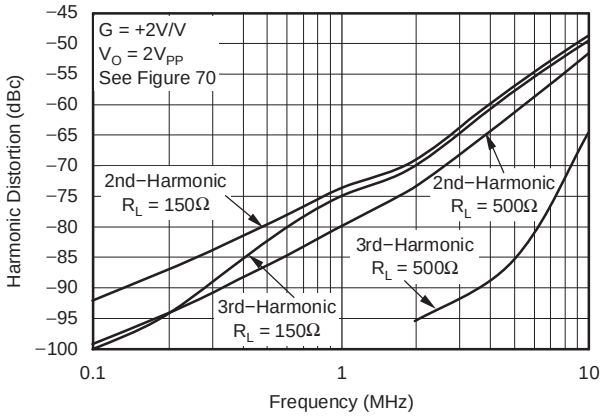

Figure 30.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

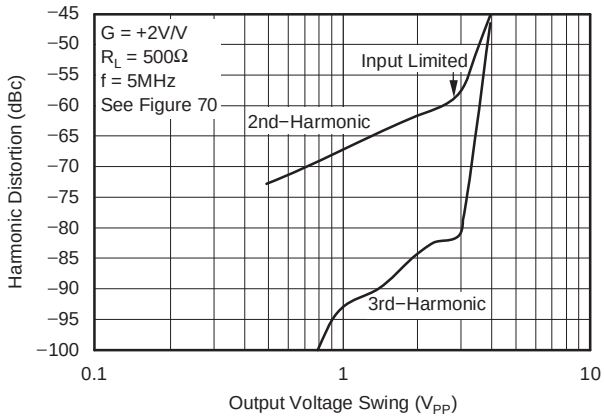

Figure 31.

HARMONIC DISTORTION vs NONINVERTING GAIN

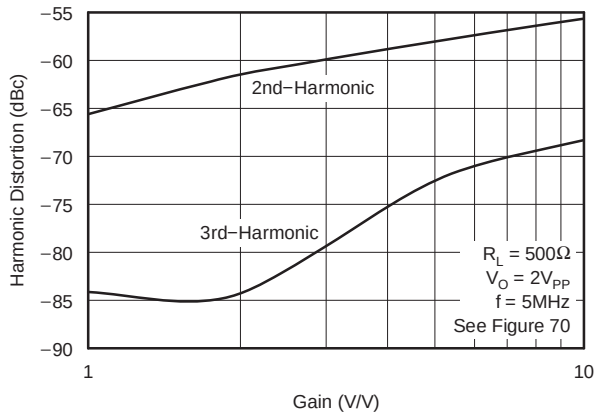

Figure 32.

HARMONIC DISTORTION vs INVERTING GAIN

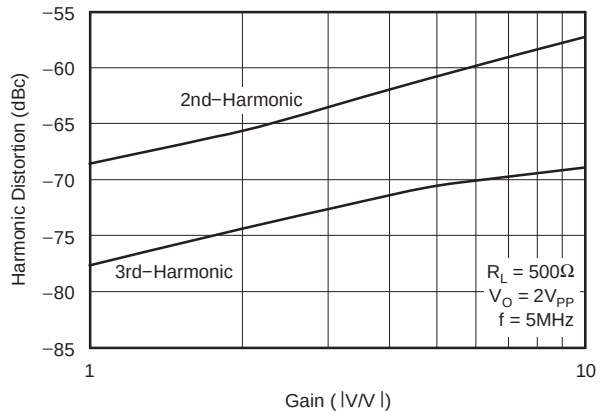

Figure 33.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

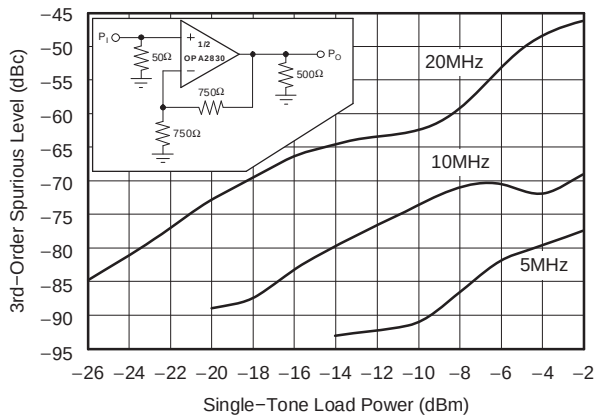

Figure 34.

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TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 70).

INPUT VOLTAGE AND CURRENT NOISE DENSITY

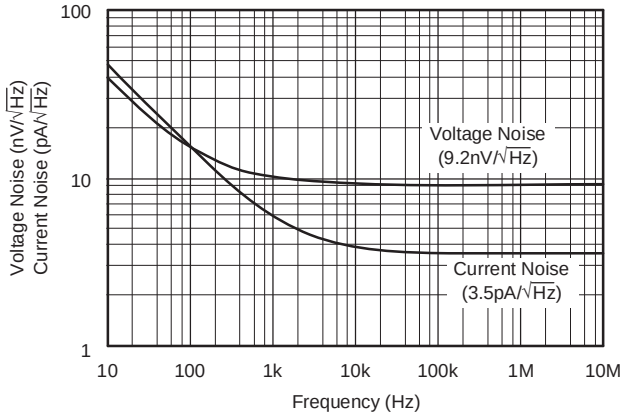

Figure 35.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

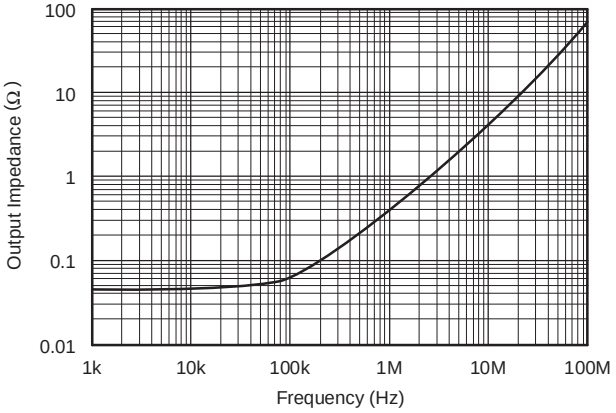

Figure 36.

RECOMMENDED R_S vs CAPACITIVE LOAD

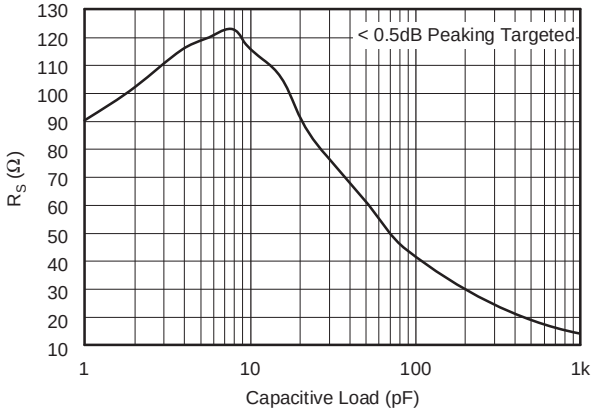

Figure 37.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

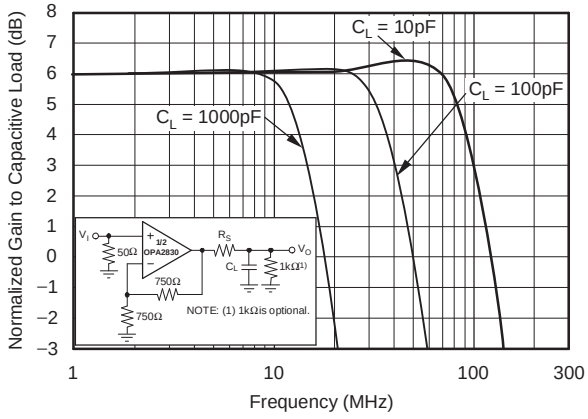

Figure 38.

OPEN-LOOP GAIN AND PHASE

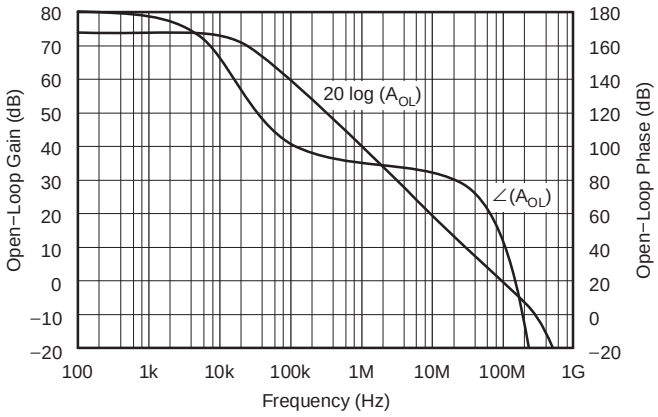

Figure 39.

VOLTAGE RANGES vs TEMPERATURE

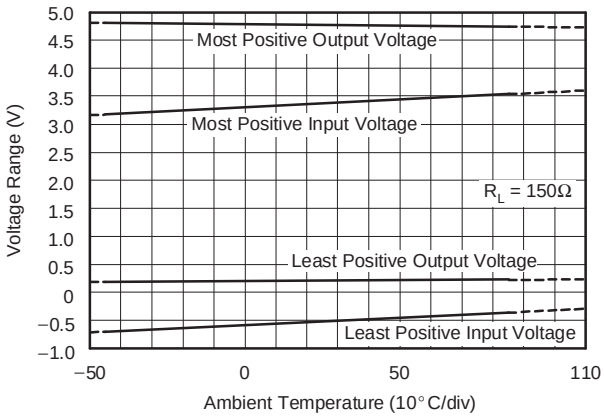

Figure 40.

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TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 70).

TYPICAL DC DRIFT OVER TEMPERATURE

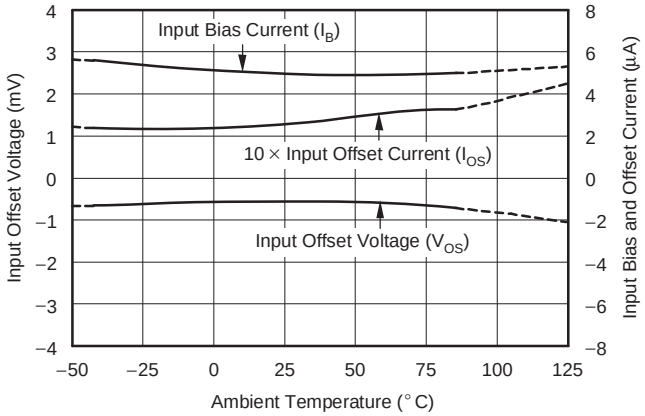

Figure 41.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

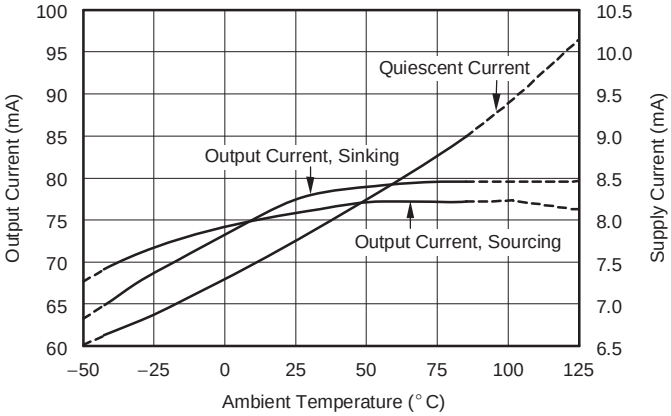

Figure 42.

CMRR AND PSRR vs FREQUENCY

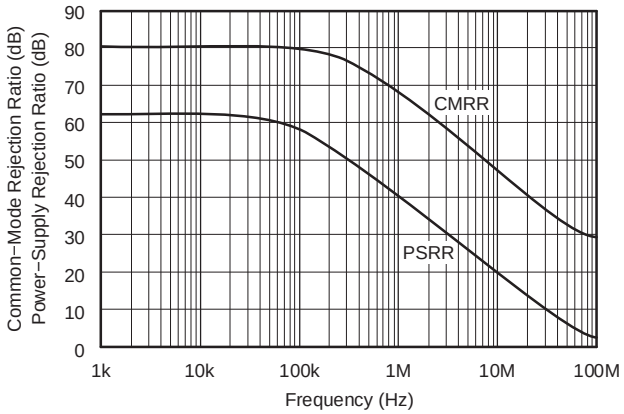

Figure 43.

OUTPUT SWING vs LOAD RESISTANCE

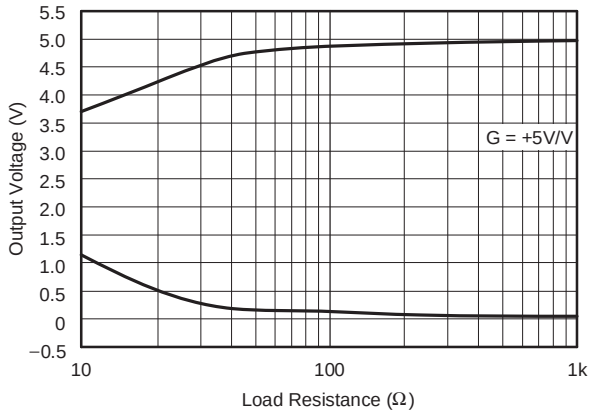

Figure 44.

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TYPICAL CHARACTERISTICS: V_S = +5V, Differential Configuration

At T_A = +25°C, R_F = 604Ω, and R_L = 500Ω differential (as shown in Figure 45), unless otherwise noted.

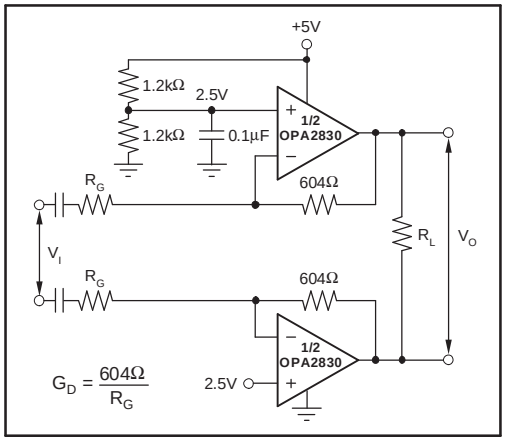

Figure 45.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

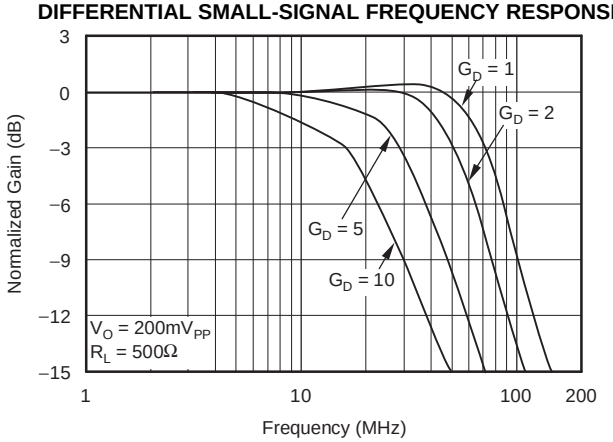

Figure 46.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

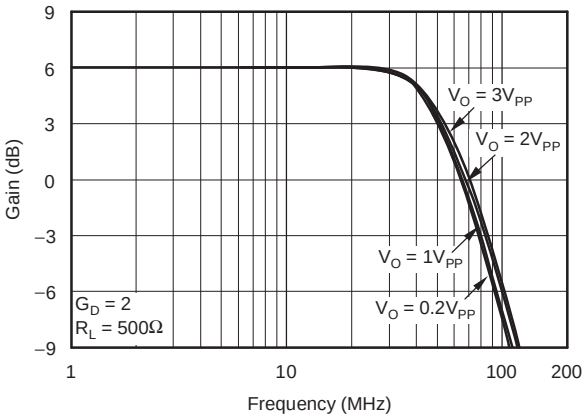

Figure 47.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

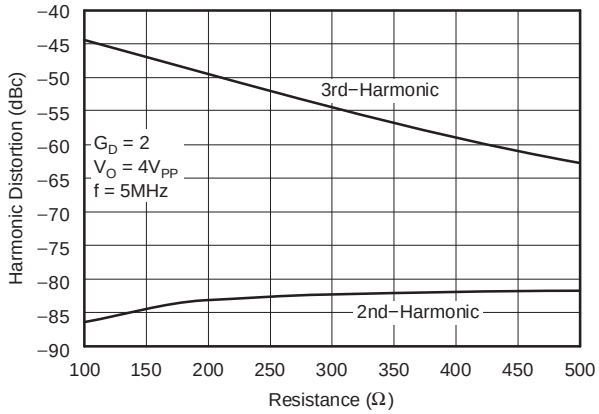

Figure 48.

DIFFERENTIAL DISTORTION vs FREQUENCY

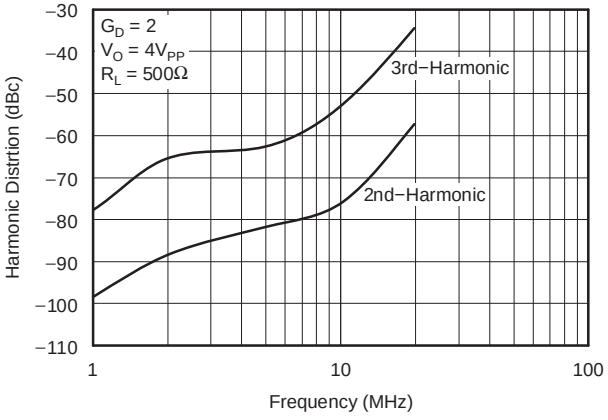

Figure 49.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

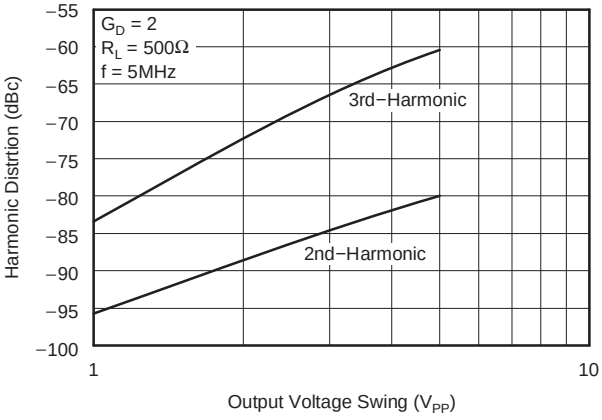

Figure 50.

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TYPICAL CHARACTERISTICS: V_S = +3V

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 71).

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

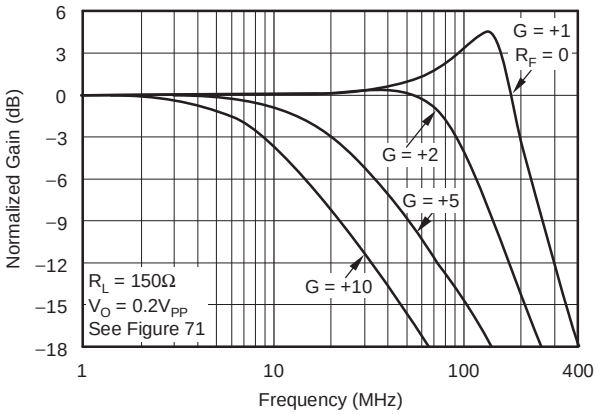

Figure 51.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

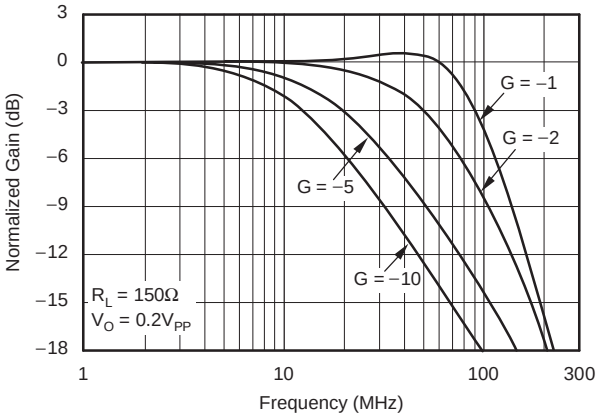

Figure 52.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

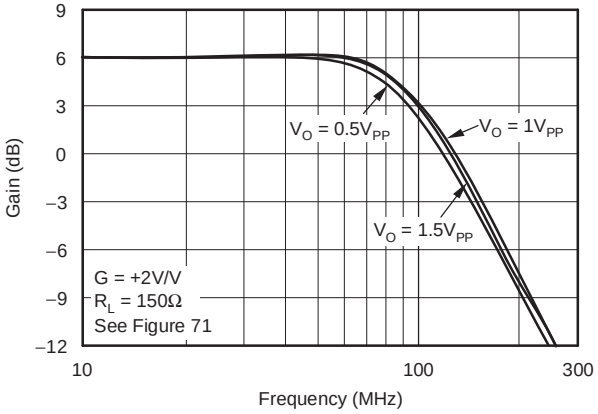

Figure 53.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

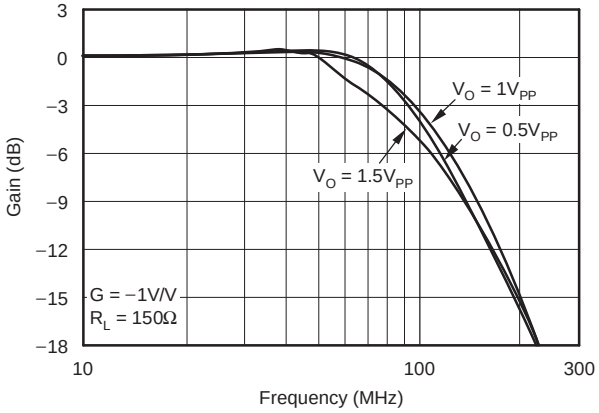

Figure 54.

NONINVERTING PULSE RESPONSE

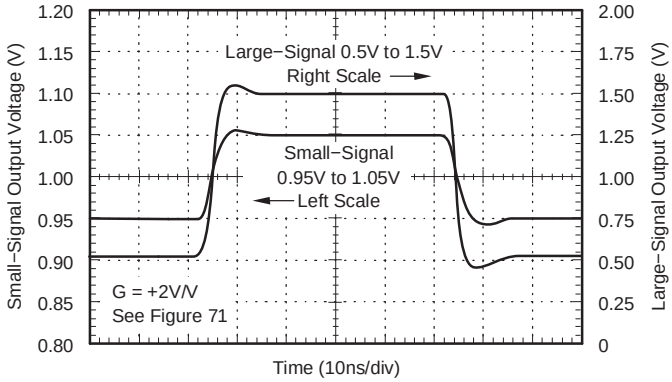

Figure 55.

INVERTING PULSE RESPONSE

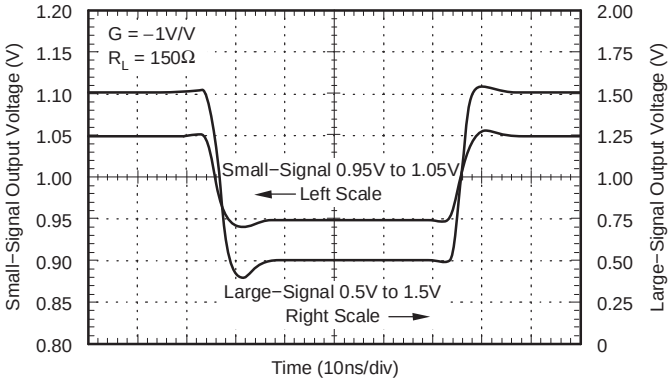

Figure 56.

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TYPICAL CHARACTERISTICS: V_S = +3V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 71).

HARMONIC DISTORTION vs LOAD RESISTANCE

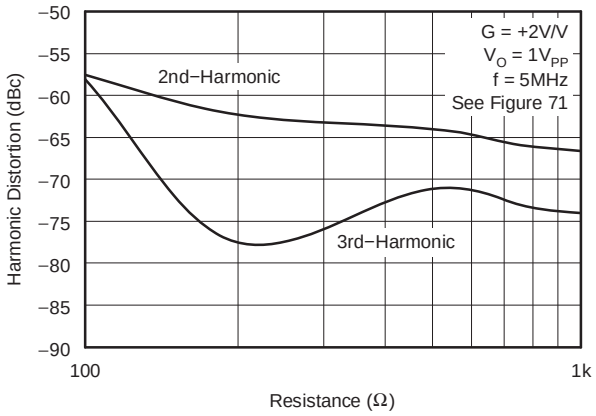

Figure 57.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

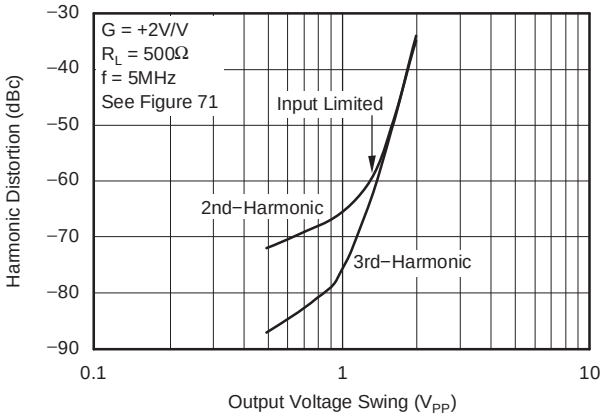

Figure 58.

HARMONIC DISTORTION vs FREQUENCY

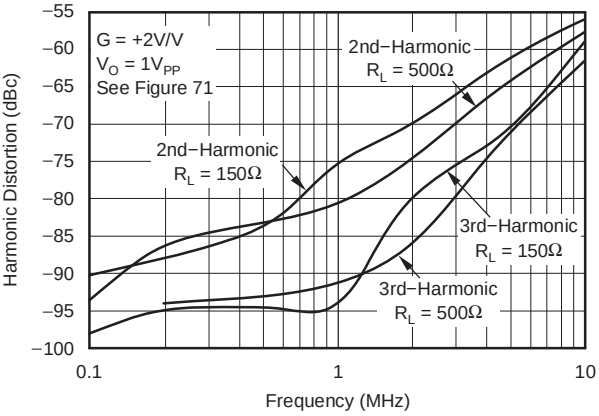

Figure 59.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

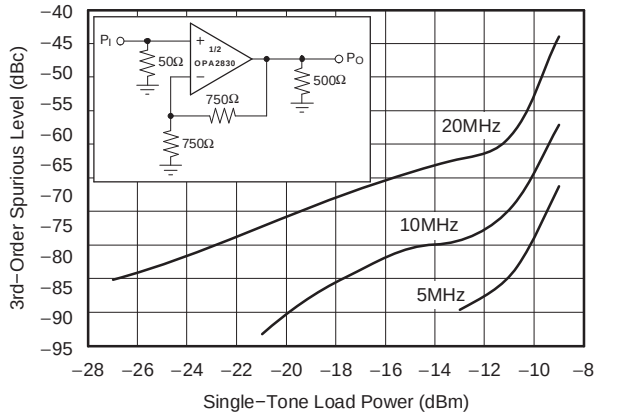

Figure 60.

RECOMMENDED R_S vs CAPACITIVE LOAD

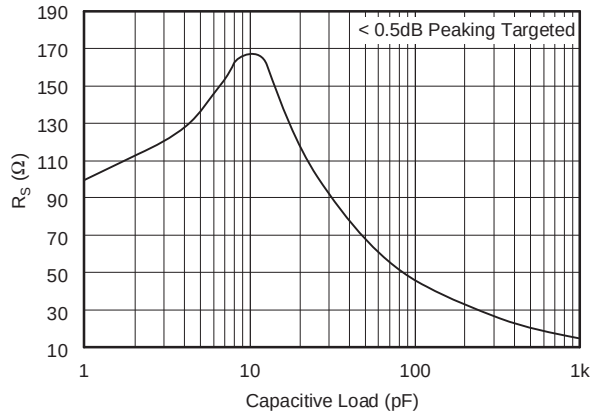

Figure 61.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

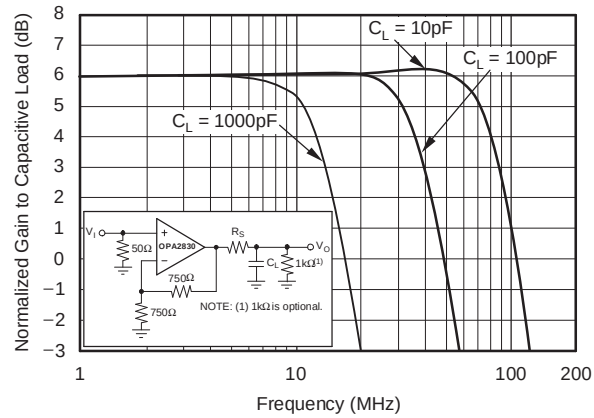

Figure 62.

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TYPICAL CHARACTERISTICS: V_S = +3V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 71).

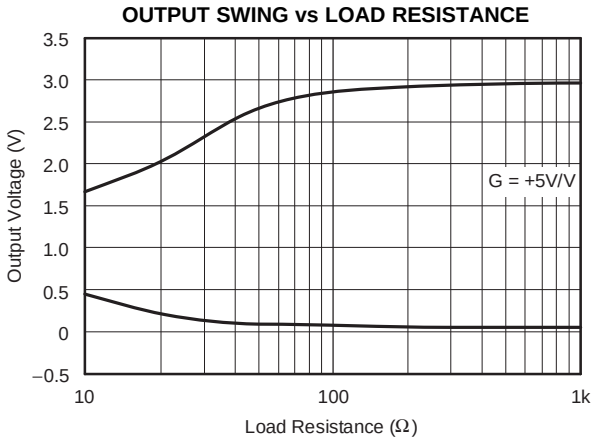

Figure 63.

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TYPICAL CHARACTERISTICS: V_S = +3V, Differential Configuration

At T_A = +25°C, R_F = 604Ω, and R_L = 500Ω differential (as shown in Figure 64), unless otherwise noted.

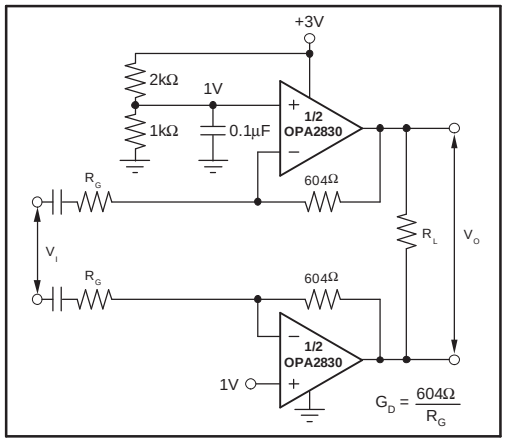

Figure 64.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

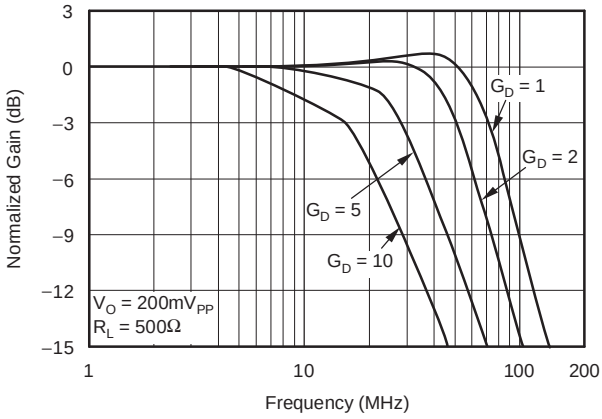

Figure 65.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

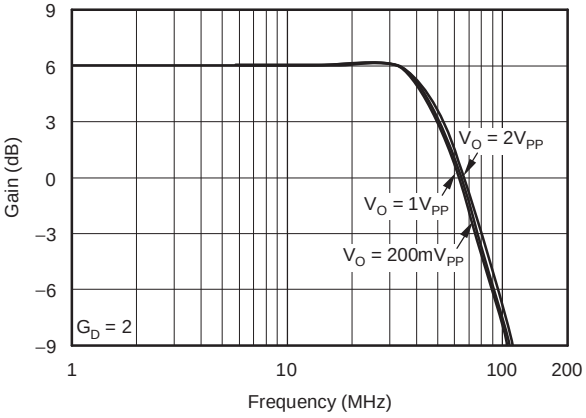

Figure 66.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

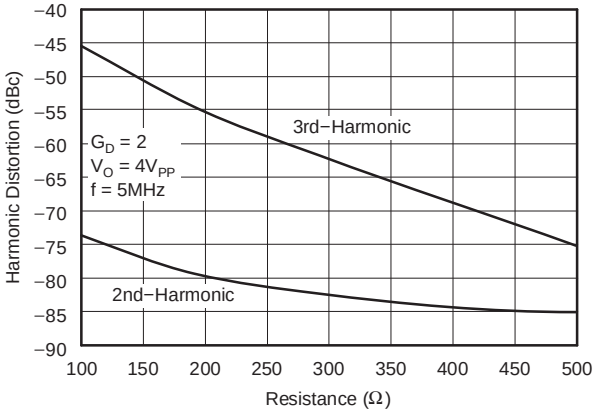

Figure 67.

DIFFERENTIAL DISTORTION vs FREQUENCY

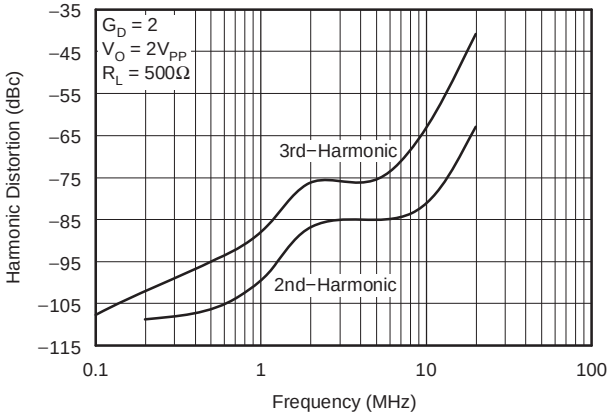

Figure 68.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

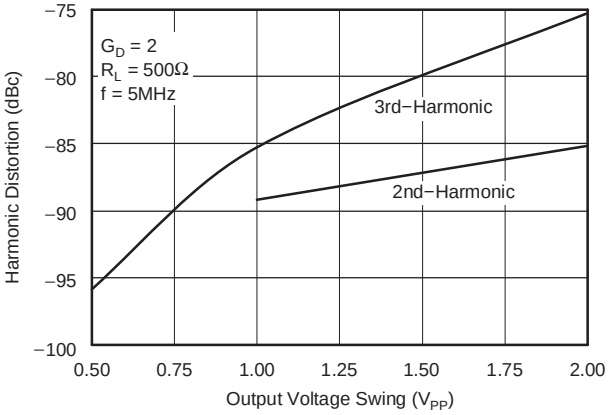

Figure 69.

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APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA2830 is a unity-gain stable, very high-speed voltage-feedback op amp designed for single-supply operation (+3V to +10V). The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of ground and the positive supply. The OPA2830 is compensated to provide stable operation with a wide range of resistive loads.

Figure 70 shows the AC-coupled, gain of +2 configuration used for the +5V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 70, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.5kΩ resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input (R_F), reducing the DC output offset due to input bias current.

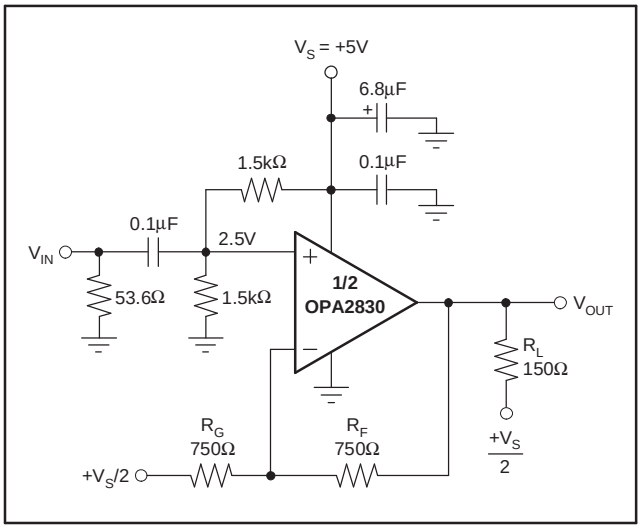

Figure 70. AC-Coupled, G = +2, +5V Single-Supply Specification and Test Circuit

Figure 71 shows the AC-coupled, gain of +2 configuration used for the +3V Specifications and Typical Characteristic Curves. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 71, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.13kΩ and 2.26kΩ resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input (R_F), reducing the DC output offset due to input bias current.

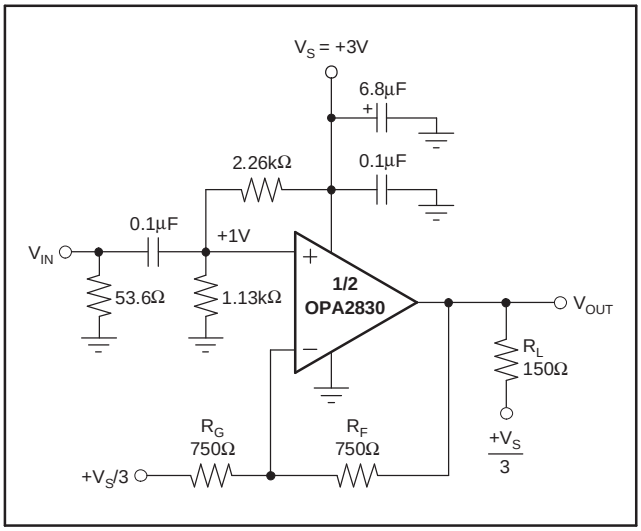

Figure 71. AC-Coupled, G = +2, +3V Single-Supply Specification and Test Circuit

Figure 72 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 72, the total effective load will be 150Ω || 1.5kΩ. Two optional components are included in Figure 72. An additional resistor (348Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 375Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical PC board layouts, this optional capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

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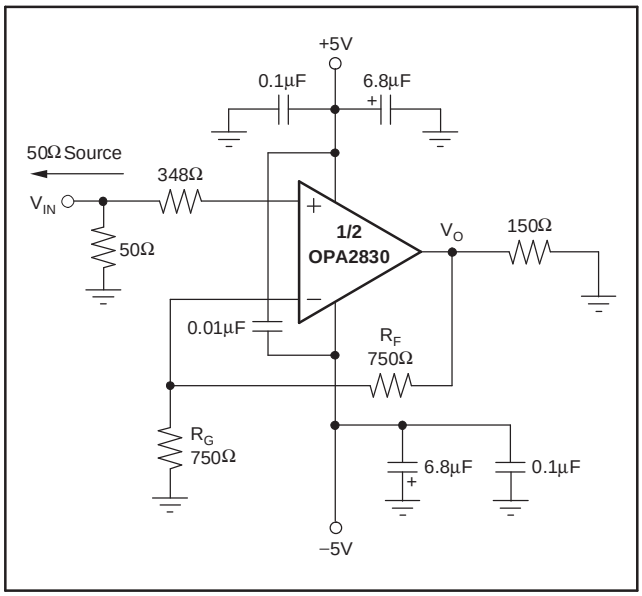

Figure 72. DC-Coupled, G = +2, Bipolar Supply Specification and Test Circuit

SINGLE-SUPPLY ADC INTERFACE

The ADC interface of Figure 73 shows a DC-coupled, single-supply ADC driver circuit. Many systems are now requiring +3V to +5V supply capability of both the ADC and its driver. The OPA2830 provides excellent performance in this demanding application. Its large input and output voltage ranges and low distortion support converters such as the ADS5203 shown in the figure on page 1. The input level-shifting circuitry was designed so that V_{IN} can be between 0V and 0.5V, while delivering an output voltage of 1V to 2V for the ADS5203.

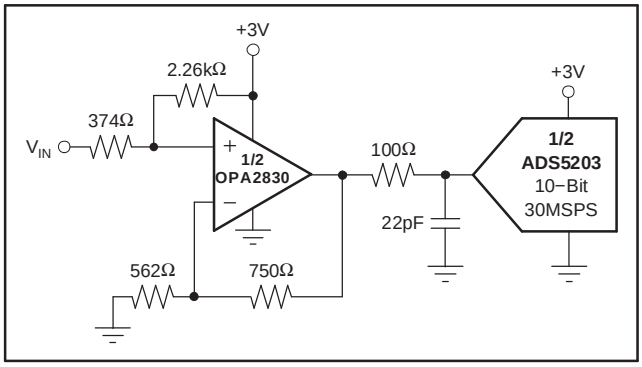

Figure 73. DC-Coupled, +3V ADC Driver

DC LEVEL-SHIFTING

Figure 74 shows the general form of Figure 73 as a DC-coupled noninverting amplifier that level-shifts the input up to accommodate the desired output voltage range. Given the desired signal gain (G), and the amount V_{OUT} needs to be shifted up (ΔV_{OUT}) when V_{IN} is at the center of its range, the following equations give the resistor values that produce the desired performance. Assume that R_4 is between 200Ω and 1.5kΩ.

- $NG = G + V_{OUT}/V_S$
- $R_1 = R_4/G$
- $R_2 = R_4/(NG – G)$
- $R_3 = R_4/(NG – 1)$

where:

- $NG = 1 + R_4/R_3$
- $V_{OUT} = (G)V_{IN} + (NG – G)V_S$

Make sure that V_{IN} and V_{OUT} stay within the specified input and output voltage ranges.

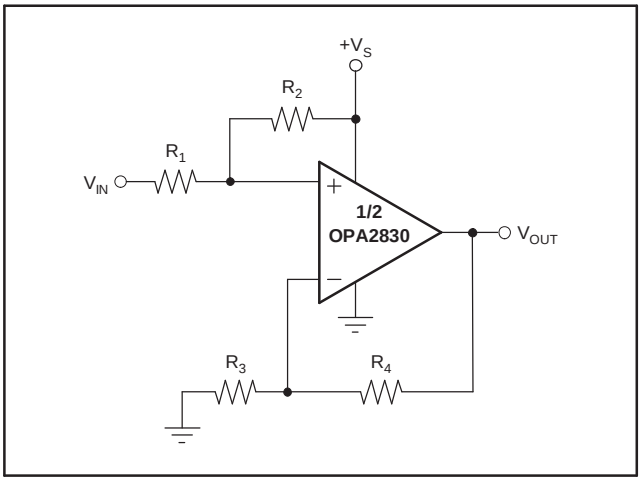

Figure 74. DC Level-Shifting

The circuit of Figure 73 is a good example of this type of application. It was designed to take V_{IN} between 0V and 0.5V and produce V_{OUT} between 1V and 2V when using a +3V supply. This means G = 2.00, and ΔV_{OUT} = 1.50V – G ɔ0.25V = 1.00V. Plugging these values into the above equations (with R_4 = 750Ω) gives: NG = 2.33, R_1 = 375Ω, R_2 = 2.25kΩ, and R_3 = 563Ω. The resistors were changed to the nearest standard values for the circuit of Figure 73.

AC-COUPLED OUTPUT VIDEO LINE DRIVER

Low-power and low-cost video line drivers often buffer digital-to-analog converter (DAC) outputs with a gain of 2 into a doubly-terminated line. Those interfaces typically require a DC blocking capacitor. For a simple solution, that interface often has used a very large value blocking capacitor (220µF) to limit tilt, or SAG, across the frames. One approach to creating a very low high-pass pole location using much lower capacitor values is shown in Figure 76. This circuit gives a voltage gain of 2 at the output pin with a high-pass pole at 8Hz. Given the 150Ω load, a simple blocking capacitor approach would require a 133µF value. The two much lower valued capacitors give this same low-pass pole using this simple *SAG correction* circuit of Figure 76.

The input is shifted slightly positive in Figure 76 using the voltage divider from the positive supply. This gives about a 200mV input DC offset that will show up at the output pin as a 400mV DC offset when the DAC output is at zero current during the sync tip portion of the video signal. This acts to hold the output in its linear operating region. This will pass on any power-supply noise to the output with a gain of approximately –20dB, so good supply decoupling is recommended on the power-supply pin. Figure 75 shows the frequency response for the circuit of Figure 76. This plot shows the 8Hz low-frequency high-pass pole and a high-end cutoff at approximately 100MHz.

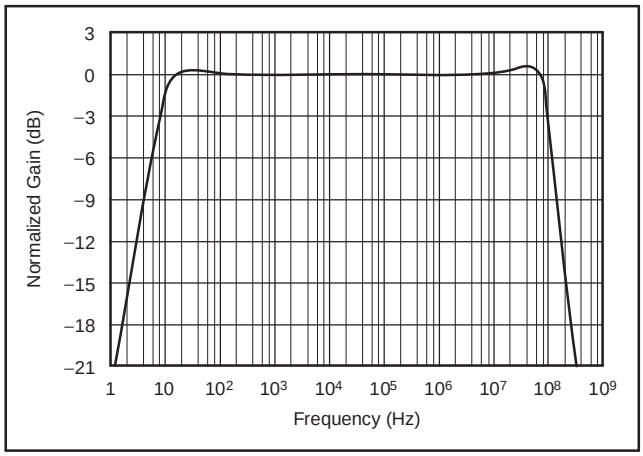

Figure 75. Video Line Driver Response to Matched Load

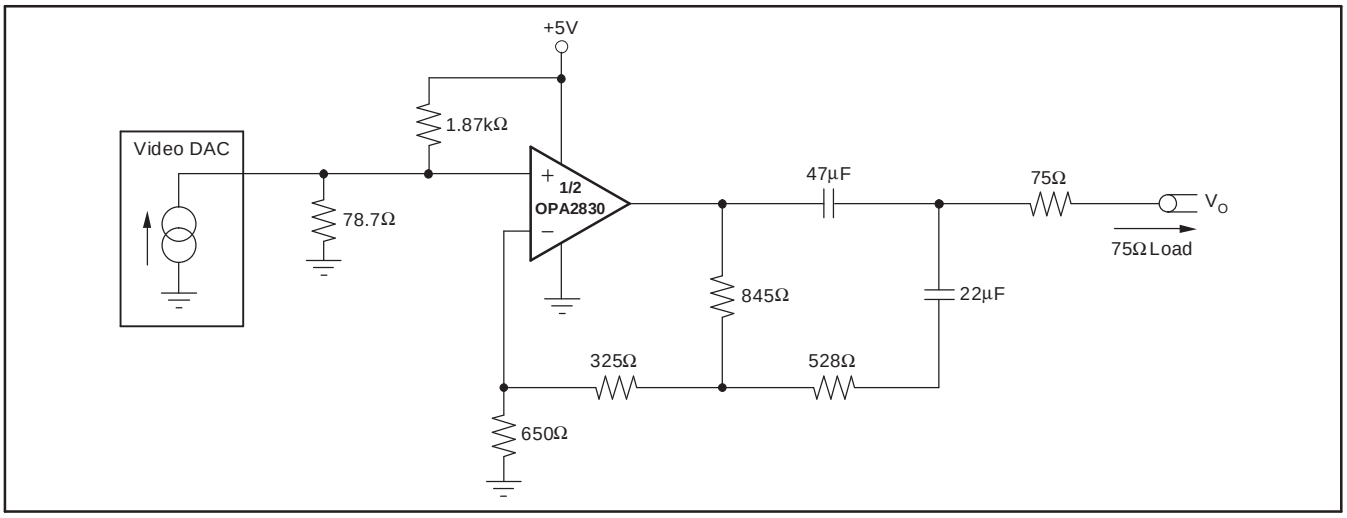

Figure 76. Video Line Driver with SAG Correction

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NONINVERTING AMPLIFIER WITH REDUCED PEAKING

Figure 77 shows a noninverting amplifier that reduces peaking at low gains. The resistor R_C compensates the OPA2830 to have higher Noise Gain (NG), which reduces the AC response peaking (typically 4dB at G = +1 without R_C) without changing the DC gain. V_{IN} needs to be a low impedance source, such as an op amp.

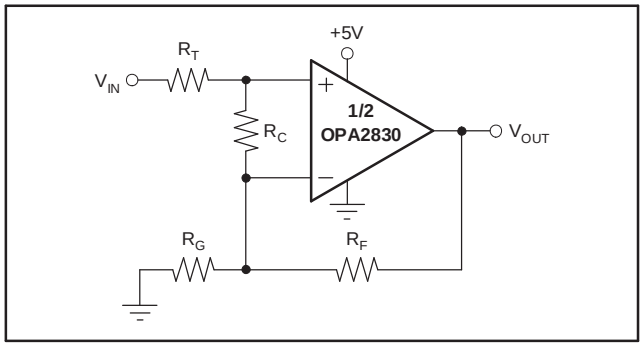

Figure 77. Compensated Noninverting Amplifier

The Noise Gain can be calculated as follows:

$$G_1 = 1 + \frac{R_F}{R_G}$$

$$G_2 = 1 + \frac{R_T + \frac{R_F}{G_1}}{R_C}$$

$$NG = G_1 \times G_2$$

A unity-gain buffer can be designed by selecting $R_T = R_F = 20.0\Omega$ and $R_C = 40.2\Omega$ (do not use R_G). This gives a noise gain of 2, so the response will be similar to the Characteristics Plots with G = +2 giving less peaking.

SINGLE-SUPPLY ACTIVE FILTER

The OPA2830 operating on a single +3V or +5V supply lends itself well to high-frequency active filter designs. The key additional requirement is to establish the DC operating point of the signal near the supply midpoint for highest dynamic range. Figure 78 shows an example design of a 1MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are AC-coupled using 0.1µF blocking capacitors (actually giving bandpass response with the low-frequency pole set to 32kHz for the component values shown). This allows the midpoint bias formed by the two 1.87kΩ resistors to appear at both the input and output pins. The midband signal gain is set to +4 (12dB) in this case. The capacitor to ground on the noninverting input is intentionally designed at a higher value to dominate input parasitic terms. At a gain of +4, the OPA2830 on a single supply will show 30MHz small- and large-signal bandwidth. The filter resistor values have been slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 1MHz, –3dB point with a maximally-flat passband (above the 32kHz AC-coupling corner), and a maximum stop band attenuation of 36dB at the amplifier's –3dB bandwidth of 30MHz.

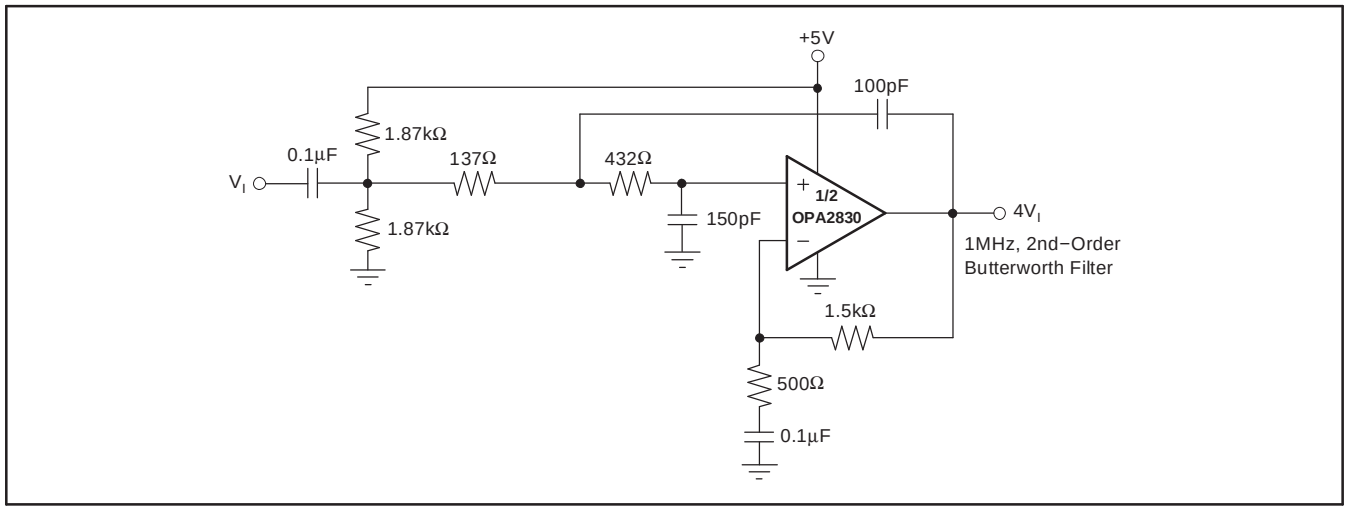

Figure 78. Single-Supply, High-Frequency Active Filter

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DIFFERENTIAL LOW-PASS ACTIVE FILTERS

The dual OPA2830 offers an easy means to implement low-power differential active filters. On a single supply, one way to implement a 2nd-order, low-pass filter is shown in Figure 79. This circuit provides a net differential gain of 1 with a precise 5MHz Butterworth response. The signal is AC-coupled (giving a high-pass pole at low frequencies) with the DC operating point for the circuit set by the unity-gain buffer—the BUF602. This buffer gives a very low output impedance to high frequencies to maintain accurate filter characteristics. If the source is a DC-coupled signal already biased into the operating range of the OPA2830 input CMR, these capacitors and the midpoint bias may be removed. To get the desired 5MHz cutoff, the input resistors to the filter is actually 119Ω. This is implemented in Figure 79 as the parallel combination of the two 238Ω resistors on each half of the differential input as part of the DC biasing network. If the BUF602 is removed, these resistors should be collapsed back to a single 119Ω input resistor.

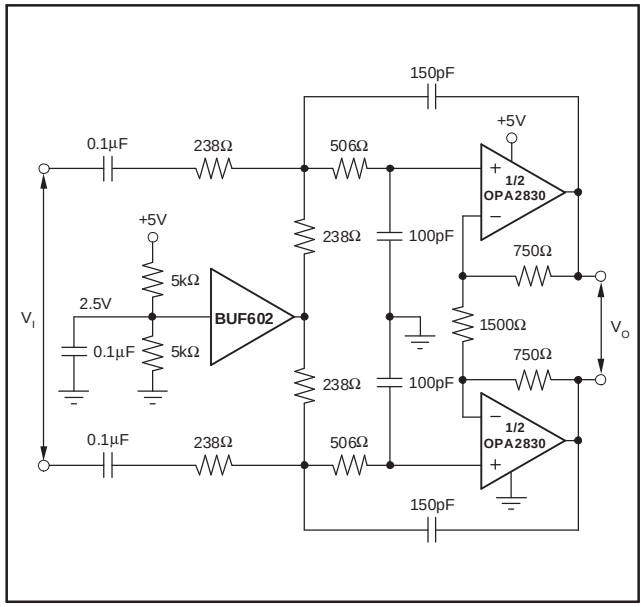

Figure 79. Single-Supply, 2nd-Order, Low-Pass Sallen-Key Filter

Implementing the DC bias in this way also attenuates the differential signal by half. This is recovered by setting the amplifier gain at 2V/V to get a net unity-gain filter characteristic from input to output. The filter design shown here has also adjusted the resistor values slightly from an ideal analysis to account for the 100MHz bandwidth in the amplifier stages. The filter capacitors at the noninverting inputs are shown as two separate capacitors to ground. While it is certainly correct to collapse these two capacitors into a single capacitor across the two inputs (which would be 50pF for this circuit) to get the same differential filtering characteristic, tests have shown two separate capacitors to a low impedance point act to attenuate the common-mode feedback present in this circuit giving more stable operation in actual implementation. Figure 80 shows the frequency response for the filter of Figure 79.

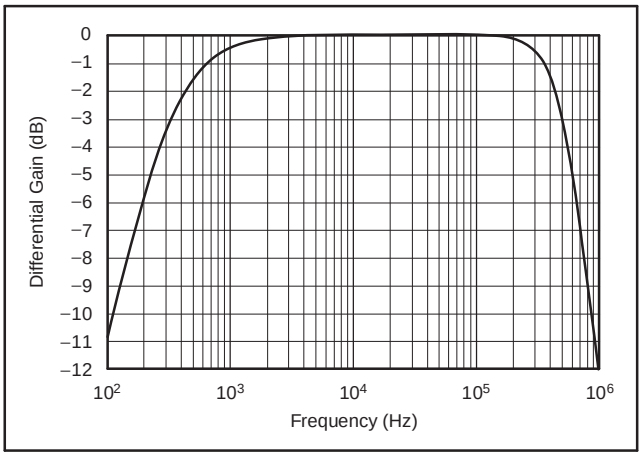

Figure 80. 5MHz, 2nd-Order, Butterworth Low-Pass Filter

HIGH-PASS FILTERS

Another approach to mid-supply biasing is shown in Figure 81. This method uses a bypassed divider network in place of the buffer used in Figure 79. The impedance is set by the parallel combination of the resistors forming the divider network, but as frequency increases it looks more and more like a short due to the capacitor. Generally, the capacitor value needs to be two to three orders of magnitude greater than the filter capacitors shown for the circuit to work properly.

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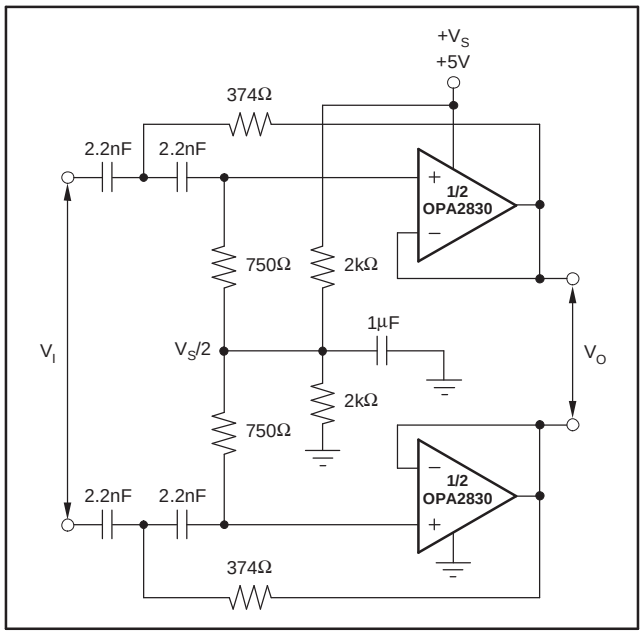

Figure 81. 138kHz, 2nd-Order, High-Pass Filter

Results showing the frequency response for the circuit of Figure 81 is shown in Figure 82.

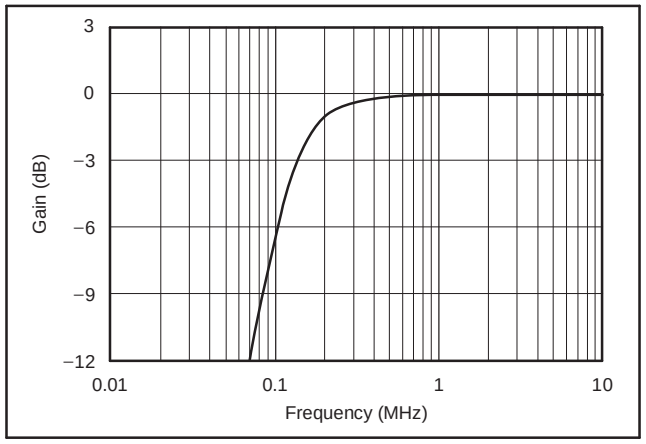

Figure 82. Frequency Response for the Filter of Figure 81

HIGH-PERFORMANCE DAC TRANSIMPEDANCE AMPLIFIER

High-frequency video Digital-to-Analog Converters (DACs) can sometimes benefit from a low distortion output amplifier to retain their SFDR performance into real-world loads. Figure 83 shows a differential output drive implementation. The diagram shows the signal output current(s) connected into the virtual ground summing junction(s) of the OPA2830, which is set up as a transimpedance stage or *I-V converter*. If the DAC requires that its outputs terminate to a compliance voltage other than ground for operation, the appropriate voltage level may be applied to the noninverting input of the OPA2830. The DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D in Figure 83) will produce a zero in the noise gain for the OPA2830 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}}$$

which will give a cutoff frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}}$$

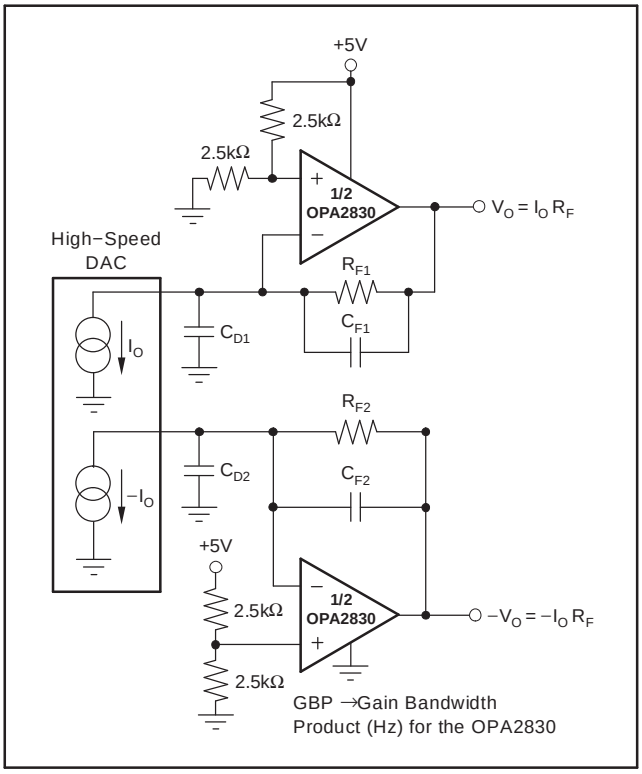

Figure 83. High-Speed DAC—Differential Transimpedance Amplifier

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DESIGN-IN TOOLS

Demonstration Fixtures

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2830 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2830ID	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2830IDGK	MSOP-8	DEM-OPA-MSOP-2A	SBOU004

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2830 product folder.

Macromodel and Applications Support

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA2830 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA2830 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS OPTIMIZING RESISTOR VALUES

Since the OPA2830 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a direct short.

Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA2830. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 72) to be less than about 400Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G < 400\Omega$ will keep this pole above 200MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) would require a 100Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see Figure 84). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH vs GAIN: NONINVERTING OPERATION

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most amplifiers will exhibit a more complex response with lower phase margin. The OPA2830 is compensated to give a slightly peaked response in a noninverting gain of 2 (see Figure 72). This results in a typical gain of +2 bandwidth of 105MHz, far exceeding that predicted by dividing the 105MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 10MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 105MHz.

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Frequency response in a gain of +2 may be modified to achieve exceptional flatness simply by increasing the noise gain to 3. One way to do this, without affecting the +2 signal gain, is to add an 2.55kΩ resistor across the two inputs, as shown in Figure 77. A similar technique may be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 750Ω feedback resistor along with a 750Ω resistor across the two op amp inputs, the voltage follower response will be similar to the gain of +2 response of Figure 71. Further reducing the value of the resistor across the op amp inputs will further dampen the frequency response due to increased noise gain. The OPA2830 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This minimal reduction is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

INVERTING AMPLIFIER OPERATION

All of the familiar op amp application circuits are available with the OPA2830 to the designer. See Figure 84 for a typical inverting configuration where the I/O impedances and signal gain from Figure 70 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. It also allows the input to be biased at $V_S/2$ without any headroom issues. The output voltage can be independently moved to be within the output voltage range with coupling capacitors, or bias adjustment resistors.

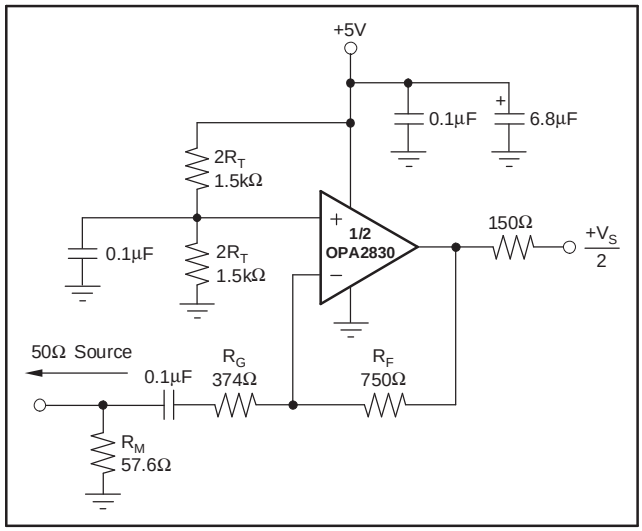

Figure 84. AC-Coupled, G = –2 Example Circuit

In the inverting configuration, three key design considerations must be noted. The first consideration is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance.

However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This configuration has the interesting advantage of the noise gain becoming equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered above. The amplifier output will now see the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values, as shown in Figure 84, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and hence influences the bandwidth. For the example in Figure 84, the R_M value combines in parallel with the external 50Ω source impedance (at high frequencies), yielding an effective driving impedance of 50Ω || 57.6Ω = 26.8Ω. This impedance is added in series with R_G for calculating the noise gain. The resulting noise gain is 2.87 for Figure 84, as opposed to only 2 if R_M could be eliminated as discussed above. The bandwidth will therefore be lower for the gain of –2 circuit of Figure 84 (NG = +2.87) than for the gain of +2 circuit of Figure 70.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistors on the noninverting input (a parallel combination of R_T = 750Ω). If this resistor is set equal to the total DC resistance looking out of the inverting node, the output DC error, due to the input bias currents, will be reduced to (Input Offset Current) times R_F. With the DC blocking capacitor in series with R_G, the DC source impedance looking out of the inverting mode is simply R_F = 750Ω for Figure 84. To reduce the additional high-frequency noise introduced by this resistor and power-supply feed-through, R_T is bypassed with a capacitor.

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OUTPUT CURRENT AND VOLTAGES

The OPA2830 provides outstanding output voltage capability. For the +5V supply, under no-load conditions at +25°C, the output voltage typically swings closer than 90mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the ensured tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2830 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristic curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2830. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see the *Board Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain will also reduce the peaking (see Figure 77).

DISTORTION PERFORMANCE

The OPA2830 provides good distortion performance into a 150Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 72) this is sum of $R_F + R_G$, while in the inverting configuration, only R_F needs to be included in parallel with the actual load. Running differentially suppresses the 2nd-harmonic, as shown in the differential typical characteristic curves.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 9.2nV/√Hz input voltage noise for the OPA2830 however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.8pA/√Hz) combine to give low output noise under a wide variety of operating conditions. Figure 85 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

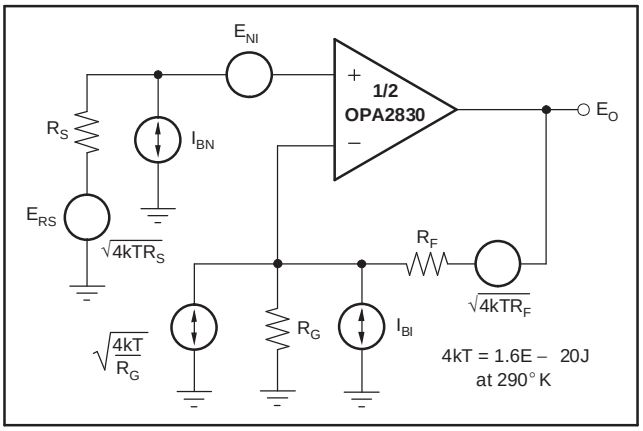

Figure 85. Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 85:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (1)$$

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Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 2:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Evaluating these two equations for the circuit and component values shown in Figure 70 will give a total output spot noise voltage of 19.3nV/√Hz and a total equivalent input spot noise voltage of 9.65nV/√Hz. This is including the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 9.2nV/√Hz specification for the op amp voltage noise alone.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output DC accuracy in a wide variety of applications. The power-supply current trim for the OPA2830 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5µA out of each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. This is done by matching the DC source resistances appearing at the two inputs. Evaluating the configuration of Figure 72 (which has matched DC input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

- (NG = noninverting signal gain at DC)
- ±(NG × $V_{OS(MAX)}$) + (R_F × $I_{OS(MAX)}$)
- = ±(2 × 7.5mV) ⨭(375Ω × 1.1µA)
- = ±15.41mV

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques are based on adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. Bring the DC offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

THERMAL ANALYSIS

Maximum desired junction temperature will set the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load; though, for resistive loads connected to mid-supply ($V_S/2$), P_{DL} is at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2/(16 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2830 (MSOP-8 package) in the circuit of Figure 72 operating at the maximum specified ambient temperature of +85°C and driving a 150Ω load at +2.5V_{DC} on both outputs.

$$P_D = 10V \times 11.9mA + 2\left[\frac{5^2}{\left(16 \times \left(150\Omega \parallel 1500\Omega\right)\right)}\right] = 142mW$$

$$\text{Maximum } T_J = +85^\circ C + \left(0.142W \times 150^\circ C/W\right) = 106^\circ C$$

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower ensured junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2830 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional

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bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Each power-supply connection should always be decoupled with one of these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the Typical Characteristics is a good starting point for design.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2830 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2830 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve *Recommended R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2830 onto the board.

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INPUT AND ESD PROTECTION

The OPA2830 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 86.

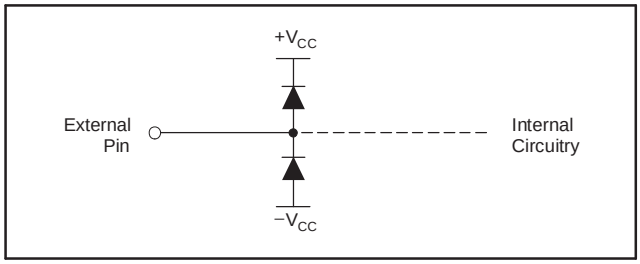

Figure 86. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA2830), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2006) to Revision D	Page
• Changed rating of storage temperature range in Absolute Maximum Ratings table from –40°C to +125°C to –65°C to +125°C	2

Changes from Revision B (February 2006) to Revision C	Page
• Changed Differential Input Voltage to ±2.5V from ±1.2V	2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2830ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2830	Samples
OPA2830IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A59	Samples
OPA2830IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A59	Samples
OPA2830IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2830	Samples
OPA2830IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2830	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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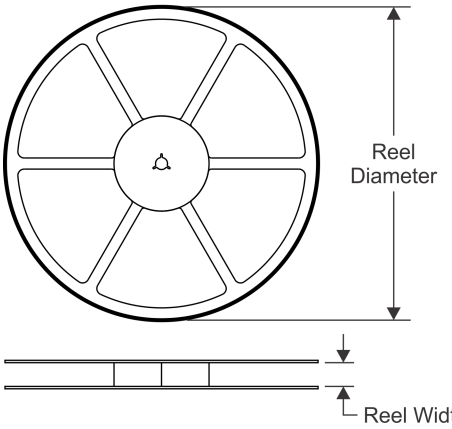
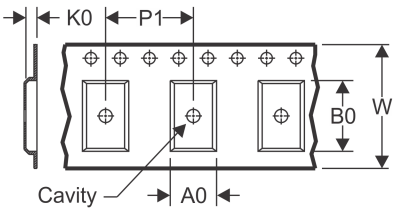
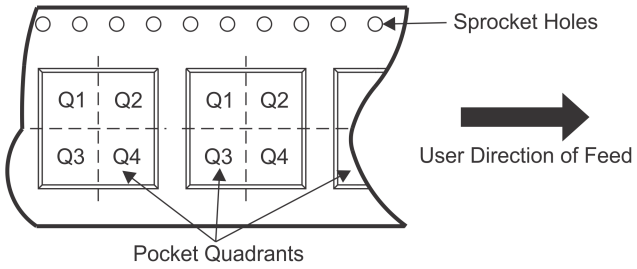


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

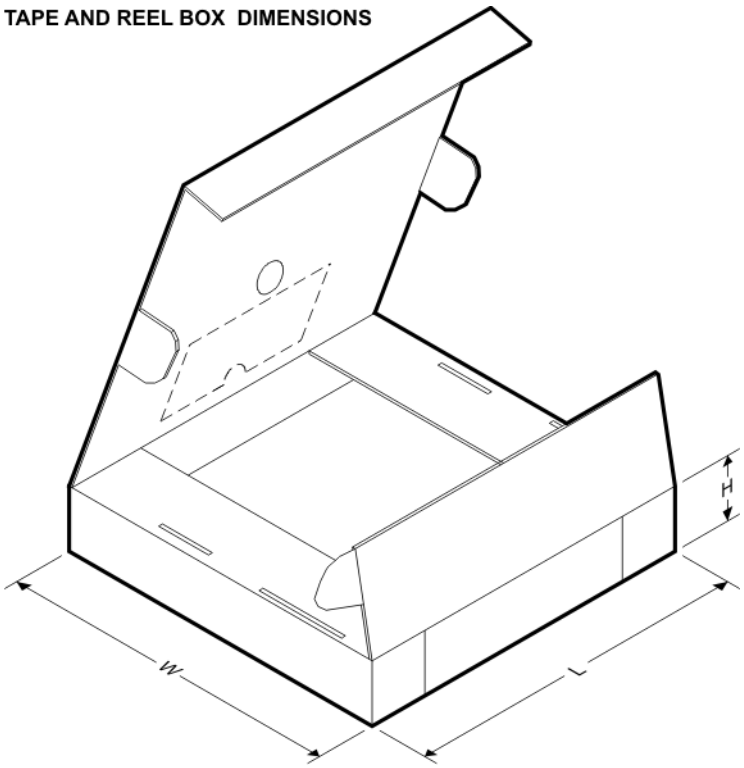
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

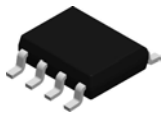
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2830IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2830IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2830IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2830IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2830IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2830IDR	SOIC	D	8	2500	367.0	367.0	35.0

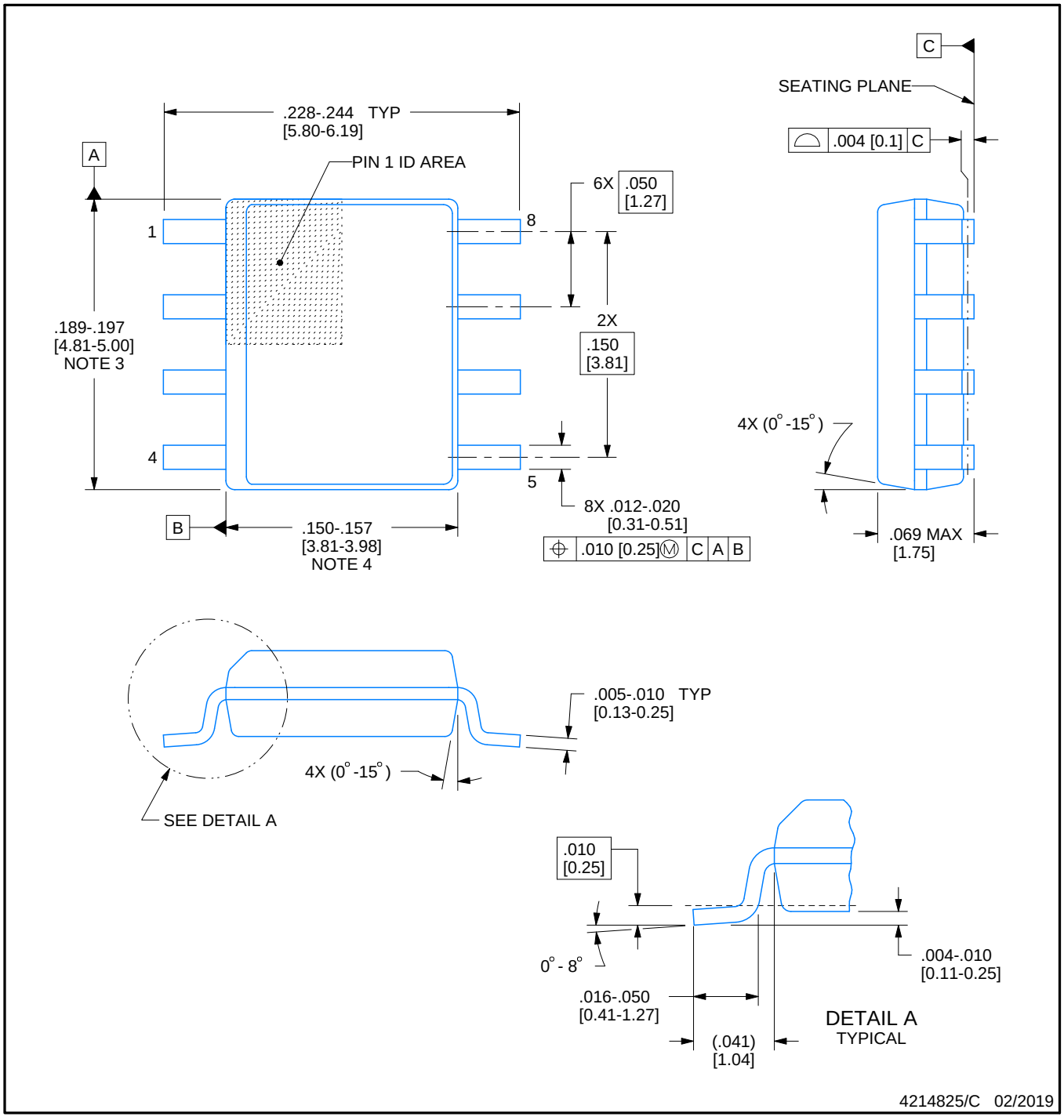


PACKAGE OUTLINE

D0008A

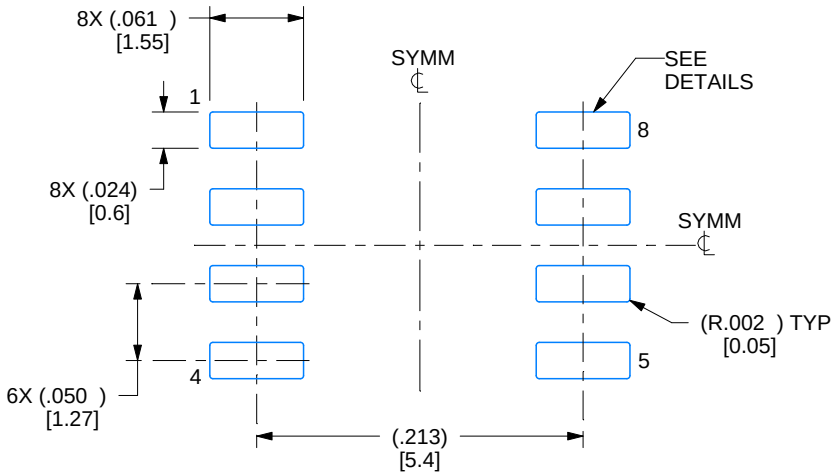
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

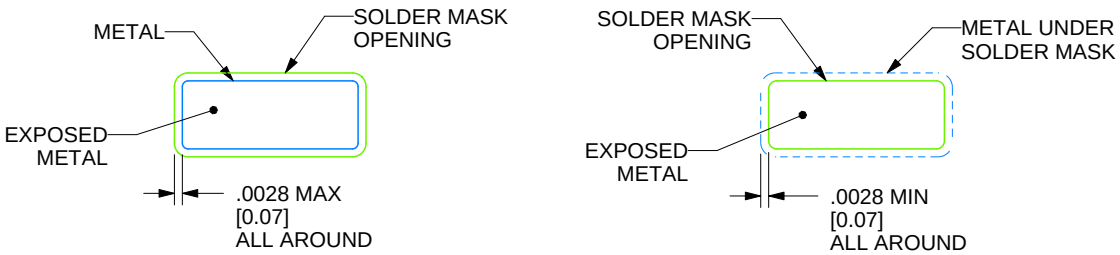


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

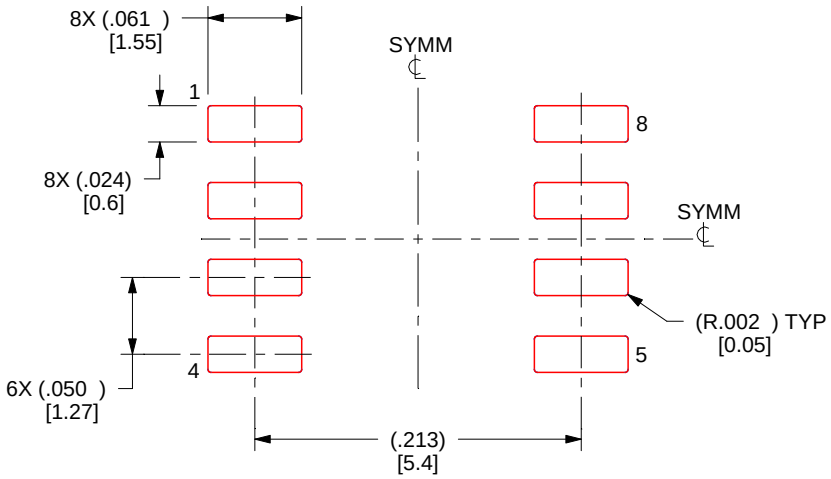
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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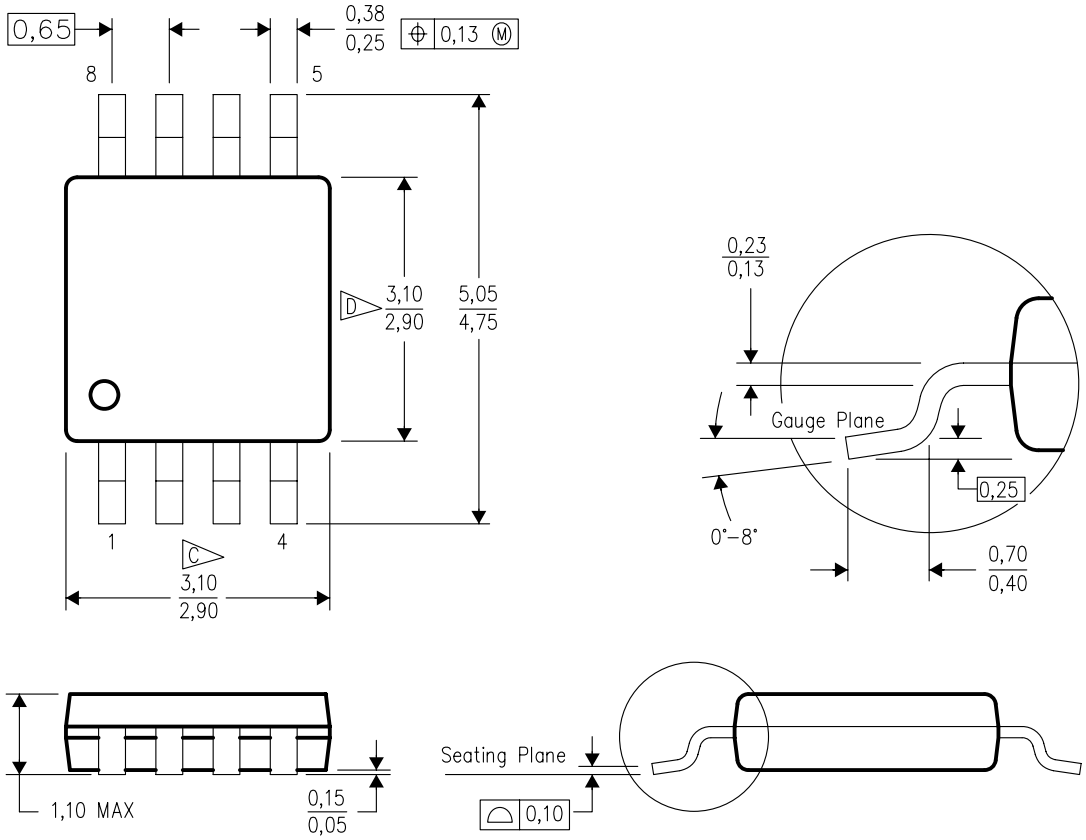
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

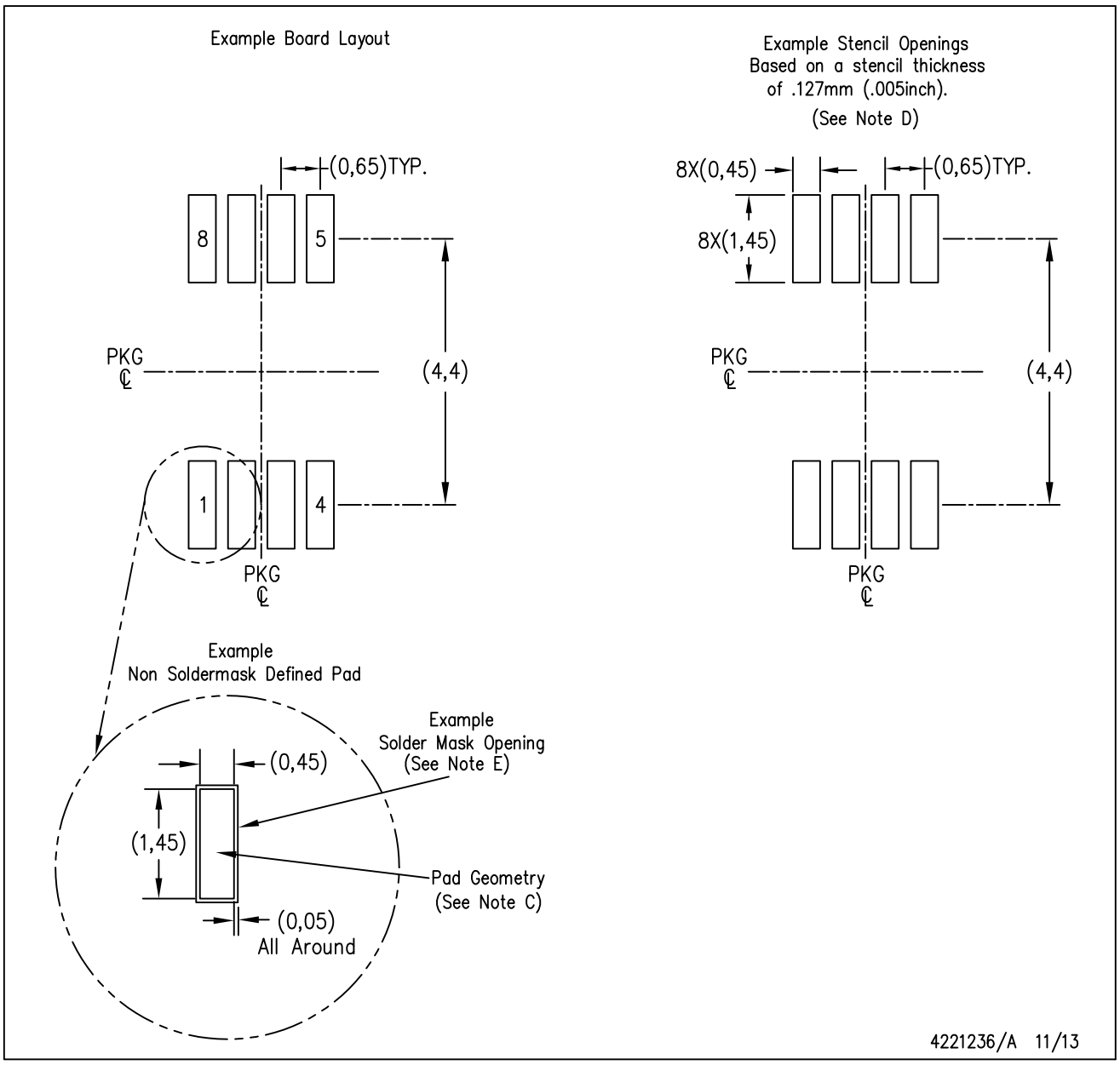
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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