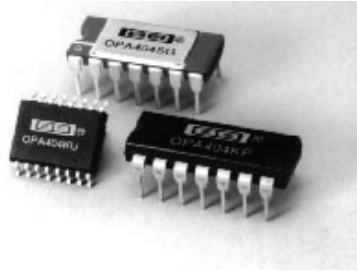




**THE DATASHEET OF
OPA404KU/1K**





OPA404

Quad High-Speed Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±750μV max
- LOW BIAS CURRENT: ±4pA max
- LOW SETTLING: 1.5μs to 0.01%
- STANDARD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

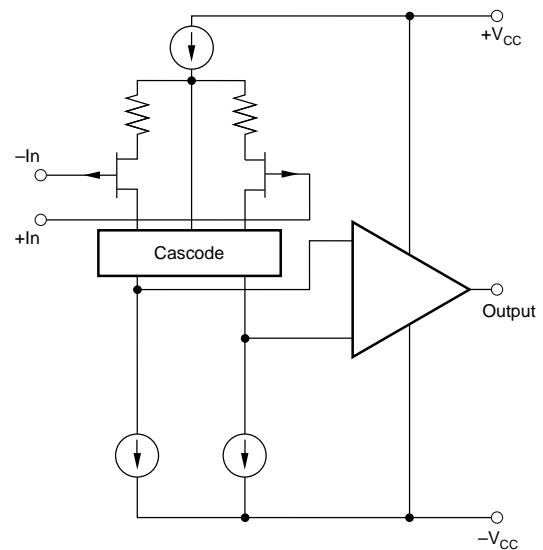
The OPA404 is a high performance monolithic *Difet*[®] (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET[®] amplifiers.

Laser-trimming of thin-film resistors gives very low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.



OPA404 Simplified Circuit
(Each Amplifier)

Difet[®], Burr-Brown Corp.
BIFET[®], National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU ⁽¹⁾			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE Voltage: $f_O = 10\text{Hz}$ $f_O = 100\text{Hz}$ $f_O = 1\text{kHz}$ $f_O = 10\text{kHz}$ $f_B = 10\text{Hz to } 10\text{kHz}$ $f_B = 0.1\text{Hz to } 10\text{Hz}$ Current: $f_B = 0.1\text{Hz to } 10\text{Hz}$ $f_O = 0.1\text{Hz thru } 20\text{kHz}$			32			*			*		$\text{nV}/\sqrt{\text{Hz}}$
				19			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				15			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				12			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				1.4			*		*		μVrms
				0.95			*		*		$\mu\text{Vp-p}$
				12			*		*		fA, p-p
			0.6			*		*		$\text{fA}/\sqrt{\text{Hz}}$	
OFFSET VOLTAGE Input Offset Voltage KP, KU Average Drift KP, KU Supply Rejection KP, KU Channel Separation	$V_{CM} = 0\text{VDC}$		± 260 ± 750	$\pm 1\text{mV}$ $\pm 2.5\text{mV}$		*	± 750		*	*	μV μV
	$T_A = T_{MIN}$ to T_{MAX}		± 3 ± 5			*			*		$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
	$\pm V_{CC} = 12\text{V to } 18\text{V}$	80 76	100 100		86	*		*	*		dB dB
	$100\text{Hz, } R_L = 2\text{k}\Omega$		125			*			*		dB
BIAS CURRENT Input Bias Current KP, KU	$V_{CM} = 0\text{VDC}$		± 1 ± 1	± 8 ± 12		*	± 4		*	*	pA pA
OFFSET CURRENT Input Offset Current KP, KU	$V_{CM} = 0\text{VDC}$		0.5 0.5	8 12		*	4		*	*	pA pA
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{14} \parallel 3$			*			*		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
VOTAGE RANGE Common-Mode Input Range Common-Mode Rejection KP, KU	$V_{IN} = \pm 10\text{VDC}$	± 10.5 88 84	$+13, -11$ 100 100		*	*		*	*		V dB dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	88	100		92	*		*	*		dB
FREQUENCY RESPONSE Gain Bandwidth Full Power Response Slew Rate Settling Time: 0.1% 0.01%	Gain = 100	4	6.4		5	*		*	*		MHz
	$20\text{Vp-p, } R_L = 2\text{k}\Omega$		570			*		*	*		kHz
	$V_O = \pm 10\text{V, } R_L = 2\text{k}\Omega$	24	35		28	*		*	*		$\text{V}/\mu\text{s}$
	Gain = -1, $R_L = 2\text{k}\Omega$		0.6			*		*	*		μs
	$C_L = 100\text{ pF, } 10\text{V Step}$		1.5			*		*	*		μs
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$	± 11.5	$+13.2, -13.8$		*	*		*	*		V
	$V_O = \pm 10\text{VDC}$	± 5	± 10		*	*		*	*		mA
	1MHz, Open Loop		80			*			*		Ω
	Gain = +1		1000			*			*		pF
		± 10	± 27	± 40	*	*	*	*	*	*	mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent			± 15			*			*		VDC
		± 5		± 18	*		*	*	*	*	VDC
	$I_O = 0\text{mADC}$		9	10		*	*	*	*	*	mA
TEMPERATURE RANGE Specification KP, KU Operating KP, KU Storage KP, KU θ Junction-Ambient KP, KU	Ambient Temperature	-25 0		+85 +70	*		*	-55		+125	$^\circ\text{C}$ $^\circ\text{C}$
	Ambient Temperature	-55		+125	*		*	*		*	$^\circ\text{C}$
	Ambient Temperature	-25		+85	*		*	*		*	$^\circ\text{C}$
	Ambient Temperature	-65		+150	*		*	*		*	$^\circ\text{C}$
	Ambient Temperature	-40		+125	*		*	*		*	$^\circ\text{C}$
			100			*		*		*	$^\circ\text{C}/\text{W}$
			120/100								$^\circ\text{C}/\text{W}$

*Specifications same as OPA404AG.

NOTE: (1) OPA404KU may be marked OPA404U.

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range KP, KU	Ambient Temperature	-25 0		+85 +70	*		*	-55		+125	°C °C
INPUT OFFSET VOLTAGE Input Offset Voltage KP, KU Average Drift KP, KU Supply Rejection	$V_{CM} = 0\text{VDC}$		± 450 ± 1 ± 3 ± 5 96	2mV ± 3.5		*	$\pm 1.5\text{mV}$		± 550 *	$\pm 2.5\text{mV}$	μV mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$ dB
BIAS CURRENT Input Bias Current	$V_{CM} = 0\text{VDC}$		± 32	± 200		*	± 100		± 500	$\pm 5\text{nA}$	pA
OFFSET CURRENT Input Offset Current	$V_{CM} = 0\text{VDC}$		17	100		*	50		260	2.5nA	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection KP, KU	$V_{IN} = \pm 10\text{VDC}$	± 10 82 80	$\pm 12.7, -10.6$ 99 99		*	*		± 10 80	$+12.6, -10.5$ 88		V dB dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	82	94		86	*		80	88		dB
RATED OUTPUT Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	± 11.5 ± 5 ± 8	$\pm 12.9, -13.8$ ± 9 ± 20	± 50	*	*	*	± 11 *	$+12.7, -13.8$ ± 8 *		V mA mA
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		9.3	10.5		*	*		9.4	11	mA

* Specification same as OPA404AG.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA404KP	14-Pin Plastic DIP	0°C to +70°C
OPA404KU ⁽¹⁾	16-Pin Plastic SOIC	0°C to +70°C
OPA404AG	14-Pin Ceramic DIP	-25°C to +85°C
OPA404BG	14-Pin Ceramic DIP	-25°C to +85°C
OPA404SG	14-Pin Ceramic DIP	-55°C to +125°C

NOTE: (1) OPA404KU may be marked OPA404U.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA404KP	14-Pin Plastic DIP	010
OPA404KU ⁽²⁾	16-Pin Plastic SOIC	211
OPA404AG	14-Pin Ceramic DIP	169
OPA404BG	14-Pin Ceramic DIP	169
OPA404SG	14-Pin Ceramic DIP	169

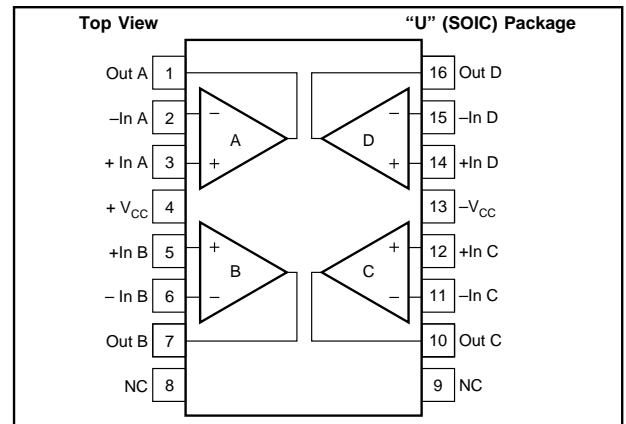
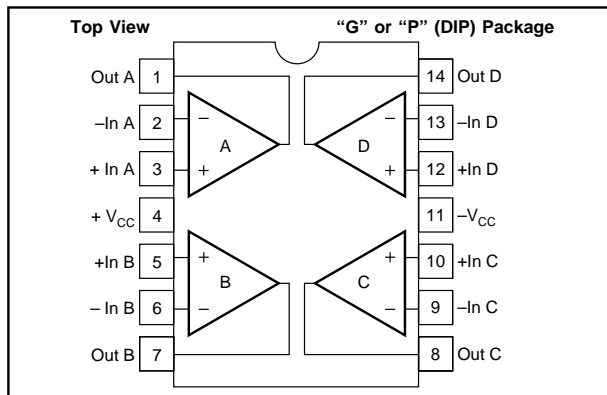
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book. (2) OPA404KU may be marked OPA404U.

ABSOLUTE MAXIMUM RATINGS

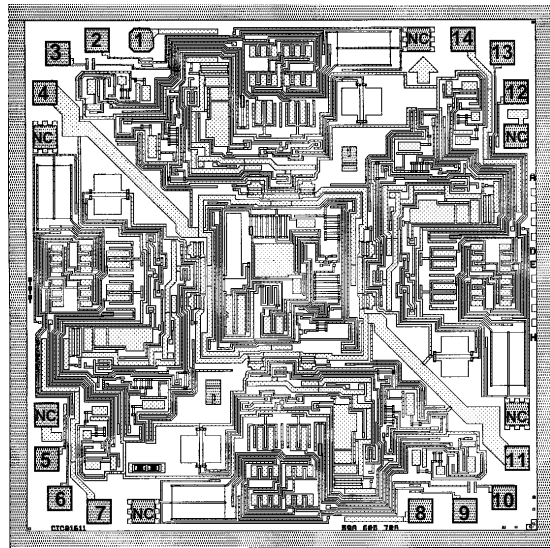
Supply	$\pm 18\text{VDC}$	Operating Temperature Range .. P, U = -25°C/+85°C, G = -55°C/+125°C	
Internal Power Dissipation ⁽¹⁾	1000mW	Lead Temperature (soldering, 10s)	300°C
Differential Input Voltage ⁽²⁾	$\pm 36\text{VDC}$	SOIC (soldering, 3s)	+260°C
Input Voltage Range ⁽²⁾	$\pm 18\text{VDC}$	Output Short-Circuit Duration ⁽³⁾	Continuous
Storage Temperature Range ... P, U = -40°C/+125°C, G = -65°C/+150°C		Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on $\theta_{JC} = 30^\circ\text{C/W}$ or $\theta_{JA} = 120^\circ\text{C/W}$. (2) For supply voltages less than $\pm 18\text{VDC}$ the absolute maximum input voltage is equal to: $18\text{V} > V_{IN} > -V_{CC} - 8\text{V}$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .

PIN CONFIGURATION



DICE INFORMATION



OPA404 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Output A	8	Output C
2	-Input A	9	-Input C
3	+Input A	10	+Input C
4	+V _{CC}	11	-V _{CC}
5	+Input B	12	+Input D
6	-Input B	13	-Input D
7	Output B	14	Output D

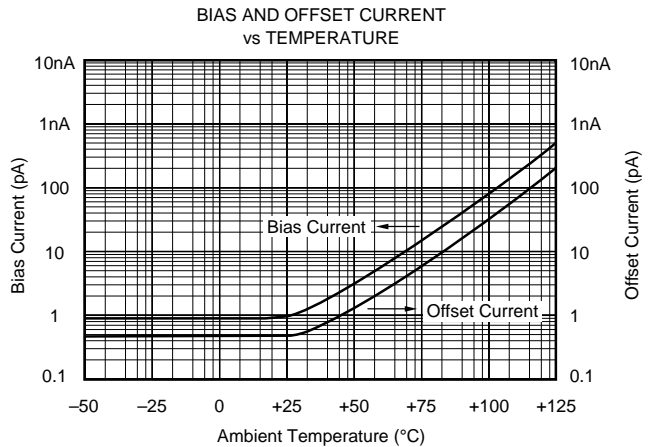
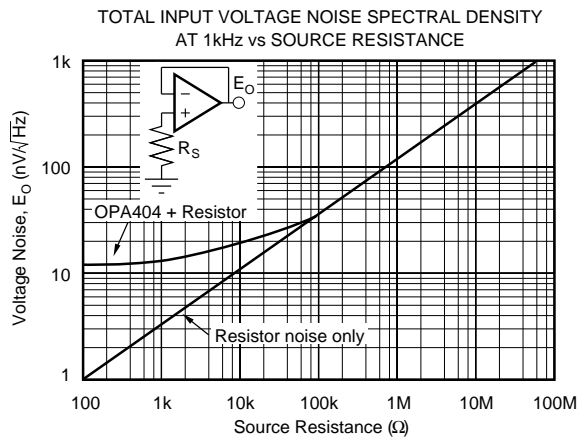
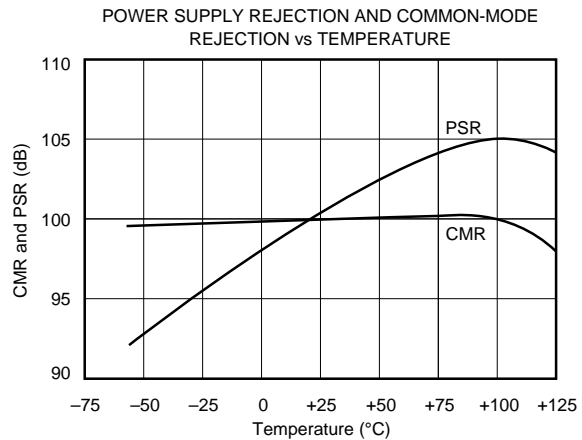
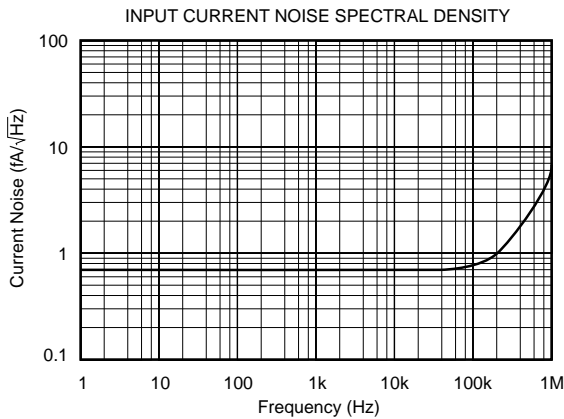
Substrate Bias: -V_{CC}
 NC: No connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	108 x 108 ±5	2.74 x 2.74 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	

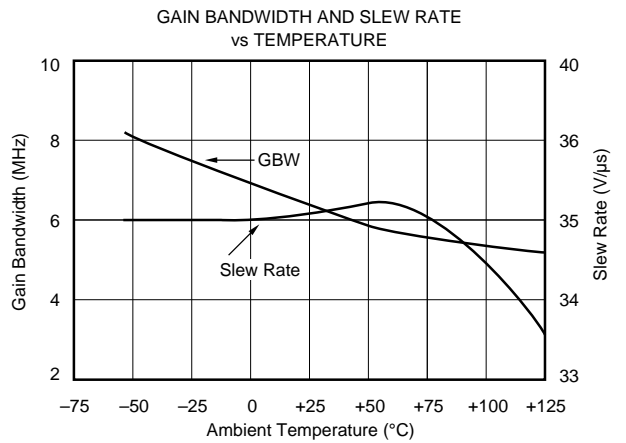
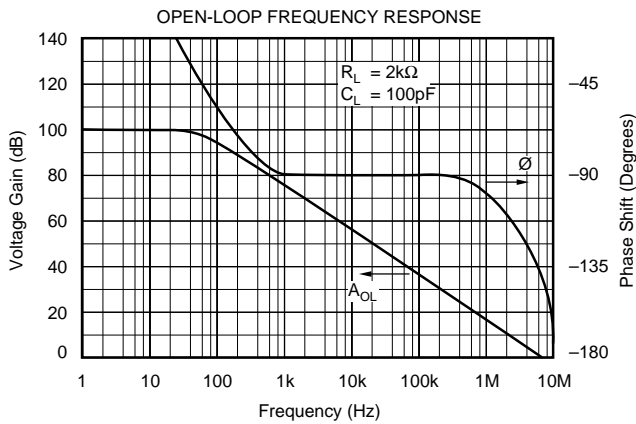
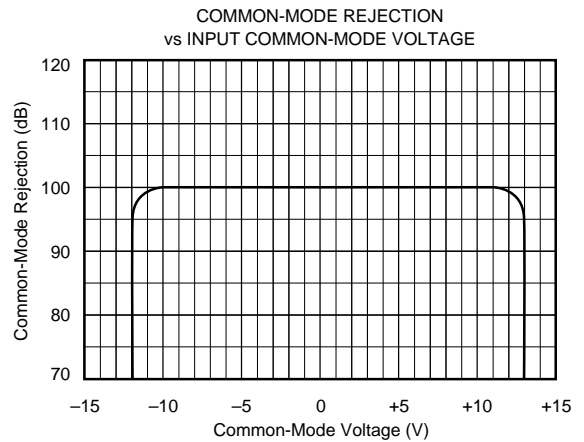
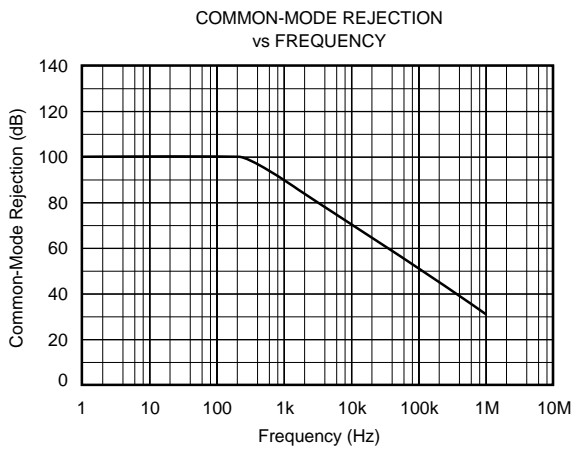
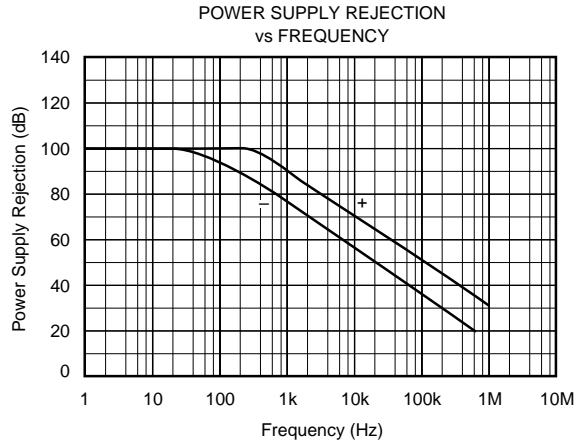
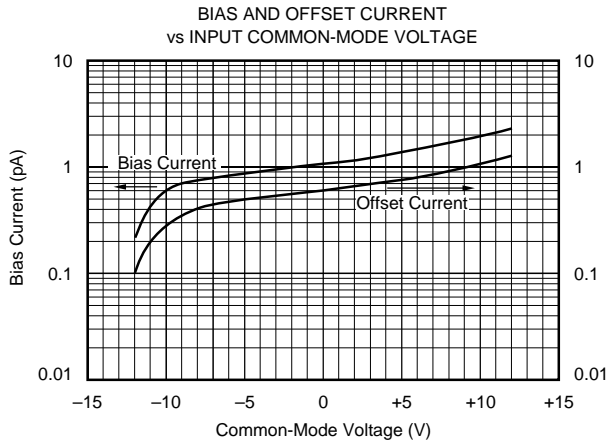
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

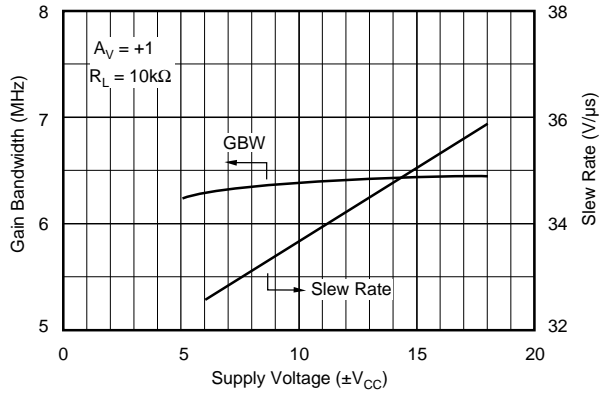
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



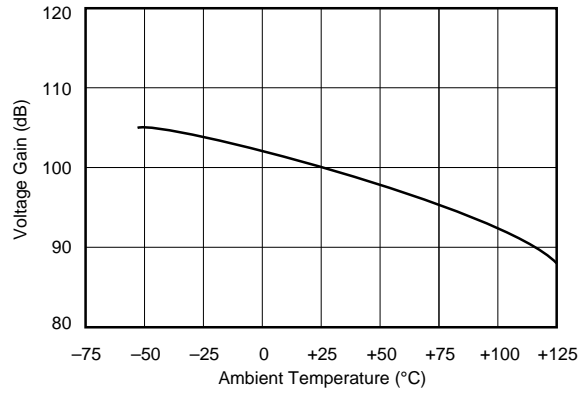
TYPICAL PERFORMANCE CURVES (CONT)

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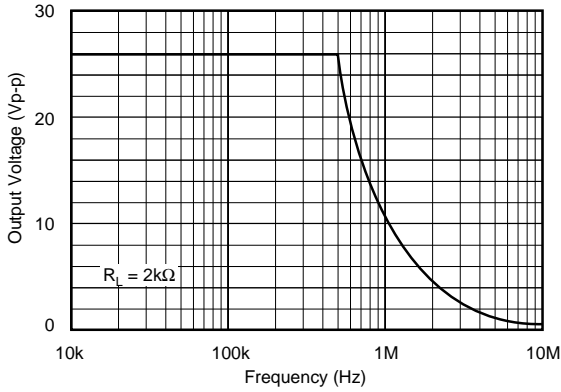
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



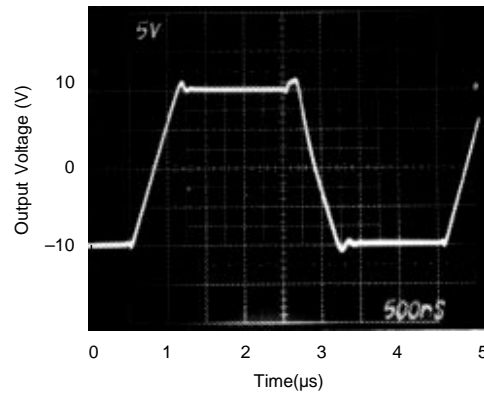
OPEN-LOOP GAIN vs TEMPERATURE



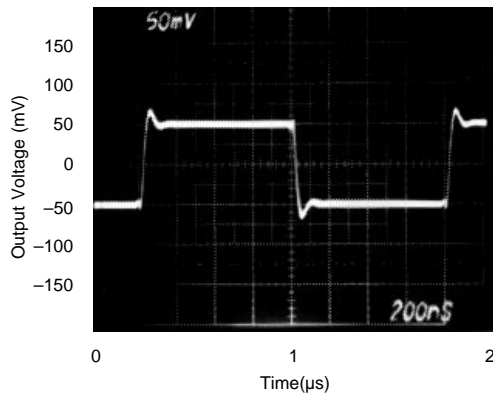
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



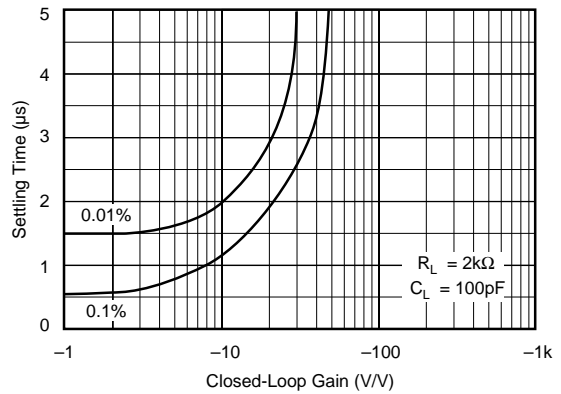
LARGE SIGNAL TRANSIENT RESPONSE



SMALL SIGNAL TRANSIENT RESPONSE

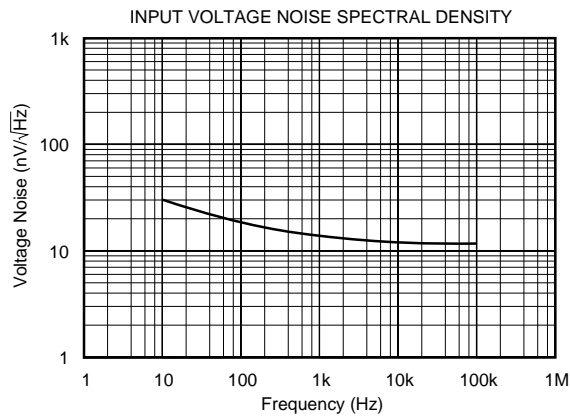
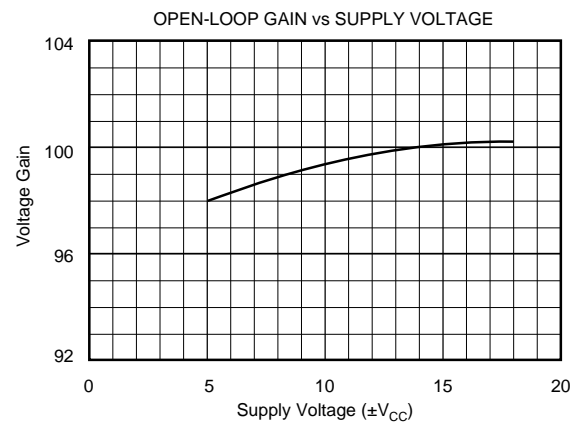
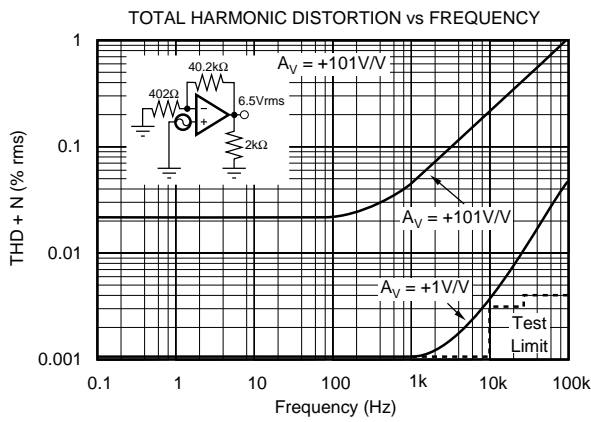
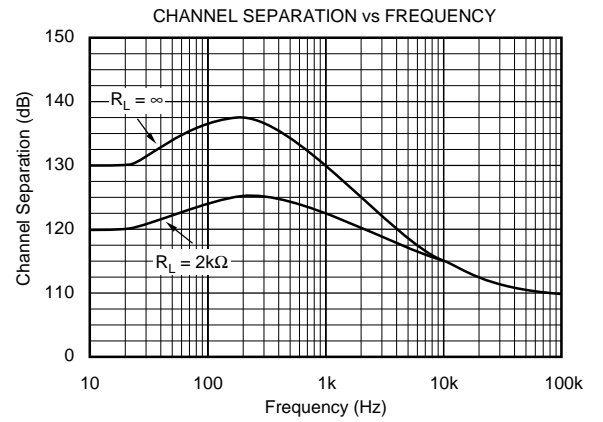
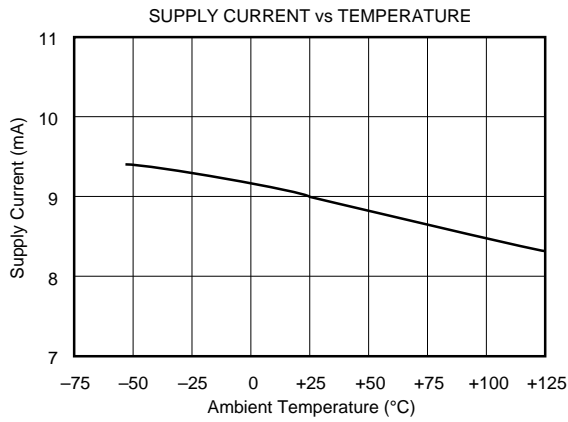


SETTLING TIME vs CLOSED-LOOP GAIN



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

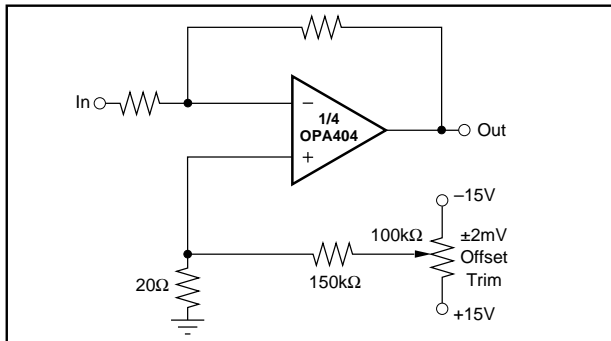


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the *Difet* OPA404 requires input current limiting resistors only if its input voltage is greater than 8 volts more negative than $-V_{CC}$. A $10k\Omega$ series resistor will limit the input current to a safe value with up to $\pm 15V$ input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

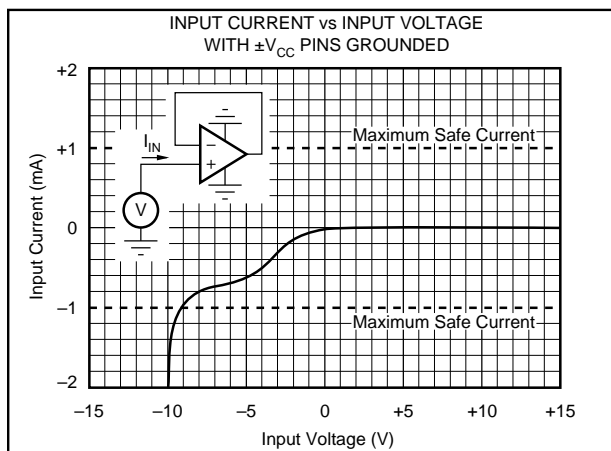


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A “guard” pattern should completely surround the high impedance input leads and should be connected to a low-impedance point which is at the signal input potential. (See Figure 3).

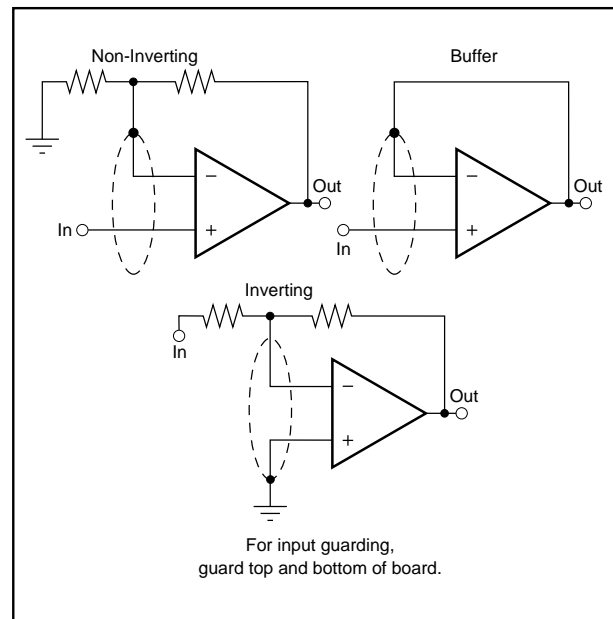


FIGURE 3. Connection of Input Guard.

HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF®, baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

BIAS CURRENT CHANGE vs COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA404 is not compromised by common-mode voltage.

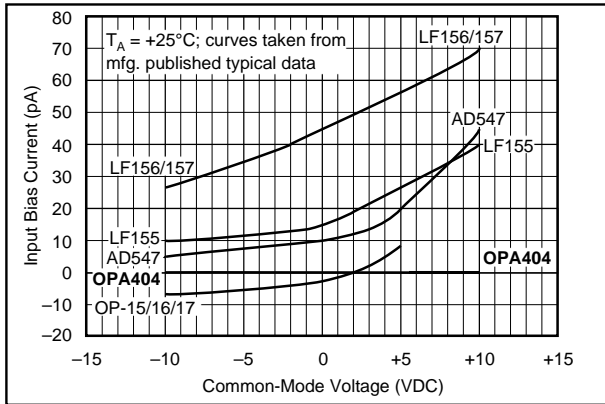


FIGURE 4. Input Bias Current vs Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 11 are circuit diagrams of various applications for the OPA404.

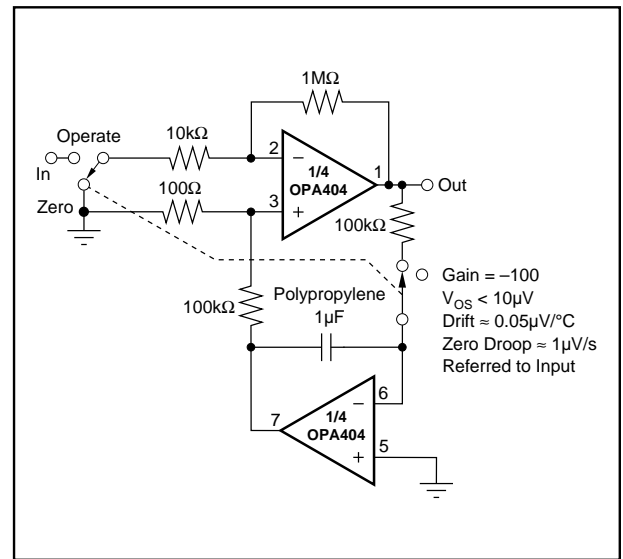


FIGURE 5. Auto-Zero Amplifier.

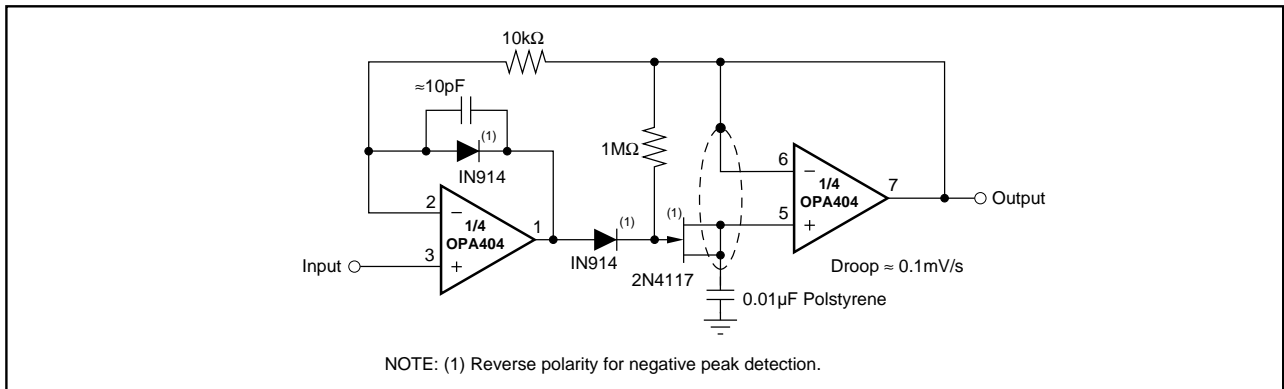


FIGURE 6. Low-Droop Positive Peak Detector.

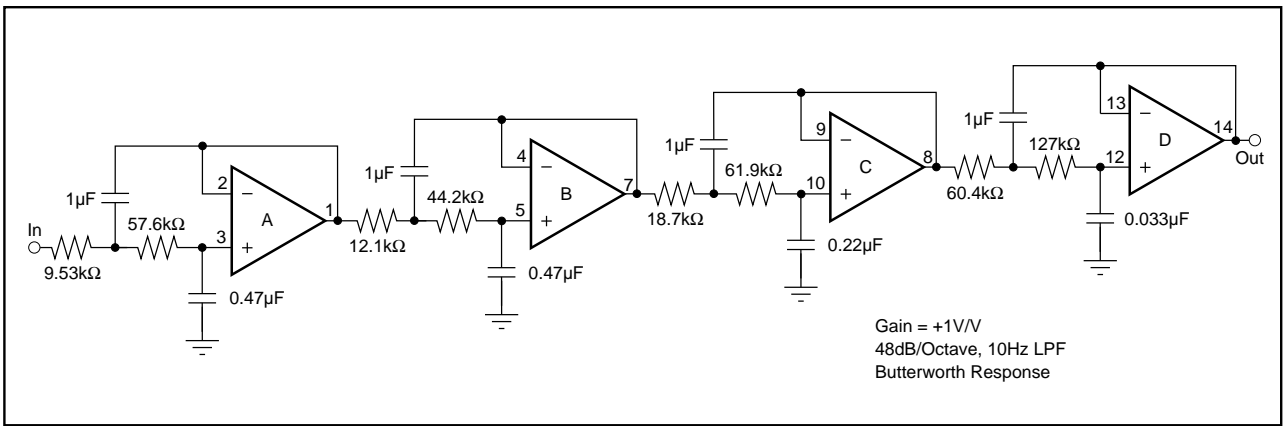


FIGURE 10. 8-Pole 10Hz Low-Pass Filter.

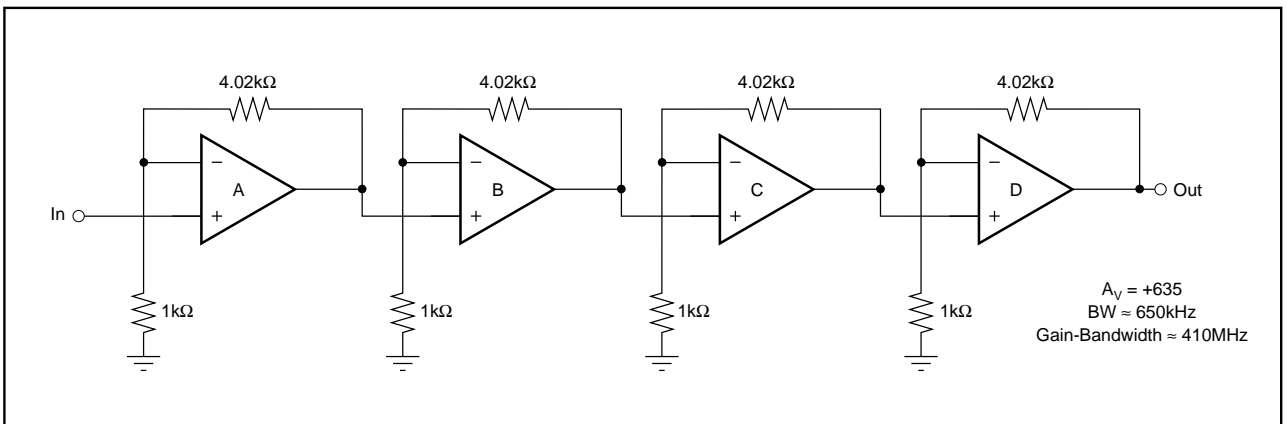


FIGURE 11. Wide-Band Amplifier.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA404AG	NRND	CDIP SB	JD	14	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA404AG	
OPA404BG	NRND	CDIP SB	JD	14	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA404BG	
OPA404KP	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA404KP	Samples
OPA404KPG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA404KP	Samples
OPA404KU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	0 to 70	OPA404KU	Samples
OPA404KU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	0 to 70	OPA404KU	Samples
OPA404SG	NRND	CDIP SB	JD	14	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA404SG	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



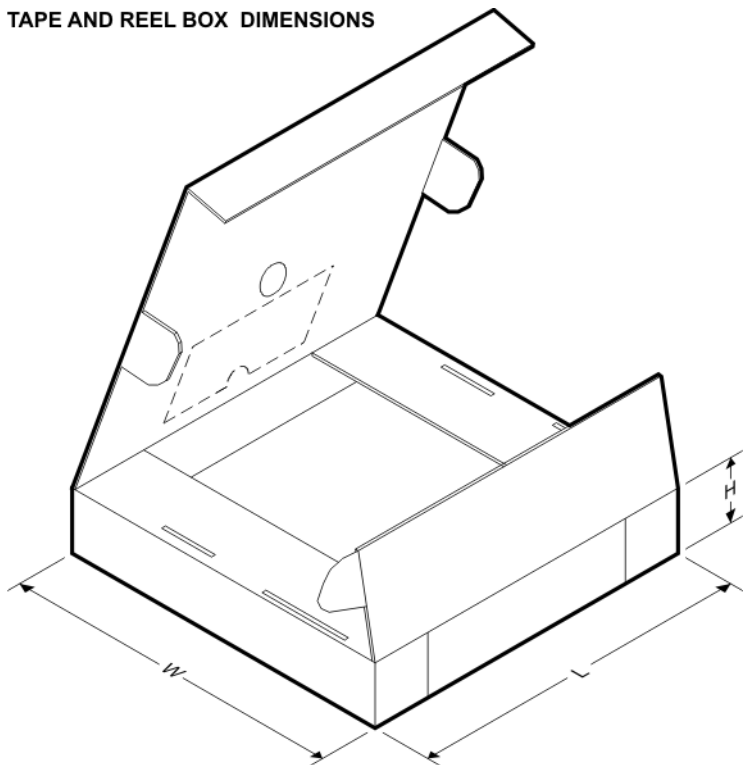
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA404KU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA404KU/1K	SOIC	DW	16	1000	367.0	367.0	38.0

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