P89LPC933/934/935/936

8-bit microcontroller with accelerated two-clock 80C51 core 4 kB/8 kB/16 kB 3 V byte-erasable flash with 8-bit ADCs

Rev. 8 — 12 January 2011 Product data sheet

1. General description

The P89LPC933/934/935/936 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC933/934/935/936 in order to reduce component count, board space, and system cost.

2. Features and benefits

2.1 Principal features

- 4 kB/8 kB/16 kB byte-erasable flash code memory organized into 1 kB/2 kB sectors and 64-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory. Both the P89LPC935 and P89LPC936 also include a 512-byte auxiliary on-chip RAM.
- 512-byte customer data EEPROM on chip allows serialization of devices, storage of setup parameters, etc. (P89LPC935/936).
- Dual 4-input multiplexed 8-bit A/D converters/DAC outputs (P89LPC935/936, single A/D on P89LPC933/934).Two analog comparators with selectable inputs and reference source.
- Two 16-bit counter/timers (each may be configured to toggle a port output upon timer overflow or to become a PWM output) and a 23-bit system timer that can also be used as an RTC.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I^2C-bus communication port and SPI communication port.
- Capture/Compare Unit (CCU) provides PWM, input capture, and output compare functions (P89LPC935/936).
- High-accuracy internal RC oscillator option allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 28-pin TSSOP, PLCC, and HVQFN packages with 23 I/O pins minimum and up to 26 I/O pins while using on-chip oscillator and reset options.

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC933/934/935/936 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

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3. Product comparison overview

Table 1 highlights the differences between the four devices. For a complete list of device features please see Section 2 “Features and benefits”.

Table 1. Product comparison overview

Device	Flash memory	Sector size	ADC1	ADC0	CCU	Data EEPROM
P89LPC933	4 kB	1 kB	X	-	-	-
P89LPC934	8 kB	1 kB	X	-	-	-
P89LPC935	8 kB	1 kB	X	X	X	X
P89LPC936	16 kB	2 kB	X	X	X	X

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC935FA	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2
P89LPC933HDH	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
P89LPC933FDH			
P89LPC934FDH			
P89LPC935FDH			
P89LPC936FDH			
P89LPC935FHN	HVQFN28	plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 6 × 6 × 0.85 mm	SOT788-1

4.1 Ordering options

Table 3. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC933HDH	4 kB	−40 °C to +125 °C	0 MHz to 18 MHz
P89LPC933FDH	4 kB	−40 °C to +85 °C	
P89LPC935FA	8 kB		
P89LPC934FDH			
P89LPC935FDH			
P89LPC935FHN			
P89LPC936FDH	16 kB		

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5. Block diagram

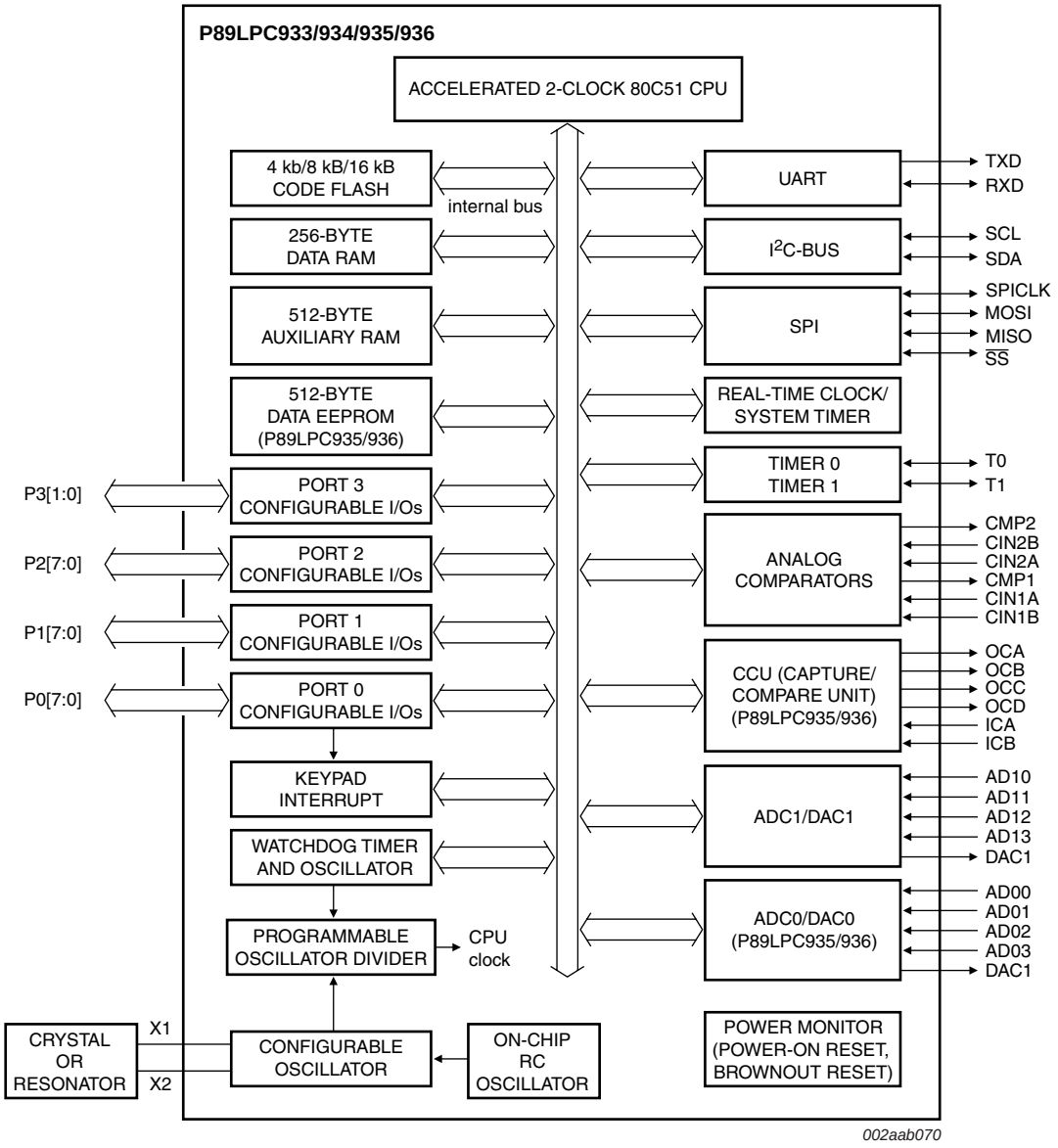

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

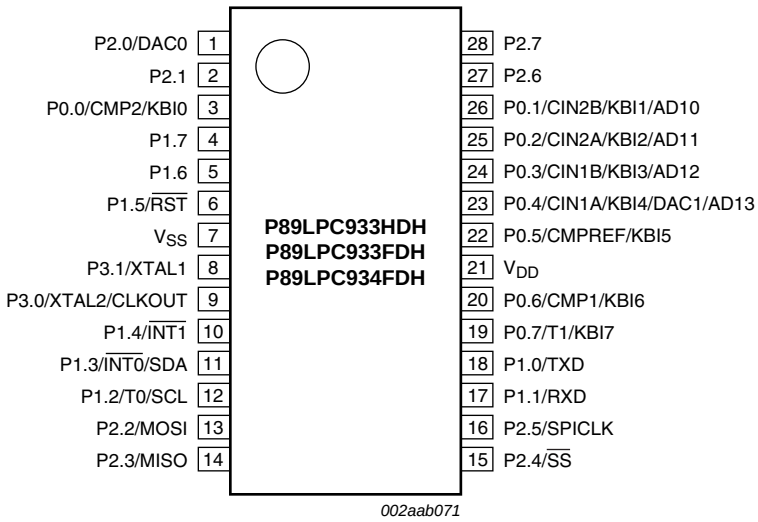

Fig 2. P89LPC933/934 TSSOP28 pin configuration

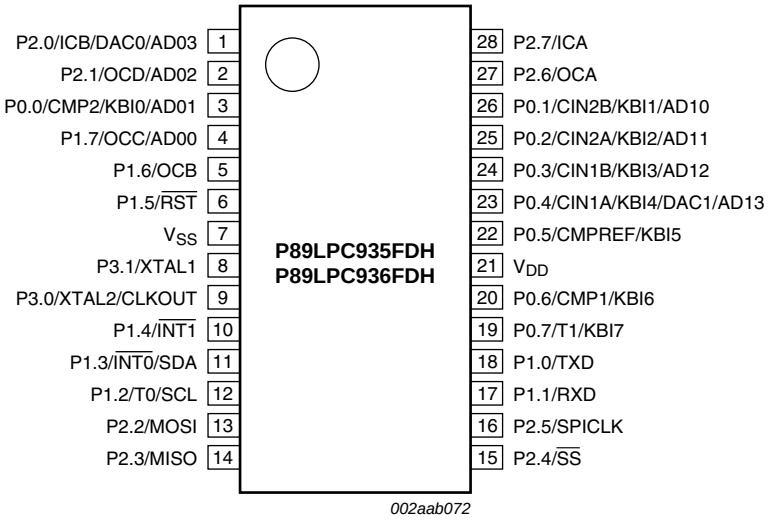

Fig 3. P89LPC935/936 TSSOP28 pin configuration

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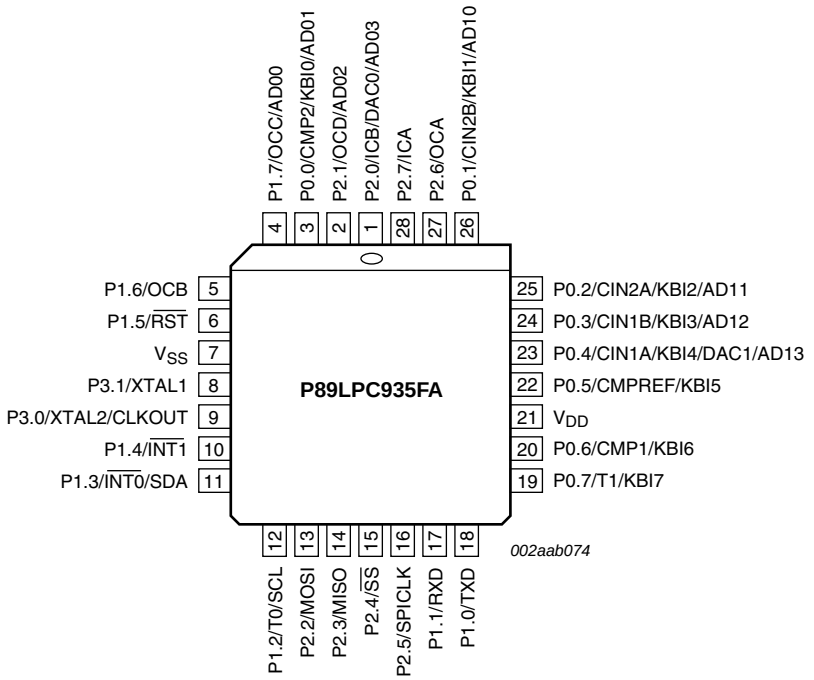

Fig 4. P89LPC935 PLCC28 pin configuration

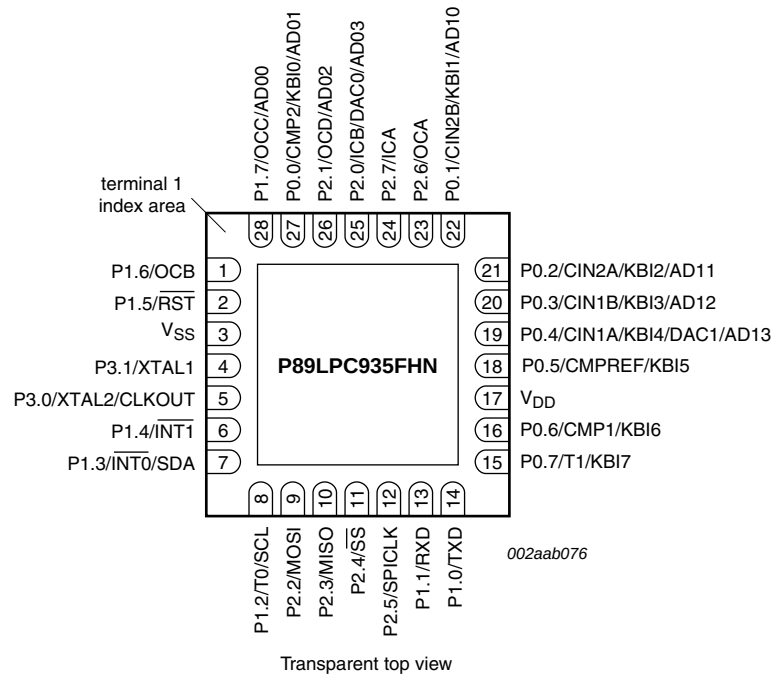

Fig 5. P89LPC935 HVQFN28 pin configuration

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6.2 Pin description

Table 4. Pin description

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.0 to P0.7			I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0/AD01	3	27	I/O	**P0.0 —** Port 0 bit 0.
			O	**CMP2 —** Comparator 2 output.
			I	**KBI0 —** Keyboard input 0.
			I	**AD01 —** ADC0 channel 1 analog input. (P89LPC935/936)
P0.1/CIN2B/ KBI1/AD10	26	22	I/O	**P0.1 —** Port 0 bit 1.
			I	**CIN2B —** Comparator 2 positive input B.
			I	**KBI1 —** Keyboard input 1.
			I	**AD10 —** ADC1 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD11	25	21	I/O	**P0.2 —** Port 0 bit 2.
			I	**CIN2A —** Comparator 2 positive input A.
			I	**KBI2 —** Keyboard input 2.
			I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD12	24	20	I/O	**P0.3 —** Port 0 bit 3.
			I	**CIN1B —** Comparator 1 positive input B.
			I	**KBI3 —** Keyboard input 3.
			I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ KBI4/DAC1/ AD13	23	19	I/O	**P0.4 —** Port 0 bit 4.
			I	**CIN1A —** Comparator 1 positive input A.
			I	**KBI4 —** Keyboard input 4.
			O	**DAC1 —** Digital-to-analog converter output 1.
			I	**AD13 —** ADC1 channel 3 analog input.
P0.5/ CMPREF/ KBI5	22	18	I/O	**P0.5 —** Port 0 bit 5.
			I	**CMPREF —** Comparator reference (negative) input.
			I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	20	16	I/O	**P0.6 —** Port 0 bit 6.
			O	**CMP1 —** Comparator 1 output.
			I	**KBI6 —** Keyboard input 6.
P0.7/T1/ KBI7	19	15	I/O	**P0.7 —** Port 0 bit 7.
			I/O	**T1 —** Timer/counter 1 external count input or overflow output.
			I	**KBI7 —** Keyboard input 7.

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Table 4. Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P1.0 to P1.7			I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 and P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	14	I/O	**P1.0 —** Port 1 bit 0.
			O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	17	13	I/O	**P1.1 —** Port 1 bit 1.
			I	**RXD —** Receiver input for the serial port.
P1.2/T0/SCL	12	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
			I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
			I/O	**SCL —** I^2C serial clock input/output.
P1.3/$\overline{\text{INT0}}$/SDA	11	7	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
			I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
			I/O	**SDA —** I^2C serial data input/output.
P1.4/$\overline{\text{INT1}}$	10	6	I	**P1.4 —** Port 1 bit 4.
			I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P1.5/$\overline{\text{RST}}$	6	2	I	**P1.5 —** Port 1 bit 5 (input only).
			I	**$\overline{\text{RST}}$ —** External reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until VDD has reached its specified level. When system power is removed VDD will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when VDD falls below the minimum specified operating voltage.**
P1.6/OCB	5	1	I/O	**P1.6 —** Port 1 bit 6.
			O	**OCB —** Output Compare B. (P89LPC935/936)
P1.7/OCC/AD00	4	28	I/O	**P1.7 —** Port 1 bit 7.
			O	**OCC —** Output Compare C. (P89LPC935/936)
			I	**AD00 —** ADC0 channel 0 analog input. (P89LPC935/936)

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Table 4. Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P2.0 to P2.7			I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 2 also provides various special functions as described below:
P2.0/ICB/ DAC0/AD03	1	25	I/O	**P2.0 —** Port 2 bit 0.
			I	**ICB —** Input Capture B. (P89LPC935/936)
			I	**DAC0 —** Digital-to-analog converter output.
			I	**AD03 —** ADC0 channel 3 analog input. (P89LPC935/936)
P2.1/OCD/ AD02	2	26	I/O	**P2.1 —** Port 2 bit 1.
			O	**OCD —** Output Compare D. (P89LPC935/936)
			I	**AD02 —** ADC0 channel 2 analog input. (P89LPC935/936)
P2.2/MOSI	13	9	I/O	**P2.2 —** Port 2 bit 2.
			I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	14	10	I/O	**P2.3 —** Port 2 bit 3.
			I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	15	11	I/O	**P2.4 —** Port 2 bit 4.
			I	**$\overline{SS}$ —** SPI Slave select.
P2.5/ SPICLK	16	12	I/O	**P2.5 —** Port 2 bit 5.
			I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6/OCA	27	23	I/O	**P2.6 —** Port 2 bit 6.
			O	**OCA —** Output Compare A. (P89LPC935/936)
P2.7/ICA	28	24	I/O	**P2.7 —** Port 2 bit 7.
			I	**ICA —** Input Capture A. (P89LPC935/936)

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Table 4. Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P3.0 to P3.1			I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 "Port configurations" and Table 11 "Static characteristics" for details. All pins have Schmitt trigger inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	9	5	I/O	**P3.0 —** Port 3 bit 0.
			O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
			O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	8	4	I/O	**P3.1 —** Port 3 bit 1.
			I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	7	3	I	**Ground:** 0 V reference.
V_{DD}	21	17	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

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7. Logic symbols

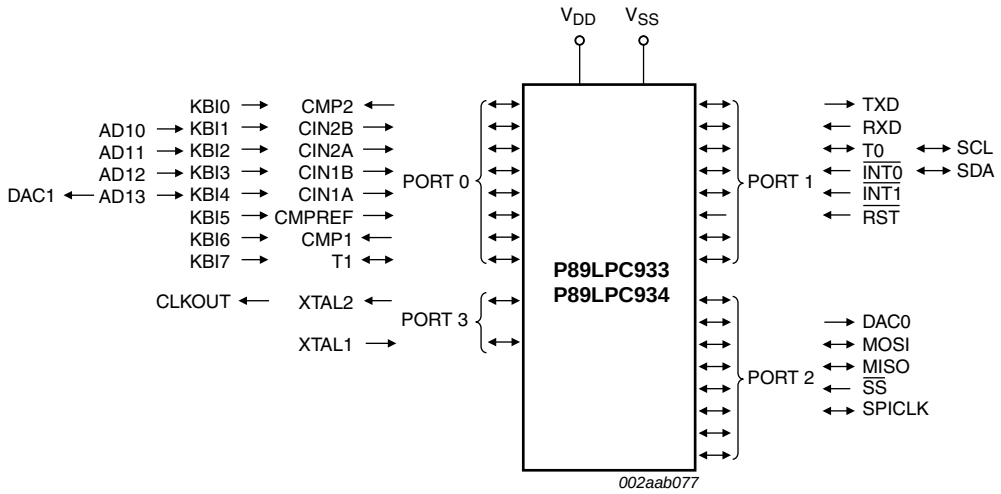

Fig 6. P89LPC933/934 logic symbol

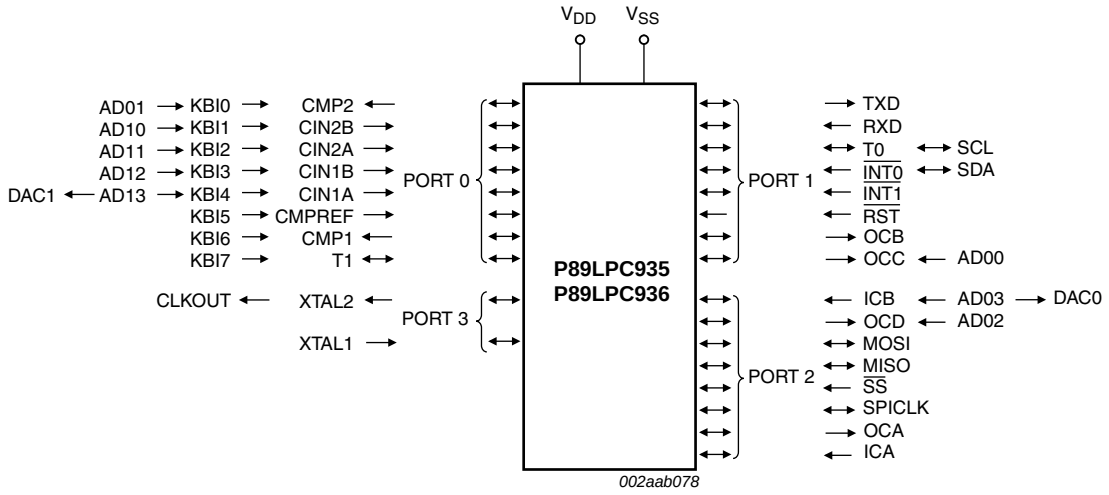

Fig 7. P89LPC935/936 logic symbol

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8. Functional description

Remark: Please refer to the P89LPC933/934/935/936 *User manual* for a more detailed functional description.

8.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', logic 0 or logic 1 can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with logic 0, but can return any value when read (even if it was written with logic 0). It is a reserved bit and may be used in future derivatives.
  - Logic 0 **must** be written with logic 0, and will return a logic 0 when read.
  - Logic 1 **must** be written with logic 1, and will return a logic 1 when read.

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Table 5. Special function registers - P89LPC933/934

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
		Bit address	E7	E6	E5	E4	E3	E2	E1
ACC*	Accumulator	E0H							
ADCON0	A/D control register 0	8EH	-	-	-	-	-	ENADC0	-
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11
ADINS	A/D input select	A3H	ADI13	ADI12	ADI11	ADI10	-	-	-
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	ENDAC0	BSA1
AD0DAT3	A/D_0 data register 3	F4H							
AD1BH	A/D_1 boundary high register	C4H							
AD1BL	A/D_1 boundary low register	BCH							
AD1DAT0	A/D_1 data register 0	D5H							
AD1DAT1	A/D_1 data register 1	D6H							
AD1DAT2	A/D_1 data register 2	D7H							
AD1DAT3	A/D_1 data register 3	F5H							
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-
		Bit address	F7	F6	F5	F4	F3	F2	F1
B*	B register	F0H							
BRGR0	Baud rate generator rate low	BEH							
BRGR1	Baud rate generator rate high	BFH							
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H							

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Table 5. Special function registers - P89LPC933/934 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
FMADRL	Program flash address low	E6H							
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1
FMDATA	Program flash data	E5H							
I2ADR	I^2C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**
I2CON*	I^2C control register	D8H	-	I2EN	STA	STO	SI	AA	-
I2DAT	I^2C data register	DAH							
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH							
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH							
I2STAT	I^2C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0
ICRAH	Input capture A register high	ABH							
ICRAL	Input capture A register low	AAH							
ICRBH	Input capture B register high	AFH							
ICRBL	Input capture B register low	AEH							
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	ESPI	EC	EKBI
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	PSPI	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	PSPIH	PCH	PKBIH

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Table 5. Special function registers - P89LPC933/934 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H							
KBPATN	Keypad pattern register	93H							
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD
		Bit address	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**
P2*	Port 2	A0H	-	-	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	-
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	SPPD	SPD
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC

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Table 5. Special function registers - P89LPC933/934 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
RTCH	Real-time clock register high	D2H							
RTCL	Real-time clock register low	D3H							
SADDR	Serial port address register	A9H							
SADEN	Serial port address enable	B9H							
SBUF	Serial Port data buffer register	99H							
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE
SP	Stack pointer	81H							
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-
SPDAT	SPI data register	E3H							
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF

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Table 5. Special function registers - P89LPC933/934 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses
			MSB
WDL	Watchdog load	C1H	
WFEED1	Watchdog feed 1	C2H	
WFEED2	Watchdog feed 2	C3H	

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits sinc purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictabl

[3] All ports are in input only (high-impedance) state after power-up.

[4] The RSTSRC register reflects the cause of the P89LPC933/934/935/936 reset. Upon a power-up reset, all reset source flags are cleared excep value is xx11 0000.

[5] The only reset source that affects these SFRs is power-on reset.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM regis

[7] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset Other resets will not affect WDTOF.

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Table 6. Special function registers - P89LPC935/936

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
		Bit address	E7	E6	E5	E4	E3	E2	E1
ACC*	Accumulator	E0H							
ADCON0	A/D control register 0	8EH	ENBI0	ENADCI 0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11
ADINS	A/D input select	A3H	ADI13	ADI12	ADI11	ADI10	ADI03	ADI02	ADI01
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	BNDI0	BURST0	SCC0
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	ENDAC0	BSA1
AD0BH	A/D_0 boundary high register	BBH							
AD0BL	A/D_0 boundary low register	A6H							
AD0DAT0	A/D_0 data register 0	C5H							
AD0DAT1	A/D_0 data register 1	C6H							
AD0DAT2	A/D_0 data register 2	C7H							
AD0DAT3	A/D_0 data register 3	F4H							
AD1BH	A/D_1 boundary high register	C4H							
AD1BL	A/D_1 boundary low register	BCH							
AD1DAT0	A/D_1 data register 0	D5H							
AD1DAT1	A/D_1 data register 1	D6H							
AD1DAT2	A/D_1 data register 2	D7H							
AD1DAT3	A/D_1 data register 3	F5H							
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-
		Bit address	F7	F6	F5	F4	F3	F2	F1
B*	B register	F0H							
BRGR0[2]	Baud rate generator rate low	BEH							
BRGR1[2]	Baud rate generator rate high	BFH							
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS
CCCRA	Capture compare A control register	EAH	ICECA2	ICECA1	ICECA0	ICESA	ICNFA	FCOA	OCMA1

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Table 6. Special function registers - P89LPC935/936 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
CCCRB	Capture compare B control register	EBH	ICECB2	ICECB1	ICECB0	ICESB	ICNFB	FCOB	OCMB1
CCCRC	Capture compare C control register	ECH	-	-	-	-	-	FCOC	OCMC1
CCCRD	Capture compare D control register	EDH	-	-	-	-	-	FCOD	OCMD1
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2
DEECON	Data EEPROM control register	F1H	EEIF	HVERR	ECTL1	ECTL0	-	-	-
DEEDAT	Data EEPROM data register	F2H							
DEEADR	Data EEPROM address register	F3H							
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H							
FMADRL	Program flash address low	E6H							
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1
FMDATA	Program flash data	E5H							
I2ADR	I^2C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**
I2CON*	I^2C control register	D8H	-	I2EN	STA	STO	SI	AA	-
I2DAT	I^2C data register	DAH							
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH							

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Table 6. Special function registers - P89LPC935/936 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH							
I2STAT	I^2C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0
ICRAH	Input capture A register high	ABH							
ICRAL	Input capture A register low	AAH							
ICRBH	Input capture B register high	AFH							
ICRBL	Input capture B register low	AEH							
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**
IEN1*	Interrupt enable 1	E8H	EADEE	EST	-	ECCU	ESPI	EC	EKBI
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**
IP1*	Interrupt priority 1	F8H	PADEE	PST	-	PCCU	PSPI	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	PAEEH	PSTH	-	PCCUH	PSPIH	PCH	PKBIH
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H							
KBPATN	Keypad pattern register	93H							
OCRAH	Output compare A register high	EFH							
OCRAL	Output compare A register low	EEH							
OCRBH	Output compare B register high	FBH							
OCRBL	Output compare B register low	FAH							

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Table 6. Special function registers - P89LPC935/936 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
OCRCH	Output compare C register high	FDH							
OCRCL	Output compare C register low	FCH							
OCRDH	Output compare D register high	FFH							
OCRDL	Output compare D register low	FEH							
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**
P1*	Port 1	90H	OCC	OCB	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD
	Bit address		**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	OCD
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD	DEEPD	VCPD	ADPD	I2PD	SPPD	SPD
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1

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Table 6. Special function registers - P89LPC935/936 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC
RTCH	Real-time clock register high	D2H							
RTCL	Real-time clock register low	D3H							
SADDR	Serial port address register	A9H							
SADEN	Serial port address enable	B9H							
SBUF	Serial Port data buffer register	99H							
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE
SP	Stack pointer	81H							
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-
SPDAT	SPI data register	E3H							
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0
TCR20*	CCU control register 0	C8H	PLEEN	HLTRN	HLTEN	ALTCD	ALTAB	TDIR2	TMOD21
TCR21	CCU control register 1	F9H	TCOU2	-	-	-	PLLDV.3	PLLDV.2	PLLDV.1
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TH2	CCU timer high	CDH							
TICR2	CCU interrupt control register	C9H	TOIE2	TOCIE2D	TOCIE2C	TOCIE2B	TOCIE2A	-	TICIE2B
TIFR2	CCU interrupt flag register	E9H	TOIF2	TOCF2D	TOCF2C	TOCF2B	TOCF2A	-	TICF2B
TISE2	CCU interrupt status encode register	DEH	-	-	-	-	-	ENCINT.2	ENCINT.1
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							

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Table 6. Special function registers - P89LPC935/936 *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
TL2	CCU timer low	CCH							
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1
TOR2H	CCU reload register high	CFH							
TOR2L	CCU reload register low	CEH							
TPCR2H	Prescaler control register high	CBH	-	-	-	-	-	-	TPCR2H.1
TPCR2L	Prescaler control register low	CAH	TPCR2L.7	TPCR2L.6	TPCR2L.5	TPCR2L.4	TPCR2L.3	TPCR2L.2	TPCR2L.1
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF
WDL	Watchdog load	C1H							
WFEED1	Watchdog feed 1	C2H							
WFEED2	Watchdog feed 2	C3H							

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits sinc purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] All ports are in input only (high-impedance) state after power-up.

[3] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictabl

[4] The RSTSRC register reflects the cause of the P89LPC933/934/935/936 reset. Upon a power-up reset, all reset source flags are cleared excep value is xx11 0000.

[5] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset Other resets will not affect WDTOF.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM regis

[7] The only reset source that affects these SFRs is power-on reset.

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8.2 Enhanced CPU

The P89LPC933/934/935/936 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.3 Clocks

8.3.1 Clock definitions

The P89LPC933/934/935/936 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 8) and can also be optionally divided to a slower frequency (see Section 8.8 “CCLK modification: DIVM register”).

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

8.3.2 CPU clock (OSCCLK)

The P89LPC933/934/935/936 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz.

8.3.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.3.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.3.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

8.3.6 Clock output

The P89LPC933/934/935/936 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator,

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external clock input on X1) and if the RTC is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC933/934/935/936. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

8.4 On-chip RC oscillator option

The P89LPC933/934/935/936 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz $\pm$ 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies.

8.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

8.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2 pin may be used as a standard port pin or a clock output. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until VDD has reached its specified level. When system power is removed VDD will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when VDD falls below the minimum specified operating voltage.**

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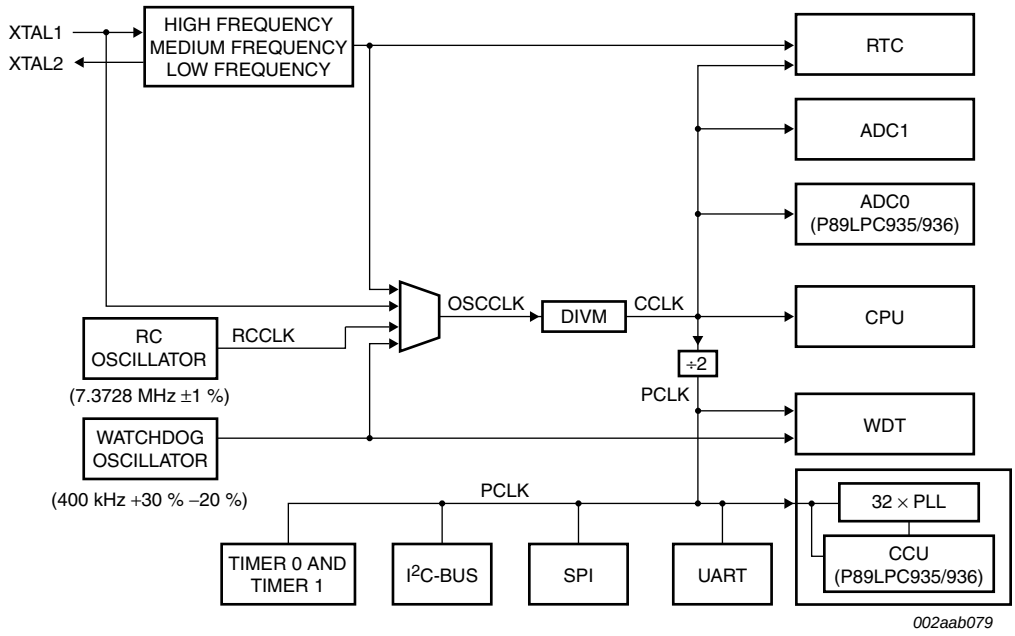

Fig 8. Block diagram of oscillator control

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8.7 CCLK wake-up delay

The P89LPC933/934/935/936 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

8.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.9 Low power select

The P89LPC933/934/935/936 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.10 Memory organization

The various P89LPC933/934/935/936 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA (P89LPC935/936)

  ‘External’ Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC935/936 has 512 bytes of on-chip XDATA memory.

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- CODE

  64 kB of code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC933/934/935/936 have 4 KB/8 kB/16 kB of on-chip Code memory.

The P89LPC935/936 also has 512 bytes of on-chip data EEPROM that is accessed via SFRs (see Section 8.27 “Data EEPROM (P89LPC935/936)”).

8.11 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 7.

Table 7. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary (‘External Data’) on-chip memory that is accessed using the MOVX instructions (P89LPC935/936)	512

8.12 Interrupts

The P89LPC933/934/935/936 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC933/934/935/936 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/Real-Time clock, I^2C-bus, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write/ADC completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking.

Remark: The arbitration ranking is only used to resolve pending requests of the same priority level.

8.12.1 External interrupt inputs

The P89LPC933/934/935/936 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

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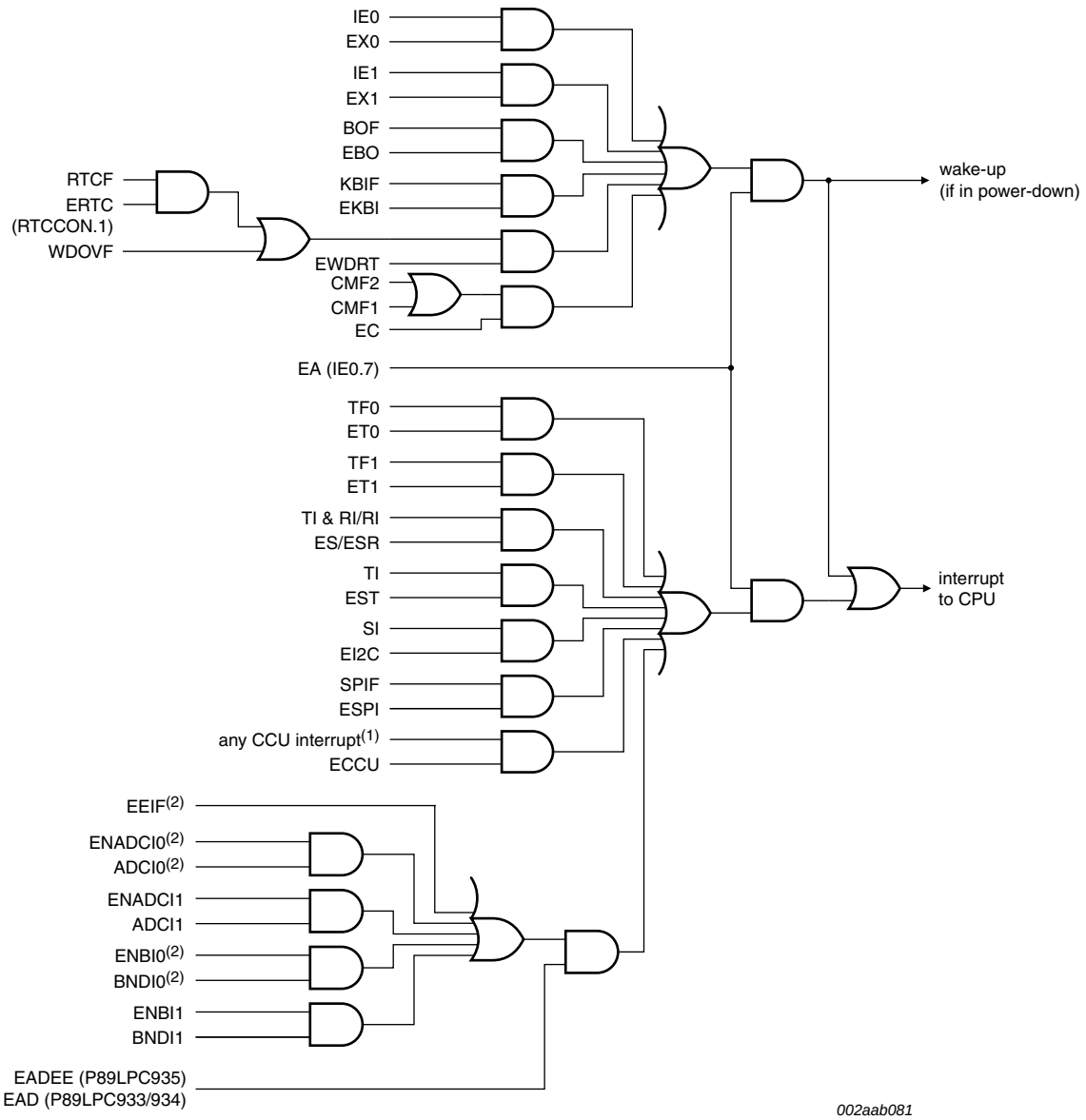
These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC933/934/935/936 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.15 “Power reduction modes” for details.



(1) See Section 8.19 “CCU (P89LPC935/936)”

(2) P89LPC935/936

Fig 9. Interrupt sources, interrupt enables, and power-down wake-up sources

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8.13 I/O ports

The P89LPC933/934/935/936 has four I/O ports: Port 0, Port 1, Port 2, and Port 3. Ports 0, 1 and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 8.

Table 8. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported[1]	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported[1]	23

[1] Required for operation above 12 MHz.

8.13.1 Port configurations

All but three I/O port pins on the P89LPC933/934/935/936 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

8.13.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC933/934/935/936 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

8.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

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An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

8.13.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

8.13.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt trigger input that also has a glitch suppression circuit.

8.13.2 Port 0 analog functions

The P89LPC933/934/935/936 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

8.13.3 Additional port features

After power-up, all pins are in Input-Only mode.

Remark: Please note that this is different from the LPC76x series of devices.

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC933/934/935/936 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 11 “Static characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.14 Power monitoring functions

The P89LPC933/934/935/936 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

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8.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 11 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC933/934/935/936 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 11 “Static characteristics” for specifications.

8.14.2 Power-on detection

The power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.15 Power reduction modes

The P89LPC933/934/935/936 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

8.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC933/934/935/936 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: brownout detect, watchdog timer, Comparators (note that Comparators can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

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8.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

8.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit. When this pin functions as a reset input, an internal pull-up resistance is connected (see Table 11 “Static characteristics”).

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1).
- Power-on detect.
- Brownout detect.
- Watchdog timer.
- Software reset.
- UART break character detect reset.

For every reset source, there is a flag in the reset register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.16.1 Reset vector

Following reset, the P89LPC933/934/935/936 will fetch instructions from either address 0000H or the boot address. The boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see P89LPC933/934/935/936 *User manual*). Otherwise, instructions will be fetched from address 0000H.

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8.17 Timers/counters 0 and 1

The P89LPC933/934/935/936 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'timer' function, the register is incremented every machine cycle.

In the 'counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both timers/counters. Mode 3 is different.

8.17.1 Mode 0

Putting either timer into Mode 0 makes it look like an 8048 timer, which is an 8-bit counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.17.3 Mode 2

Mode 2 configures the timer register as an 8-bit counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.17.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.17.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.18 RTC/system timer

The P89LPC933/934/935/936 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is

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not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

8.19 CCU (P89LPC935/936)

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- Four compare/PWM outputs with selectable polarity.
- Symmetrical/asymmetrical PWM selection.
- Two capture inputs with event counter and digital noise rejection filter.
- Seven interrupts with common interrupt vector (one overflow, two capture, four compare).
- Safe 16-bit read/write via shadow registers.

8.19.1 CCU clock

The CCU runs on the CCUCLK, which is either PCLK in basic timer mode, or the output of a Phase-Locked Loop (PLL). The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

8.19.2 CCUCLK prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

8.19.3 Basic timer operation

The timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU timer may also be used as an 8-bit up/down timer.

8.19.4 Output compare

There are four output compare channels A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

8.19.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input

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Capture Noise Filter bit. If set, the capture logic needs to see four consecutive samples of the same value in order to recognize an edge as a capture event. An event counter can be set to delay a capture by a number of capture events.

8.19.6 PWM operation

PWM operation has two main modes, symmetrical and asymmetrical.

In asymmetrical PWM operation the CCU timer operates in down-counting mode regardless of the direction control bit.

In symmetrical mode, the timer counts up/down alternately. The main difference from basic timer operation is the operation of the compare module, which in PWM mode is used for PWM waveform generation.

As with basic timer operation, when the PWM (compare) pins are connected to the compare logic, their logic state remains unchanged. However, since bit FCO is used to hold the halt value, only a compare event can change the state of the pin.

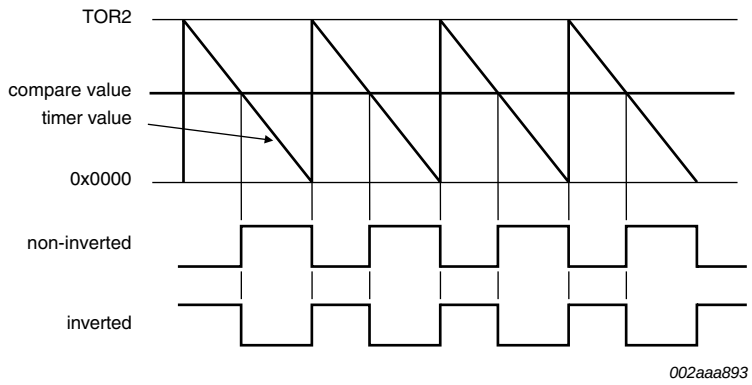

Fig 10. Asymmetrical PWM, down-counting mode

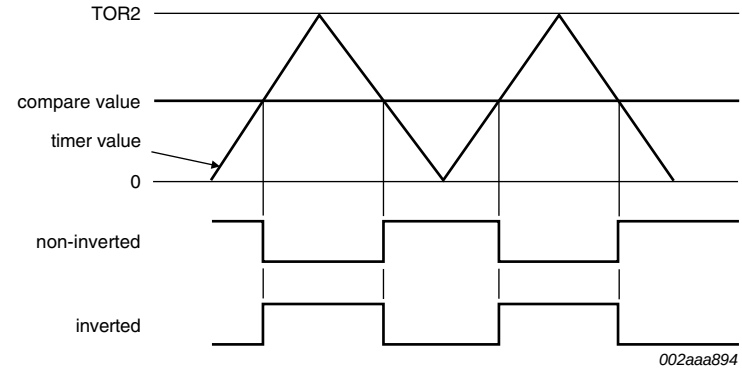

Fig 11. Symmetrical PWM

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8.19.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.

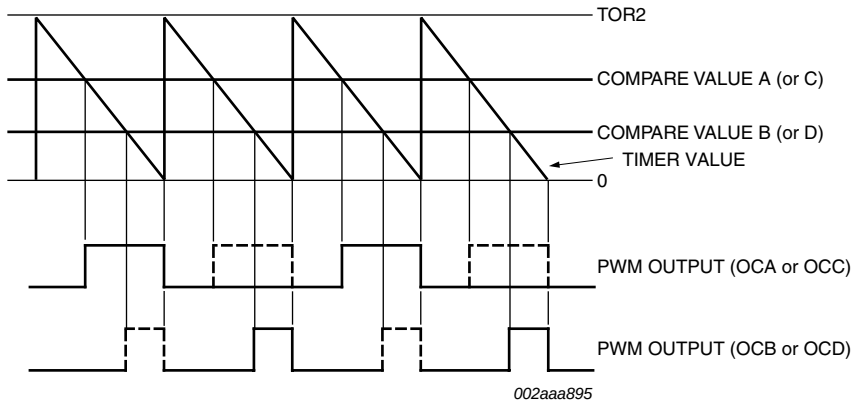

Fig 12. Alternate output mode

8.19.8 PLL operation

The PWM module features a PLL that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal from 0.5 MHz to 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor from 1 to 16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in Equation 1.

$$\text{PLL frequency} = \frac{\text{PCLK}}{(N+1)} \quad (1)$$

Where: N is the value of PLLDV.3 to PLLDV.0.

Since N ranges from 0 to 15, the CCLK frequency can be in the range of PCLK to $^{PCLK}/_{16}$.

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8.19.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

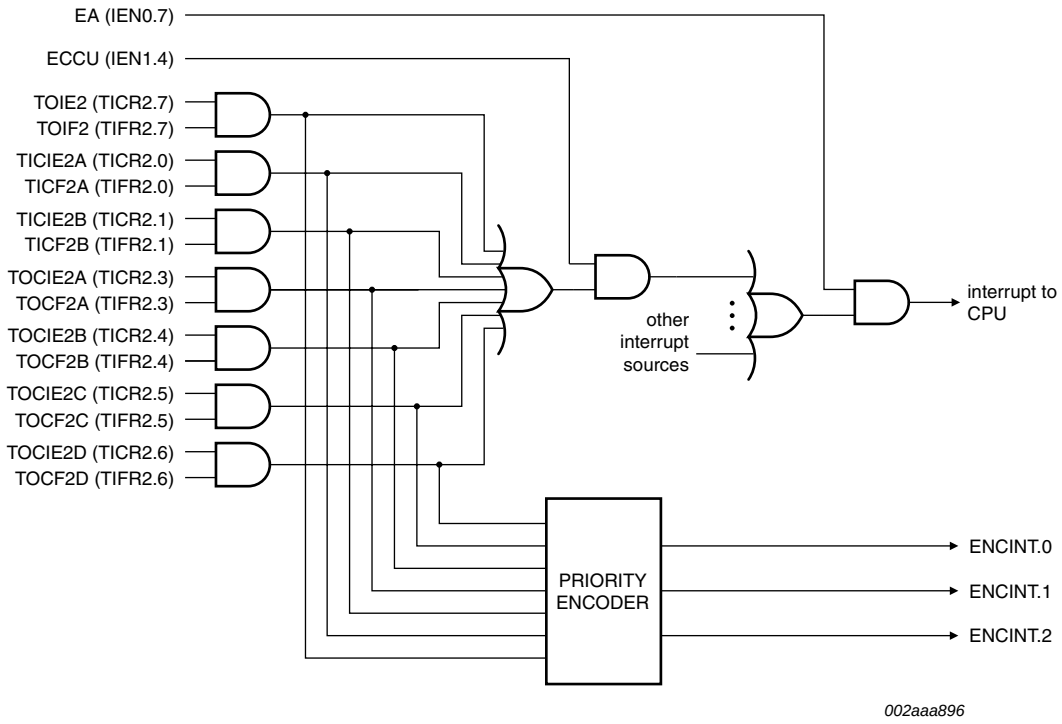

Fig 13. Capture/compare unit interrupts

8.20 UART

The P89LPC933/934/935/936 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC933/934/935/936 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU $^{clock}/_{32}$ or CPU $^{clock}/_{16}$.

8.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

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8.20.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 8.20.5 “Baud rate generator and selection”).

8.20.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is not saved. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.20.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 8.20.5 “Baud rate generator and selection”).

8.20.5 Baud rate generator and selection

The P89LPC933/934/935/936 enhanced UART has an independent baud rate generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 14). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent baud rate generator uses CCLK.

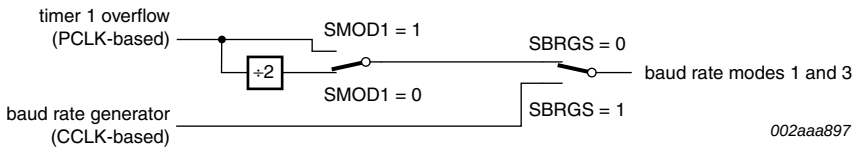

Fig 14. Baud rate sources for UART (Modes 1, 3)

8.20.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

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8.20.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

8.20.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

8.20.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.20.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

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8.21 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 15. The P89LPC933/934/935/936 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

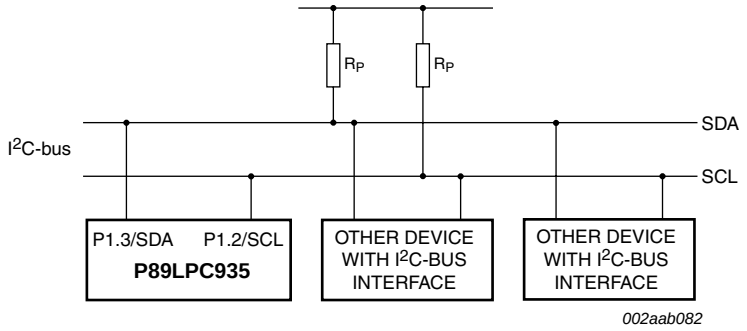

Fig 15. I²C-bus configuration

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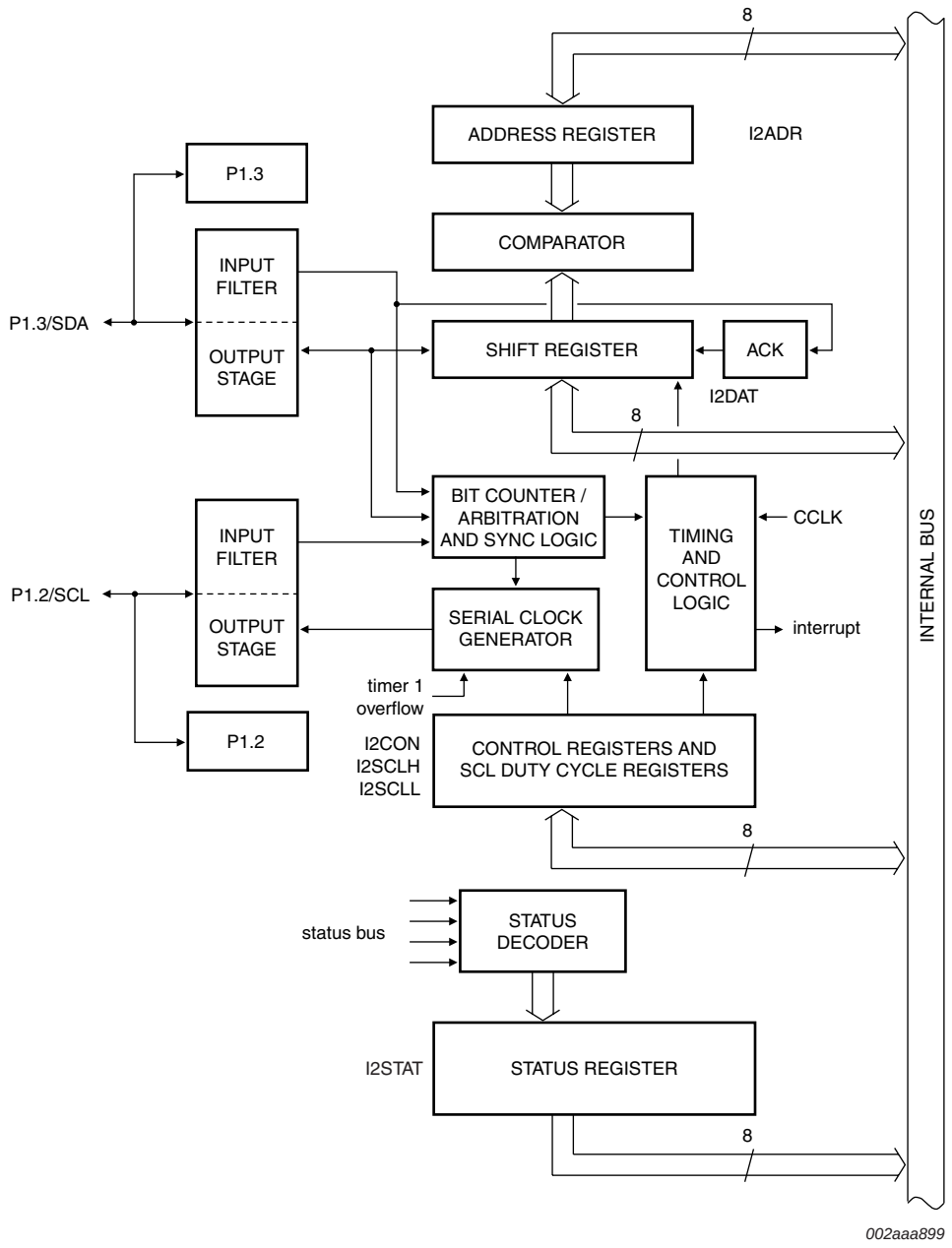

Fig 16. I²C-bus serial interface block diagram

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8.22 SPI

The P89LPC933/934/935/936 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in Master mode or up to 2 Mbit/s in Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

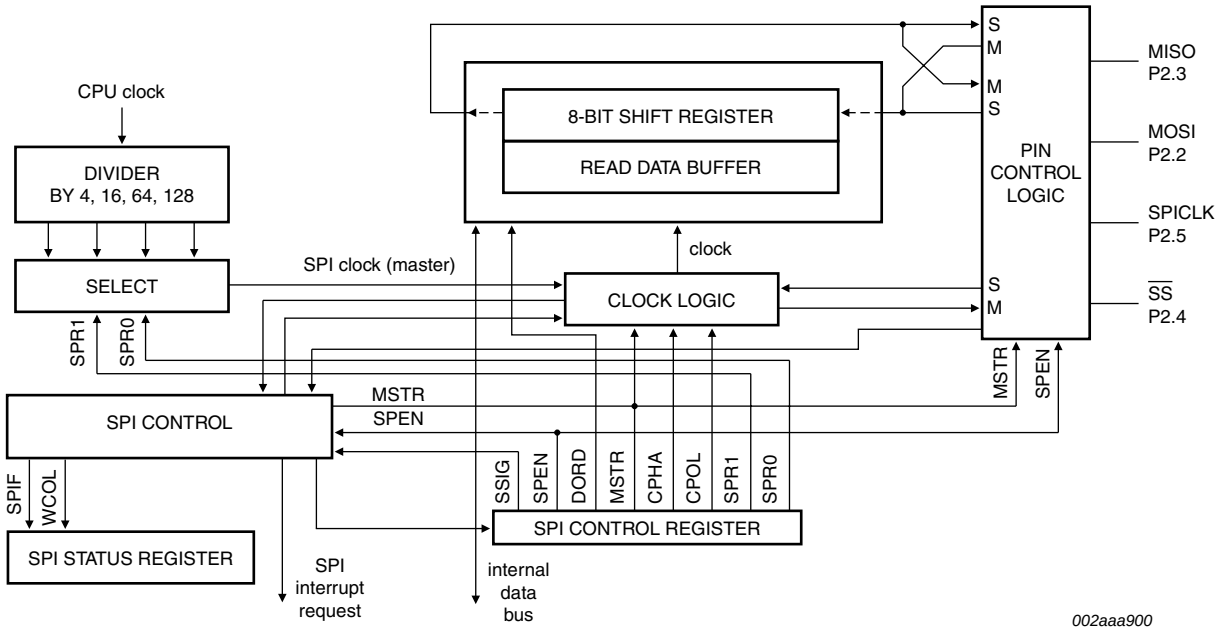

Fig 17. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 18 through Figure 20.

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8.22.1 Typical SPI configurations

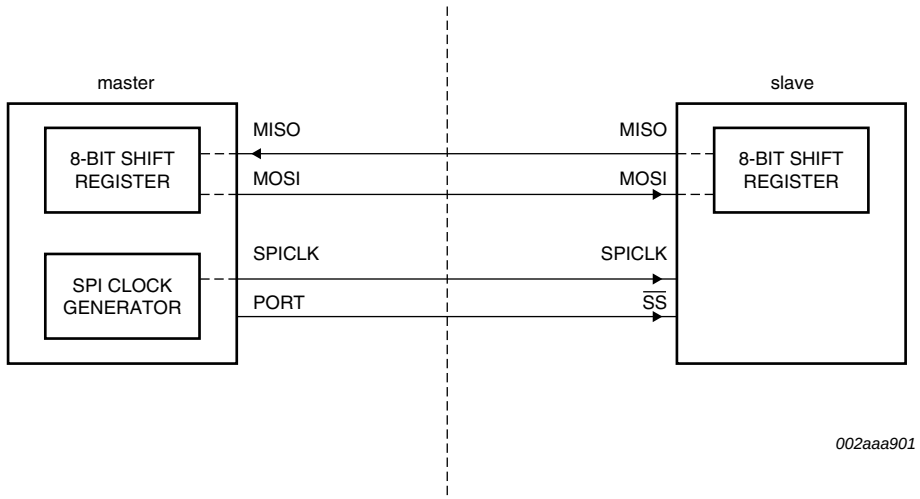

Fig 18. SPI single master single slave configuration

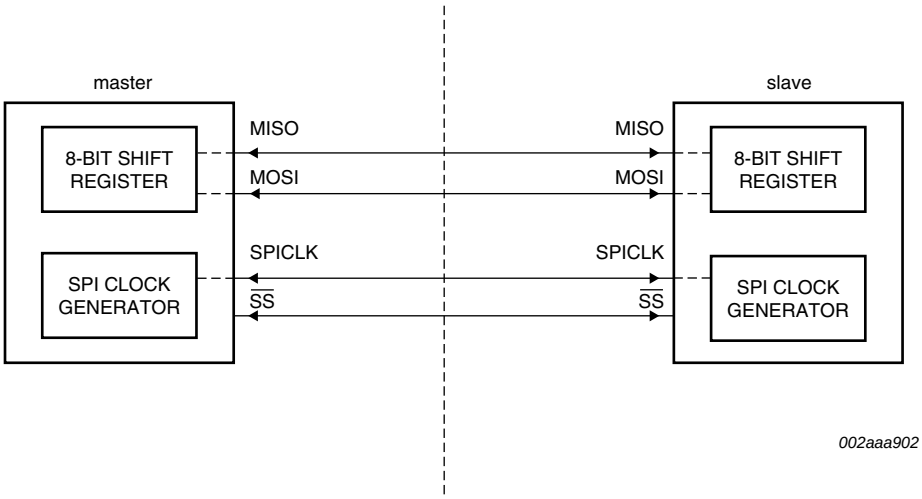

Fig 19. SPI dual device configuration, where either can be a master or a slave

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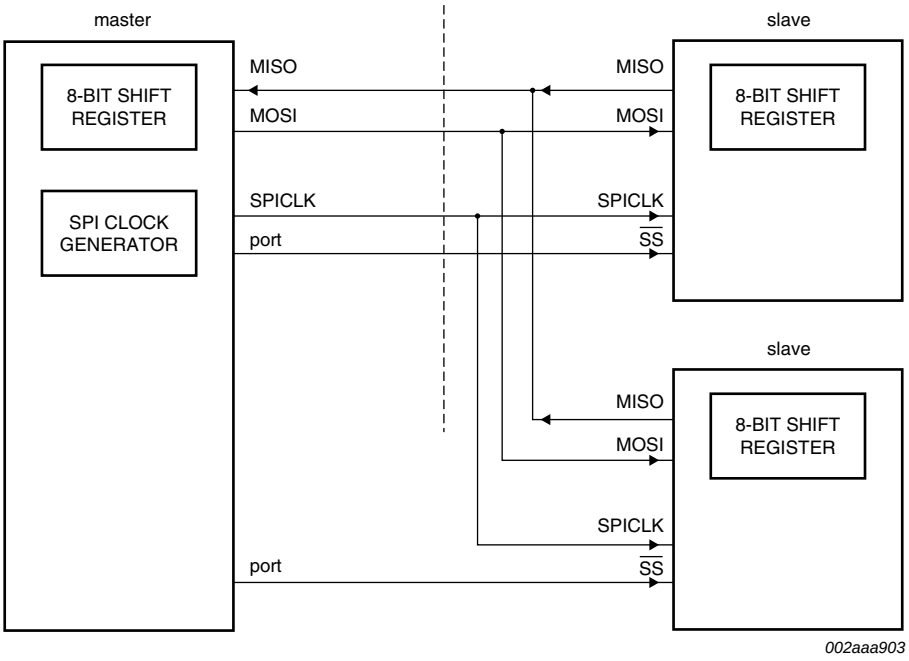

Fig 20. SPI single master multiple slaves configuration

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8.23 Analog comparators

Two analog comparators are provided on the P89LPC933/934/935/936. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 21. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, COn, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFn. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFn, after disabling the comparator.

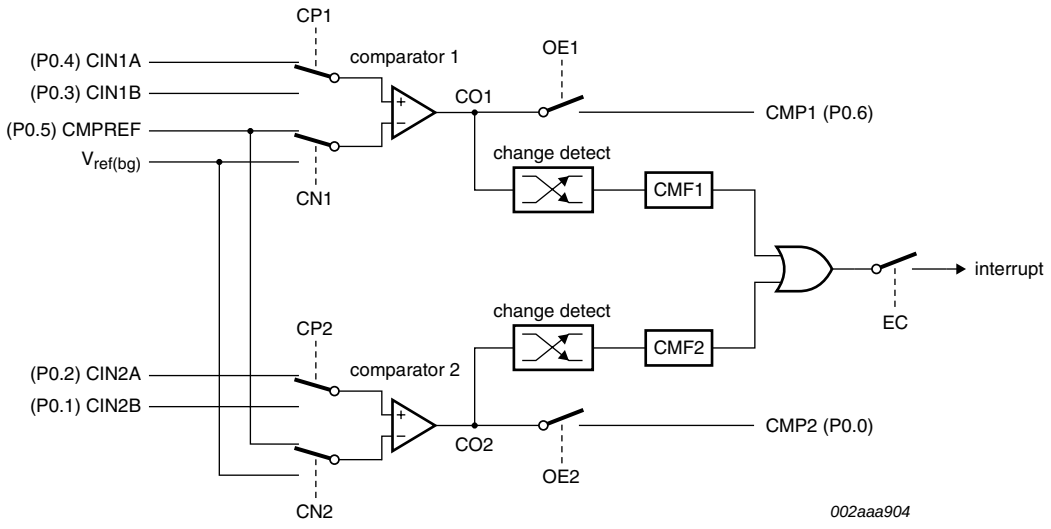

Fig 21. Comparator input and output connections

8.23.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 10 %.

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8.23.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

8.23.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.24 Keypad interrupt

The Keypad Interrupt (KBI) function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

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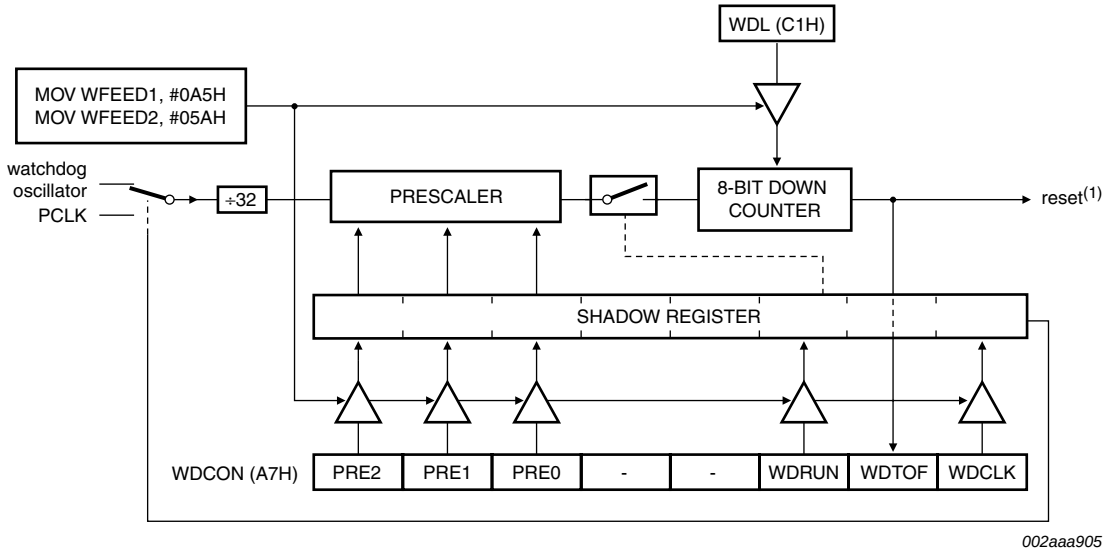
8.25 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 22 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few μs to a few seconds. Please refer to the P89LPC933/934/935/936 *User manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 22. Watchdog timer in Watchdog mode (WDTE = 1)

8.26 Additional features

8.26.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.26.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

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8.27 Data EEPROM (P89LPC935/936)

The P89LPC935/936 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- **Byte mode:** In this mode, data can be read and written one byte at a time.
- **Row fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- **Sector fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

8.28 Flash program memory

8.28.1 General description

The P89LPC933/934/935/936 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB or 2 kB depending on the device) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC933/934/935/936 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC933/934/935/936 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

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8.28.3 Flash organization

The program memory consists of eight 2 kB sectors on the P89LPC936 device, eight 1 kB sectors on the P89LPC934/935 devices, and four 1 kB sectors on the P89LPC933 device. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

8.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.28.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock - serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

8.28.6 In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC933/934/935/936 through a two-wire serial interface. The Philips ICP facility has made ICP in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC933/934/935/936 *User manual*.

8.28.7 In-application programming

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips IAP has made IAP in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The boot ROM occupies the program memory space at the top of the address space from FF00H to FFEFH, thereby not conflicting with the user program memory space.

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In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC933/934/935/936 *User manual*.

8.28.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC933/934/935/936 through the serial port. This firmware is provided by Philips and embedded within each P89LPC933/934/935/936 device. The Philips ISP facility has made ISP in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

8.28.9 Power-on reset code execution

The P89LPC933/934/935/936 contains two special flash elements: the boot vector and the boot status bit. Following reset, the P89LPC933/934/935/936 examines the contents of the boot status bit. If the boot status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the boot status bit is set to a value other than zero, the contents of the boot vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 9 shows the factory default boot vector settings for these devices.

Remark: These settings are different than the original P89LPC932. Tools designed to support the P89LPC933/934/935/936 should be used to program this device, such as Flash Magic version 1.98, or later.

A factory-provided boot loader is preprogrammed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user.

Remark: Users who wish to use this loader should take precautions to avoid erasing the sector that contains this boot loader. Instead, the page erase function can be used to erase the pages located in this sector which are not used by the boot loader.

A custom boot loader can be written with the boot vector set to the custom boot loader, if desired.

Table 9. Default boot vector values and ISP entry points

Device	Default boot vector	Default boot loader entry point	Default boot loader code range	Boot sector range
P89LPC933	0FH	0F00H	0E00H to 0FFFH	0C00H to 0FFFH
P89LPC934	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH
P89LPC935	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH
P89LPC936	3FH	3F00H	3E00H to 3FFFH	3C00H to 3FFFH

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8.28.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC933/934/935/936 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector is changed, it will no longer point to the factory preprogrammed ISP boot loader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

8.29 User configuration bytes

Some user-configurable features of the P89LPC933/934/935/936 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC933/934/935/936 *User manual* for additional details.

8.30 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC933/934/935/936 device. Each byte corresponds to one sector. Please see the P89LPC933/934/935/936 *User manual* for additional details.

9. A/D converter

9.1 General description

The P89LPC935/936 have two 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter modules sharing common control logic. The P89LPC933/934 have a single 8-bit, 4-channel multiplexed analog-to-digital converter and an additional DAC module. A block diagram of the A/D converter is shown in Figure 23. Each A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the SAR drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

9.2 Features and benefits

- Two (P89LPC935/936) 8-bit, 4-channel multiplexed input, successive approximation A/D converters with common control logic (one A/D on the P89LPC933/934).
- Four result registers for each A/D.
- Six operating modes:
  - Fixed channel, single conversion mode.
  - Fixed channel, continuous conversion mode.
  - Auto scan, single conversion mode.
  - Auto scan, continuous conversion mode.
  - Dual channel, continuous conversion mode.
  - Single step mode.
- Four conversion start modes:
  - Timer triggered start.

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- Start immediately.
- Edge triggered.
- Dual start immediately (P89LPC935/936).

- 8-bit conversion time of ≥3.9 μs at an A/D clock of 3.3 MHz.
- Interrupt or polled operation.
- Boundary limits interrupt.
- DAC output to a port pin with high output impedance.
- Clock divider.
- Power-down mode.

9.3 Block diagram

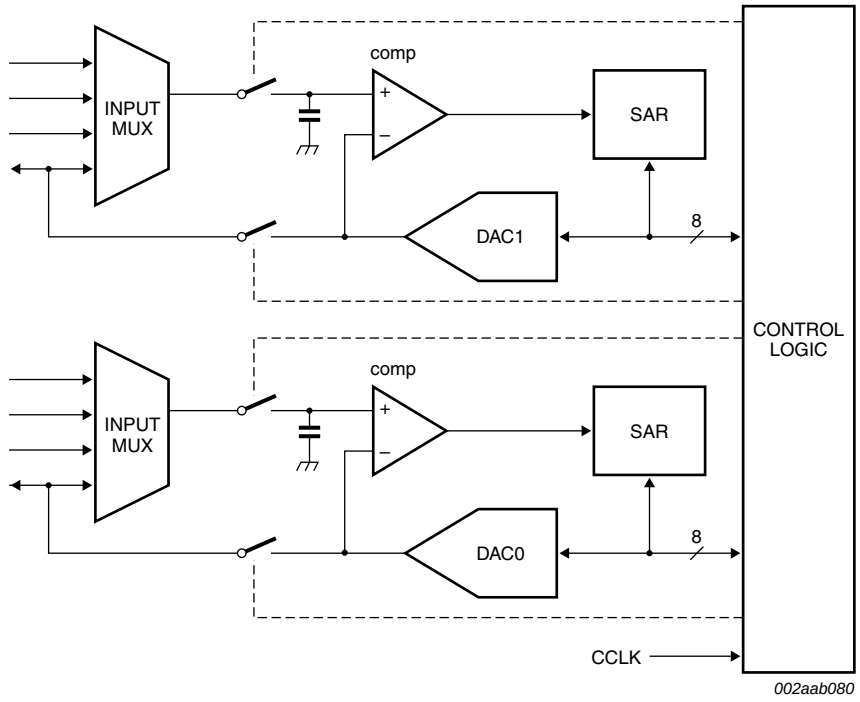

Fig 23. ADC block diagram

9.4 A/D operating modes

9.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

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9.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in result register, ADxDAT0. The result of the conversion of the second channel is placed in result register, ADxDAT1. The first channel is again converted and its result stored in ADxDAT2. The second channel is again converted and its result placed in ADxDAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

9.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

9.5 Conversion start modes

9.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

9.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all A/D operating modes.

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9.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

9.5.4 Dual start immediately (P89LPC935/936)

Programming this mode starts a synchronized conversion of both A/D converters. This start mode is available in all A/D operating modes. Both A/D converters must be in the same operating mode. In the continuous conversion modes, both A/D converters must select an identical number of channels. Any trigger of either A/D will start a simultaneous conversion of both A/Ds.

9.6 Boundary limits interrupt

Each of the A/D converters has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

9.7 DAC output to a port pin with high output impedance

Each A/D converter's DAC block can be output to a port pin. In this mode, the ADxDAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC (written to ADxDAT3), the DAC output will appear on the channel 3 pin.

9.8 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

9.9 Power-down and Idle mode

In Idle mode the A/C converter, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

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10. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	100	mA
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pin to V_{SS}	-	V_{DD} + 0.5	V
V_n	voltage on any other pin	except XTAL1, XTAL2 to V_{SS}	–0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 10:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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11. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	11	18	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	3.25	5	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	5	7	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.6 V; voltage comparators powered down	[2]	-	55	80	µA
$I_{DD(tpd)}$	total Power-down mode supply current	all devices except P89LPC933HDH; V_{DD} = 3.6 V	[3]	-	1	5	µA
		P89LPC933HDH only; V_{DD} = 3.6 V	[3]	-	-	25	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{POR}	power-on reset voltage			-	-	0.5	V
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z	[4]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V to 3.6 V all ports, all modes except high-Z		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 µA; V_{DD} = 2.4 V to 3.6 V; all ports, quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V to 3.6 V; all ports, push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −10 mA; V_{DD} = 3.6 V; all ports, push-pull mode		-	3.2	-	V
V_{xtal}	crystal voltage	on XTAL1, XTAL2 pins; with respect to V_{SS}		−0.5	-	+4.0	V
V_n	voltage on any other pin	except XTAL1, XTAL2, V_{DD}; with respect to V_{SS}	[5]	−0.5	-	+5.5	V
C_{iss}	input capacitance		[6]	-	-	15	pF

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Table 11. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{IL}	LOW-level input current	V_I = 0.4 V	[7]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}$, V_{IH} or $V_{th(HL)}$	[8]	-	-	±10	µA
I_{THL}	HIGH-LOW transition current	all ports; V_I = 1.5 V at V_{DD} = 3.6 V	[9]	−30	-	−450	µA
$R_{RST_N(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0		2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage			1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 10 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

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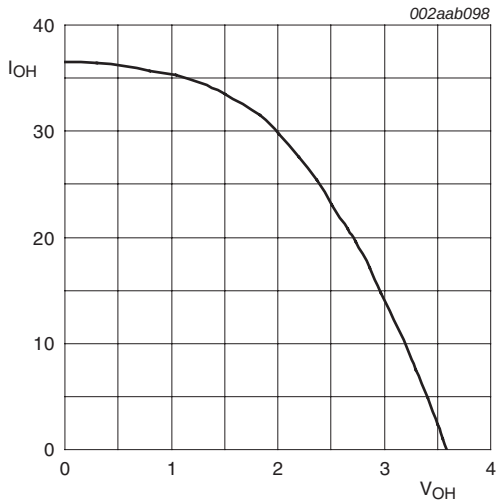
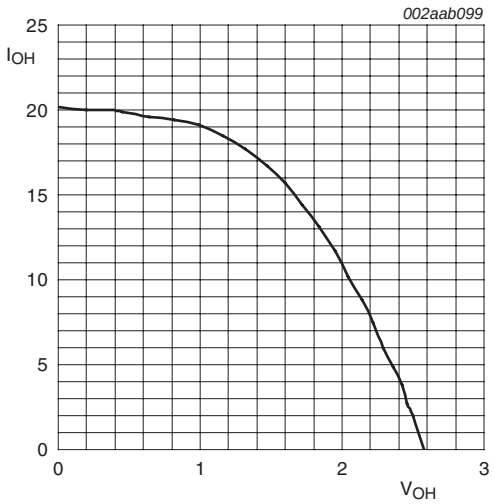
11.1 I_{OH} as a function of V_{OH}



a. T_{amb} = 25 °C; V_{DD} = 3.6 V; push-pull mode



b. T_{amb} = 25 °C; V_{DD} = 2.6 V; push-pull mode

Fig 24. I_{OH} as a function of V_{OH} (typical values)

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12. Dynamic characteristics

Table 12. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 27	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 27	33	$T_{cy(CLK)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time	see Figure 27	33	$T_{cy(CLK)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time	see Figure 27	-	8	-	8	ns
t_{CHCL}	clock fall time	see Figure 27	-	8	-	8	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 25	$16T_{cy(CLK)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 25	$13T_{cy(CLK)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 25	-	$T_{cy(CLK)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 25	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 25	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	2.0	MHz
	master		-	$^{CCLK}/_{4}$	-	3.0	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 28, 29, 30					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 29, 30					
	slave		250	-	250	-	ns

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Table 12. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
t_{SPILAG}	SPI enable lag time	see Figure 29, 30					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 29, 30					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 29, 30					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 26, 28, 29, 30					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 26, 28, 29, 30	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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Table 13. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency		7.189	7.557	7.189	7.557	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(CLK)}$	clock cycle	see Figure 27	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{\text{RST}}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{\text{RST}}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{\text{RST}}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{\text{RST}}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 27	22	$T_{cy(CLK)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 27	22	$T_{cy(CLK)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 27	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 27	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 25	$16T_{cy(CLK)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 25	$13T_{cy(CLK)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 25	-	$T_{cy(CLK)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 25	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 25	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 26, 28, 29, 30					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 29, 30					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 29, 30					
	slave		250	-	250	-	ns

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Table 13. Dynamic characteristics (18 MHz) *…continued*

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 26, 28, 29, 30					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 26, 28, 29, 30					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 29, 30					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 29, 30					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 26, 28, 29, 30					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 26, 28, 29, 30	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 26, 28, 29, 30					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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12.1 Waveforms

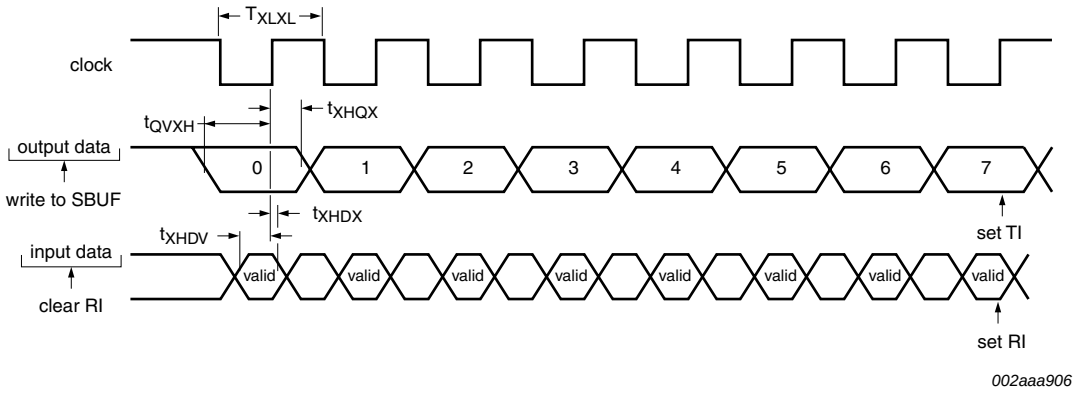

Fig 25. Shift register mode timing

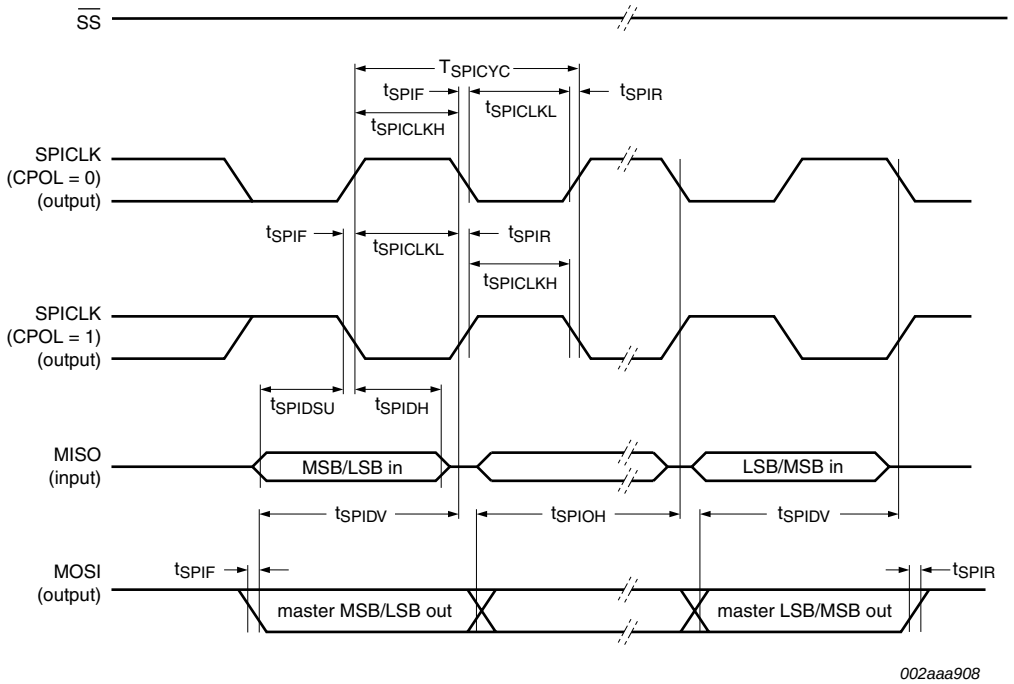

Fig 26. SPI master timing (CPHA = 0)

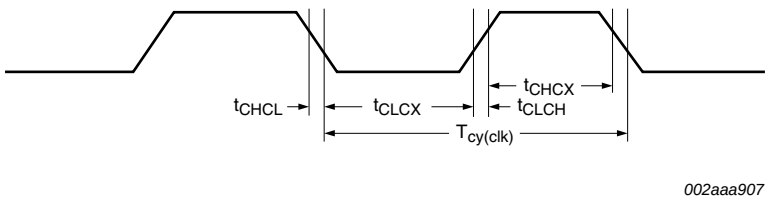

Fig 27. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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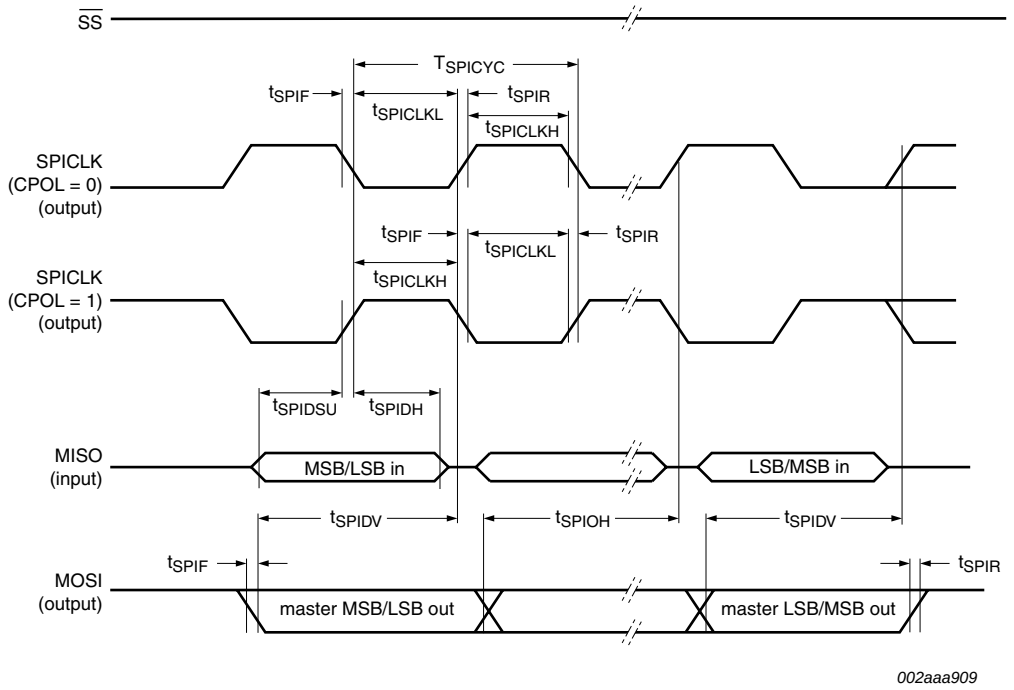

Fig 28. SPI master timing (CPHA = 1)

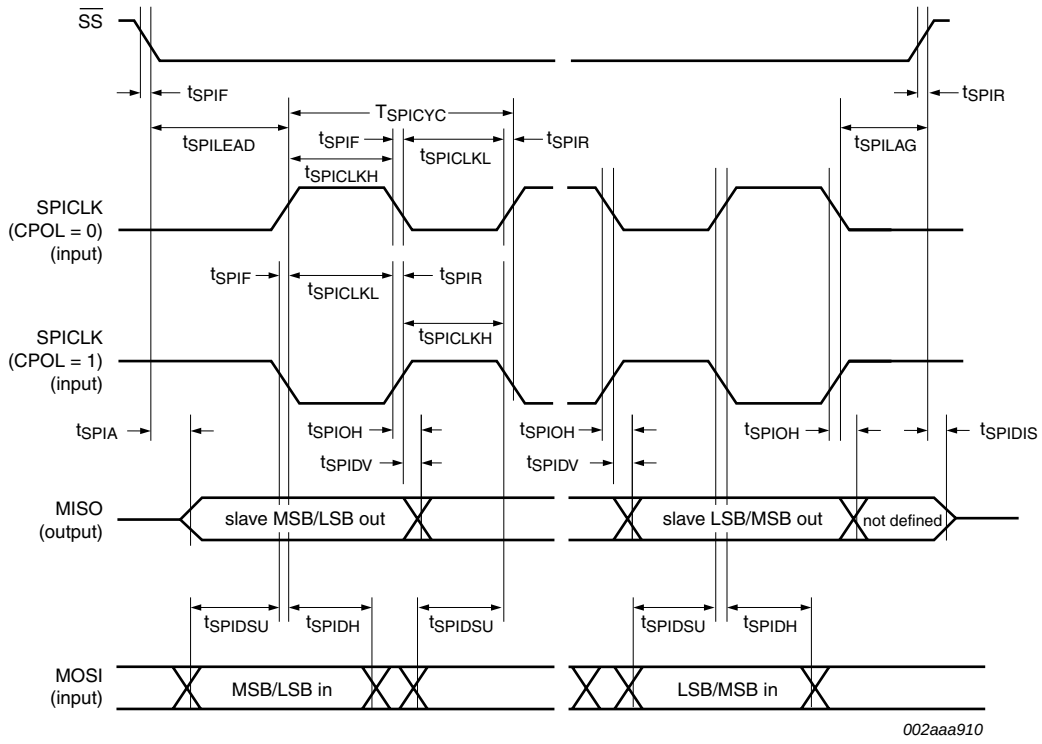

Fig 29. SPI slave timing (CPHA = 0)

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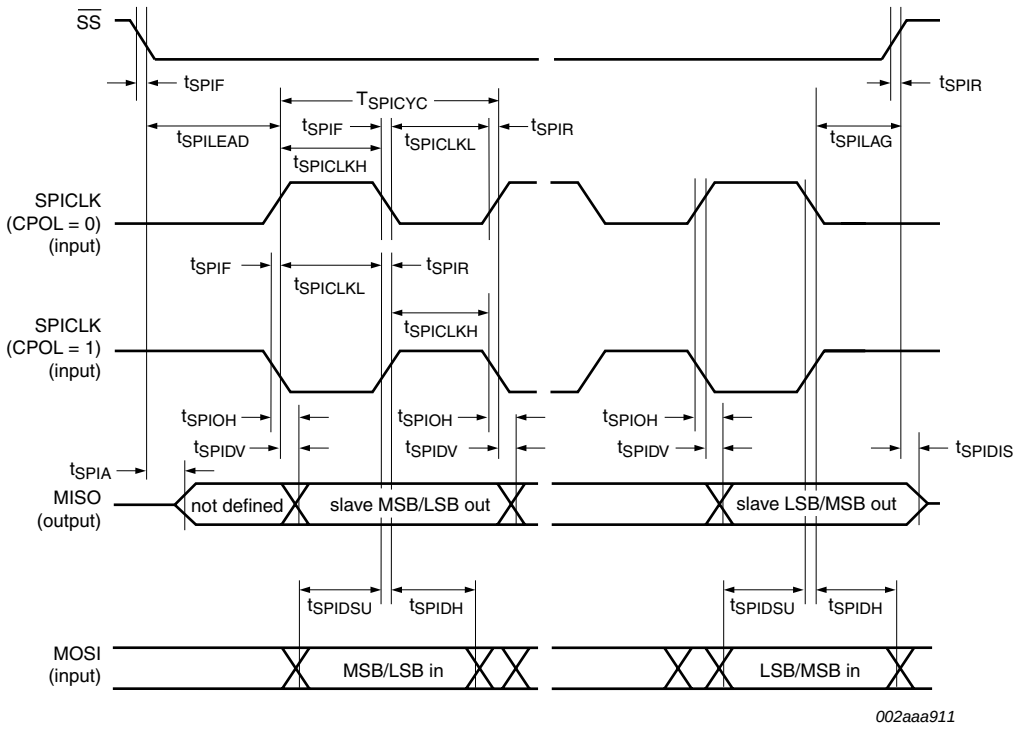

Fig 30. SPI slave timing (CPHA = 1)

12.2 ISP entry mode

Table 14. Dynamic characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{RST}$ delay from V_{DD} active time		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

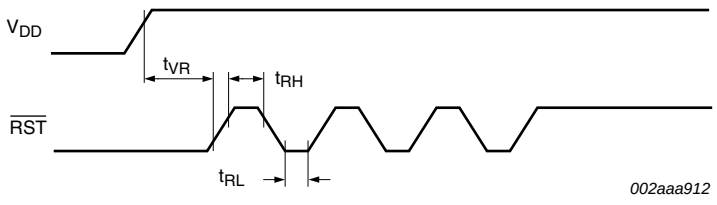

Fig 31. ISP entry timing

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13. Other characteristics

13.1 Comparator electrical characteristics

Table 15. Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±20	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	$0 < V_I < V_{DD}$	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

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13.2 ADC electrical characteristics

Table 16. ADC electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, −40 °C to +125 °C for extended, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		V_{SS} −0.2	-	V_{DD} +0.2	V
C_{iss}	input capacitance		-	-	15	pF
E_D	differential linearity error		-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		-	-	±1	LSB
E_O	offset error		-	-	±2	LSB
E_G	gain error		-	-	±1	%
$E_{u(tot)}$	total unadjusted error		-	-	±2	LSB
M_{CTC}	channel-to-channel matching		-	-	±1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 kHz to 100 kHz	-	-	−60	dB
SR_{in}	input slew rate		-	-	100	V/ms
$T_{cy(ADC)}$	ADC clock cycle time		111	-	2000	ns
t_{ADC}	ADC conversion time	A/D enabled	-	-	$13T_{cy(ADC)}$	ns

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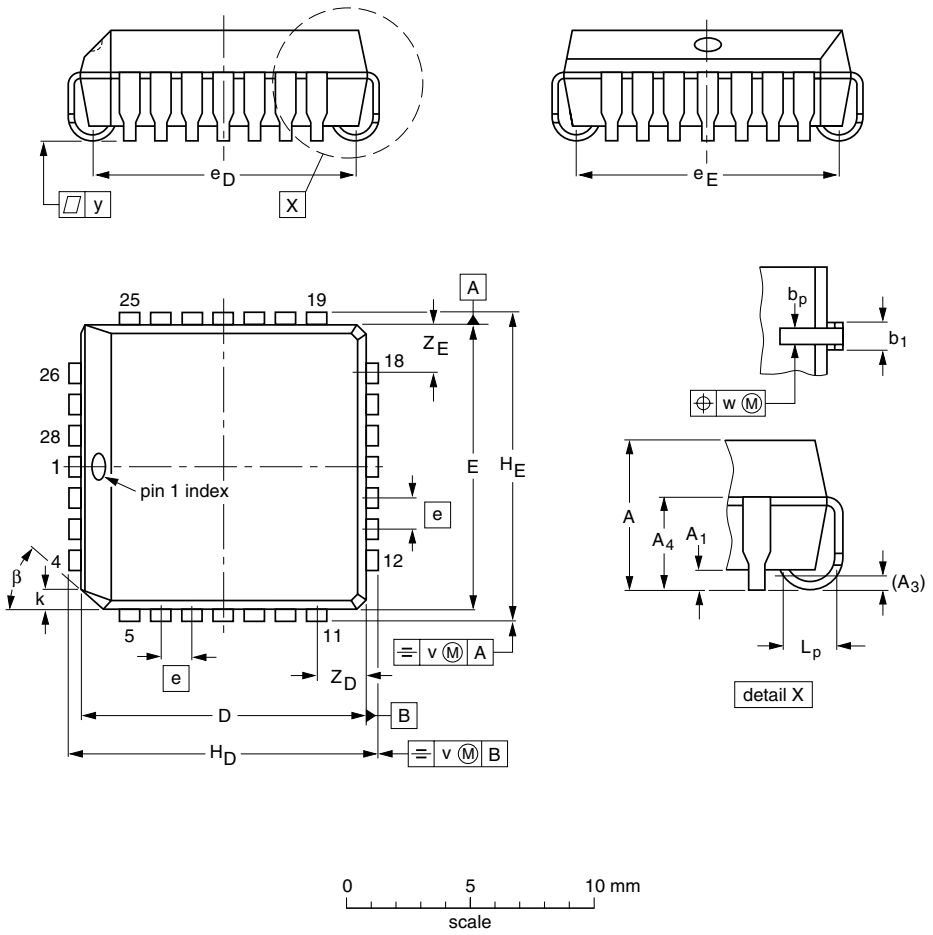
14. Package outline

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 32. Package outline SOT261-2 (PLCC28)

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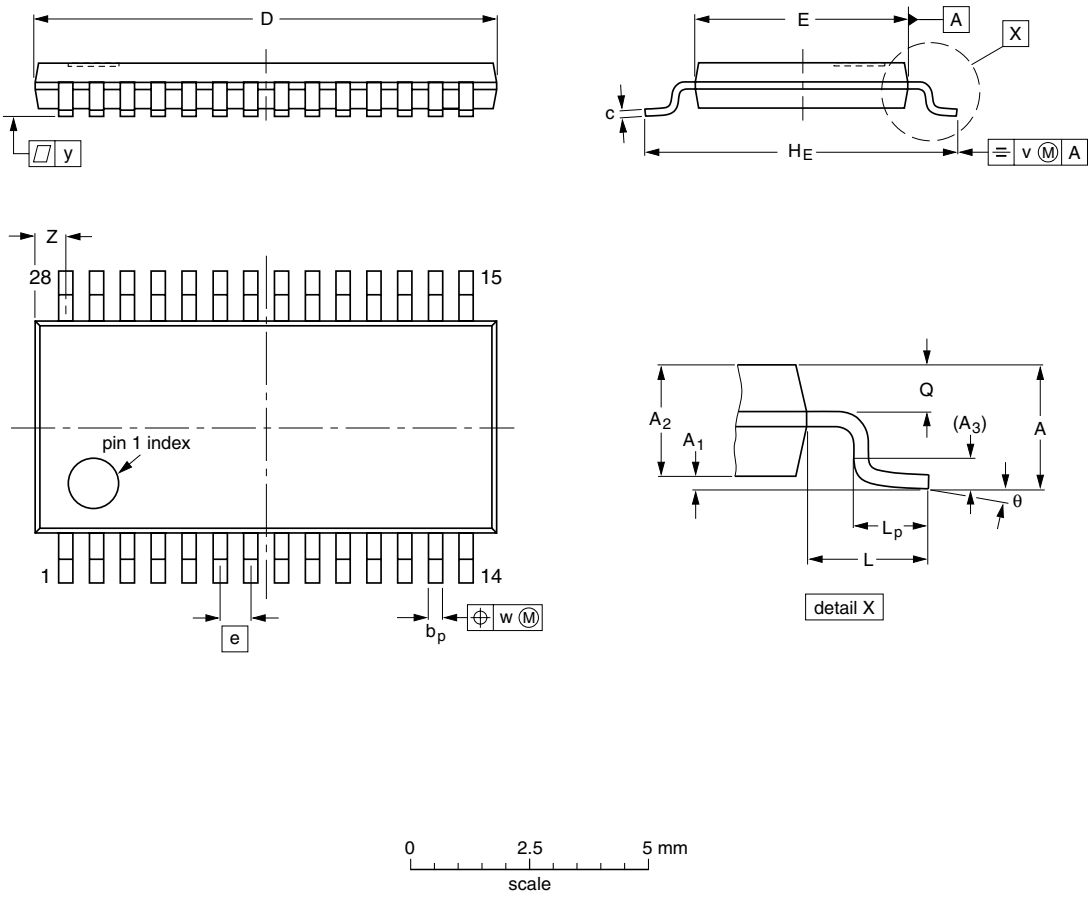
TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 33. Package outline SOT361-1 (TSSOP28)

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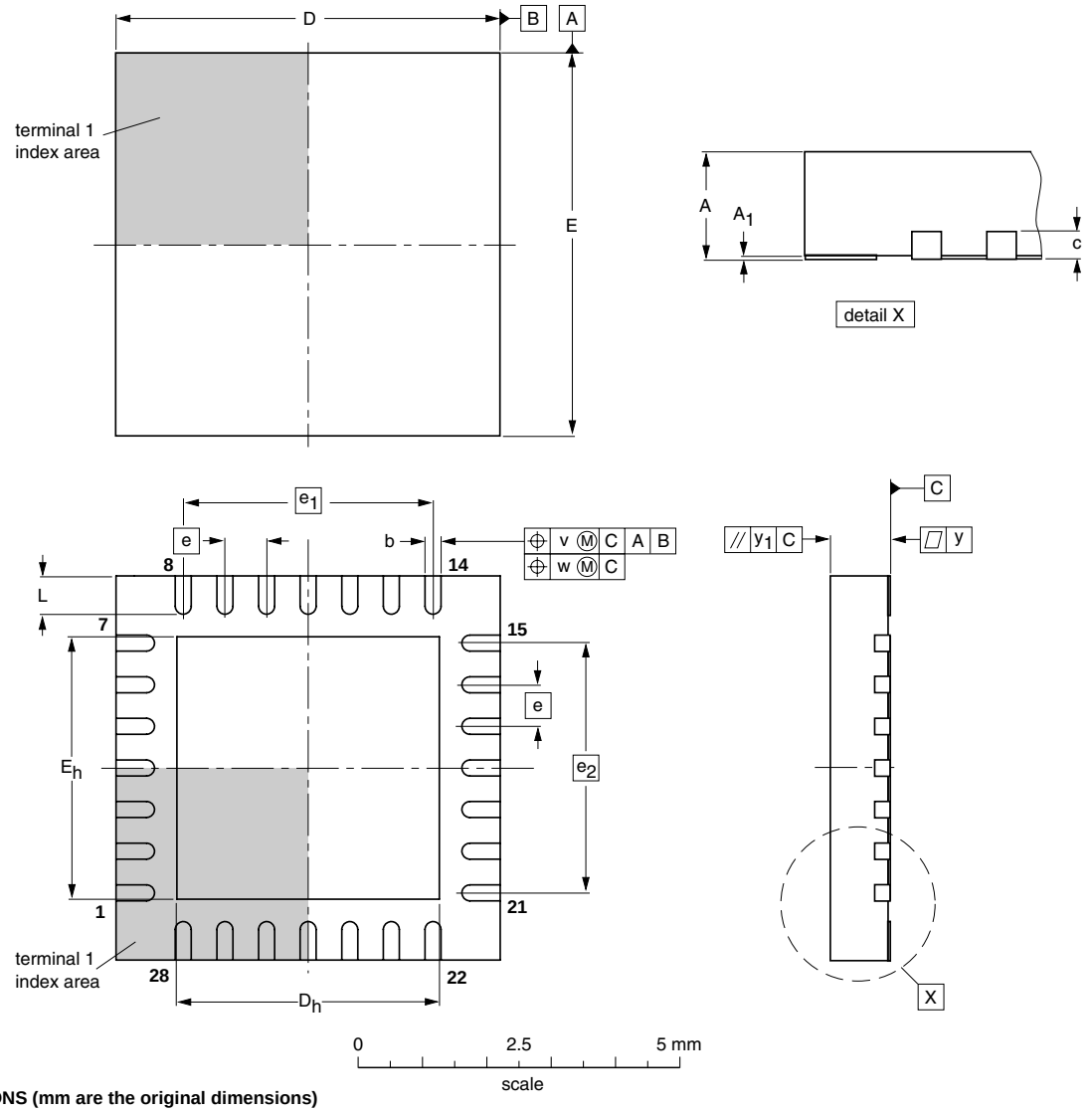
HVQFN28: plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 6 x 6 x 0.85 mm **SOT788-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.35 0.25	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.65	3.9	3.9	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT788-1	- - -	MO-220	- - -			02-10-22

Fig 34. Package outline SOT788-1 (HVQFN28)

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15. Abbreviations

Table 17. Acronym list

Acronym	Description
A/D	Analog to Digital
CPU	Central Processing Unit
DAC	Digital to Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
LED	Light Emitting Diode
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

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16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC933_934_ 935_936 v.8	20110112	Product data sheet	-	P89LPC933_934_ 935_936 v.7
Modifications:	• Table 10 “Limiting values”: Changed V_n max to 5.5 V. • Table 11 “Static characteristics”: Added V_{POR}. • Table 16 “ADC electrical characteristics”: Corrected V_{IA} max. • Section 8.16 “Reset”: Added sentence “When this pin functions as a reset input....”			
P89LPC933_934_ 935_936 v.7	20081126	Product data sheet	-	P89LPC933_934_ 935_936 v.6
P89LPC933_934_ 935_936 v.6	20050620	Product data sheet	-	P89LPC933_934_ 935_936 v.5
P89LPC933_934_ 935_936 v.5	20041103	Product data sheet	-	P89LPC933_934_ 935 v.4
P89LPC933_934_ 935 v.4	20040209	Objective data	-	P89LPC933_934_ 935 v.3

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Document status[1][2]	Product status[3]	Definition
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[2] The term 'short data sheet' is explained in section "Definitions".

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19. Contents

1 General description 1
2 Features and benefits 1
2.1 Principal features 1
2.2 Additional features 2
3 Product comparison overview 3
4 Ordering information 3
4.1 Ordering options 3
5 Block diagram 4
6 Pinning information 5
6.1 Pinning 5
6.2 Pin description 7
7 Logic symbols 11
8 Functional description 12
8.1 Special function registers 12
8.2 Enhanced CPU 24
8.3 Clocks 24
8.3.1 Clock definitions 24
8.3.2 CPU clock (OSCCLK) 24
8.3.3 Low speed oscillator option 24
8.3.4 Medium speed oscillator option 24
8.3.5 High speed oscillator option 24
8.3.6 Clock output 24
8.4 On-chip RC oscillator option 25
8.5 Watchdog oscillator option 25
8.6 External clock input option 25
8.7 CCLK wake-up delay 27
8.8 CCLK modification: DIVM register 27
8.9 Low power select 27
8.10 Memory organization 27
8.11 Data RAM arrangement 28
8.12 Interrupts 28
8.12.1 External interrupt inputs 28
8.13 I/O ports 30
8.13.1 Port configurations 30
8.13.1.1 Quasi-bidirectional output configuration 30
8.13.1.2 Open-drain output configuration 30
8.13.1.3 Input-only configuration 31
8.13.1.4 Push-pull output configuration 31
8.13.2 Port 0 analog functions 31
8.13.3 Additional port features 31
8.14 Power monitoring functions 31
8.14.1 Brownout detection 32
8.14.2 Power-on detection 32
8.15 Power reduction modes 32
8.15.1 Idle mode 32
8.15.2 Power-down mode 32
8.15.3 Total Power-down mode 33
8.16 Reset 33
8.16.1 Reset vector 33
8.17 Timers/counters 0 and 1 34
8.17.1 Mode 0 34
8.17.2 Mode 1 34
8.17.3 Mode 2 34
8.17.4 Mode 3 34
8.17.5 Mode 6 34
8.17.6 Timer overflow toggle output 34
8.18 RTC/system timer 34
8.19 CCU (P89LPC935/936) 35
8.19.1 CCU clock 35
8.19.2 CCUCLK prescaling 35
8.19.3 Basic timer operation 35
8.19.4 Output compare 35
8.19.5 Input capture 35
8.19.6 PWM operation 36
8.19.7 Alternating output mode 37
8.19.8 PLL operation 37
8.19.9 CCU interrupts 38
8.20 UART 38
8.20.1 Mode 0 38
8.20.2 Mode 1 39
8.20.3 Mode 2 39
8.20.4 Mode 3 39
8.20.5 Baud rate generator and selection 39
8.20.6 Framing error 39
8.20.7 Break detect 40
8.20.8 Double buffering 40
8.20.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3) 40
8.20.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3) 40
8.21 I^2C-bus serial interface 41
8.22 SPI 43
8.22.1 Typical SPI configurations 44
8.23 Analog comparators 46
8.23.1 Internal reference voltage 46
8.23.2 Comparator interrupt 47
8.23.3 Comparators and power reduction modes . . . 47
8.24 Keypad interrupt 47
8.25 Watchdog timer 48
8.26 Additional features 48
8.26.1 Software reset 48
8.26.2 Dual data pointers 48
8.27 Data EEPROM (P89LPC935/936) 49
8.28 Flash program memory 49

continued >>

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8.28.1 General description 49
8.28.2 Features 49
8.28.3 Flash organization 50
8.28.4 Using flash as data storage 50
8.28.5 Flash programming and erasing 50
8.28.6 In-circuit programming 50
8.28.7 In-application programming 50
8.28.8 ISP 51
8.28.9 Power-on reset code execution 51
8.28.10 Hardware activation of the boot loader 52
8.29 User configuration bytes 52
8.30 User sector security bytes 52
9 A/D converter 52
9.1 General description 52
9.2 Features and benefits 52
9.3 Block diagram 53
9.4 A/D operating modes 53
9.4.1 Fixed channel, single conversion mode 53
9.4.2 Fixed channel, continuous conversion mode . 54
9.4.3 Auto scan, single conversion mode 54
9.4.4 Auto scan, continuous conversion mode 54
9.4.5 Dual channel, continuous conversion mode . . 54
9.4.6 Single step mode 54
9.5 Conversion start modes 54
9.5.1 Timer triggered start 54
9.5.2 Start immediately 54
9.5.3 Edge triggered 55
9.5.4 Dual start immediately (P89LPC935/936) . . . 55
9.6 Boundary limits interrupt 55
9.7 DAC output to a port pin with high output impedance 55
9.8 Clock divider 55
9.9 Power-down and Idle mode 55
10 Limiting values 56
11 Static characteristics 57
11.1 I_{OH} as a function of V_{OH} 59
12 Dynamic characteristics 60
12.1 Waveforms 64
12.2 ISP entry mode 66
13 Other characteristics 67
13.1 Comparator electrical characteristics 67
13.2 ADC electrical characteristics 68
14 Package outline 69
15 Abbreviations 72
16 Revision history 73
17 Legal information 74
17.1 Data sheet status 74
17.2 Definitions 74
17.3 Disclaimers 74
17.4 Trademarks 75
18 Contact information 75
19 Contents 76

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