



**THE DATASHEET OF  
PCM1741E/2K**





## +3.3V Single-Supply, 24-Bit, 96kHz Sampling Enhanced Multilevel, Delta-Sigma, Audio DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- 24-BIT RESOLUTION
- ANALOG PERFORMANCE ( $V_{CC} = +3.3V$ ):  
Dynamic Range: 98dB typ  
SNR: 98dB typ  
THD+N: 0.005% typ  
Full-Scale Output: 2.05Vp-p typ
- 8x OVERSAMPLING DIGITAL FILTER:  
Stopband Attenuation: -55dB  
Passband Ripple:  $\pm 0.03$ dB
- SAMPLING FREQUENCY: 5kHz to 100kHz
- SYSTEM CLOCK: 256, 384, 512, 768f<sub>s</sub> with Auto Detect
- ACCEPTS 16-, 18-, 20-, AND 24-BIT AUDIO DATA
- DATA FORMATS: Standard, I<sup>2</sup>S, and Left-Justified
- USER-PROGRAMMABLE MODE CONTROLS:  
Digital Attenuation: 0dB to -63dB, 0.5dB/Step  
Digital De-Emphasis  
Digital Filter Roll-Off: Sharp or Slow  
Soft Mute  
Zero Flags for Each Output
- 3.3V SINGLE POWER SUPPLY
- 5V TOLERANT DIGITAL INPUTS
- SMALL SSOP-16 PACKAGE

### APPLICATIONS

- AV RECEIVERS
- DVD MOVIE PLAYERS
- DVD ADD-ON CARDS FOR HIGH-END PCs
- HDTV RECEIVERS
- CAR AUDIO SYSTEMS
- OTHER APPLICATIONS REQUIRING 24-BIT AUDIO

### DESCRIPTION

The PCM1741 is a CMOS, monolithic, integrated circuit which includes stereo Digital-to-Analog Converters (DACs) and support circuitry in a small SSOP-16 package. The data converters utilize Texas Instrument's enhanced multilevel delta-sigma architecture that employs fourth-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1741 accepts industry standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 100kHz are supported. A full set of user-programmable functions are accessible through a 3-wire serial control port that supports register write functions.



# SPECIFICATIONS (Cont.)

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ ,  $V_{DD} = 3.3\text{V}$ , system clock =  $384f_S$  ( $f_S = 44.1\text{kHz}$ ), and 24-bit data, unless otherwise noted.

| PARAMETER                                      | CONDITIONS                               | PCM1741E |                |      | UNITS              |
|--|--|----------|----------------|------|--------------------|
|  |  | MIN      | TYP            | MAX  |                    |
| <b>ANALOG FILTER PERFORMANCE</b>               |  |          |                |      |                    |
| Frequency Response                             | $f = 20\text{kHz}$<br>$f = 44\text{kHz}$ |          | -0.03<br>-0.20 |      | dB<br>dB           |
| <b>POWER SUPPLY REQUIREMENTS<sup>(4)</sup></b> |  |          |                |      |                    |
| Voltage Range, $V_{DD}$                        |  | +2.7     | +3.3           | +3.6 | VDC                |
| $V_{CC}$                                       |  | +2.7     | +3.0           | +3.6 | VDC                |
| Supply Current, $I_{DD}$                       | $f_S = 44.1\text{kHz}$                   |          | 6.0            | 10   | mA                 |
|  | $f_S = 96\text{kHz}$                     |          | 13.0           |      | mA                 |
| $I_{CC}$                                       | $f_S = 44.1\text{kHz}$                   |          | 7.0            | 11   | mA                 |
|  | $f_S = 96\text{kHz}$                     |          | 7.0            |      | mA                 |
| Power Dissipation                              | $f_S = 44.1\text{kHz}$                   |          | 43             | 88   | mW                 |
|  | $f_S = 96\text{kHz}$                     |          | 66             |      | mW                 |
| <b>TEMPERATURE RANGE</b>                       |  |          |                |      |                    |
| Operation Temperature                          |  | -25      |                | +85  | $^\circ\text{C}$   |
| Thermal Resistance $\theta_{JA}$               | SSOP-16                                  |          | 115            |      | $^\circ\text{C/W}$ |

NOTES: (1) Pins 1, 2, 3, 16 (SCK, BCK, LRCK, DATA). (2) Pins 13-15 (MD, MC, ML). (3) Pins 11, 12 (ZEROR, ZEROL). (4) Analog performance specifications are tested with a Shibasoku #725 THD Meter with 400Hz HPF on, 30kHz LPF on, and an average mode with 20kHz bandwidth limiting. The load connected to the analog output is  $5\text{k}\Omega$  or larger, via capacitive coupling.

## ABSOLUTE MAXIMUM RATINGS

|                                      |   |
|--------------------------------------|---|
| Power Supply Voltage, $V_{DD}$       | +4.0V                                       |
| $V_{CC}$                             | +6.5V                                       |
| Ground Voltage Differences           | $\pm 0.1\text{V}$                           |
| Digital Input Voltage                | -0.3V to (6.5V + 0.3V)                      |
| Input Current (except power supply)  | $\pm 10\text{mA}$                           |
| Ambient Temperature Under Bias       | $-40^\circ\text{C}$ to $+125^\circ\text{C}$ |
| Storage Temperature                  | $-55^\circ\text{C}$ to $+150^\circ\text{C}$ |
| Junction Temperature                 | $+150^\circ\text{C}$                        |
| Lead Temperature (soldering, 5s)     | $+260^\circ\text{C}$                        |
| Package Temperature (IR reflow, 10s) | $+235^\circ\text{C}$                        |



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

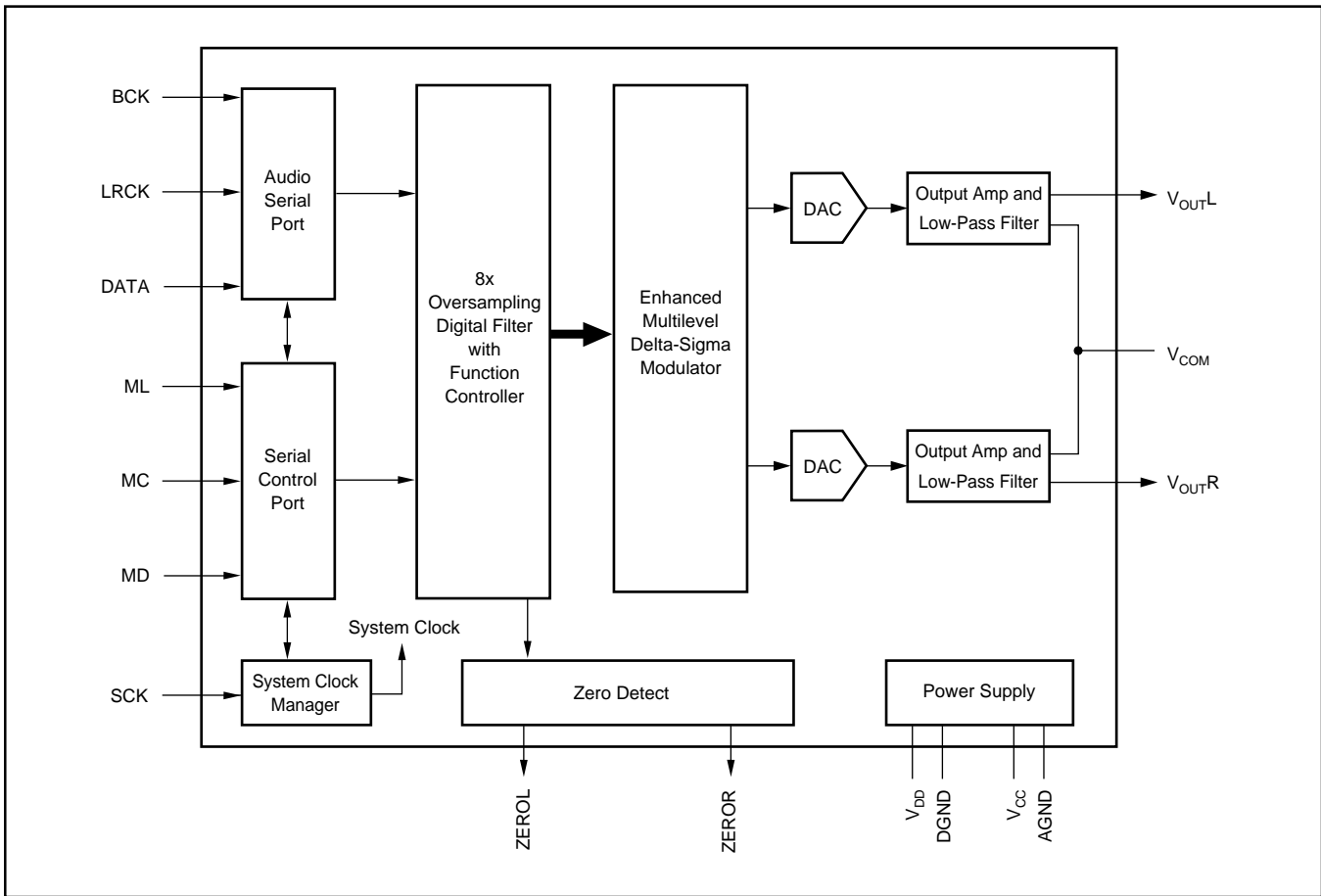
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

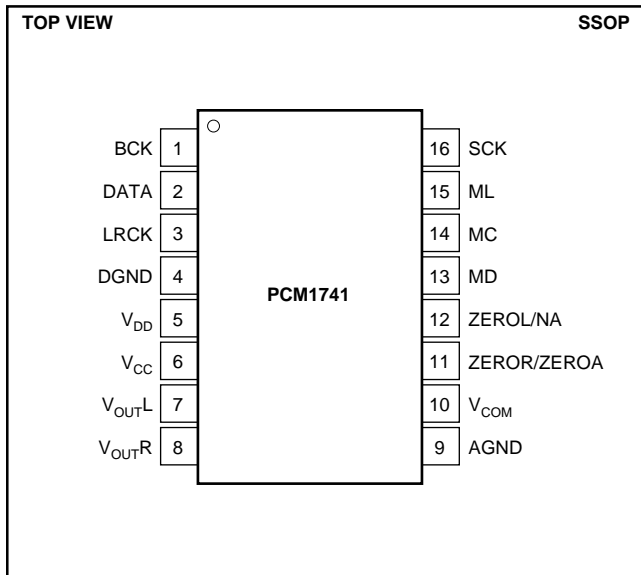
| PRODUCT  | PACKAGE | PACKAGE DRAWING NUMBER | SPECIFIED TEMPERATURE RANGE                | PACKAGE MARKING | ORDERING NUMBER <sup>(1)</sup> | TRANSPORT MEDIA |
|----------|---------|------------------------|--|-----------------|--------------------------------|-----------------|
| PCM1741E | SSOP-16 | 322                    | $-25^\circ\text{C}$ to $+85^\circ\text{C}$ | PCM1741E        | PCM1741E                       | Rails           |
| "        | "       | "                      | "  | "               | PCM1741E/2K                    | Tape and Reel   |

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1741E/2K" will yield a single 2000-piece Tape and Reel.

## BLOCK DIAGRAM



## PIN CONFIGURATION



## PIN ASSIGNMENTS

| PIN | NAME              | TYPE | FUNCTION  |
|-----|-------------------|------|---|
| 1   | BCK               | IN   | Audio Data Bit Clock Input. <sup>(1)</sup>                            |
| 2   | DATA              | IN   | Audio Data Digital Input. <sup>(1)</sup>                              |
| 3   | LRCK              | IN   | L-Channel and R-Channel Audio Data Latch Enable Input. <sup>(1)</sup> |
| 4   | DGND              | –    | Digital Ground  |
| 5   | V <sub>DD</sub>   | –    | Digital Power Supply, +3.3V   |
| 6   | V <sub>CC</sub>   | –    | Analog Power Supply, +3.3V  |
| 7   | V <sub>OUTL</sub> | OUT  | Analog Output for L-Channel.  |
| 8   | V <sub>OUTR</sub> | OUT  | Analog Output for R-Channel.  |
| 9   | AGND              | –    | Analog Ground   |
| 10  | V <sub>COM</sub>  | –    | Common Voltage Decoupling.  |
| 11  | ZEROR/<br>ZEROA   | OUT  | Zero Flag Output for R-Channel/Zero Flag Output for L/R-Channel.      |
| 12  | ZEROL/NA          | OUT  | Zero Flag Output for L-Channel/No Assign.                             |
| 13  | MD                | IN   | Mode Control Data Input. <sup>(2)</sup>                               |
| 14  | MC                | IN   | Mode Control Clock Input. <sup>(2)</sup>                              |
| 15  | ML                | IN   | Mode Control Latch Input. <sup>(2)</sup>                              |
| 16  | SCK               | IN   | System Clock Input.   |

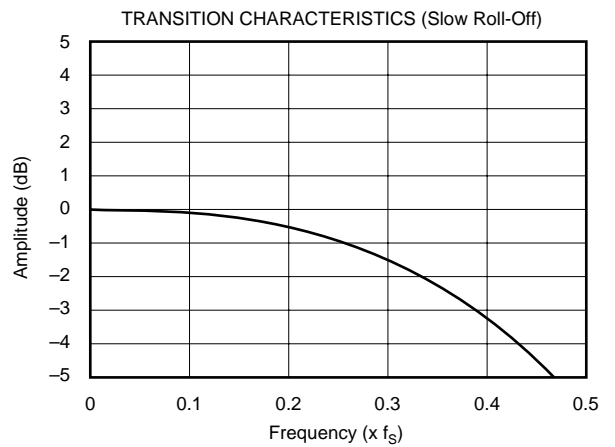
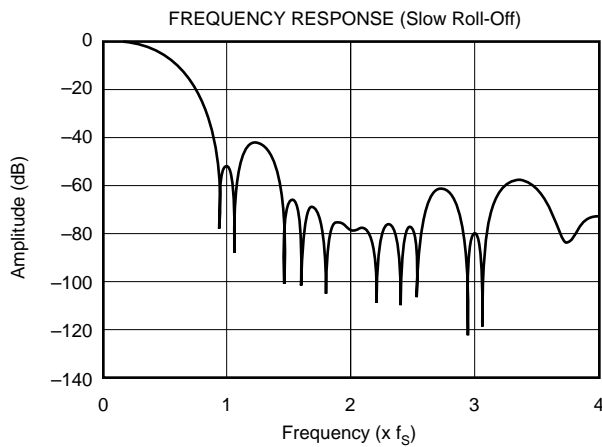
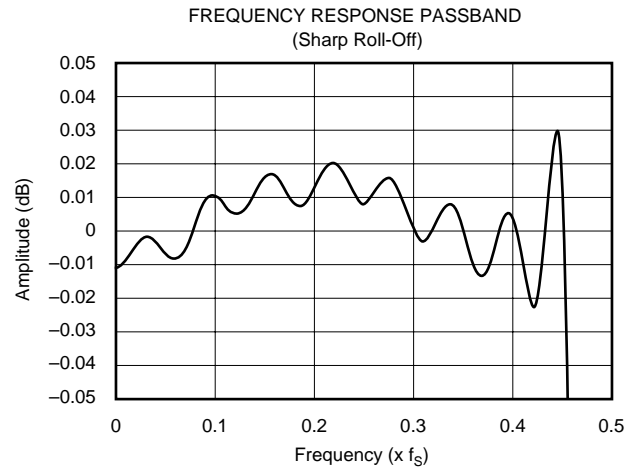
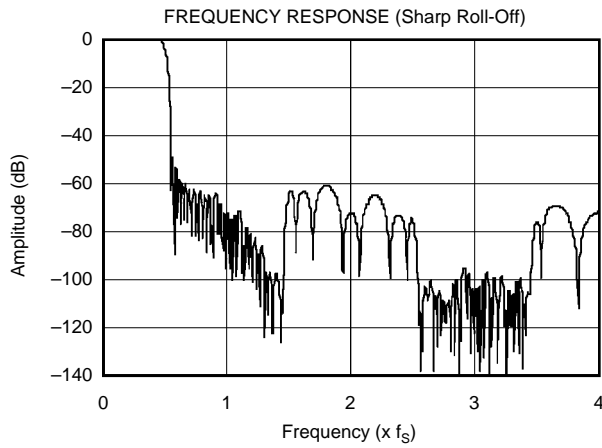
NOTES: (1) Schmitt-trigger input, 5V tolerant. (2) Schmitt-trigger with internal pull-down, 5V tolerant.

# TYPICAL PERFORMANCE CURVES

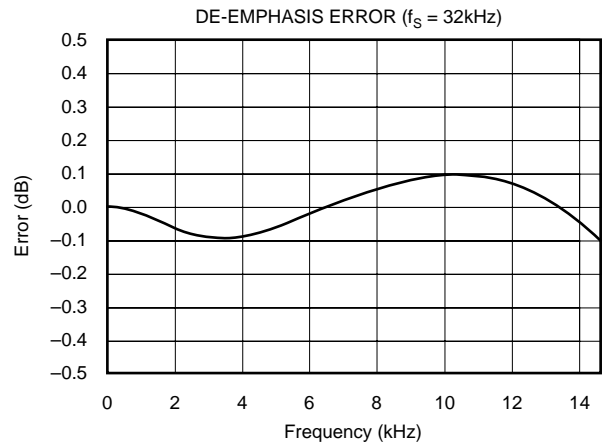
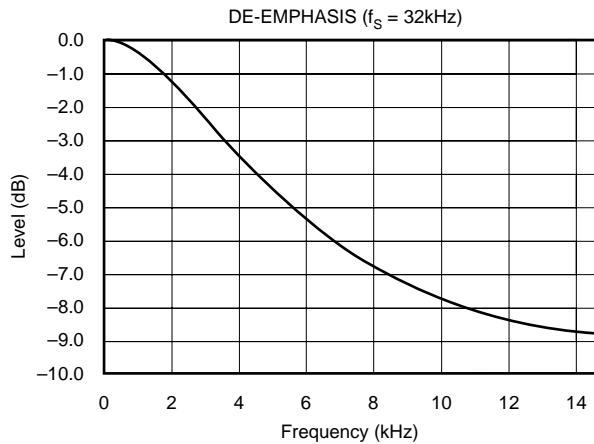
All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = 3.3\text{V}$ , system clock =  $384f_S$  ( $f_S = 44.1\text{kHz}$ ), and 24-bit input data, unless otherwise noted.

## DIGITAL FILTER

### Digital Filter (De-Emphasis Off)



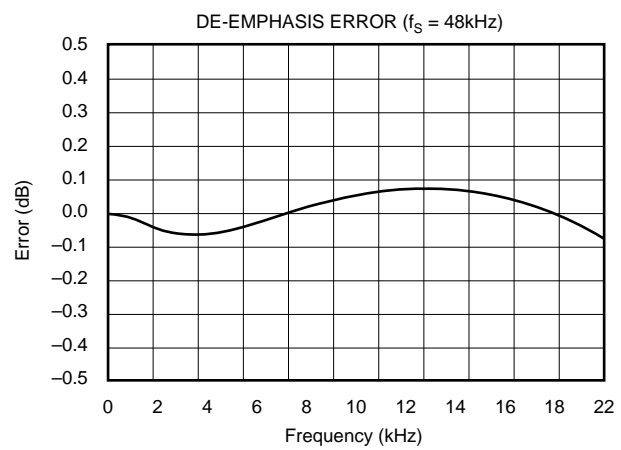
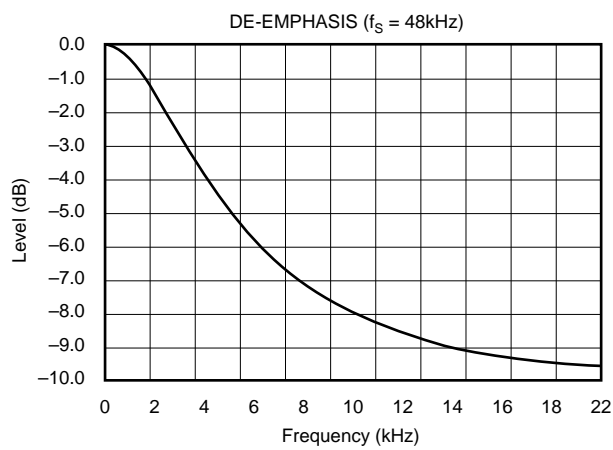
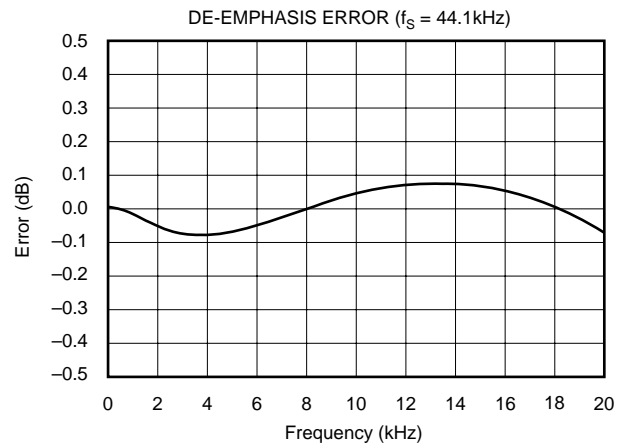
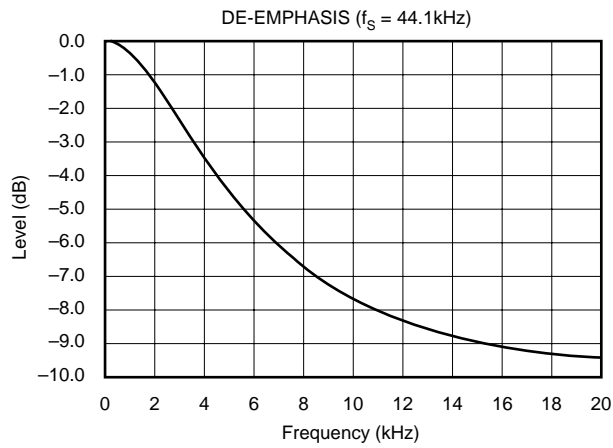
### De-Emphasis



# TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = 3.3\text{V}$ , system clock =  $384f_S$  ( $f_S = 44.1\text{kHz}$ ), and 24-bit input data, unless otherwise noted.

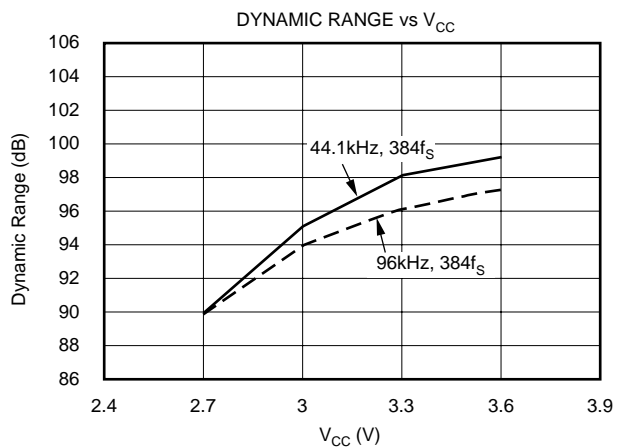
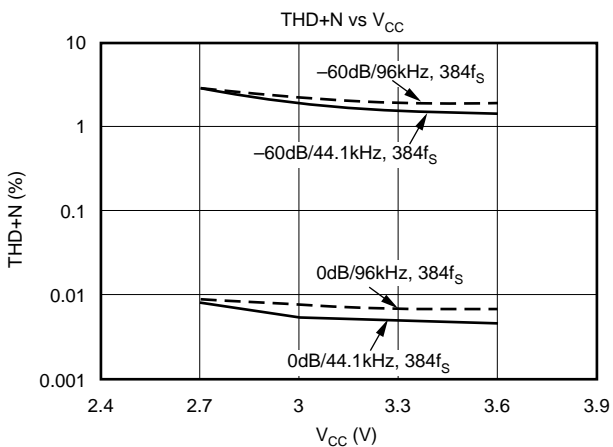
## De-Emphasis (Cont.)



## ANALOG DYNAMIC PERFORMANCE

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ ,  $V_{DD} = 3.3\text{V}$ , and 24-bit input data, unless otherwise noted.

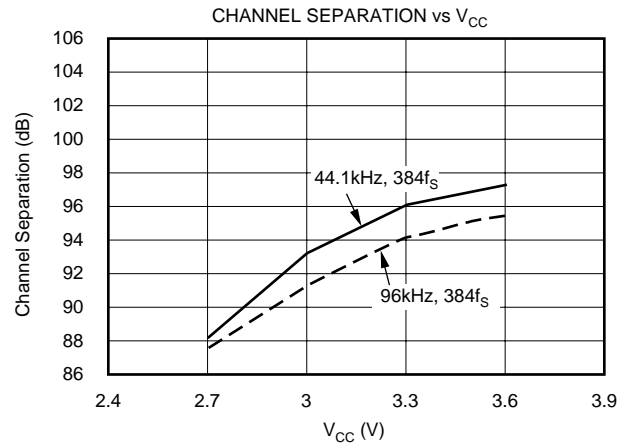
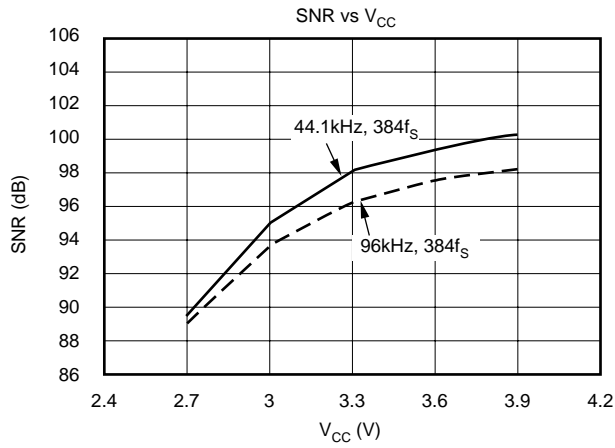
### Supply-Voltage Characteristics



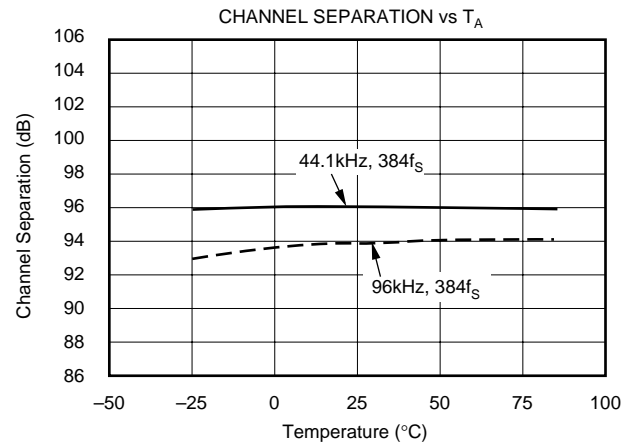
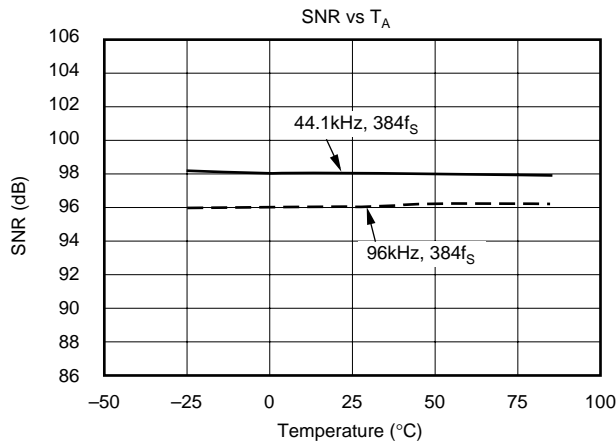
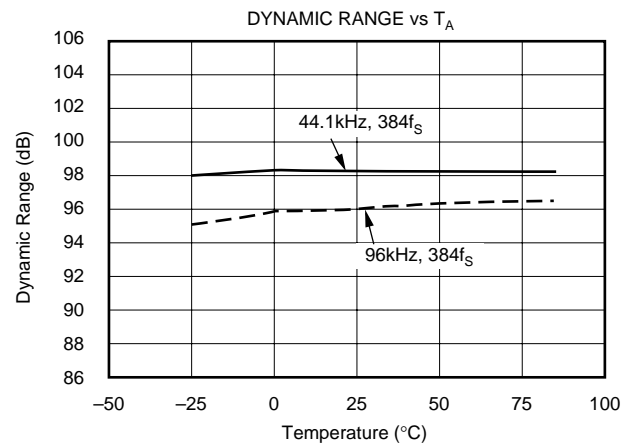
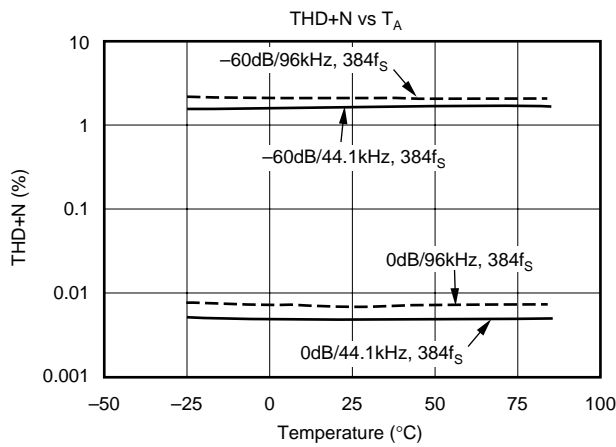
# TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{DD} = 3.3\text{V}$ , and 24-bit input data, unless otherwise noted.

## Supply-Voltage Characteristics (Cont.)



## Temperature Characteristics



# SYSTEM CLOCK AND RESET FUNCTIONS

## SYSTEM CLOCK INPUT

The PCM1741 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 16). Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The PLL1700 multi-clock generator from Texas Instruments is an excellent choice for providing the PCM1741 system clock.

## POWER-ON RESET FUNCTIONS

The PCM1741 includes a power-on reset function, as shown in Figure 2. With the system clock active, and  $V_{DD} > 2.0V$  (typical 1.6V to 2.4V), the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time  $V_{DD} > 2.0V$ . After the initialization period, the PCM1741 will be set to its reset default state, as described in the Mode Control Register section of this data sheet.

During the reset period (1024 system clocks), the analog outputs are forced to the bipolar zero level, or  $V_{CC}/2$ . After the reset period, the internal register is initialized in the next  $1/f_s$  period and, if SCK, BCK, and LRCK are provided continuously, the PCM1741 provides proper analog output with unit group delay against the input data.

| SAMPLING FREQUENCY | SYSTEM CLOCK FREQUENCY ( $f_{SCLK}$ ) (MHz) |          |          |              |
|--------------------|---|----------|----------|--------------|
|                    | $256f_s$                                    | $384f_s$ | $512f_s$ | $768f_s$     |
| 8kHz               | 2.0480                                      | 3.0720   | 4.0960   | 6.1440       |
| 16kHz              | 4.0960                                      | 6.1440   | 8.1920   | 12.2880      |
| 32kHz              | 8.1920                                      | 12.2880  | 16.3840  | 24.5760      |
| 44.1kHz            | 11.2896                                     | 16.9344  | 22.5792  | 33.8688      |
| 48kHz              | 12.2880                                     | 18.4320  | 24.5760  | 36.8640      |
| 88.2kHz            | 22.5792                                     | 33.8688  | 45.1584  | See Note (1) |
| 96kHz              | 24.5760                                     | 36.8640  | 49.1520  | See Note (1) |

NOTE: (1) The  $768f_s$  system clock rate is not supported for  $f_s > 64kHz$ .

TABLE I. System Clock Rates for Common Audio Sampling Frequencies.

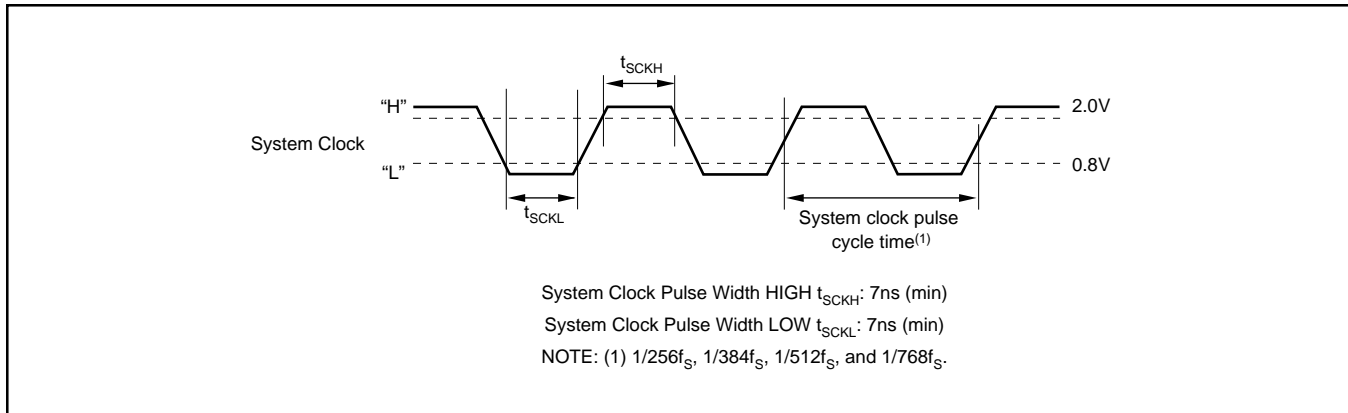


FIGURE 1. System Clock Input Timing.

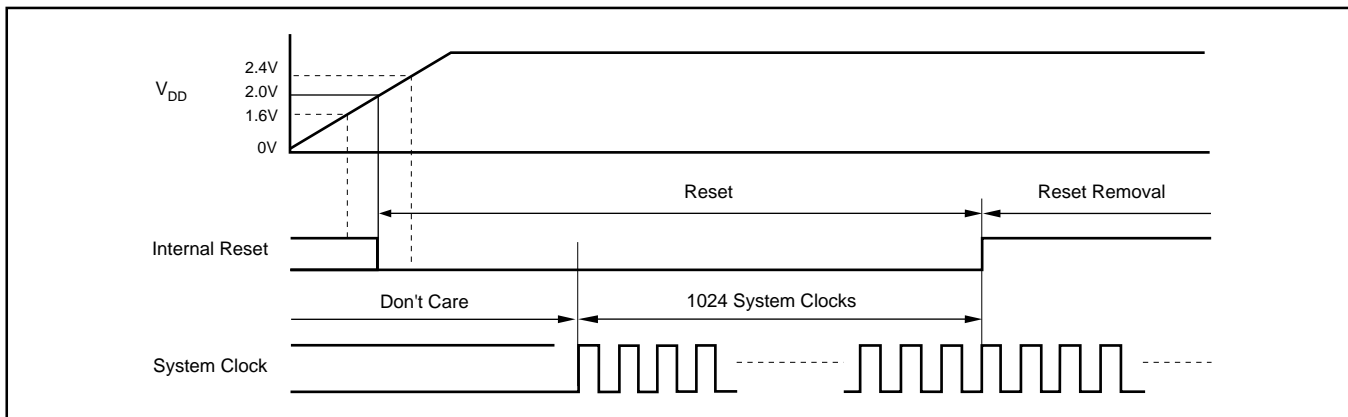


FIGURE 2. Power-On Reset Timing.

## AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1741 is comprised of a 3-wire synchronous serial port. It includes LRCK (pin 3), BCK (pin 1), and DATA (pin 2). BCK is the serial audio bit clock, and is used to clock the serial data present on DATA into the audio interface's serial shift register. Serial data is clocked into the PCM1741 on the rising edge of BCK. LRCK is the serial audio left/right word clock used to latch serial data into the serial audio interface's internal registers.

Both LRCK and BCK should be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCK. LRCK is operated at the sampling frequency,  $f_s$ . BCK may be operated at 32, 48, or 64 times the sampling frequency (I<sup>2</sup>S format except BCK =  $32f_s$ ). Internal operation of the PCM1741 is synchronized with LRCK. Accordingly, it is

held when the sampling rate clock of LRCK is changed or SCK and/or BCK is broken at least for one clock cycle. If SCK, BCK, and LRCK are provided continuously after this hold condition, the internal operation will be resynchronized automatically, less than  $3/f_s$  period. In this resynchronize period, and following  $3/f_s$ , analog output is forced to the bipolar zero level, or  $V_{CC}/2$ . External resetting is not required.

## AUDIO DATA FORMATS AND TIMING

The PCM1741 supports industry-standard audio data formats, including Standard, I<sup>2</sup>S, and Left-Justified, as shown in Figure 3. Data formats are selected using the format bits, FMT[2:0], in Control Register 20. The default data format is 24-bit left justified. All formats require Binary Two's Complement, MSB-first audio data. See Figure 4 for a detailed timing diagram of the serial audio interface.

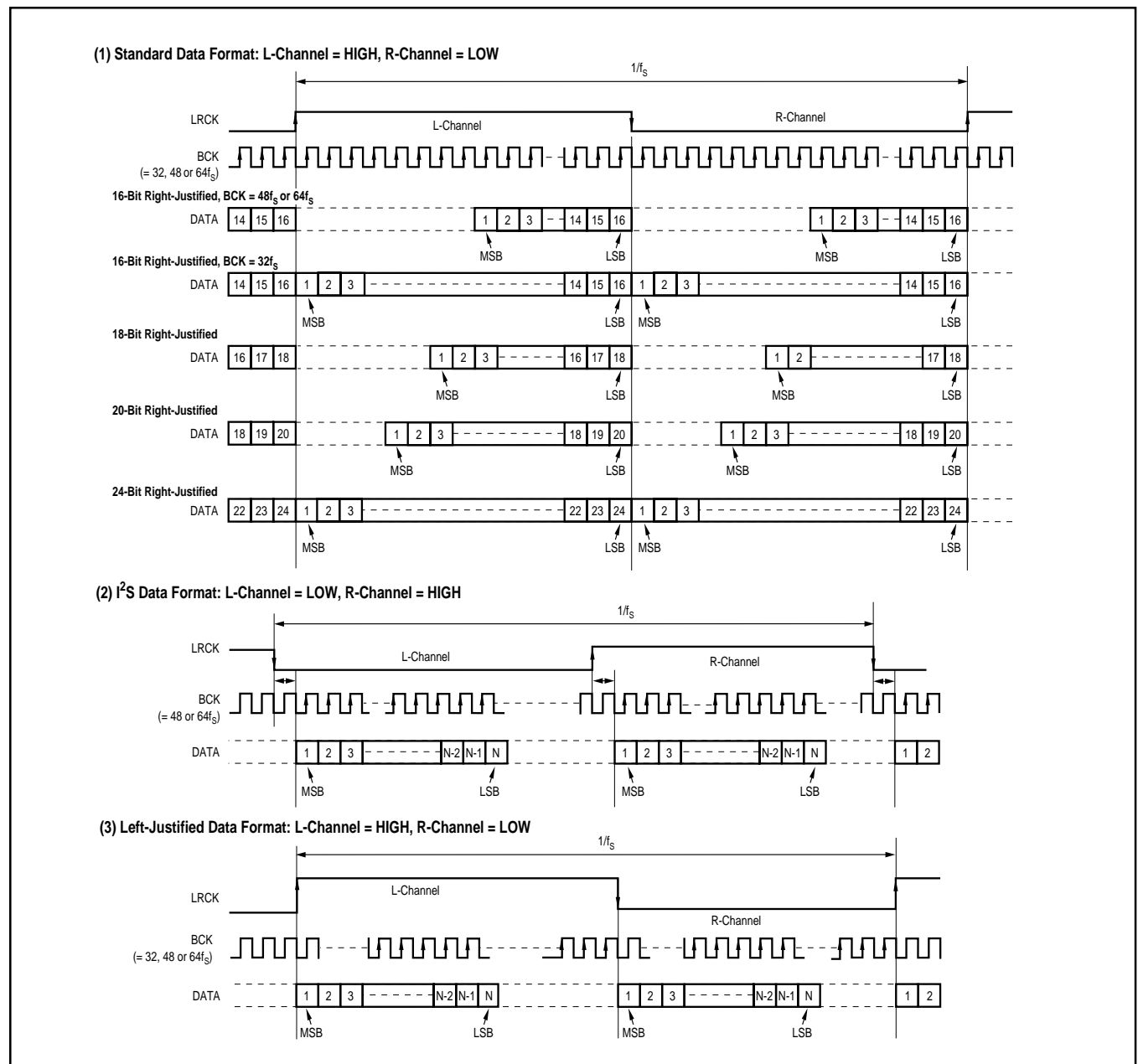


FIGURE 3. Audio Data Input Formats.

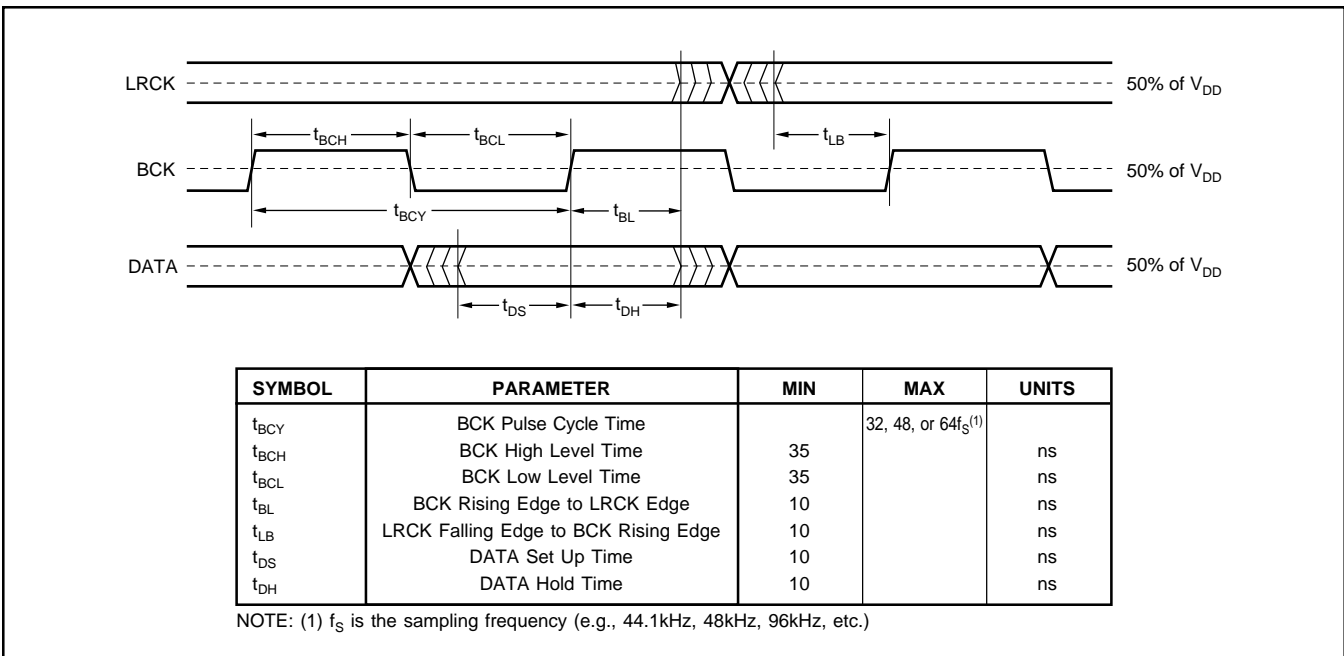


FIGURE 4. Audio Interface Timing.

### SERIAL CONTROL INTERFACE

The serial control interface is a 3-wire serial port that operates asynchronously to the serial audio interface. The serial control interface is utilized to program the on-chip mode registers. The control interface includes MD (pin 13), MC (pin 14), and ML (pin 15). MD is the serial data input, used to program the mode registers, MC is the serial bit clock, used to shift data into the control port, and ML is the control port latch clock.

### REGISTER WRITE OPERATION

All write operations for the serial control port use 16-bit data words. Figure 5 shows the control data word format. The most significant bit must be a "0". There are seven bits, labeled  $IDX[6:0]$ , that set the register index (or address) for

the write operation. The least significant eight bits,  $D[7:0]$ , contain the data to be written to the register specified by  $IDX[6:0]$ .

Figure 6 shows the functional timing diagram for writing the serial control port. ML is held at a logic "1" state until a register needs to be written. To start the register write cycle, ML is set to logic "0". Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, ML is set to logic "1" to latch the data into the indexed mode control register.

### CONTROL INTERFACE TIMING REQUIREMENTS

See Figure 7 for a detailed timing diagram of the serial control interface. These timing parameters are critical for proper control port operation.

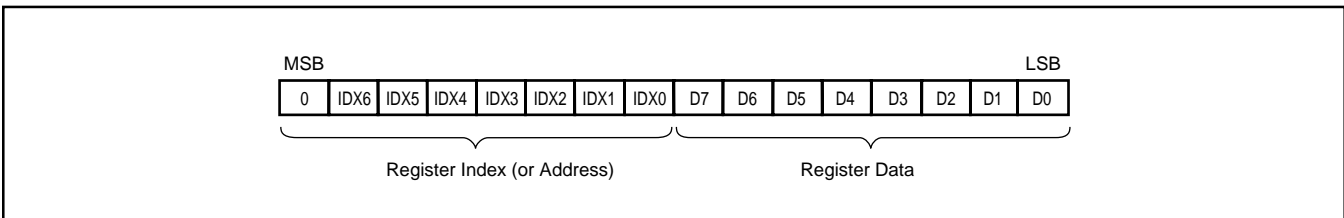


FIGURE 5. Control Data Word Format for MDI.

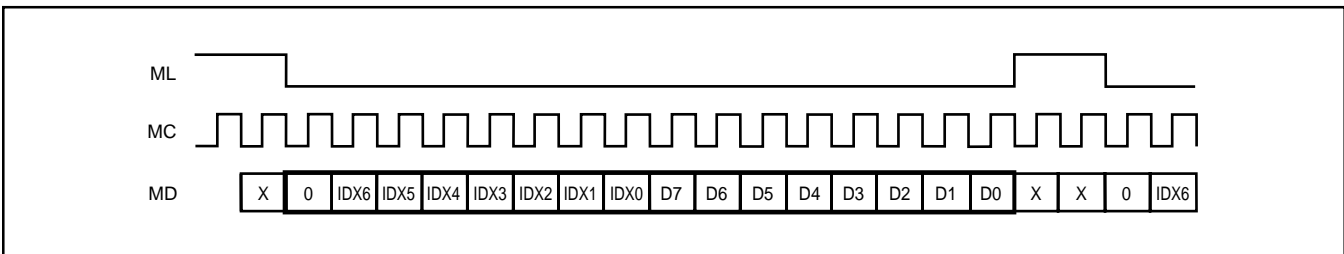


FIGURE 6. Register Write Operation.

## MODE CONTROL REGISTERS

### User-Programmable Mode Controls

The PCM1741 includes a number of user-programmable functions that are accessed via control registers. The registers are programmed using the Serial Control Interface that was previously discussed in the “Serial Control Interface”

section of this data sheet. Table II lists the available mode control functions, along with their reset default conditions and associated register index.

### Register Map

The mode control register map is shown in Table III. Each register includes an index (or address) indicated by the IDX[6:0] bits.

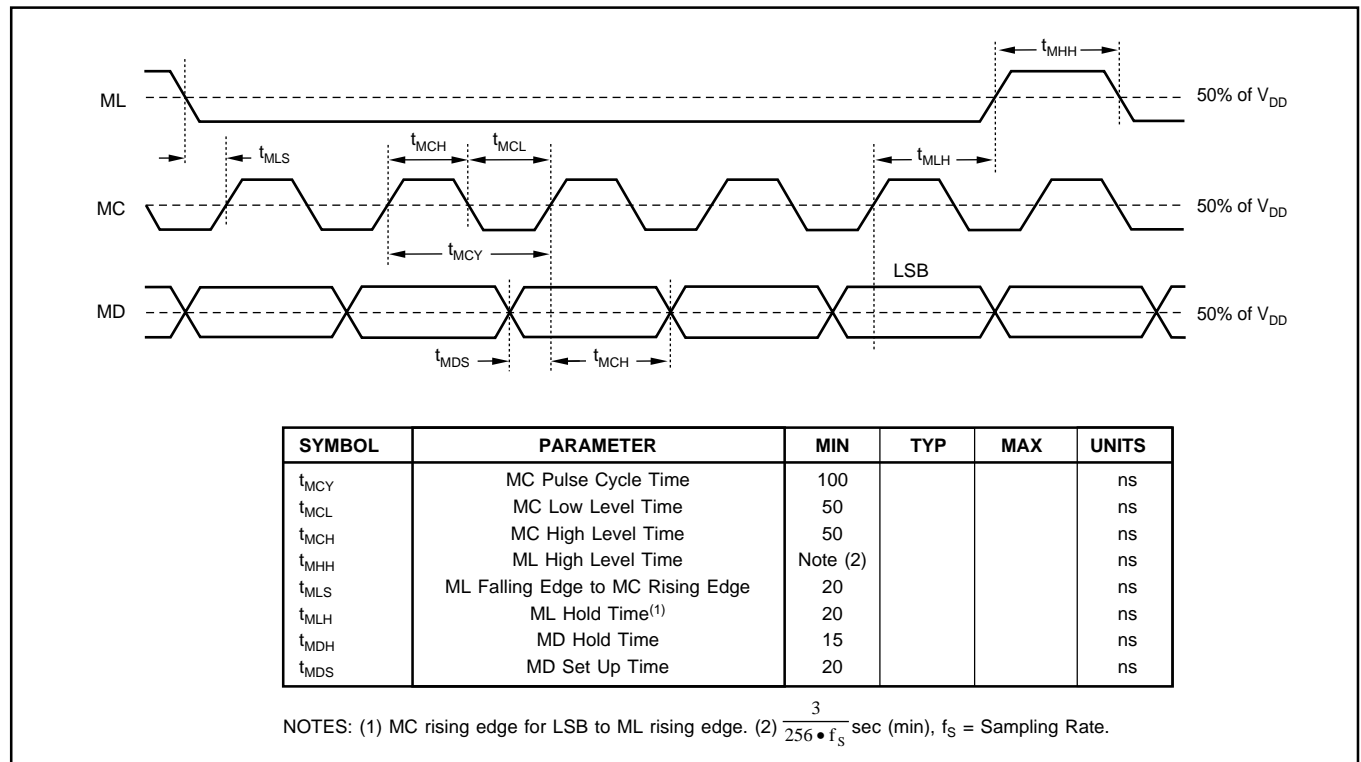


FIGURE 7. Control Interface Timing.

| FUNCTION   | RESET DEFAULT            | CONTROL REGISTER | INDEX, IDX[6:0]    |
|--|--------------------------|------------------|--------------------|
| Digital Attenuation Control, 0dB to -63dB in 0.5dB Steps | 0dB, No Attenuation      | 16 and 17        | AT1[7:0], AT2[7:0] |
| Soft Mute Control  | Mute Disabled            | 18               | MUT[2:0]           |
| Oversampling Rate Control (64 or 128 $f_s$ )             | 64 $f_s$ Oversampling    | 18               | OVER               |
| DAC Operation Control                                    | DAC1 and DAC2 Enabled    | 19               | DAC[2:1]           |
| De-Emphasis Function Control                             | De-Emphasis Disabled     | 19               | DM12               |
| De-Emphasis Sample Rate Selection                        | 44.1kHz                  | 19               | DMF[1:0]           |
| Audio Data Format Control                                | 24-Bit Left Justified    | 20               | FMT[2:0]           |
| Digital Filter Roll-Off Control                          | Sharp Roll-Off           | 20               | FLT                |
| Zero Flag Function Select                                | L-/R-Channel Independent | 22               | AZRO               |
| Output Phase Select                                      | Normal Phase             | 22               | DREV               |
| Zero Flag Polarity Select                                | High                     | 22               | ZREV               |

TABLE II. User-Programmable Mode Controls.

| IDX (B8-B14)    | REGISTER | B15 | B14  | B13  | B12  | B11  | B10  | B9   | B8   | B7                 | B6                 | B5                 | B4                 | B3                 | B2                 | B1                 | B0                 |
|-----------------|----------|-----|------|------|------|------|------|------|------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 10 <sub>H</sub> | 16       | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | AT17               | AT16               | AT15               | AT14               | AT13               | AT12               | AT11               | AT10               |
| 11 <sub>H</sub> | 17       | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | AT27               | AT26               | AT25               | AT24               | AT23               | AT22               | AT21               | AT20               |
| 12 <sub>H</sub> | 18       | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV <sup>(1)</sup> | OVER               | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | MUT2               | MUT1               |
| 13 <sub>H</sub> | 19       | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV <sup>(1)</sup> | DMF1               | DMF0               | DM12               | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | DAC2               | DAC1               |
| 14 <sub>H</sub> | 20       | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | FLT                | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | FMT2               | FMT1               | FMT0               |
| 15 <sub>H</sub> | 21       | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> |
| 16 <sub>H</sub> | 22       | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | RSV <sup>(1)</sup> | AZRO               | ZREV               | DREV               |

NOTE: (1) RSV = Reserved for test operation. It should be set to “0” when in regular operation.

TABLE III. Mode Control Register Map.

## REGISTER DEFINITIONS

|             |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|-------------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
|             | B15 | B14  | B13  | B12  | B11  | B10  | B9   | B8   | B7   | B6   | B5   | B4   | B3   | B2   | B1   | B0   |
| Register 16 | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | AT17 | AT16 | AT15 | AT14 | AT13 | AT12 | AT11 | AT10 |
| Register 17 | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | AT27 | AT26 | AT25 | AT24 | AT23 | AT22 | AT21 | AT20 |

### ATx[7:0] Digital Attenuation Level Setting

where  $x = 1$  or  $2$ , corresponding to the DAC output  $V_{OUTL}$  ( $x = 1$ ) and  $V_{OUTR}$  ( $x = 2$ ).

Default Value: 1111 1111<sub>B</sub>

Each DAC channel ( $V_{OUTL}$  and  $V_{OUTR}$ ) includes a digital attenuator function. The attenuation level may be set from 0dB to -63dB, in 0.5dB steps. Changes in attenuator levels are made by incrementing or decrementing, by one step (0.5dB), for every  $8/f_s$  time interval until the programmed attenuator setting is reached. Alternatively, the attenuator level may be set to infinite attenuation (or mute). The attenuation data for each channel can be set individually.

The attenuation level may be set using the formula below.

$$\text{Attenuation Level (dB)} = 0.5 (\text{ATx}[7:0]_{\text{DEC}} - 255)$$

where:  $\text{ATx}[7:0]_{\text{DEC}} = 0$  through 255

for:  $\text{ATx}[7:0]_{\text{DEC}} = 0$  through 128, the attenuator is set to infinite attenuation.

The following table shows attenuator levels for various settings.

| ATx[7:0]               | Decimal Value | Attenuator Level Setting      |
|------------------------|---------------|-------------------------------|
| 1111 1111 <sub>B</sub> | 255           | 0dB, No Attenuation (default) |
| 1111 1110 <sub>B</sub> | 254           | -0.5dB                        |
| 1111 1101 <sub>B</sub> | 253           | -1.0dB                        |
| 1000 0011 <sub>B</sub> | 131           | -62.0dB                       |
| 1000 0010 <sub>B</sub> | 130           | -62.5dB                       |
| 1000 0001 <sub>B</sub> | 129           | -63.0dB                       |
| 1000 0000 <sub>B</sub> | 128           | Mute                          |
| •                      | •             | •                             |
| •                      | •             | •                             |
| •                      | •             | •                             |
| 0000 0000 <sub>B</sub> | 0             | Mute                          |

|             |     |      |      |      |      |      |      |      |     |      |     |     |     |     |      |      |
|-------------|-----|------|------|------|------|------|------|------|-----|------|-----|-----|-----|-----|------|------|
|             | B15 | B14  | B13  | B12  | B11  | B10  | B9   | B8   | B7  | B6   | B5  | B4  | B3  | B2  | B1   | B0   |
| Register 18 | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | OVER | RSV | RSV | RSV | RSV | MUT2 | MUT1 |

### MUTx Soft Mute Control

Where  $x = 1$  or  $2$ , corresponding to the DAC output  $V_{OUTL}$  ( $x = 1$ ) and  $V_{OUTR}$  ( $x = 2$ ).

Default Value: 0

|          |                         |
|----------|-------------------------|
| MUTx = 0 | Mute Disabled (default) |
| MUTx = 1 | Mute Enabled            |

The mute bits, MUT1 and MUT2, are used to enable or disable the Soft Mute function for the corresponding DAC outputs,  $V_{OUTL}$  and  $V_{OUTR}$ . The Soft Mute function is incorporated into the digital attenuators. When Mute is disabled ( $\text{MUTx} = 0$ ), the attenuator and DAC operate normally. When Mute is enabled by setting  $\text{MUTx} = 1$ , the digital attenuator for the corresponding output will be decreased from the current setting to the infinite attenuation setting, one attenuator step (0.5dB) at a time. This provides a “pop”-free muting of the DAC output. By setting  $\text{MUTx} = 0$ , the attenuator will be increased one step at a time to a previously programmed attenuation level.

### OVER Oversampling Rate Control

Default Value: 0

|          |                            |
|----------|----------------------------|
| OVER = 0 | 64x Oversampling (default) |
| OVER = 1 | 128x Oversampling          |

The OVER bit is used to control the oversampling rate of the delta-sigma DACs.

|             |     |      |      |      |      |      |      |      |     |      |      |      |     |     |      |      |
|-------------|-----|------|------|------|------|------|------|------|-----|------|------|------|-----|-----|------|------|
|             | B15 | B14  | B13  | B12  | B11  | B10  | B9   | B8   | B7  | B6   | B5   | B4   | B3  | B2  | B1   | B0   |
| REGISTER 19 | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | DMF1 | DMF0 | DM12 | RSV | RSV | DAC2 | DAC1 |

### DACx DAC Operation Control

where  $x = 1$  or  $2$ , corresponding to the DAC output  $V_{OUTL}$  ( $x = 1$ ) or  $V_{OUTR}$  ( $x = 2$ ).

Default Value: 0

|          |                                 |
|----------|---------------------------------|
| DACx = 0 | DAC Operation Enabled (default) |
| DACx = 1 | DAC Operation Disabled          |

The DAC operation controls are used to enable and disable the DAC outputs,  $V_{OUTL}$  and  $V_{OUTR}$ . When  $DACx = 0$ , the corresponding output will generate the audio waveform dictated by the data present on the DATA pin. When  $DACx = 1$ , the corresponding output will be set to the bipolar zero level, or  $V_{CC}/2$ .

### DM12 Digital De-Emphasis Function Control

Default Value: 0

|          |                                |
|----------|--------------------------------|
| DM12 = 0 | De-Emphasis Disabled (default) |
| DM12 = 1 | De-Emphasis Enabled            |

The DM12 bit is used to enable or disable the Digital De-Emphasis function. Refer to the Typical Performance Curves of this data sheet for more information.

### DMF[1:0] Sampling Frequency Selection for the De-Emphasis Function

Default Value: 00

| DMF[1:0] | De-Emphasis Same Rate Selection |
|----------|---------------------------------|
| 00       | 44.1kHz (default)               |
| 01       | 48kHz                           |
| 10       | 32kHz                           |
| 11       | Reserved                        |

The DMF[1:0] bits are used to select the sampling frequency used for the Digital De-Emphasis function when it is enabled.

|             |     |      |      |      |      |      |      |      |     |     |     |     |     |      |      |      |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|------|------|------|
|             | B15 | B14  | B13  | B12  | B11  | B10  | B9   | B8   | B7  | B6  | B5  | B4  | B3  | B2   | B1   | B0   |
| REGISTER 20 | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | FLT | RSV | RSV | FMT2 | FMT1 | FMT0 |

### FMT[2:0] Audio Interface Data Format

Default Value: 101

The FMT[2:0] bits are used to select the data format for the serial audio interface. The following table shows the available format options.

| FMT[2:0] | Audio Data Format Selection                     |
|----------|---|
| 000      | 24-Bit Standard Format, Right-Justified Data    |
| 001      | 20-Bit Standard Format, Right-Justified Data    |
| 010      | 18-Bit Standard Format, Right-Justified Data    |
| 011      | 16-Bit Standard Format, Right-Justified Data    |
| 100      | I <sup>2</sup> S Format, 16- to 24-bits         |
| 101      | Left-Justified Format, 16- to 24-Bits (default) |
| 110      | Reserved  |
| 111      | Reserved  |

## Register 20 (Cont.)

### FLT Digital Filter Roll-Off Control

Default Value: 0

|         |                          |
|---------|--------------------------|
| FLT = 0 | Sharp Roll-Off (default) |
| FLT = 1 | Slow Roll-Off            |

The FLT bit allows the user to select the digital filter roll-off that is best suited to their application. Two filter roll-off sections are available: Sharp or Slow. The filter responses for these selections are shown in the Typical Performance Curves section of this data sheet.

| REGISTER 22 | B15 | B14  | B13  | B12  | B11  | B10  | B9   | B8   | B7  | B6  | B5  | B4  | B3  | B2   | B1   | B0   |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|------|------|------|
|             | 0   | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | RSV | RSV | AZRO | ZREV | DREV |

### DREV Output Phase Select

Default Value: 0

|          |                         |
|----------|-------------------------|
| DREV = 0 | Normal Output (default) |
| DREV = 1 | Inverted Output         |

The DREV bit is used to set the output phase of  $V_{OUTL}$  and  $V_{OUTR}$ .

### ZREV Zero Flag Polarity Select

Default Value: 0

|          |  |
|----------|--|
| ZREV = 0 | Zero Flag Pins HIGH at a Zero Detect (default) |
| ZREV = 1 | Zero Flag Pins LOW at a Zero Detect            |

The ZREV bit allows the user to select the active polarity of Zero Flag pins.

### AZRO Zero Flag Function Select

Default Value: 0

|          |  |
|----------|--|
| AZRO = 0 | L-/R-Channel Independent Zero Flag (default) |
| AZRO = 1 | L-/R-Channel Common Zero Flag                |

## Register22 (Cont.)

The AZRO bit allows the user to select the function of Zero Flag pins.

AZRO = 0:

|  |
|--|
| Pin11: ZEROR; Zero Flag Output for R-Channel |
| Pin12: ZEROL; Zero Flag Output for L-Channel |

AZRO = 1:

|   |
|---|
| Pin11: ZEROA; Zero Flag Output for L-/R-Channel |
| Pin12: NA; No Assign                            |

# ANALOG OUTPUTS

The PCM1741 includes two independent output channels:  $V_{OUTL}$  and  $V_{OUTR}$ . These are unbalanced outputs, each capable of driving 2.05V<sub>p-p</sub> typical into a 5k $\Omega$  AC-coupled load. The internal output amplifiers for  $V_{OUTL}$  and  $V_{OUTR}$  are biased to the DC common-mode (or bipolar zero) voltage, equal to  $V_{CC}/2$ .

The output amplifiers include an RC continuous-time filter that helps to reduce the out-of-band noise energy present at the DAC outputs, due to the noise shaping characteristics of the PCM1741's delta-sigma DACs. The frequency response of this filter is shown in Figure 8. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications, therefore, an external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

## $V_{COM}$ OUTPUT

One unbuffered common-mode voltage output pin,  $V_{COM}$  (pin 10), is brought out for decoupling purposes. This pin is

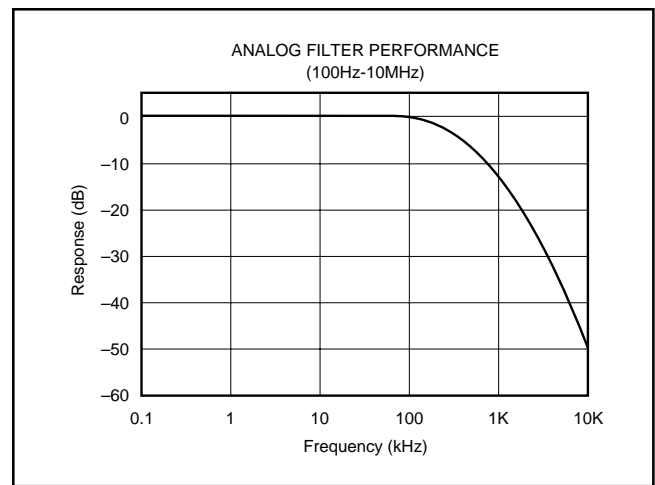


FIGURE 8. Output Filter Frequency Response.

nominally biased to a DC voltage level equal to  $V_{CC}/2$ . This pin may be used to bias external circuits. Figure 9 shows an example of using the  $V_{COM}$  pin for external biasing applications.

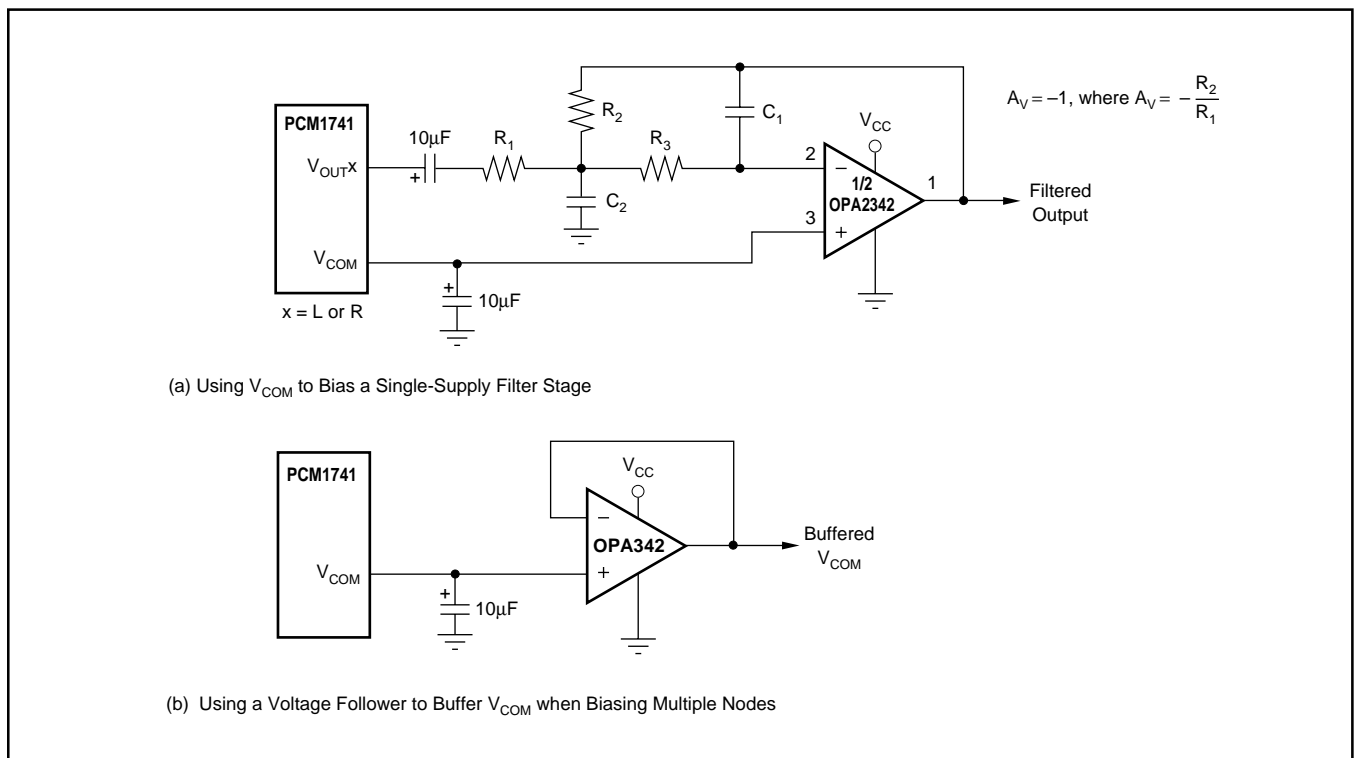


FIGURE 9. Biasing External Circuits Using the  $V_{COM}$  Pin.

## ZERO FLAGS

### Zero Detect Condition

Zero Detection for each output channel is independent from the other. If the data for a given channel remains at a “0” level for 1024 sample periods (or LRCK clock periods), a Zero Detect condition exists for that channel.

### Zero Output Flags

Given that a Zero Detect condition exists for one or more channels, the Zero Flag pins for those channels will be set to a logic “1” state. There are Zero Flag pins for each channel: ZEROL (pin 12) and ZEROR (pin 11). These pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled functions.

The active polarity of Zero Flag output can be inverted by setting the ZREV bit of Control Register 22 to “1”. The reset default is active high output, or ZREV = 0.

The L-channel and R-channel common Zero Flag can be selected by setting the AZRO bit of Control Register 22 to “1”. The reset default is L-channel and R-channel independent Zero Flag, or AZRO = 0.

## APPLICATIONS INFORMATION

### CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 11, with the necessary power-supply bypassing and decoupling components. Texas Instruments recommends using the component values shown in Figure 11 for all designs.

The use of series resistors (22Ω to 100Ω) are recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with stray PCB and device input capacitance to form a low-pass filter that reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

## POWER SUPPLIES AND GROUNDING

The PCM1741 requires a +3.3V analog supply ( $V_{CC}$ ) and a +3.3V digital supply ( $V_{DD}$ ). The +3.3V supply ( $V_{CC}$ ) is used to power the DAC analog and output filter circuitry, while the +3.3V ( $V_{DD}$ ) supply is used to power the digital filter and serial interface circuitry. For best performance, the +3.3V ( $V_{DD}$ ) supply should be derived from the +3.3V ( $V_{CC}$ ) supply using a linear regulator, as shown in Figure 11.

Proper power-supply bypassing is shown in Figure 10. The 10μF capacitors should be tantalum or aluminum electrolytic, while the 0.1μF capacitors are ceramic (X7R type is recommended for surface-mount applications).

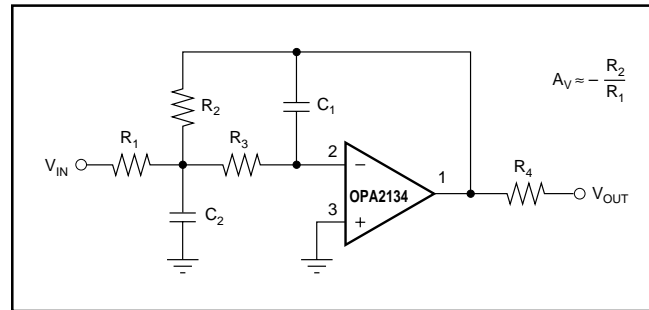


FIGURE 10. Dual-Supply Filter Circuit.

### DAC OUTPUT FILTER CIRCUITS

Delta-sigma DACs utilize noise-shaping techniques to improve in-band Signal-to-Noise Ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist Frequency, or  $f_s/2$ . The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figures 9(a) and 10 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are second-order Butterworth filters

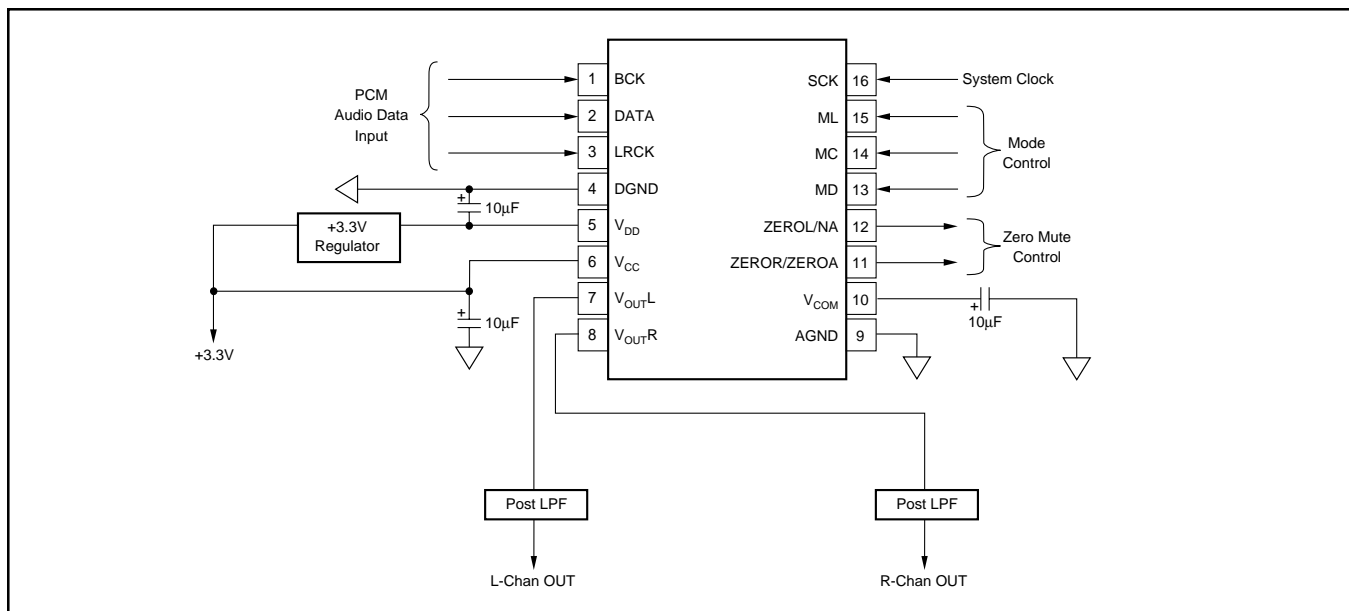


FIGURE 11. Basic Connection Diagram.

using a Multiple FeedBack (MFB) circuit arrangement that reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please refer to Burr-Brown Applications Bulletin #34 AB-034 (SBFA001), available from our web site at <http://www.ti.com>.

Since the overall system performance is defined by the quality of the DACs and their associated analog output circuitry, high-quality audio op amps are recommended for the active filters. The OPA2353 and OPA2134 dual op amps from Texas Instruments are recommended for use with the PCM1741, see Figures 9(a) and 10.

## PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1741 is shown in Figure 12. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1741 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

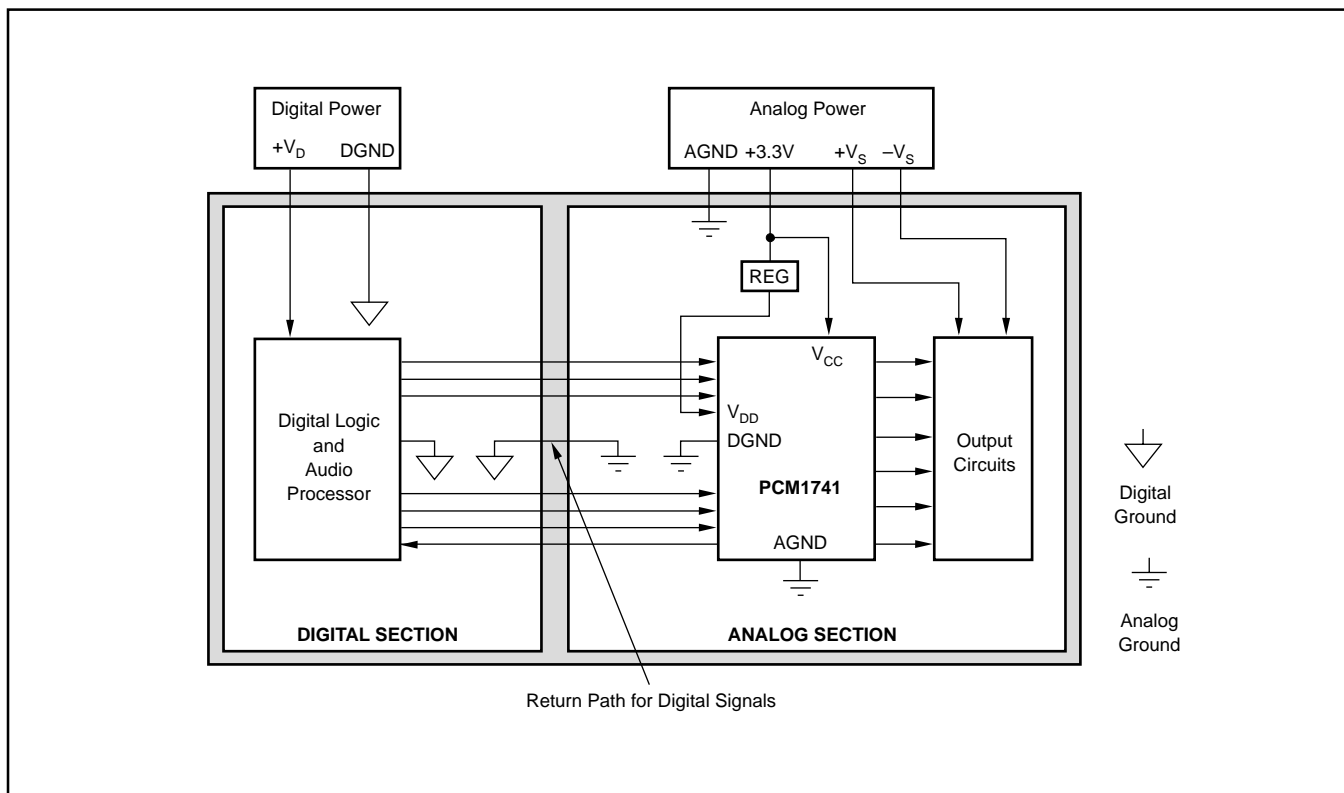


FIGURE 12. Recommended PCB Layout.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1741. In cases where a common +3.3V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital +3.3V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 13 shows the recommended approach for single-supply applications.

## THEORY OF OPERATION

The delta-sigma section of the PCM1741 is based on an 8-level amplitude quantizer and a fourth-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 14. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the interpolation filter is  $64f_s$ .

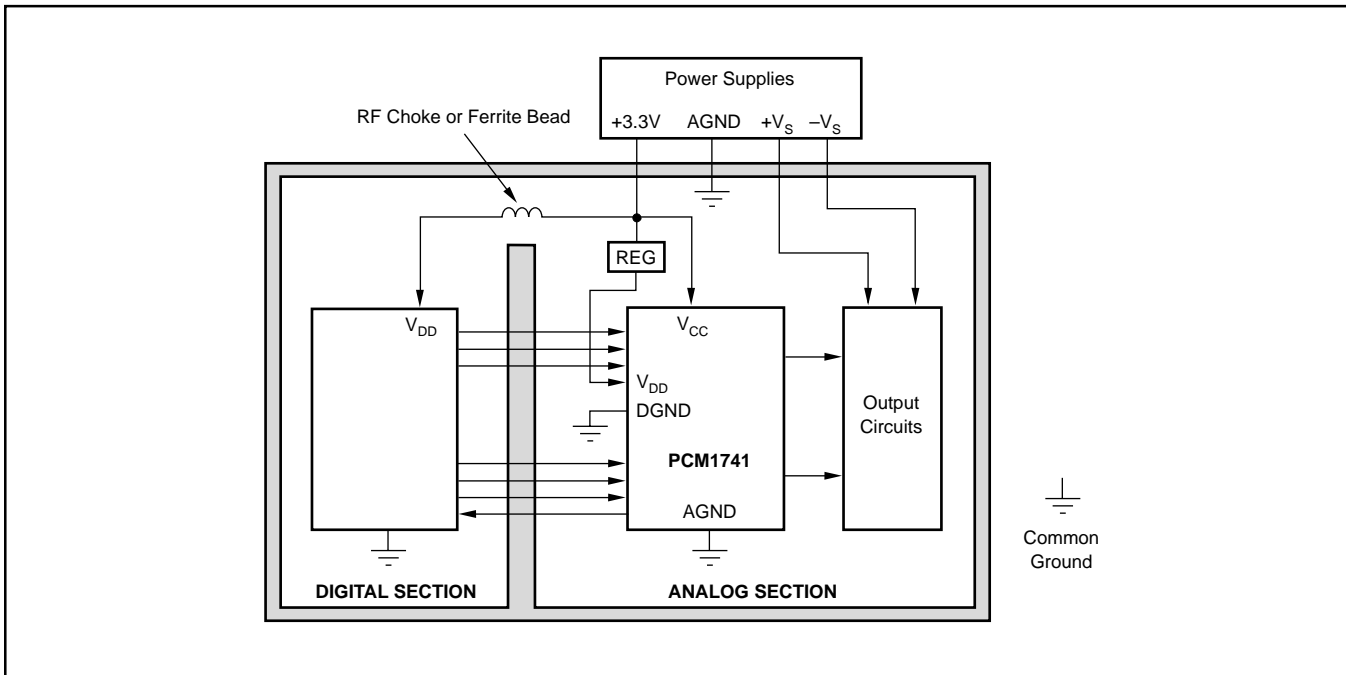


FIGURE 13. Single-Supply PCB Layout.

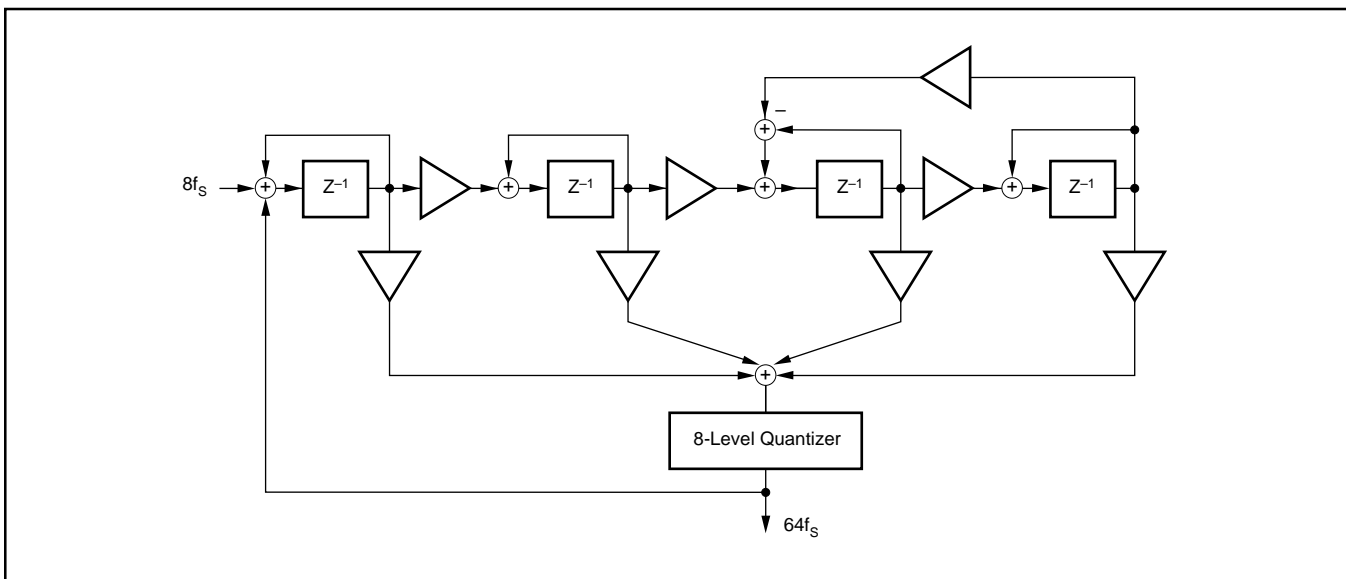


FIGURE 14. 8-Level Delta-Sigma Modulator.

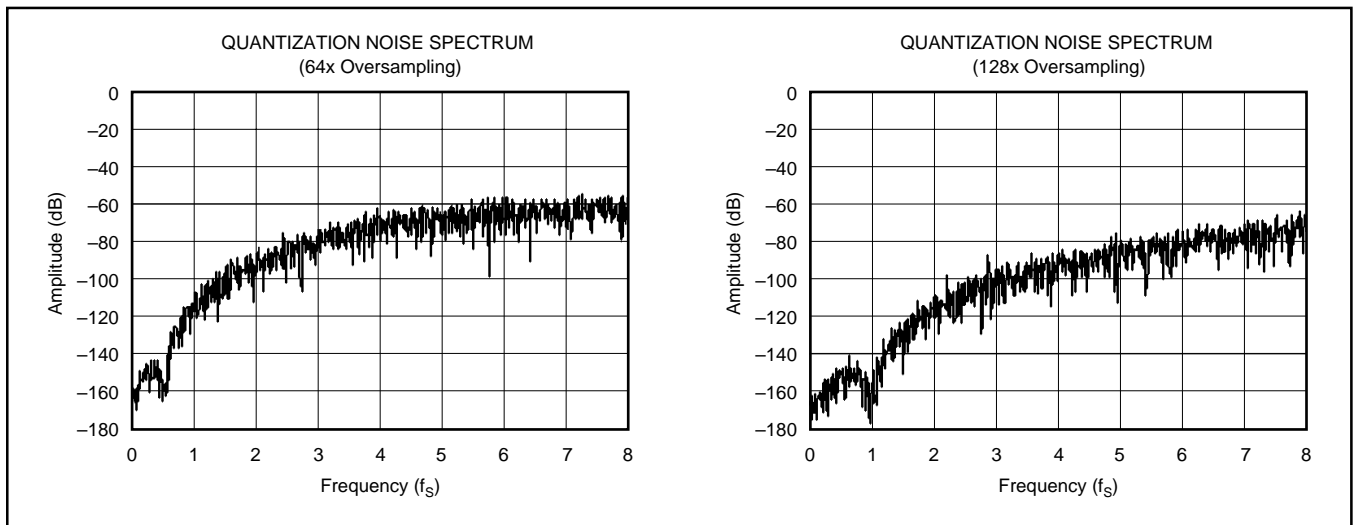


FIGURE 15. Quantization Noise Spectrum.

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 15. The enhanced multilevel delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multilevel quantizer, with the simulated jitter sensitivity, as shown in Figure 16.

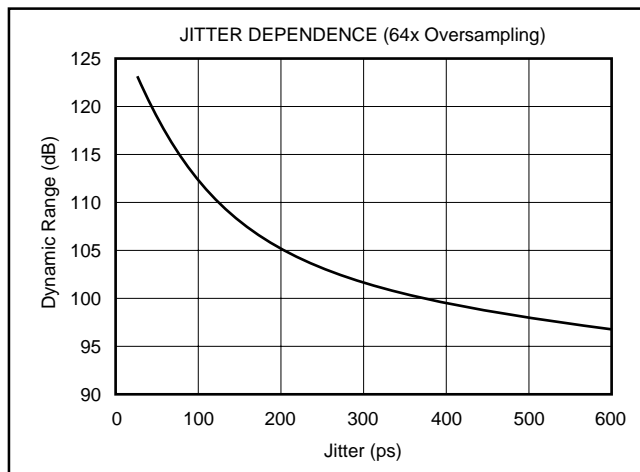


FIGURE 16. Jitter Sensitivity.

## KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1741. In all cases, an Audio Precision System Two Cascade or equivalent audio measurement system is utilized to perform the testing.

### TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion + Noise (THD+N) is a significant figure of merit for audio DACs, since it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N. Figure 17 shows the test setup for THD+N measurements.

For the PCM1741, THD+N is measured with a full-scale, 1kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to a 24-bit audio word length and a sampling frequency of 44.1kHz or 96kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF

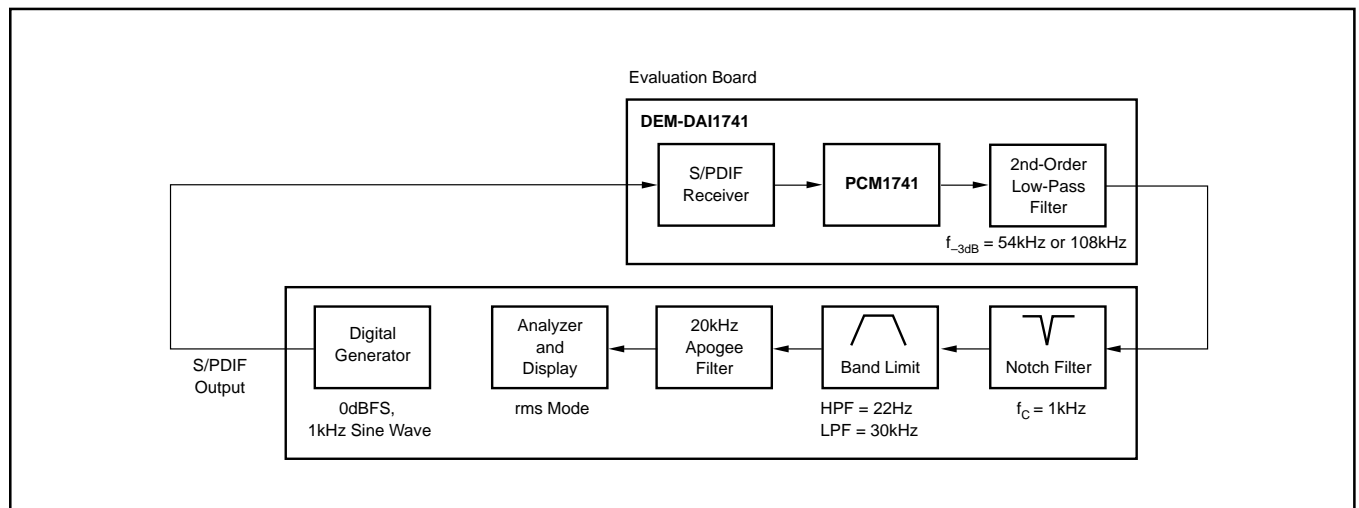


FIGURE 17. Test Setup for THD+N Measurements.

data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1741 demo board. The receiver is then configured to output 24-bit data in either I<sup>2</sup>S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

### DYNAMIC RANGE

Dynamic range is specified as A-Weighted, THD+N measured with a -60dBFS, 1kHz digital sine wave stimulus at the input of the DAC. This measurement is designed to give a good indicator of how the DAC will perform given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 18, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-Weighting filter, and the -60dBFS input level.

### IDLE CHANNEL SIGNAL-TO-NOISE RATIO

The SNR test provides a measure of the noise floor of the DAC. The input to the DAC is all “0”s data, and the DAC’s Infinite Zero Detect Mute function must be disabled (default condition at power up for the PCM1741). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and effect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all “0”s data stream at the input of the DAC. The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level (see the notes provided in Figure 18).

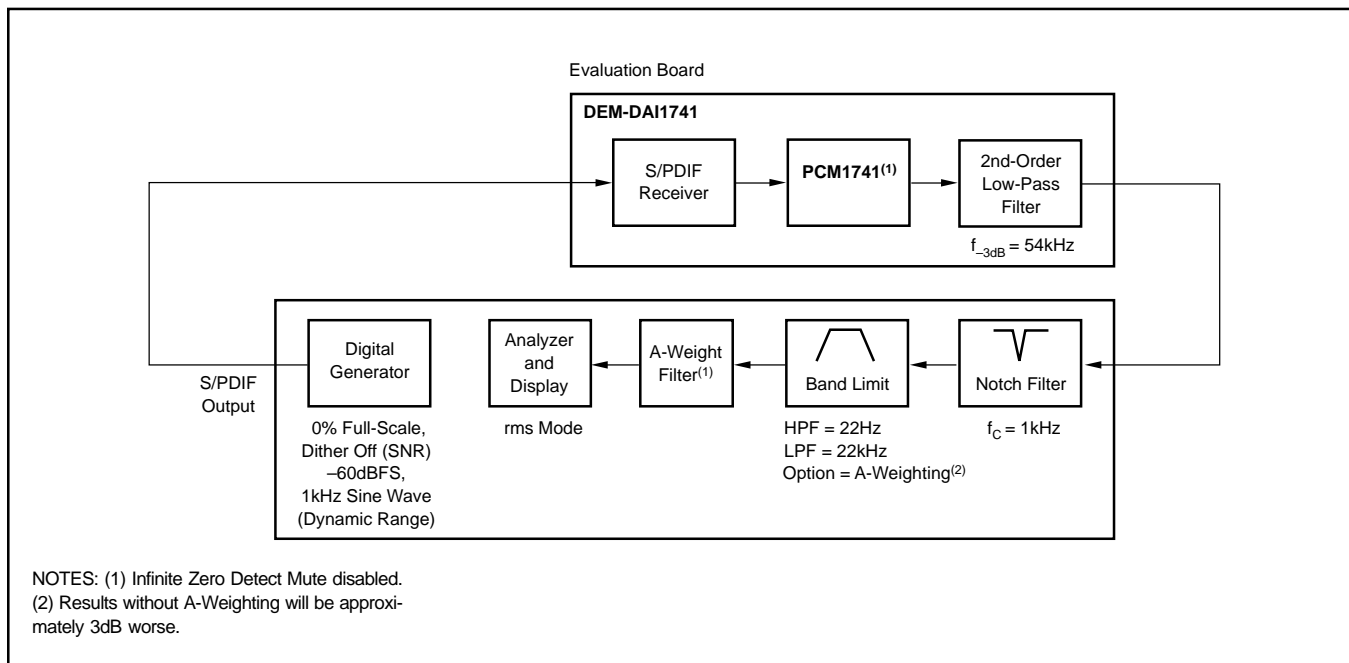


FIGURE 18. Test Setup for Dynamic Range and SNR Measurements.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type  | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|---------------|-----------------|------|-------------|----------------------------|------------------|------------------------------|
| PCM1741E         | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 75          | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCM1741E/2K      | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCM1741E/2KG4    | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCM1741EG4       | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 75          | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

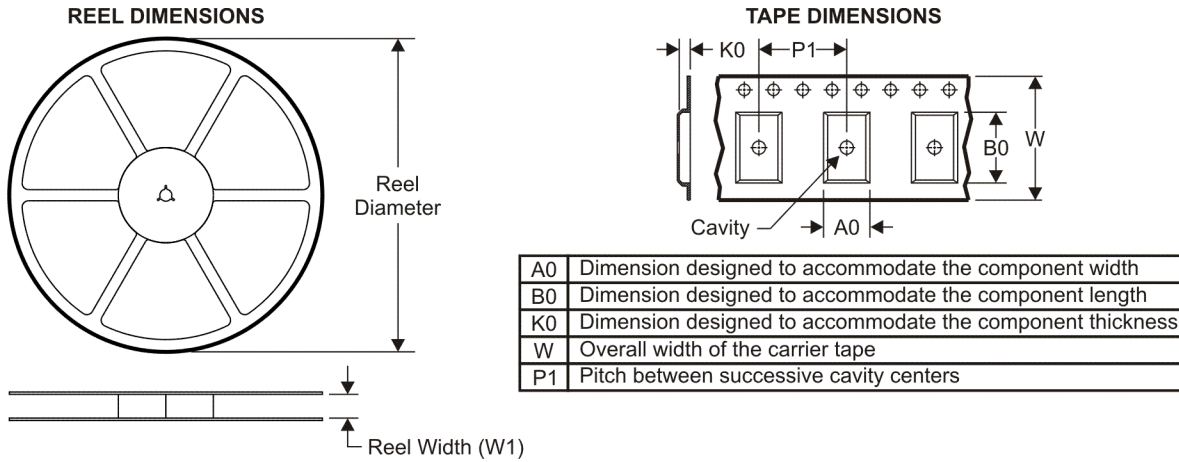
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

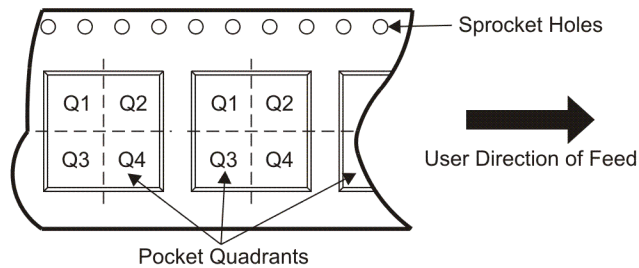
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**TAPE AND REEL INFORMATION**



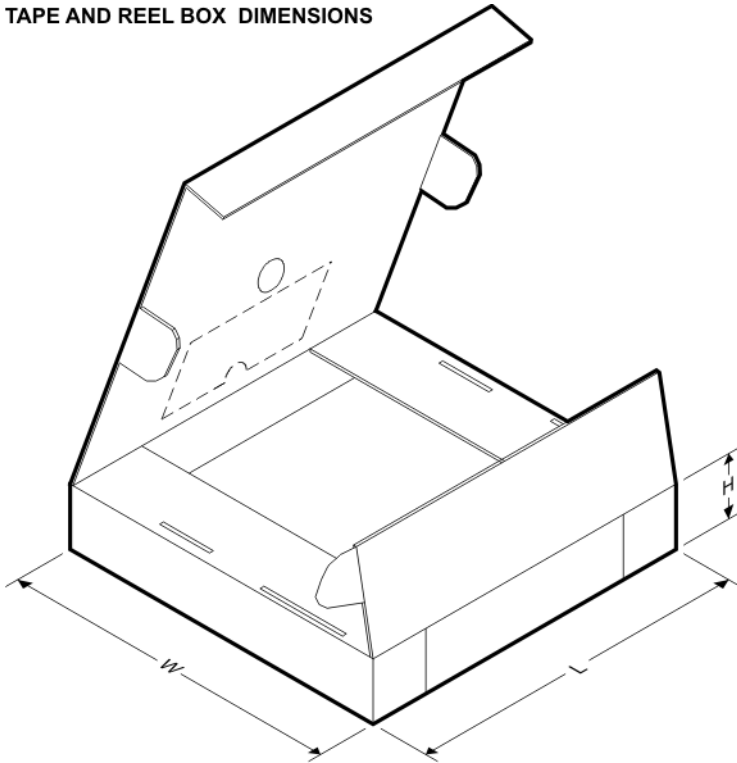
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM1741E/2K | SSOP/QSOP    | DBQ             | 16   | 2000 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM1741E/2K | SSOP/QSOP    | DBQ             | 16   | 2000 | 346.0       | 346.0      | 29.0        |

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